74LVC2G08
Dual 2-Input AND Gate

GENERAL DESCRIPTION

The 74LVC2G08 is a dual 2-input AND gate that is designed for 1.65V to 5.5V V_{CC} operation. The device can be used as a down translator in a mixed 3.3V and 5.5V system environment. The device features the Boolean function Y = A × B or $Y = \overline{\overline{A} + \overline{B}}$.

This device is highly suitable for partial power-down applications using power-off leakage current (I_{OFF}) circuit. When the device is powered down, the current backflow will be prevented from passing through the device.

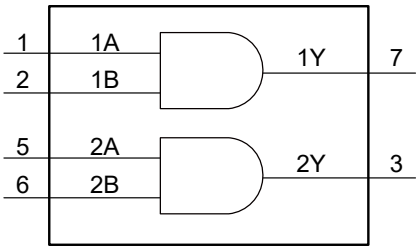
FEATURES

- **Wide Supply Voltage Range: 1.65V to 5.5V**
- **Inputs Accept Voltage up to 5.5V**
- **+24mA/-24mA Output Current at V_{CC} = 3V**
- **Low Power Dissipation**
- **Propagation Delay: 4ns (TYP) at 3.3V**
- **Support Live Insertion, Partial-Power-Down Mode and Back-Drive Protection**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green VSSOP-8 Package**

APPLICATIONS

Wireless Basestation
Networking
Access Device
Signal Process
Notebook PC
Mobile Phone

LOGIC SYMBOL

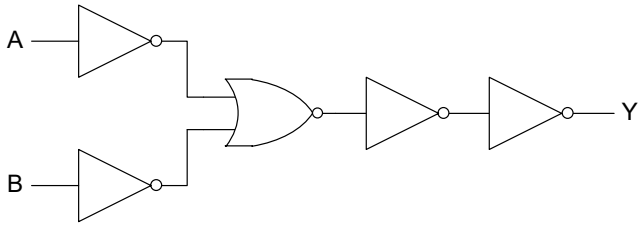


FUNCTION TABLE

INPUT		OUTPUT
nA	**nB**	**nY**
H	H	H
L	*X*	L
X	L	L

Y = A × B or $Y = \overline{\overline{A} + \overline{B}}$
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

LOGIC DIAGRAM

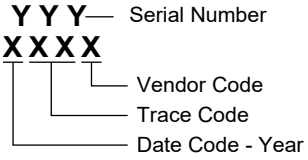


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVC2G08	VSSOP-8	-40℃ to +125℃	74LVC2G08XVS8G/TR	01P XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, V_{CC} ..... -0.5V to 6.5V
Input Voltage, V_I (2) ..... -0.5V to 6.5V
Output Voltage, V_O (2) (3)
High-State or Low-State.....-0.5V to V_{CC} + 0.5V
High-Impedance or Power-Off State ..... -0.5V to 6.5V
Input Clamping Current, I_{IK} (V_I < 0V).....-50mA
Output Clamping Current, I_{OK} (V_O < 0V) .....-50mA
Output Current, I_O .....±50mA
Supply Current, I_{CC} 100mA
Ground Current, I_{GND}.....-100mA
Junction Temperature (4).....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....5000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC}.....1.65V to 5.5V
Data Retention Only, V_{CC}..... 1.5V (MIN)
Input Voltage, V_I.....0V to 5.5V
Output Voltage, V_O..... 0V to V_{CC}
High-Level Output Current, I_{OH}
V_{CC} = 1.65V.....-4mA (MAX)
V_{CC} = 2.3V.....-8mA (MAX)
V_{CC} = 3V.....-24mA (MAX)
V_{CC} = 4.5V.....-32mA (MAX)
Low-Level Output Current, I_{OL}
V_{CC} = 1.65V.....4mA (MAX)
V_{CC} = 2.3V.....8mA (MAX)
V_{CC} = 3V.....24mA (MAX)
V_{CC} = 4.5V.....32mA (MAX)
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V..... 20ns/V (MAX)
V_{CC} = 3.3V ± 0.3V..... 10ns/V (MAX)
V_{CC} = 5V ± 0.5V..... 5ns/V (MAX)
Operating Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. When V_{CC} = 0V (power-down mode), the output voltage can be 5.5V in normal operation.

4. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

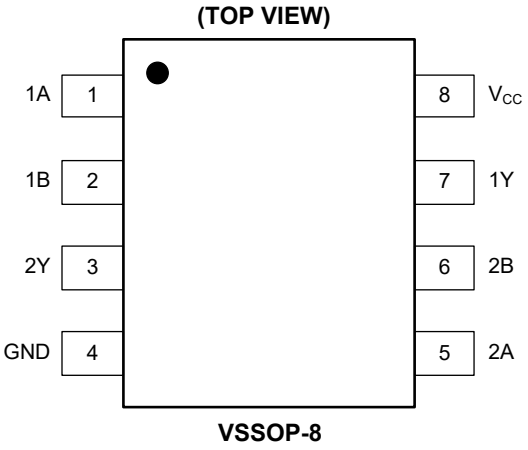
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

NAME	PIN	FUNCTION
1A, 2A	1, 5	Data Inputs.
1B, 2B	2, 6	Data Inputs.
1Y, 2Y	7, 3	Data Outputs.
GND	4	Ground.
V_{CC}	8	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 1.65V to 1.95V	Full	0.65 × V_{CC}			V
		V_{CC} = 2.3V to 2.7V	Full	1.7			
		V_{CC} = 3V to 3.6V	Full	2			
		V_{CC} = 4.5V to 5.5V	Full	0.6 × V_{CC}			
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.65V to 1.95V	Full			0.35 × V_{CC}	V
		V_{CC} = 2.3V to 2.7V	Full			0.7	
		V_{CC} = 3V to 3.6V	Full			1	
		V_{CC} = 4.5V to 5.5V	Full			0.3 × V_{CC}	
High-Level Output Voltage	V_{OH}	V_{CC} = 1.65V to 5.5V, I_O = -100μA	Full	V_{CC} - 0.1	V_{CC} - 0.01		V
		V_{CC} = 1.65V, I_O = -4mA	Full	1.2	1.5		
		V_{CC} = 2.3V, I_O = -8mA	Full	1.9	2.1		
		V_{CC} = 3.0V, I_O = -16mA	Full	2.4	2.8		
		V_{CC} = 3.0V, I_O = -24mA	Full	2.3	2.7		
		V_{CC} = 4.5V, I_O = -32mA	Full	3.8	4.2		
Low-Level Output Voltage	V_{OL}	V_{CC} = 1.65V to 5.5V, I_O = 100μA	Full		0.01	0.1	V
		V_{CC} = 1.65V, I_O = 4mA	Full		0.15	0.45	
		V_{CC} = 2.3V, I_O = 8mA	Full		0.2	0.3	
		V_{CC} = 3.0V, I_O = 16mA	Full		0.25	0.4	
		V_{CC} = 3.0V, I_O = 24mA	Full		0.35	0.55	
		V_{CC} = 4.5V, I_O = 32mA	Full		0.4	0.55	
Input Leakage Current	I_I	nA or nB inputs, V_{CC} = 0V to 5.5V, V_I = 5.5V or GND	Full		±0.1	±3	μA
Power-Off Leakage Current	I_{OFF}	V_{CC} = 0V, V_I or V_O = 5.5V	Full		±0.1	±3	μA
Supply Current	I_{CC}	V_{CC} = 1.65V to 5.5V, V_I = 5.5V or GND, I_O = 0A	Full		0.1	±3	μA
Additional Supply Current	ΔI_{CC}	V_{CC} = 3.0V to 5.5V, one input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	Full		0.05	3	μA
Input Capacitance	C_I	V_{CC} = 3.3V, V_I = V_{CC} or GND	+25℃		5		pF

DYNAMIC CHARACTERISTICS

(For test circuit, see Figure 1. Full = -40℃ to +125℃, all typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay (2)	t_{PD}	nA, nB to nY	V_{CC} = 1.8V ± 0.15V	Full	2.6	8.6	16	ns
			V_{CC} = 2.5V ± 0.2V	Full	1	5.5	9.5	
			V_{CC} = 3.3V ± 0.3V	Full	1	4	7.5	
			V_{CC} = 5V ± 0.5V	Full	1	3.9	6	
Power Dissipation Capacitance (3)	C_{PD}	f = 10MHz	V_{CC} = 1.8V to 3.3V	+25℃		18		pF
			V_{CC} = 5V	+25℃		19		

NOTES:

1. Specified by design and characterization, not production tested.
2. t_{PD} is the same as t_{PLH} and t_{PHL}.
3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

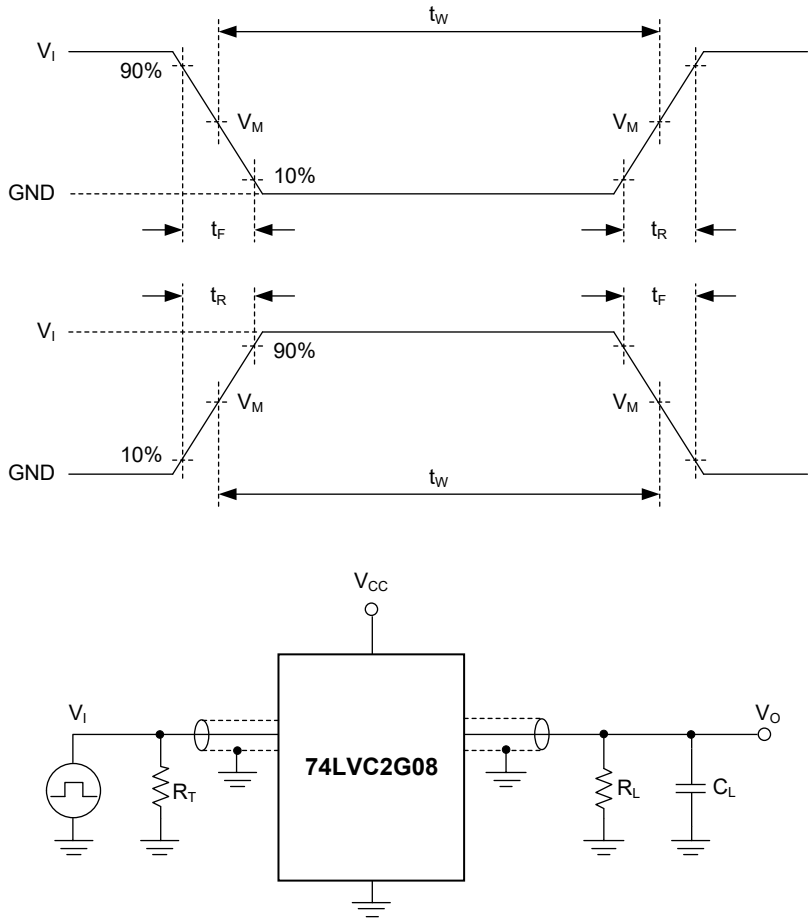
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

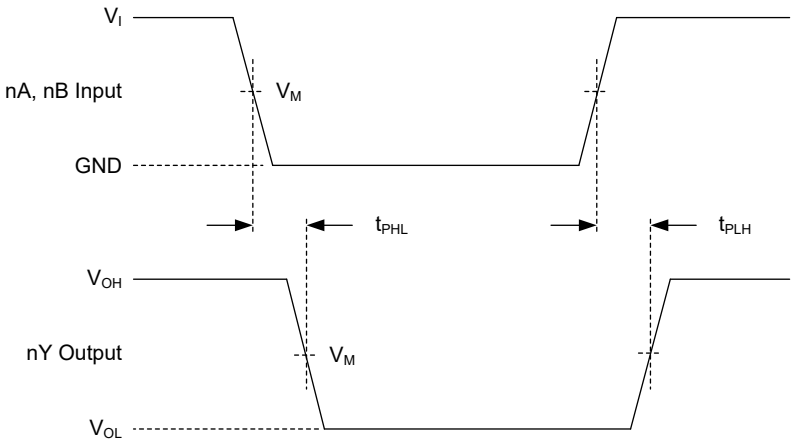
R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD	
V_{CC}	V_I	t_R, t_F	C_L	R_L
1.8V ± 0.15V	V_{CC}	≤ 2ns	30pF	1kΩ
2.5V ± 0.2V	V_{CC}	≤ 2ns	30pF	500Ω
3.3V ± 0.3V	3V	≤ 2.5ns	50pF	500Ω
5V ± 0.5V	V_{CC}	≤ 2.5ns	50pF	500Ω

WAVEFORMS



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (nA, nB) to Output (nY) Propagation Delay Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT
V_{CC}	V_I	V_M (1)	V_M
1.8V ± 0.15V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
2.5V ± 0.2V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
3.3V ± 0.3V	3V	1.5V	1.5V
5V ± 0.5V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}

NOTE:
1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.

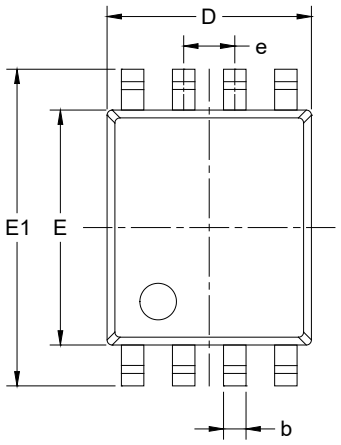
REVISION HISTORY

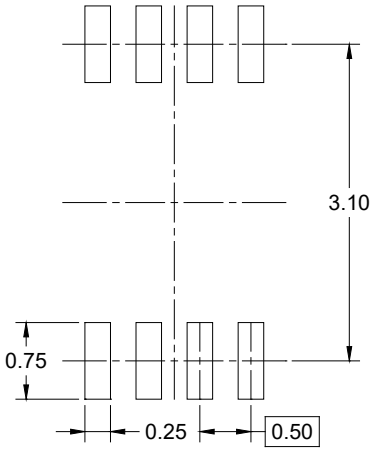
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (OCTOBER 2022) to REV.A	Page
Changed from product preview to production data	All

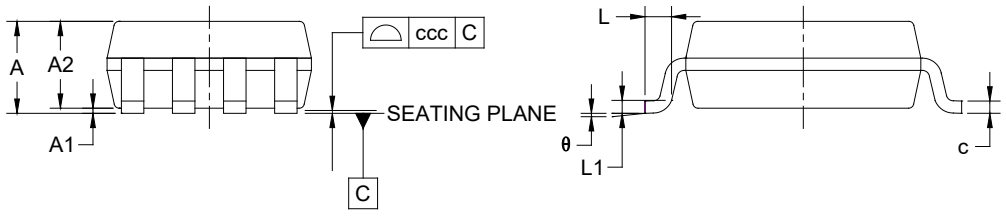
PACKAGE OUTLINE DIMENSIONS

VSSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)

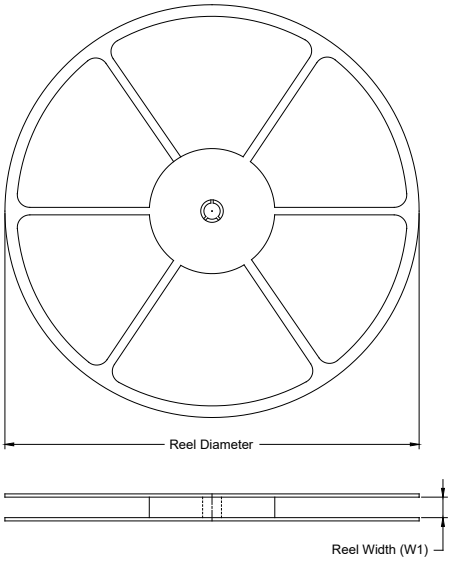


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.000
A1	0.000	-	0.150
A2	0.600		0.850
b	0.170	-	0.270
c	0.080		0.230
D	1.900	-	2.100
E	2.200	-	2.400
E1	3.000	-	3.200
e	0.500 BSC		
L	0.150	-	0.400
L1	0.120 BSC		
θ	0°	-	8°
ccc	0.100		

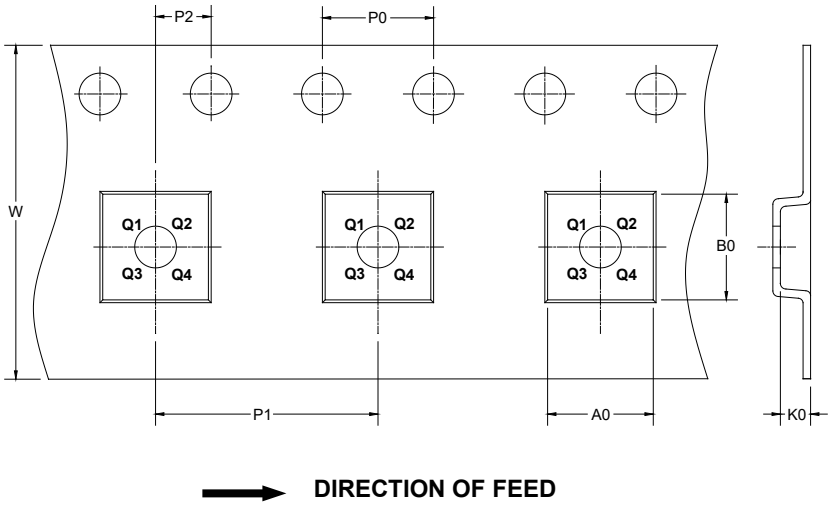
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187 CA.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



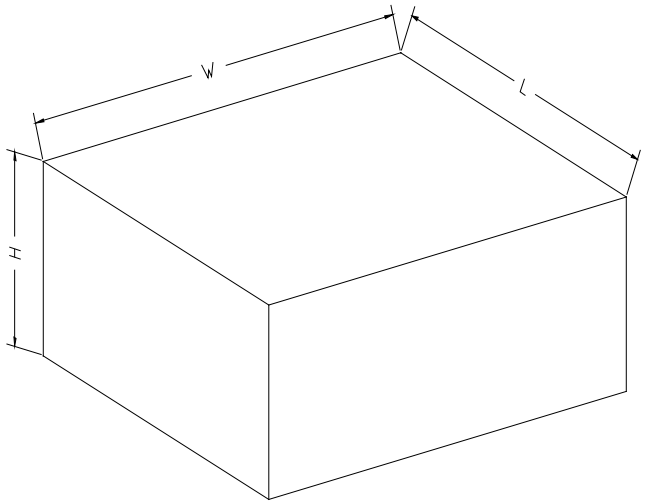
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
VSSOP-8	7″	9.5	2.25	3.35	1.05	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002