

GENERAL DESCRIPTION

The SGM72112B is a dual single-pole/six-throw (2×SP6T) antenna switch, which supports from 0.1GHz to 3.8GHz. The device features low insertion loss and high isolation, which make it suitable for high linearity receiving applications. It also has the advantage of high linearity performance for diversity receiving in carrier aggregation applications.

The SGM72112B has the ability to integrate a DP12T (2×SP6T) RF switch and a programmable MIPI controller on silicon-on-insulator (SOI) process. Internal driver and decoder for switch control signals are offered by the controller, which makes it flexible in RF path band and routing selection.

No external DC blocking capacitors are required on the RF paths as long as no external DC voltage is applied, which can save PCB area and cost.

The SGM72112B is available in a Green ULGA-2.4×2-18L package.

APPLICATIONS

3G/4G Applications
Carrier Aggregation Diversity

FEATURES

- **Supply Voltage Range: 2.4V to 4.8V**
- **Advanced Silicon-On-Insulator (SOI) Process**
- **Frequency Range: 0.1GHz to 3.8GHz**
- **Low Insertion Loss: 1.0dB (TYP) at 3.8GHz**
- **MIPI RFFE Interface Compatible**
- **No External DC Blocking Capacitors Required**
- **Available in a Green ULGA-2.4×2-18L Package**

BLOCK DIAGRAM

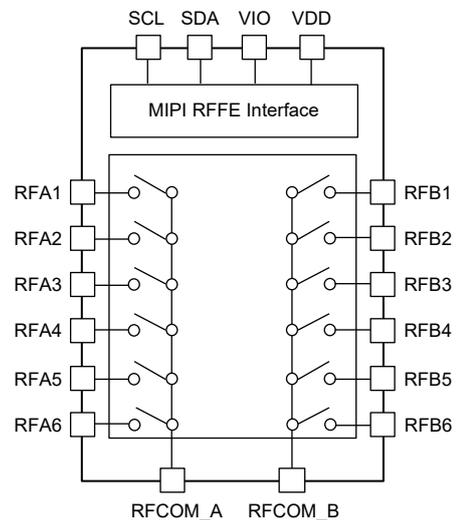


Figure 1. SGM72112B Block Diagram

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM72112B	ULGA-2.4x2-18L	-40°C to +85°C	SGM72112BYULB18G/TR	SGMPC XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage, V_{DD}5V
- Supply Voltage for MIPI, V_{IO} 2V
- SDA, SCL Control Voltage, V_{CTL} 2V
- RF Input Power, P_{IN} 26dBm
- Junction Temperature.....+150°C
- Storage Temperature Range-55°C to +150°C
- Lead Temperature (Soldering, 10s).....+260°C
- ESD Susceptibility
- HBM..... 1000V

RECOMMENDED OPERATING CONDITIONS

- Operating Temperature Range-40°C to +85°C
- Operating Frequency Range..... 0.1GHz to 3.8GHz
- Supply Voltage, V_{DD}2.4V to 4.8V
- Supply Voltage for MIPI, V_{IO} 1.65V to 1.95V

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

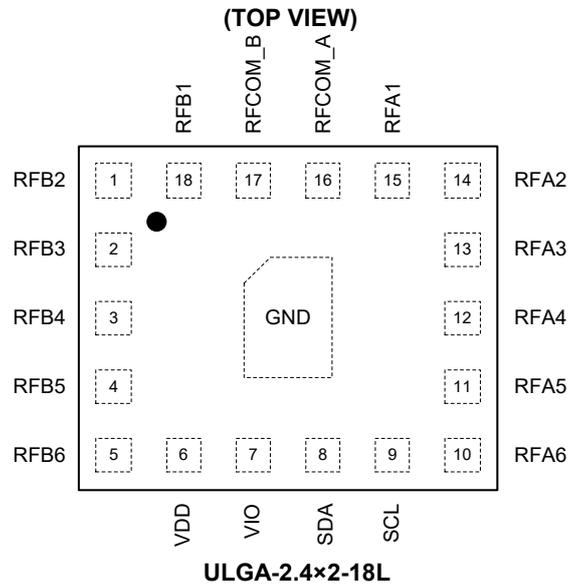
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	RFB2	RF Port B2.	10	RFA6	RF Port A6.
2	RFB3	RF Port B3.	11	RFA5	RF Port A5.
3	RFB4	RF Port B4.	12	RFA4	RF Port A4.
4	RFB5	RF Port B5.	13	RFA3	RF Port A3.
5	RFB6	RF Port B6.	14	RFA2	RF Port A2.
6	VDD	DC Power Supply.	15	RFA1	RF Port A1.
7	VIO	Supply Voltage for MIPI.	16	RFCOM_A	RF Common Port A.
8	SDA	RFFE Data Signal.	17	RFCOM_B	RF Common Port B.
9	SCL	RFFE Clock Signal.	18	RFB1	RF Port B1.
Exposed Pad	GND	Ground.			

Register_0 TRUTH TABLE (RFCOM_B)

Table 1. Register_0 Truth Table (RFCOM_B)

State	Mode	Register_0 Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
1	All Isolation	0	0	0	0	0	0	0	0
2	RFB1	0	0	0	0	0	0	0	1
3	RFB2	0	0	0	0	0	0	1	0
4	RFB3	0	0	0	0	0	0	1	1
5	RFB4	0	0	0	0	0	1	0	0
6	RFB5	0	0	0	0	0	1	0	1
7	RFB6	0	0	0	0	0	1	1	0
8	RFB6 + RFB5	0	0	0	0	0	1	1	1
9	RFB6 + RFB4	0	0	0	0	1	0	0	0
10	RFB6 + RFB3	0	0	0	0	1	0	0	1
11	RFB6 + RFB2	0	0	0	0	1	0	1	0
12	RFB6 + RFB1	0	0	0	0	1	0	1	1
13	RFB5 + RFB4	0	0	0	0	1	1	0	0
14	RFB5 + RFB3	0	0	0	0	1	1	0	1
15	RFB5 + RFB2	0	0	0	0	1	1	1	0
16	RFB5 + RFB1	0	0	0	0	1	1	1	1
17	RFB4 + RFB3	0	0	0	1	0	0	0	0
18	RFB4 + RFB2	0	0	0	1	0	0	0	1
19	RFB4 + RFB1	0	0	0	1	0	0	1	0
20	RFB3 + RFB2	0	0	0	1	0	0	1	1
21	RFB3 + RFB1	0	0	0	1	0	1	0	0
22	RFB2 + RFB1	0	0	0	1	0	1	0	1

Register_1 TRUTH TABLE (RFCOM_A)

Table 2. Register_1 Truth Table (RFCOM_A)

State	Mode	Register_1 Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
1	All Isolation	0	0	0	0	0	0	0	0
2	RFA1	0	0	0	0	0	0	0	1
3	RFA2	0	0	0	0	0	0	1	0
4	RFA3	0	0	0	0	0	0	1	1
5	RFA4	0	0	0	0	0	1	0	0
6	RFA5	0	0	0	0	0	1	0	1
7	RFA6	0	0	0	0	0	1	1	0
8	RFA6 + RFA5	0	0	0	0	0	1	1	1
9	RFA6 + RFA4	0	0	0	0	1	0	0	0
10	RFA6 + RFA3	0	0	0	0	1	0	0	1
11	RFA6 + RFA2	0	0	0	0	1	0	1	0
12	RFA6 + RFA1	0	0	0	0	1	0	1	1
13	RFA5 + RFA4	0	0	0	0	1	1	0	0
14	RFA5 + RFA3	0	0	0	0	1	1	0	1
15	RFA5 + RFA2	0	0	0	0	1	1	1	0
16	RFA5 + RFA1	0	0	0	0	1	1	1	1
17	RFA4 + RFA3	0	0	0	1	0	0	0	0
18	RFA4 + RFA2	0	0	0	1	0	0	0	1
19	RFA4 + RFA1	0	0	0	1	0	0	1	0
20	RFA3 + RFA2	0	0	0	1	0	0	1	1
21	RFA3 + RFA1	0	0	0	1	0	1	0	0
22	RFA2 + RFA1	0	0	0	1	0	1	0	1

ELECTRICAL CHARACTERISTICS(T_A = +25°C, V_{DD} = 2.4V to 4.8V, P_{IN} = 0dBm, 50Ω, typical values are at V_{DD} = 2.8V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics						
Supply Voltage	V _{DD}		2.4	2.8	4.8	V
Supply Current	I _{VDD}			32	70	μA
Supply Voltage for MIPI	V _{IO}		1.65	1.8	1.95	V
Supply Current for MIPI	I _{VIO}			4.8	10	μA
Control Voltage	V _{CTL_H}	High	0.8 × V _{IO}	V _{IO}	1.95	V
	V _{CTL_L}	Low	0		0.45	
Switching Time	t _{SW}	50% of control voltage to 90% of RF power		1	2	μs
Turn-On Time	t _{ON}	Time from V _{DD} = 0V to part on and RF at 90%		5	10	μs
RF Characteristics						
Insertion Loss (RFCOM to All RF Ports)	IL	f ₀ = 0.1GHz to 1.0GHz		0.4	0.62	dB
		f ₀ = 1.0GHz to 2.0GHz		0.5	0.84	
		f ₀ = 2.0GHz to 2.7GHz		0.6	1.20	
		f ₀ = 2.7GHz to 3.8GHz		1.0	1.32	
Isolation (RFCOM_A to Any Off RFA Port, RFCOM_B to Any Off RFB Port)	ISO	f ₀ = 0.1GHz to 1.0GHz	24	41		dB
		f ₀ = 1.0GHz to 2.0GHz	16	32		
		f ₀ = 2.0GHz to 2.7GHz	14	27		
		f ₀ = 2.7GHz to 3.8GHz	12	25		
Isolation (RFCOM_A to RFCOM_B)	ISO	f ₀ = 0.1GHz to 1.0GHz	27	41		dB
		f ₀ = 1.0GHz to 2.0GHz	21	32		
		f ₀ = 2.0GHz to 2.7GHz	19	27		
		f ₀ = 2.7GHz to 3.8GHz	15	25		
0.1dB Compression Point (RFCOM to All RF Ports)	P _{0.1dB}	f ₀ = 0.1GHz to 3.8GHz		25		dBm

MIPI READ AND WRITE TIMING

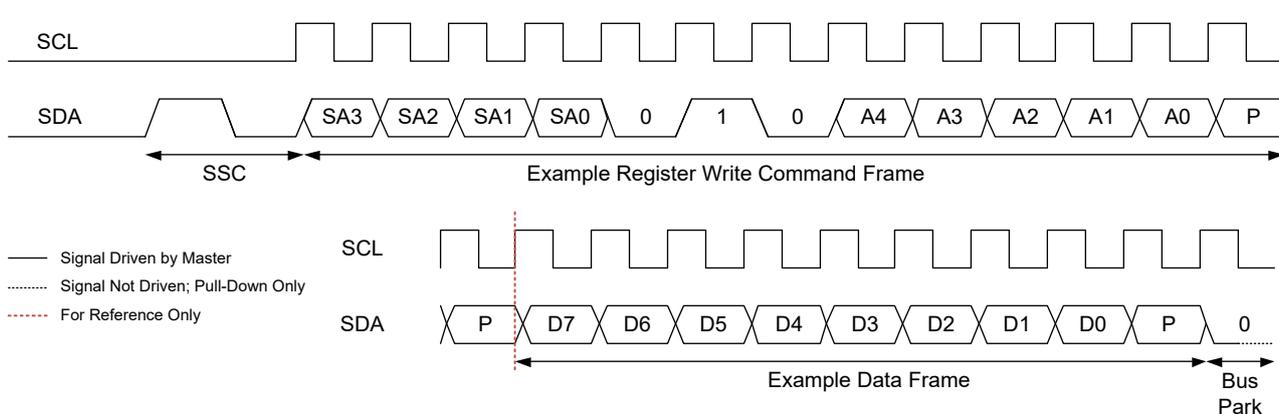


Figure 2. Register Write Command Timing Diagram

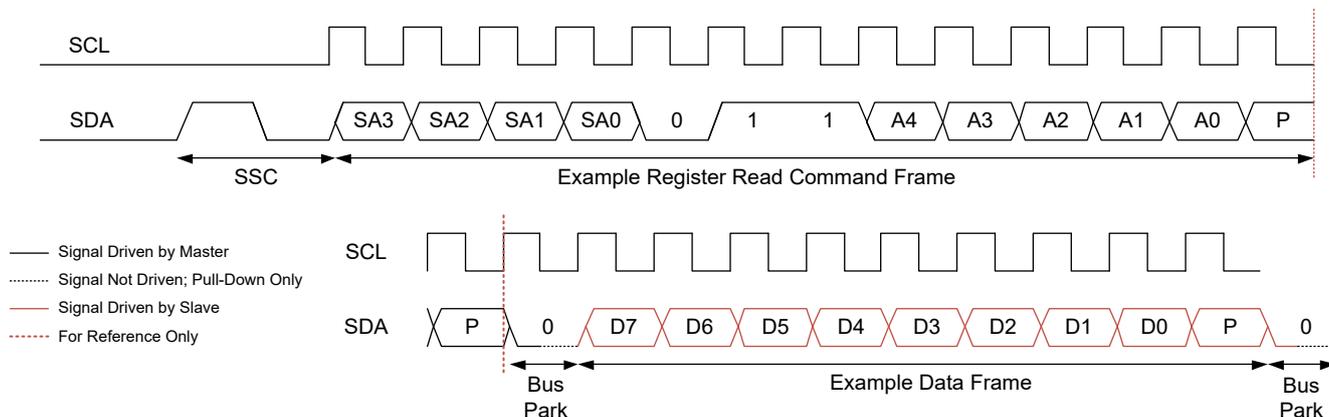


Figure 3. Register Read Command Timing Diagram

COMMAND SEQUENCE BIT DEFINITIONS

Type	SSC	Command Frame Bits					Parity Bits	Bus Park Cycle	Extended Operation					
		C[11:8]	C[7]	C[6:5]	C[4]	C[3:0]			Data Frame Bits	Parity Bits	Bus Park Cycle	Data Frame Bits	Parity Bits	Bus Park Cycle
Reg Write	Y	SA[3:0]	0	10	A[4]	A[3:0]	Y	-	D[7:0]	Y	Y	-	-	-
Reg Read	Y	SA[3:0]	0	11	A[4]	A[3:0]	Y	Y	D[7:0]	Y	Y	-	-	-
Reg0 Write	Y	SA[3:0]	1	D[6:5]	D[4]	D[3:0]	Y	Y	-	-	-	-	-	-

Legends:

SSC = Sequence Start Command

SA = Slave Address

A = Register Address

D = Data Bit

REGISTER MAPS

Register_0

Register Address: 0x00; R/W

Table 3. Register_0 Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:0]	MODE_CTRL	See Table 1 section.	00000000	R/W	No	0, 1, 2

Register_1

Register Address: 0x01; R/W

Table 4. Register_1 Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:0]	MODE_CTRL	See Table 2 section.	00000000	R/W	No	0, 1, 2

PM_TRIG

Register Address: 0x1C; R/W and W

Table 5. PM_TRIG Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7]	PWR_MODE_1	0: Normal 1: Low power	0	R/W	Yes	No
D[6]	PWR_MODE_0	0: Active - Normal 1: Startup - All registers are reset to the default	0	R/W	Yes	No
D[5]	TRIGGER_MASK_2	0: TRIGGER_2 enabled 1: TRIGGER_2 disabled	0	R/W	No	No
D[4]	TRIGGER_MASK_1	0: TRIGGER_1 enabled 1: TRIGGER_1 disabled				
D[3]	TRIGGER_MASK_0	0: TRIGGER_0 enabled 1: TRIGGER_0 disabled				
D[2]	TRIGGER_2	0: Keep its associated destination registers unchanged 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_2 is set to logic '0'	0	W	Yes	No
D[1]	TRIGGER_1	0: Keep its associated destination registers unchanged 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_1 is set to logic '0'	0	W	Yes	No
D[0]	TRIGGER_0	0: Keep its associated destination registers unchanged 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_0 is set to logic '0'	0	W	Yes	No

PRODUCT_ID

Register Address: 0x1D; R

Table 6. PRODUCT_ID Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:0]	PRODUCT_ID	Product number.	00000000	R	No	No

REGISTER MAPS (continued)**MANUFACTURER_ID**

Register Address: 0x1E; R

Table 7. MANUFACTURER_ID Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:0]	MANUFACTURER_ID[7:0]	Lower eight bits of Manufacturer ID. Read-only. Note that during USID programming, the write command sequence is executed on the register, but the value does not change.	01001010	R	No	No

MAN_USID

Register Address: 0x1F; R and R/W

Table 8. MAN_USID Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:6]	Reserved	Reserved.	00	R	No	No
D[5:4]	MANUFACTURER_ID[9:8]	Upper two bits of Manufacturer ID. Read-only. Note that during USID programming, the write command sequence is executed on the register, but the value does not change.	00	R	No	No
D[3:0]	USID	USID of the device.	1011	R/W	No	No

TYPICAL APPLICATION CIRCUIT

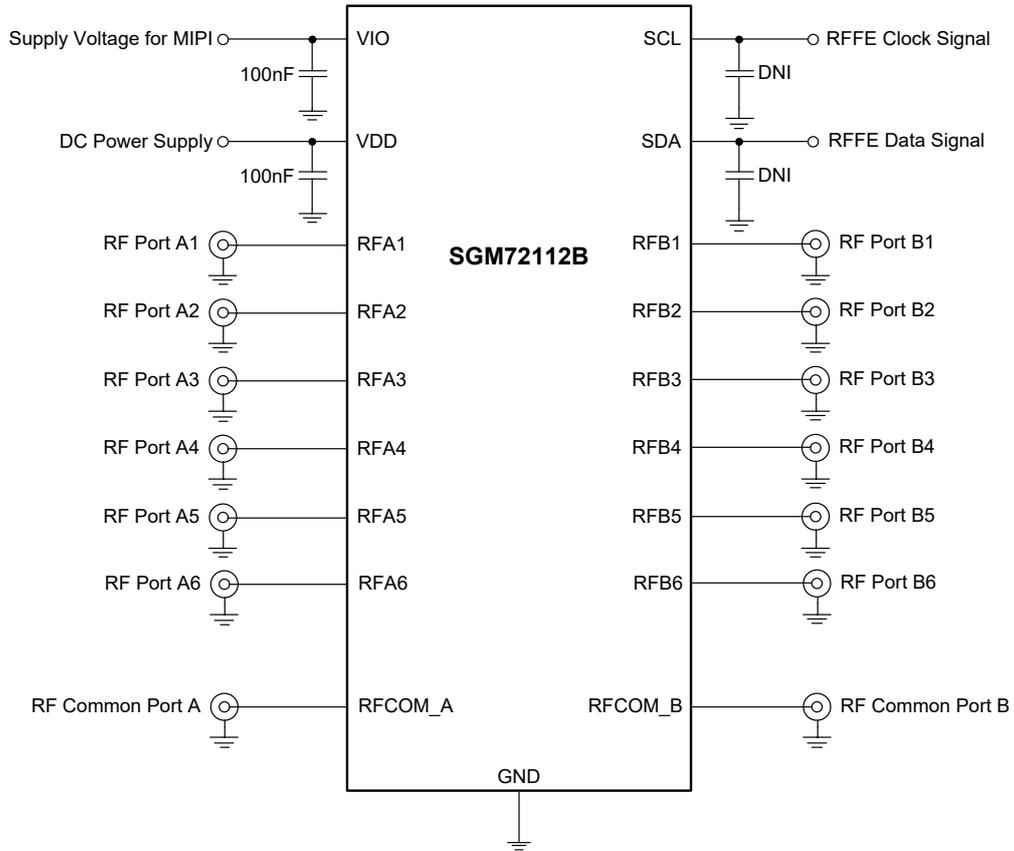


Figure 4. SGM72112B Typical Application Circuit

EVALUATION BOARD LAYOUT

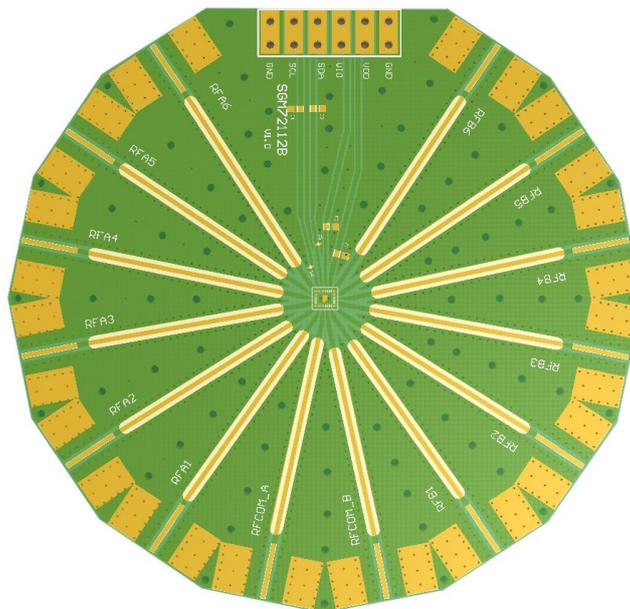


Figure 5. SGM72112B Evaluation Board Layout

REVISION HISTORY

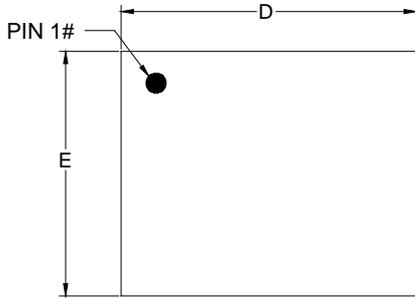
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DECEMBER 2022 - REV.A to REV.A.1	Page
Updated Electrical Characteristics	6

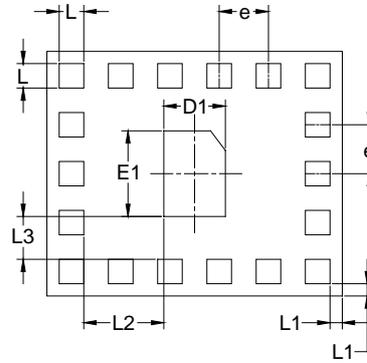
Changes from Original (MAY 2022) to REV.A	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

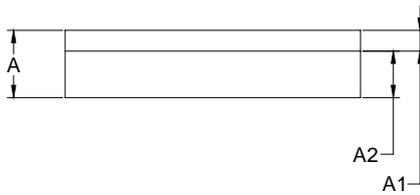
ULGA-2.4x2-18L



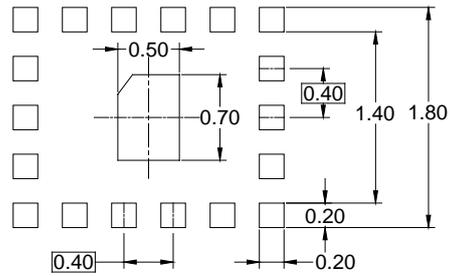
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

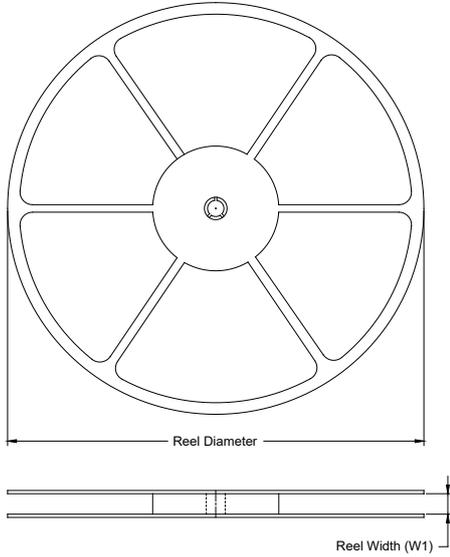
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.500	0.550	0.600
A1	0.140	0.170	0.200
A2	0.380 BSC		
D	2.300	2.400	2.500
E	1.900	2.000	2.100
D1	0.500		
E1	0.700		
e	0.400 BSC		
L	0.200		
L1	0.100		
L2	0.650		
L3	0.350		

NOTE: This drawing is subject to change without notice.

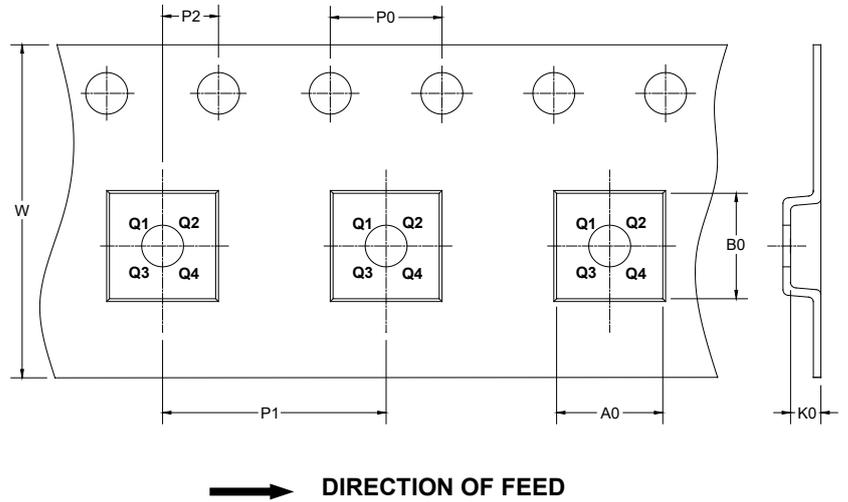
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

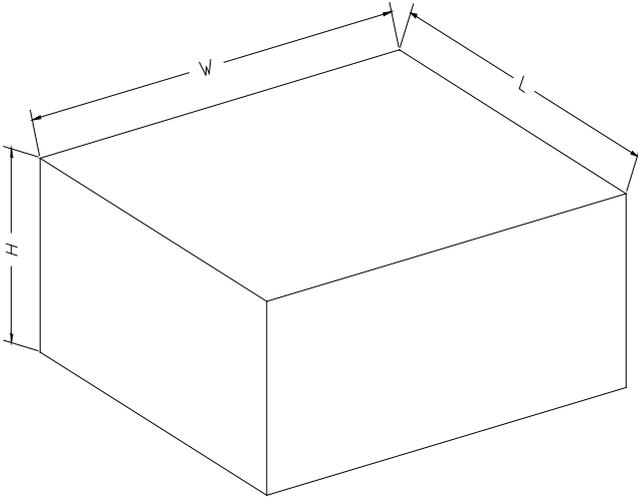
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
ULGA-2.4×2-18L	7"	9.5	2.25	2.65	0.75	4.0	4.0	2.0	8.0	Q2

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

DD0002