SGM41535

2-6 Cell Li+ Battery SMBus Charge Controller with N-Channel Power MOSFET Selector and Advanced Circuit Protection

GENERAL DESCRIPTION

The SGM41535 is a high-efficiency, synchronous battery charger designed for space-constrained applications requiring multi-chemistry battery support. It achieves a compact solution through a low external component count.

This device utilizes two independent charge pumps to drive the N-Channel MOSFETs (ACFET, BATFET, and RBFET) controlling the power path. This architecture enables automated system power source selection.

Input current, charge current, and charge voltage are programmable via SMBus-controlled digital-to-analog converters (DACs). This allows the system power management microcontroller to achieve high regulation accuracies.

The SGM41535 provides charge current limiting through either an internal register or an external ILIM pin, modulating the PWM operation to regulate charge current as required. The device supports charging configurations for 2 to 6 series-connected Li+ cells.

The SGM41535 is available in a Green TQFN-3.5×3.5-20L package.

APPLICATIONS

Industrial and Medical Equipment
Handheld Terminal
Personal Digital Assistant
Ultra-Thin Notebook, and Netbook
Portable Notebook Computers, UMPC
Portable Equipment

FEATURES

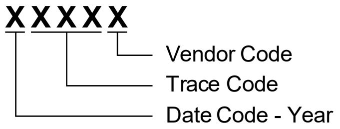
- **SMBus Host-Controlled NMOS-NMOS Synchronous Buck Converter with 615kHz, 750kHz, and 885kHz Programmable Switching Frequencies**
- **Automatic Power Source Selection (Adapter or Battery) through N-channel MOSFETs Driven by Internal Charge Pumps**
- **0.6mA Adapter Standby Quiescent Current for Energy Star**
- **Enhanced Safety Features for Over-Voltage Protection, Over-Current Protection, Battery, Inductor and MOSFET Short-Circuit Protection**
- **Accurate Charge Voltage, Charge Current, and Input Current Limit Programming**
    - **±0.5% Charge Voltage Accuracy up to 27.6V**
    - **±3% Charge Current Accuracy up to 8.128A**
    - **±3% Input Current Accuracy up to 8.128A**
    - **±2% 20× Adapter Current or Charge Current Amplifier Output Accuracy**
- **Comprehensive Integrated Charging Functions**
    - **Battery LEARN Function**
    - **Programmable Battery Depletion Threshold**
    - **Bootstrap (BTST) Diode**
- **Programmable Adapter Presence Monitoring with Indicator**
- **Integrated Charge Current Soft-Start**
- **Integrated Loop Compensation**
- **Real Time System Control with ILIM Pin Charge Current Limit**
- **AC Adapter Operating Range: 4.5V to 30V**
- **Off-State Battery Discharge Current: 2μA**
- **Available in the Green TQFN-3.5×3.5-20L Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41535	TQFN-3.5×3.5-20L	-40℃ to +125℃	SGM41535YTRL20G/TR	SGM1TK YTRL20 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range
ACN, ACP, SRN, SRP, CMSRC, VCC .... -0.3V to 32V
PHASE .... -2V to 32V
ACDET, SDA, SCL, LODRV, REGN, IOUT, ILIM, ACOK .... -0.3V to 6.5V
BTST, HIDRV, ACDRV, BATDRV.................... -0.3V to 38V
Maximum Difference Voltage
SRP-SRN, ACP-ACN..................................... -0.5V to 0.5V
Package Thermal Resistance
TQFN-3.5×3.5-20L, θ_{JA} .... 35.9℃/W
TQFN-3.5×3.5-20L, θ_{JB} .... 12.1℃/W
TQFN-3.5×3.5-20L, $\theta_{JC\ (TOP)}$ .... 31.2℃/W
TQFN-3.5×3.5-20L, $\theta_{JC\ (BOT)}$ .... 2.2℃/W
Junction Temperature...+150℃
Storage Temperature Range ....-65℃ to +150℃
Lead Temperature (Soldering, 10s)............................+260℃
ESD Susceptibility (1) (2)
HBM...±3000V
CDM ....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Voltage Range
ACN, ACP, SRN, SRP, CMSRC, VCC ....0V to 30V
PHASE .... -2V to 30V
ACDET, SDA, SCL, IOUT, ILIM, ACOK ....0V to 5V
LODRV, REGN..0V to 6V
BTST, HIDRV, ACDRV, BATDRV ....0V to 36V
Differential Voltage
SRP-SRN, ACP-ACN ....-0.4V to 0.4V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

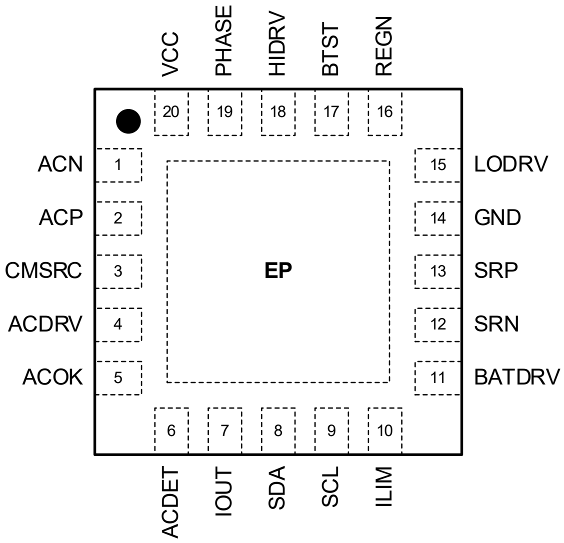
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3.5×3.5-20L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	ACN	Input Current Sense Resistor Negative Input. It is recommended to place a 0.1μF ceramic capacitor between the ACN pin and GND for common mode filtering, and a 0.1μF ceramic capacitor between ACN and ACP for differential mode filtering.
2	ACP	Input Current Sense Resistor Positive Input. It is recommended to place a 0.1μF ceramic capacitor between the ACP pin and GND for common mode filtering, and a 0.1μF ceramic capacitor between ACN and ACP for differential mode filtering.
3	CMSRC	ACDRV Charge Pump Source Input. Connect the CMSRC pin to the common-source node of ACFET (Q1) and RBFET (Q2) via a 4.02kΩ resistor to limit the inrush current at the CMSRC pin.
4	ACDRV	Charge Pump Output to Drive both Adapter Input N-MOSFET (ACFET) and Reverse Blocking N-MOSFET (RBFET). The ACDRV pin generates a voltage 6V above the CMSRC pin under specific operational prerequisites. These prerequisites include: a voltage on the ACDET pin within the range of 2.4V to 3.15V, a voltage on the VCC pin exceeding its under-voltage lockout (UVLO) threshold, and a voltage on the VCC pin exceeding the voltage on the SRN pin by at least 355mV. When these conditions are satisfied, the ACDRV voltage enables the ACFET and RBFET, allowing the system to be powered from the AC adapter source. Connect the ARDRV pin to the common-gate node of ACFET (Q_1) and RBFET (Q_2) via a 4.02kΩ resistor to limit the inrush current during ACFET/RBFET turn-on.
5	ACOK	AC Adapter Detection Open-Drain Output. The ACOK output is asserted high when the following conditions are simultaneously met: the ACDET pin voltage is within the range of 2.4V to 3.15V; the VCC pin voltage exceeds its under-voltage lockout (UVLO) threshold; and the VCC pin voltage is at least 355mV above the SRN pin voltage. This state indicates the presence of a valid adapter, enabling the initiation of charging. Under these conditions, the ACOK pin is pulled high to the external pull-up supply rail via a 10kΩ external pull-up resistor. If any one of the above conditions is not satisfied, the ACOK output is de-asserted. In this state, an internal MOSFET actively pulls the ACOK pin low to GND.
6	ACDET	Adapter Detection Input. A resistor divider from the input adapter positive line is connected to this pin to program the detection voltage threshold. Upon meeting the following conditions simultaneously: the voltage on the ACDET pin exceeds 0.6V, the voltage on the VCC pin is above its under-voltage lockout (UVLO) threshold, and the REGN low-dropout regulator (LDO) is operational, the ACOK comparator and the IOUT function are enabled.
7	IOUT	Sensed Adapter or Charge Current Buffered Output. The input of buffer is selectable through SMBus command ChargeOption register. The IOUT pin provides an output voltage that scales proportionally with the differential voltage present across the external current sense resistor. To ensure stable operation, a ceramic decoupling capacitor with a maximum value of 100pF must be connected between the IOUT pin and ground (GND).
8	SDA	SMBus Open-Drain Data I/O. The SDA pin should be linked to the host controller or smart battery SMBus data line. A 10kΩ pull-up resistor must be implemented between the SDA line and the supply voltage in accordance with SMBus specifications.

PIN DESCRIPTION (continued)

PIN	NAME	FUNCTION
9	SCL	SMBus Open-Drain Clock Input. The SCL pin should be linked to the host controller or smart battery SMBus clock line. A 10kΩ pull-up resistor must be implemented between the SCL line and the supply voltage in accordance with SMBus specifications.
10	ILIM	Charge Current Limit Input. The ILIM pin voltage is programmed using a resistor divider network connected between the 3.3V reference rails, the ILIM pin, and ground (GND). The effective charge current regulation limit is determined by the lower value between the programmed ILIM pin voltage and the DAC limit voltage. When the ILIM pin voltage exceeds 1.6V, the ILIM-based current regulation is disabled. Charge operation is disabled when the ILIM pin voltage falls below 75mV. Charging resumes once the voltage on the ILIM pin exceeds 105mV.
11	BATDRV	Charge Pump Output to Drive Battery to System N-MOSFET (BATFET). The BATDRV pin is configured to generate a voltage 5.7V above the SRN pin potential. This bias voltage turns on the BATFET (Q5), enabling the system to be powered from the battery source. During AC adapter operation, the BATDRV pin voltage is maintained at the SRN pin potential. This configuration turns off the BATFET (Q5), isolating the battery path while the system is powered from the adapter. Connect a 4.02kΩ series resistor between BATDRV and the gate of BATFET (Q_5) to limit inrush current during BATFET turn-on.
12	SRN	Charge Current Sense Resistor Negative Input. The SRN pin serves as the input for battery voltage sensing. To implement common-mode filtering, connect a 0.1μF ceramic capacitor between the SRN pin and ground (GND) for common-mode filtering. A series 10Ω resistor must be connected between the SRN pin and the current sensing resistor network. A 0.1μF ceramic capacitor should be placed directly across the terminals of the current-sense resistor for differential-mode filtering. For protection against hard short-circuit conditions (battery-to-ground faults or reverse battery connections), refer to the Application Information section regarding negative output voltage protection. This section details the implementation using an additional small-value series resistor.
13	SRP	Charge Current Sense Resistor Positive Input. A 10Ω series resistor must connect the SRP pin to the current sense resistor network. For differential-mode noise suppression, connect a 0.1μF ceramic capacitor directly across the current sense resistor terminals and a 0.1μF ceramic capacitor (SRP to GND) for common-mode filtering. Refer to the Application Information section for negative output voltage protection during hard short-circuit conditions (battery-to-ground faults or reverse battery connections). This protection is implemented through an additional small-value series resistor in the current path.
14	GND	Device Ground Return. Connect this pin to the analog ground plane of the PCB and also to the PCB power ground plane only at one point (at the thermal pad under the device).
15	LODRV	Low-side (LS) Switching N-MOSFET Gate Driving Output.
16	REGN	Linear Regulator Output. The REGN pin provides the 6.15V output from an internal low-dropout (LDO) linear regulator. This regulator derives its input supply directly from the VCC pin. The LDO becomes operational when both of the following conditions are satisfied: the voltage on the ACDET pin exceeds 0.6V, and the voltage on the VCC pin remains above its under-voltage lockout (UVLO) threshold. A 1μF ceramic capacitor must be connected between the REGN pin and ground (GND) to ensure stable regulator operation and suppress noise.
17	BTST	High-side (HS) Switching N-MOSFET Gate Driver Power Supply. Connect BTST and PHASE pins with a 47nF bootstrap capacitor from BTST to PHASE. The bootstrap diode is integrated.
18	HIDRV	High-side (HS) Switching N-MOSFET Gate Driving Output.
19	PHASE	High-side (HS) Switching MOSFET Source Connection. PHASE is connected to the switching node of the converter.
20	VCC	Device Supply Pin. It is powered from adapter or battery. Use a 10Ω (1206 size is recommended) and a 1μF low pass filter on VCC to limit inrush current. Connect VCC to the battery and adapter lines with a Schottky diode
-	Exposed Pad	Exposed Pad beneath the Device. Analog and power grounds are star-connected only at this point (Exposed pad plane). Solder this pad to the PCB copper plane and consider sufficient number of thermal vias under the device connected to other layers ground planes to facilitate heat relief.

ELECTRICAL CHARACTERISTICS

(V_{VCC} = 4.5V to 30V, T_J = 0℃ to +125℃, typical values are measured at T_A = +25℃, with respect to GND unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Conditions						
VCC Input Voltage Operating Range	V_{CC_OP}		4.5		30	V
Charge Voltage Regulation						
BAT Voltage Regulation Range	$V_{BAT\_REG\_RNG}$		1.024		27.6	V
Charge Voltage Regulation Initial Accuracy	$V_{BAT\_REG\_ACC}$	ChargeVoltage register = 0x6270	25.074	25.2	25.326	
			-0.5%		0.5%	
		ChargeVoltage register = 0x5210	20.903	21.008	21.113	
			-0.5%		0.5%	
		ChargeVoltage register = 0x41A0	16.733	16.8	16.867	
			-0.4%		0.4%	
		ChargeVoltage register = 0x3130	12.542	12.592	12.667	
			–0.4%		0.6%	
		ChargeVoltage register = 0x20D0	8.375	8.4	8.492	
Charge Current Regulation						
Charge Current Regulation Differential Voltage Range	$V_{IREG\_CHG\_RNG}$	$V_{IREG\_CHG} = V_{SRP} - V_{SRN}$	0		81.28	mV
Charge Current Regulation Accuracy 10mΩ Current Sensing Resistor	$I_{CHRG\_REG\_ACC}$	ChargeCurrent register = 0x1000	3994	4096	4198	mA
			-2.5%		2.5%	
		ChargeCurrent register = 0x0800	1967	2048	2129	
			-4%		4%	
		ChargeCurrent register = 0x0200	436	512	588	
			-15%		15%	
		ChargeCurrent register = 0x0100	192	256	320	
			-25%		25%	
		ChargeCurrent register = 0x0080	64	128	192	
			-50%		50%	
Input Current Regulation						
Input Current Regulation Differential Voltage Range	$V_{IREG\_DPM\_RNG}$	$V_{IREG\_DPM} = V_{ACP} – V_{ACN}$	0		81.28	mV
Input Current Regulation Accuracy 10mΩ Current Sensing Resistor	$I_{DPM\_REG\_ACC}$	InputCurrent register = 0x1000	3974	4096	4218	mA
			-3%		3%	
		InputCurrent register = 0x0800	1946	2048	2150	
			-5%		5%	
		InputCurrent register = 0x0400	871	1024	1177	
			-15%		15%	
		InputCurrent register = 0x0200	384	512	640	
			-25%		25%	
Input Current or Charge Current Sense Amplifier						
Input common mode range	V_{ACP/N_OP}	Voltage on ACP/ACN	4.5		30	V
Output Common Mode Range	V_{SRP/N_OP}	Voltage on SRP/SRN	0		27.6	V
IOUT Output Voltage Range	V_{IOUT}		0		3.2	V
IOUT Output Current	I_{IOUT}		0		1	mA
Current Sense Amplifier Gain	A_{IOUT}	$V_{ICOUT}/V_{SRP-SRN}$ or $V_{ACP} - V_{ACN}$		20		V/V

ELECTRICAL CHARACTERISTICS (continued)

(V_{VCC} = 4.5V to 30V, T_J = 0℃ to +125℃, typical values are measured at T_A = +25℃, with respect to GND unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Output Accuracy	V_{IOUT_ACC}	$V_{SRP-SRN}$ or $V_{ACP-ACN}$ = 40.96mV	-2		2	%
		$V_{SRP-SRN}$ or $V_{ACP-ACN}$ = 20.48mV	-4		4	
		$V_{SRP-SRN}$ or $V_{ACP-ACN}$ = 10.24mV	-15		15	
		$V_{SRP-SRN}$ or $V_{ACP-ACN}$ = 5.12mV	-20		20	
		$V_{SRP-SRN}$ or $V_{ACP-ACN}$ = 2.56mV	-30		30	
		$V_{SRP-SRN}$ or $V_{ACP-ACN}$ = 1.28mV	-50		50	
Maximum Output Load Capacitance	C_{IOUT_MAX}	For stability with 0mA to 1mA load			100	pF
REGN Regulator						
REGN Regulator Voltage	V_{REGN_REG}	V_{VCC} > 6.5V, V_{ACDET} > 0.6V (0mA to 55mA load)	5.8	6.15	6.5	V
REGN Current Limit	I_{REGN_LIM}	V_{REGN} = 0V, V_{VCC} > UVLO charge enabled and not in TSD	40	60		mA
		V_{REGN} = 0V, V_{VCC} > UVLO charge disabled or in TSD	7	13		
REGN Output Capacitor Required for Stability	C_{REGN}	I_{LOAD} = 100μA to 65mA		1		μF
Input Under-Voltage Lockout Comparator (UVLO)						
Under-Voltage Rising Threshold	V_{UVLO}	V_{CC} rising	3.4	3.65	3.9	V
Under-Voltage Falling Hysteresis	$V_{UVLO\_HYS\_F}$	V_{CC} falling		300		mV
Fast DPM Comparator (FAST_DPM)						
Fast DPM Comparator Stop Charging Rising Threshold with Respect to Input Current Limit, Voltage across Input Sense Resistor Rising Edge	V_{FAST_DPM}	Specified by design		107		%
Quiescent Current						
Battery BATFET Off State Current, BATFET Off, I_{SRP} + I_{SRN} + I_{PHASE} + I_{ACP} + I_{ACN}	$I_{BAT\_BATFET\_OFF}$	V_{BAT} = 16.8V, VCC disconnect from battery, BATFET charge pump off, BATFET turns off, T_J = 0℃ to +85℃			2	μA
Battery BATFET On State Current, BATFET On, I_{SRP} + I_{SRN} + I_{PHASE} + I_{VCC} + I_{ACP} + I_{ACN}	$I_{BAT\_BATFET\_ON}$	V_{BAT} = 16.8V, VCC connect from battery, BATFET charge pump on, BATFET turns on, T_J = 0℃ to +85℃			20	μA
Standby Quiescent Current, I_{VCC} + I_{ACP} + I_{ACN}	$I_{STANDBY}$	V_{CC} > UVLO, V_{ACDET} > 2.4V, charge disabled, T_J = 0℃ to +85℃		0.6	1	mA
Adapter Bias Current during Charge, I_{VCC} + I_{ACP} + I_{ACN}	I_{AC_NOSW}	V_{CC} > UVLO, 2.4V < V_{ACDET} < 3.15V, charge enabled, no switching, T_J = 0℃ to +85℃		1.5	2.5	mA
Adapter Bias Current during Charge, I_{VCC} + I_{ACP} + I_{ACN}	I_{AC_SW}	V_{CC} > UVLO, 2.4V < V_{ACDET} < 3.15V, charge enabled, switching, MOSFET Sis412DN		10		mA
ACOK Comparator						
ACOK Rising Threshold	V_{ACOK_RISE}	V_{CC} > UVLO, V_{ACDET} rising	2.35	2.4	2.46	V
ACOK Falling Hysteresis	$V_{ACOK\_FALL\_HYS}$	V_{CC}> UVLO, V_{ACDET} falling	35	55	75	mV
ACOK Rising Deglitch	$V_{ACOK\_RISE\_DEG}$	V_{CC}> UVLO, V_{ACDET} rising above 2.4V, First time or ChargeOption bit[15] = 0 (default, Specified by design)	100	140	180	ms
		V_{CC}> UVLO, V_{ACDET} rising above 2.4V, (NOT First time) and ChargeOption bit[15] = 1	0.8	1.1	1.4	s
WAKEUP Detect Rising Threshold	V_{WAKEUP_RISE}	V_{CC}> UVLO, V_{ACDET} rising		0.6	0.7	V
WAKEUP Detect Falling Threshold	V_{WAKEUP_FALL}	V_{CC}> UVLO, V_{ACDET} falling	0.4	0.5		V
VCC to SRN Comparator (VCC_SRN)						
VCC to SRN Falling Threshold	$V_{VCC-SRN\_F}$	V_{CC} falling towards V_{SRN}	55	115	175	mV
VCC to SRN Rising Hysteresis	$V_{VCC-SRN\_R\_HYS}$	V_{CC} rising above V_{SRN}	190	240	290	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{VCC} = 4.5V to 30V, T_J = 0℃ to +125℃, typical values are measured at T_A = +25℃, with respect to GND unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACN to SRN Comparator (ACN_SRN)						
ACN to BAT Falling Threshold	$V_{\text{ACN-SRN\_F}}$	V_{ACN} falling towards V_{SRN}	110	195	270	mV
ACN to BAT Rising Hysteresis	$V_{\text{ACN-SRN\_R\_HYS}}$	V_{ACN} rising above V_{SRN}	40	80	120	mV
High-side IFAULT Comparator (IFAULT_HI) (1)						
ACP to PHASE Rising Threshold	$V_{\text{IFAULT\_HI\_RISE}}$	ChargeOption register bit[8:7] = 00	350	500	650	mV
		ChargeOption register bit[8:7] = 01	500	700	900	
		ChargeOption register bit[8:7] = 10 (default)	650	900	1150	
		ChargeOption register bit[8:7] = 11	800	1100	1400	
Low-side IFAULT Comparator (IFAULT_LOW)						
PHASE to GND Rising Threshold	$V_{\text{IFAULT\_LOW\_RISE}}$		50	130	230	mV
Input Over-Voltage Comparator (ACOV)						
ACDET Over-Voltage Rising Threshold	V_{ACOV}	V_{ACDET} rising	3.05	3.15	3.25	V
ACDET Over Voltage Falling Hysteresis	$V_{\text{ACOV\_HYS}}$	V_{ACDET} falling	50	80	110	mV
Input Over-Current Comparator (ACOC) (1)						
Adapter Over-Current Rising Threshold with Respect to Input Current Limit, Voltage across Input Sense Resistor Rising Edge	V_{ACOC}	ChargeOption register bit[2:1] = 01	120	133	145	%
		ChargeOption register bit[2:1] = 10 (default)	150	166	180	
		ChargeOption register bit[2:1] = 11	200	222	240	
Min ACOC Threshold Clamp Voltage	$V_{\text{ACOC\_MIN}}$	ChargeOption register bit[2:1] = 01 (133%), InputCurrent register = 0x0400 (10.24mV)	40	45	50	mV
Max ACOC Threshold Clamp Voltage	$V_{\text{ACOC\_MAX}}$	ChargeOption register bit[2:1] = 11 (222%), InputCurrent register = 0x1F80 (80.64mV)	140	150	160	mV
ACOC Deglitch Time	$t_{\text{ACOC\_DEG}}$	Voltage across input sense resistor rising to disable charge (specified by design)	1.6	2.15	2.7	ms
BAT Over-Voltage Comparator (BAT_OVP)						
Over-Voltage Rising Threshold as Percentage of $V_{\text{BAT\_REG}}$	$V_{\text{OVP\_RISE}}$	V_{SRN} rising	103	104	106	%
Over-Voltage Falling Threshold as Percentage of $V_{\text{BAT\_REG}}$	$V_{\text{OVP\_FALL}}$	V_{SRN} falling		102		%
Charge Over-Current Comparator (CHG_OCP)						
Charge Over-Current Rising Threshold, Measure Voltage Drop across Current Sensing Resistor	$V_{\text{OCP\_RISE}}$	ChargeCurrent register = 0x0xxx	49	55	61	mV
		ChargeCurrent register = 0x1000 - 0x17C0	75	85	95	mV
		ChargeCurrent register = 0x1800 - 0x1FC0	95	110	125	mV
Charge Under-Current Comparator (CHG_UCP)						
Charge Under-Current Falling Threshold	$V_{\text{UCP\_FALL}}$	V_{SRP} falling towards V_{SRN}	1	6	11	mV
Light Load Comparator (LIGHT_LOAD)						
Light Load Falling Threshold	$V_{\text{LL\_FALL}}$	Measure the voltage drop across current sensing resistor		1.25		mV
Light Load Rising Hysteresis	$V_{\text{LL\_RISE\_HYS}}$			1.25		mV
Battery Depletion Comparator (BAT_DEPL) (1)						
Battery Depletion Falling Threshold, Percentage of Voltage Regulation Limit, VSRN Falling	$V_{\text{BATDEPL\_FALL}}$	ChargeOption register bit[12:11] = 00	57	60	63	%
		ChargeOption register bit[12:11] = 01	60	63	66	
		ChargeOption register bit[12:11] = 10	64	67	70	
		ChargeOption register bit[12:11] = 11 (default)	69	72	75	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VCC} = 4.5V to 30V, T_J = 0℃ to +125℃, typical values are measured at T_A = +25℃, with respect to GND unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery Depletion Rising Hysteresis, VSRN Rising	$V_{BATDEPL\_RHYST}$	ChargeOption register bit[12:11] = 00	205	285	425	mV
		ChargeOption register bit[12:11] = 01	215	300	465	mV
		ChargeOption register bit[12:11] = 10	230	320	495	mV
		ChargeOption register bit[12:11] = 11 (default)	245	345	525	mV
Battery Depletion Rising Deglitch (Specified by Design)	$t_{BATDEPL\_RDEG}$	Delay to turn off ACFET and turn on BATFET during LEARN cycle		550		ms
Battery LOWV Comparator (BAT_LOWV)						
Battery LOWV Falling Threshold	V_{BATLV_FALL}	V_{SRN} falling	2.35	2.5	2.65	V
Battery LOWV Rising Hysteresis	V_{BATLV_RHYST}	V_{SRN} rising		230		mV
Battery LOWV Charge Current Limit	I_{BATLV}	10mΩ current sensing resistor		0.5		A
Thermal Shutdown Comparator (TSD)						
Thermal Shutdown Rising Temperature	T_{SD}	Temperature rising		155		℃
Thermal Shutdown Falling Hysteresis	T_{HYS}	Temperature falling		20		℃
ILIM Comparator						
ILIM as CE Falling Threshold	V_{ILIM_FALL}	V_{ILIM} falling	50	75	100	mV
ILIM as CE Rising Threshold	VI_{LIM_RISE}	V_{ILIM} rising	80	105	130	mV
Logic Input (SDA, SCL)						
Input Low Threshold	V_{IN_LO}				0.7	V
Input High Threshold	V_{IN_HI}		2.1			V
Input Bias Current	I_{IN_LEAK}	V = 7V	-1		1	μA
Logic Output Open-Drain (ACOK, SDA)						
Output Saturation Voltage	V_{OUT_LO}	5mA drain current			400	mV
Leakage Current	I_{OUT_LEAK}	V = 7V	-1		1	μA
Analog Input (ACDET, ILIM)						
Input Bias Current	I_{IN_LEAK}	V = 7V	-1		1	μA
PWM Oscillator						
PWM Switching Frequency	f_{SW}	ChargeOption register bit[9] = 0 (default)	650	750	850	kHz
PWM Increase Frequency	f_{SW+}	ChargeOption register bit[10:9] = 11	770	885	1000	kHz
PWM Decrease Frequency	f_{SW-}	ChargeOption register bit[10:9] = 01	515	615	715	kHz
BATFET Gate Driver (BATDRV)						
BATDRV Charge Pump Current Limit	I_{BATFET}		20	60		μA
Gate Drive Voltage on BATFET	V_{BATFET}	V_{BATDRV} - V_{SRN} when V_{SRN} > UVLO	5.1	5.7	6.2	V
Minimum Load Resistance between BATDRV and SRN	R_{BATDRV_LOAD}			500		kΩ
BATDRV Turn-Off Resistance	R_{BATDRV_OFF}	I = 30μA	4.1	6.2	7.3	kΩ
ACFET Gate Driver (ACDRV)						
ACDRV Charge Pump Current Limit	I_{ACFET}		70	160		μA
Gate Drive Voltage on ACFET	V_{ACFET}	V_{ACDRV} - V_{CMSRC} when V_{CC} > UVLO	5.5	6.0	6.5	V
Minimum Load Resistance between ACDRV and CMSRC	R_{ACDRV_LOAD}			50		kΩ
ACDRV Turn-Off Resistance	R_{ACDRV_OFF}	I = 30μA	3.8	6.3	7.7	kΩ
ACDRV Turn-Off When VGS Voltage is Low	V_{ACFET_LOW}	Specified By design		5.4		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{VCC} = 4.5V to 30V, T_J = 0℃ to +125℃, typical values are measured at T_A = +25℃, with respect to GND unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM High-side Driver (HIDRV)						
High-side Driver (HSD) Turn-On Resistance	R_{DSON}	V_{BTST} - V_{PH} = 5.5V, I = 10mA		7	12	Ω
High-side Driver Turn-Off Resistance		V_{BTST} - V_{PH} = 5.5V, I = 10mA		0.5	1.3	Ω
Bootstrap Refresh Comparator Threshold Voltage	$V_{BTST\_REFRESH}$	V_{BTST} - V_{PH} when low side refresh pulse is requested	3.1	3.5	3.8	V
PWM Low-side Driver (LODRV)						
Low-side Driver (LSD) Turn-On Resistance	R_{DSON}	V_{REGN} = 6V, I = 10mA		7	12	Ω
Low-side Driver Turn-Off Resistance		V_{REGN} = 6V, I = 10mA		0.5	1.3	Ω
PWM Driver Timing						
Driver Dead Time from Low-side to High-side	t_{LOW_HIGH}			20		ns
Driver Dead Time from High-side to Low-side	t_{HIGH_LOW}			20		ns
Internal Soft-Start						
Soft-Start Current Step	I_{STEP}	In CCM mode 10mΩ current sensing resistor		64		mA
Soft-Start Current Step Time	t_{STEP}			240		µs

NOTE: 1. User can adjust threshold via ChargeOption register REG0x12 of the SMBus.

TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCLK/SDATA Rise Time	t_R			1	μs
SCLK/SDATA Fall Time	t_F			300	ns
SCLK Pulse Width High	t_{W_H}	4		50	μs
SCLK Pulse Width Low	t_{W_L}	4.7			μs
Setup Time for START Condition	t_{SU_STA}	4.7			μs
START Condition Hold Time after Which First Clock Pulse is Generated	t_{H_STA}	4			μs
Data Setup Time	t_{SU_DAT}	250			ns
Data Hold Time	$t_{H\text{-}DAT}$	300			ns
Setup Time for STOP Condition	t_{SU_STOP}	4			μs
Bus Free Time between START and STOP Condition	t_{BUF}	4.7			μs
Clock Frequency	f_{S_CL}	10		100	kHz

HOST COMMUNICATION FAILURE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SMBus Bus Release Timeout (1)	$t_{TIMEOUT}$	18	25	35	ms
Watchdog Timeout Period, ChargeOption register bit[14:13] = 01 (2)	t_{WDI}	30	38	46	s
Watchdog Timeout Period, ChargeOption register bit[14:13] = 10 (2)		60	76	92	s
Watchdog Timeout Period, ChargeOption register bit[14:13] = 11 (2) (default)		120	152	184	s

NOTES:

1. For transfer devices, a timeout is triggered if the clock low level exceeds the 25ms timeout value; upon detecting a timeout, the device must reset communication within the 35ms maximum timeout value.

2. User can adjust threshold via ChargeOption register REG0x12 of the SMBus.

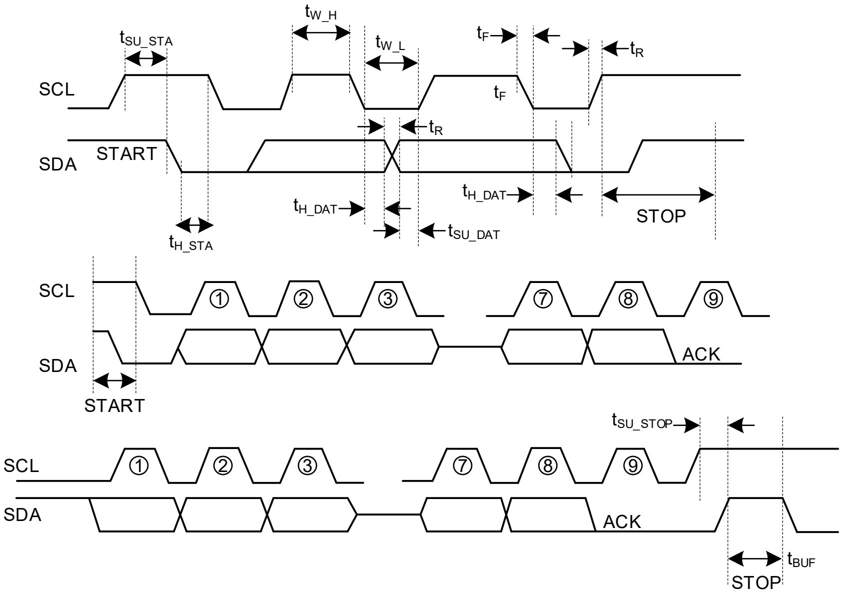
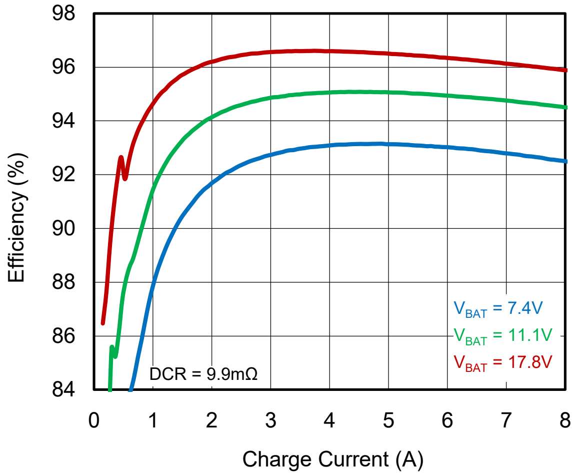


Figure 1. SMBus Communication Timing Waveforms

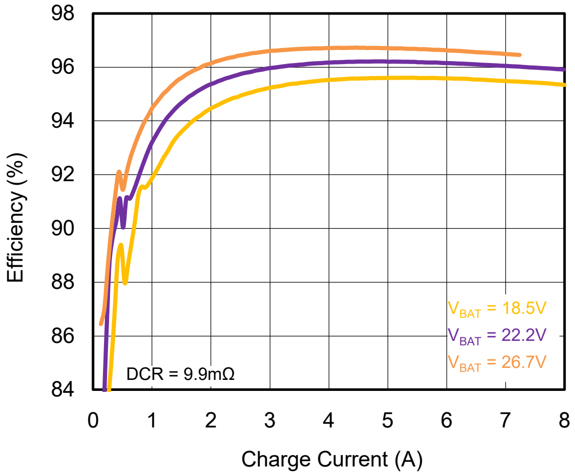
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

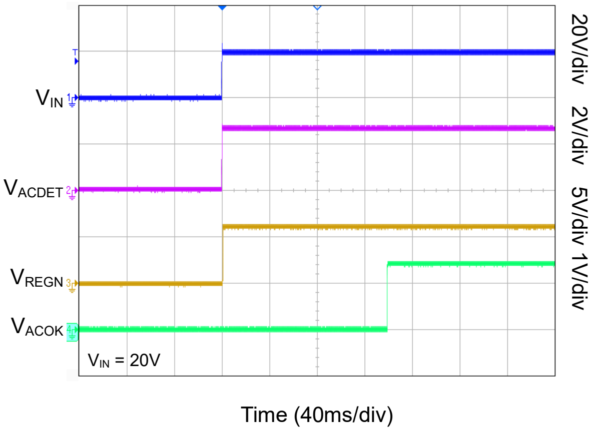
Efficiency at V_{IN} = 20V



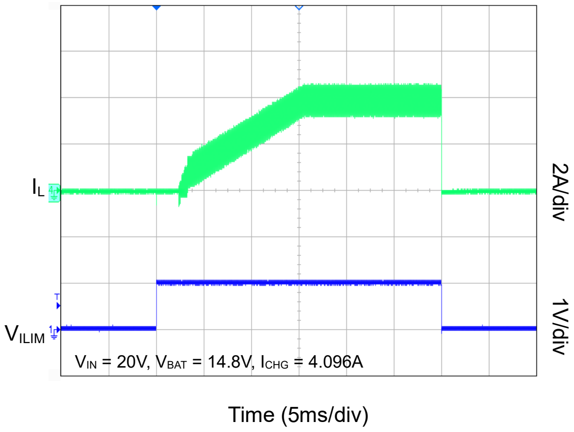
Efficiency at V_{IN} = 30V



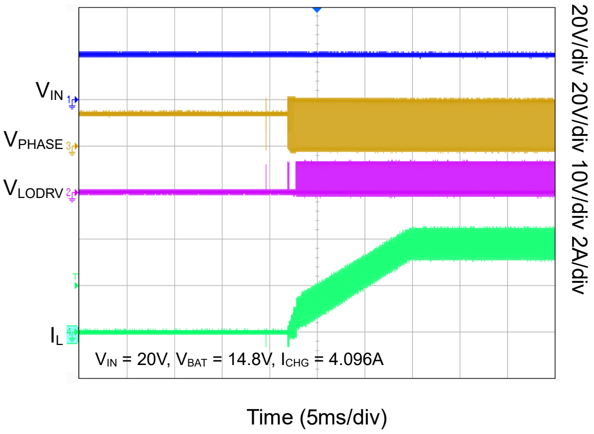
VCC, ACDET, REGN and ACOK during Power-Up



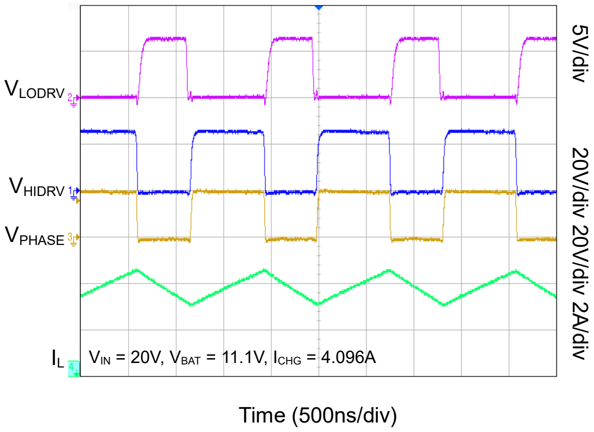
Charge Enable by ILIM



Current Soft-Start



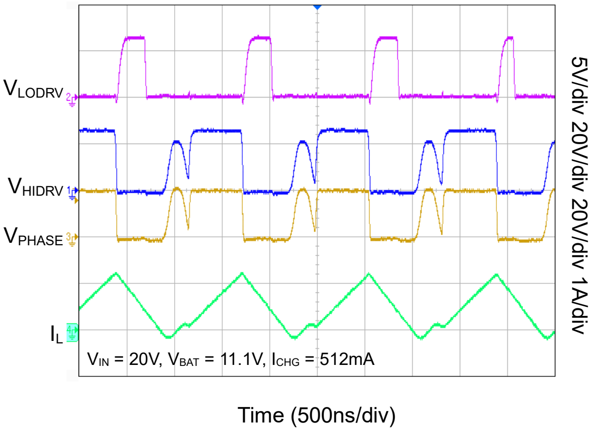
CCM during Charging



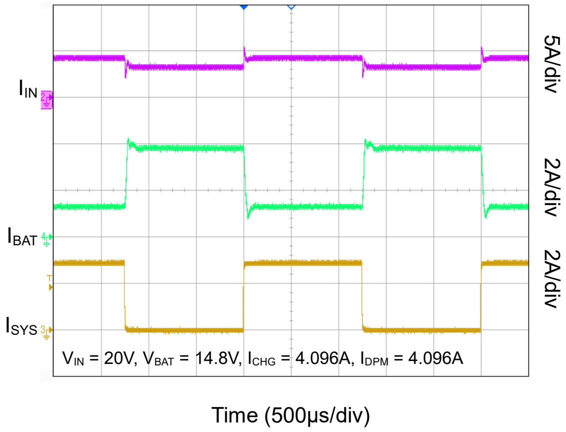
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

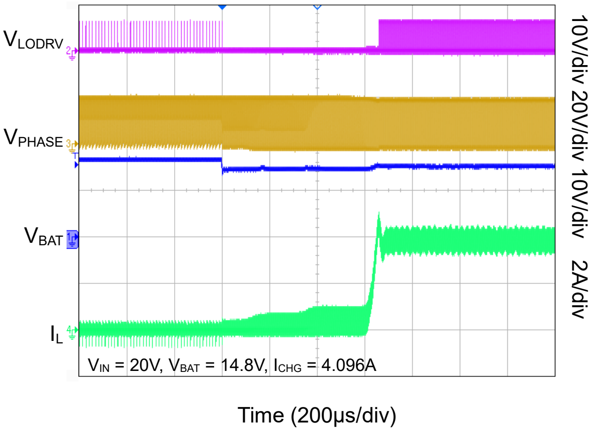
DCM during Charging



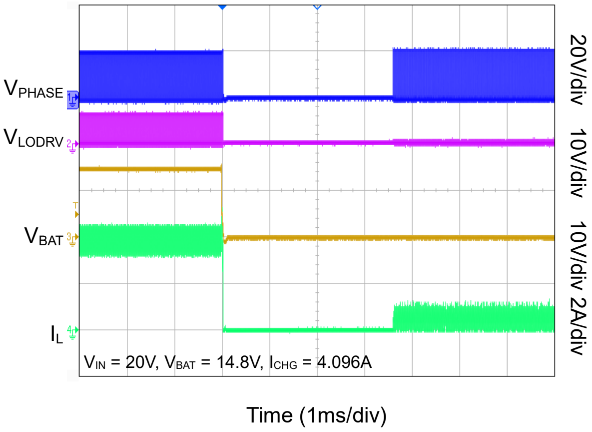
System Load Transient



Battery Insertion



Battery to Ground Short Protection



FUNCTIONAL BLOCK DIAGRAM

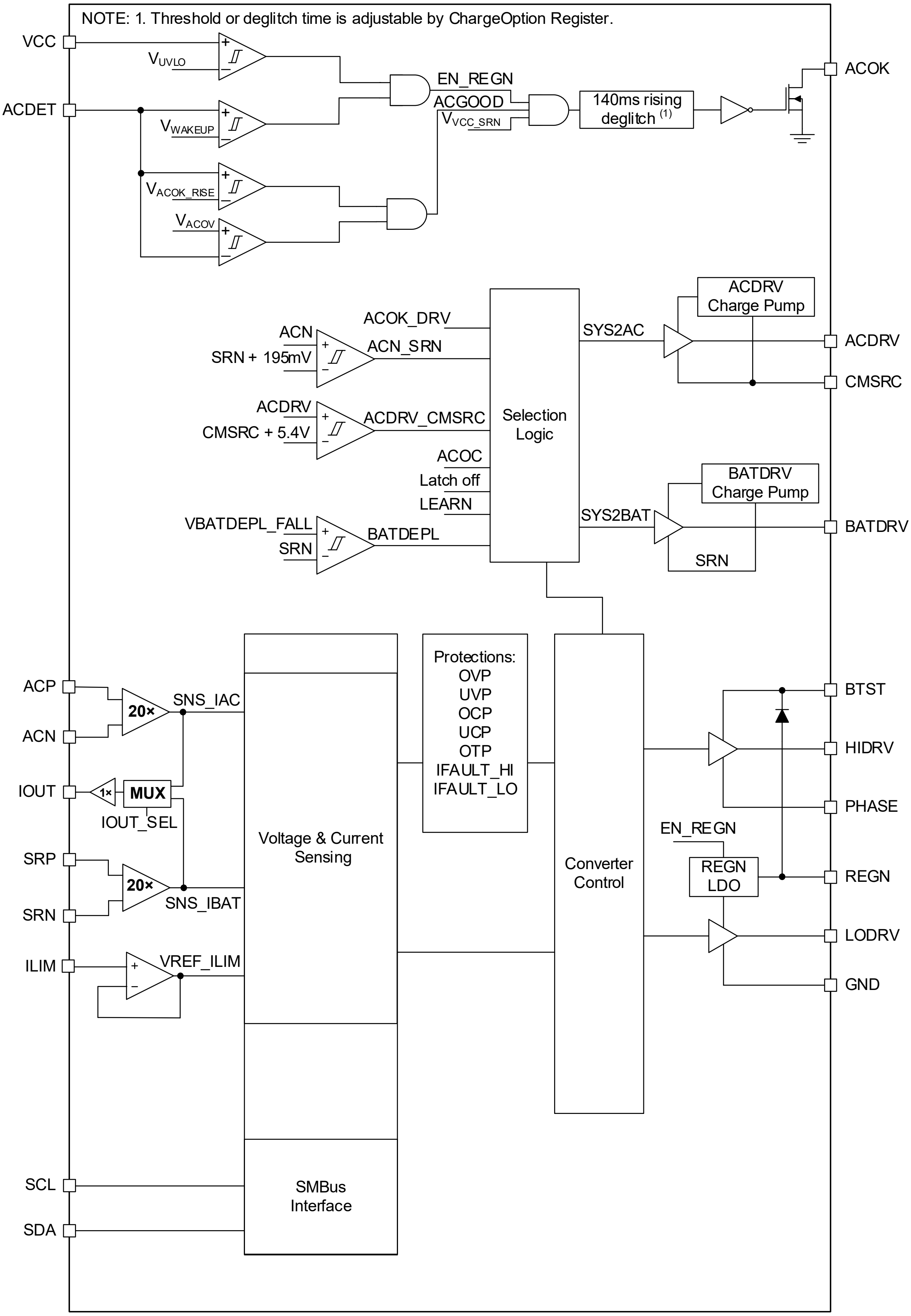


Figure 2. Block Diagram

DETAILED DESCRIPTION

Adapter Detect and ACOK Output

The SGM41535 determines the power source on its VCC pin, battery or adapter, using an ACOK comparator. The ACDET input senses the adapter voltage through an external resistor divider. The adapter detection threshold is configured to exceed the maximum battery voltage and remain below the minimum acceptable adapter input voltage.

The ACOK pin is an open-drain output that requires an external pull-up resistor to assert a high logic level. This resistor is typically connected to the system digital power rail. The output is pulled high only when all of the following conditions are met:

- The VCC voltage exceeds the under-voltage lockout threshold ($V_{VCC} > V_{UVLO}$).
- V_{ACDET} is between 2.4V and 3.15V, and the device is not in an adapter over-voltage (ACOVP) or low input voltage condition.
- $V_{VCC} - V_{SRN}$ > 355mV (Note that V_{SRN} is the sensed battery voltage or V_{BAT})

The ACOK signal asserts high with a default rising-edge delay of 140ms once a valid voltage is present on ACDET. This 140ms delay is unconditionally applied following the initial power-on reset of the device, irrespective of the value stored in the ChargeOption register. To modify this timing, the V_{CC} must exceed the UVLO threshold, enabling SMBus communication. The ACOK rising-edge deglitch period can be extended to 1.1s via SMBus (ChargeOption register bit[15] (ACOK Deglitch Time Adjust) = 1). If the battery is already installed and ACOK Deglitch Time Adjust bit is programmed to 1 prior to the first adapter insertion, the first plug-in event will also utilize the 1.1s deglitch interval. The extended 1.1s deglitch period is designed to maintain the ACFET in the off state for a sufficient duration when the V_{ACDET} is pulled below 2.4V due to high current demands, such as during over-current or short-circuit events.

Adapter Over-Voltage (ACOVP)

When the ACDET pin voltage exceeds 3.15V, an adapter over-voltage condition is triggered. Once detected, charging is halted, the ACOK signal is driven low, and the ACFET and RBFET are switched off to isolate the system from the elevated input voltage. If valid turn-on conditions are met, the BATFET is turned on. Refer to the System Power Selection section for further details.

When the ACDET voltage recovers to a level between 2.4V and 3.15V, the adapter is considered to have returned to normal operation. The device then releases the ACOK signal to go high, deactivates the BATFET, and re-enables the ACFET and RBFET to restore system power from the adapter. Charging may resume provided the required enable conditions are satisfied. Additional information is provided in the Enable and Disable Charging section.

System Power Selection

The SGM41535 selects between adapter or battery power to supply the system automatically. At power-on reset (POR), the battery is connected to the system if no adapter is present. Once the ACOK signal goes high, the battery is disconnected from the system and the adapter is connected after a configurable deglitch delay (140ms by default, programmable to 1.1s). A break-before-make switching logic is implemented to prevent shoot-through current during power source transitions.

Two N-MOSFETs with common-source configuration are placed between the adapter input and the ACP pin, as shown in Figure 5. Their common gates are driven by the ACDRV output and both sources are connected to the CMSRC pin. The ACFET is used to separate adapter from system and battery. It also limits the inrush current rise (di/dt) by controlling the turn-on time when the adapter is plugged in. The ACFET also protects the adapter if a short-circuit occurs in the battery or system. The RBFET blocks negative voltage if a reverse input voltage is accidentally applied and protects the battery discharge to the input if a short occurs on the adapter side. Compared to a reverse blocking Schottky diode, the RBFET has much lower power dissipation due to its low R_{DSON}.

When V_{ACDET} drops below 2.4V, it indicates that a valid adapter is not connected. In this condition, the ACDRV is pulled to CMSRC, turning off the ACFET and the RBFET to disconnect the adapter from the system. Meanwhile, the BATDRV is maintained at V_{SRN} + 5.7V to connect the battery to the system, provided all of the following conditions are satisfied:

- V_{VCC} > UVLO
- V_{SRN} > UVLO
- $V_{ACN} < V_{SRN}$ + 195mV

After adapter detection, indicated by an ACDET pin voltage within the 2.4V to 3.15V range, the ACDRV signal will go high after a configurable delay of approximately 140ms (default) or 1.1s. This action turns on ACFET and RBFET, switching the system power source from battery to adapter when all of the following conditions are satisfied:

- The device is not in LEARN mode, or the V_{SRN} is below the battery depletion threshold (if in LEARN mode).
- The ACOK signal remains high.

DETAILED DESCRIPTION (continued)

The ACFET/RBFET gate drive voltage is V_{CMSRC} + 6V. The ACFET/RBFET are turned off if the gate-source voltage remains below 5.4V for 20ms after turn-on. A turn-on retry will repeat after a 1.2s delay, and if the same failure occurs for seven times within a 90s period, the ACFET/RBFET will latch off. In this case, it is necessary to remove the adapter and shut down the system to reset the device by forcing V_{ACDET} below 0.6V. After reset, the ACFET/RBFET can turn on again. The failure counter automatically resets to zero after 90s to avoid false latch off. Charging remains disabled while ACFET/RBFET are off.

To turn off ACFET/RBFET, one of the following conditions must be satisfied:

- The device is in LEARN mode, and the V_{SRN} voltage is above the battery depletion threshold.
- ACOK signal remains low.

It is recommended that 4.02kΩ gate drive current limiting and slow-down resistors be used in series with the ACDRV, CMSRC and BATDRV pins in order to increase the gate voltage rise time, as well as to limit inrush and fault currents.

To control adapter inrush current when the ACFET is enabled for system power, careful selection of the external C_{GS} and C_{GD} capacitors is required. Increasing these capacitances slows the turn-on transition of the ACFET, thereby reducing inrush current. However, excessively large C_{GS} or C_{GD} values may prevent the ACDRV-to-CMSRC voltage from reaching its target level within the allotted 20ms turn-on window. To avoid false triggering of the ACFET during hot-plug events, C_{GS} should be at least 20 times greater than C_{GD}. The most economical method for limiting inrush current remains minimizing the total system capacitance.

Battery LEARN Cycle

A battery LEARN cycle can be initiated via SMBus command. A LEARN cycle can be enabled by setting the ChargeOption register bit[6] (LEARN Enable) to 1. To calibrate the battery gas gauge, a full discharge and charge cycle can be completed through the LEARN function. After enabling the LEARN, the system is only powered from battery and not the adapter by turning ACFET/RBFET off and BATFET on. The LEARN cycle is automatically terminated when the battery voltage falls below the depletion threshold and then the controller turns BATFET off and ACFET/RBFET on to switch back to the normal power input from adapter. The LEARN bit automatically resets to 0 after completing a LEARN cycle. The battery depletion threshold is programmable via SMBus command, allowing it to be set to 60%, 63%, 67%, or 72% of the voltage regulation level. This adjustment is controlled through the ChargeOption register bits[12:11] (BAT Depletion Comparator Threshold Adjust[1:0]).

Enable and Disable Charging

Charge Initiation Requirements

Charging begins in Charge mode when all of the following conditions are met:

- Charge is enabled via SMBus (ChargeOption register bit [0] (Charge Inhibit) = 0, default enables charging)
- The voltage on the ILIM pin exceeds 105mV
- Valid values are set through SMBus in ChargeCurrent, ChargeVoltage and InputCurrent Registers
- The ACOK signal is asserted high (refer to the ***Adapter Detect and ACOK Output*** section)
- ACFET and RBFET are turned on with sufficient gate drive voltage, refer to the System Power Selection section
- The VSRN voltage is below BATOVP threshold
- Device Temperature is below thermal shutdown threshold
- An adapter over-current (ACOC) condition is not present, refer to the ***Input Over-Current Protection (ACOC)*** section

Charge Termination Conditions

An ongoing charge cycle is stopped if any one of the following events occurs:

- Charge is inhibited via SMBus (ChargeOption register bit [0] (Charge Inhibit) = 1)
- The voltage on the ILIM pin drops below 75mV
- The value in the ChargeCurrent, ChargeVoltage, or InputCurrent registers is set to zero or programmed out of the valid range
- ACOK signal de-asserts (goes low), refer to the ***Adapter Detect and ACOK Output*** section
- ACFET is turned off
- The VSRN voltage is above BATOVP threshold
- Thermal shutdown
- An adapter over-current (ACOC) condition is present, refer to the ***Input Over-Current Protection (ACOC)*** section
- Detection of a short-circuit condition, refer to the ***Inductor Short, MOSFET Short Protection*** section
- Expiration of the watchdog timer, if enabled, refer to the ***Charge Timeout*** section

DETAILED DESCRIPTION (continued)

Automatic Internal Soft-Start Charger Current

After charging is enabled, the charge current will start to rise with an automatic soft-start to prevent stress or over-current/overshoot on the converter and output capacitors. With a 10mΩ sense resistor the charge current starts at 128mA and in CCM mode rises with 64mA steps in each around 240μs until it reaches the programmed value. No external components are needed for this function. While the converter is in DCM mode, the step size is larger and lasts longer due to the slower converter response.

High Accuracy Current Sense Amplifier

Following industry practice, a high-precision current sense amplifier (C_{SA}) is integrated to measure either input current or charge current. The host selects the measurement target via via the SMBus through bit[5] (IOUT Selection) of the ChargeOption register: a value of 0 selects input current, and 1 selects charge current.

The C_{SA} amplifies the voltage across the sense resistor by a factor of 20 and outputs the result on the IOUT pin. The amplifier becomes active and the I_{OUT} signal becomes valid once V_{CC} rises above the UVLO threshold and V_{ACDET} exceeds 0.6V. If a lower monitoring voltage is required, a resistor divider can be added between IOUT and GND without compromising the C_{SA} high accuracy across temperature.

To attenuate high-frequency noise, a 100pF capacitor should be connected to the IOUT pin. For additional filtering, an RC network may be implemented, but a lower cutoff frequency results in a slower C_{SA} response.

Charge Timeout

A watchdog timer is included in the SGM41535 that can terminate charging if it is timed out and not receive a write ChargeVoltage register or write ChargeCurrent register command within a timer setting. A watchdog timer is included in this device that can suspend charging operation, if it is timed out and not reset by ChargeVoltage register or ChargeCurrent register write commands within a timer setting. After a watchdog timeout, the register values are not affected, but converter will suspend. The converter does not resume until watchdog is reset by a write to ChargeVoltage register or ChargeCurrent register or a change is made in the WDTMR_ADJ[1:0] bits.

Converter Operation

The synchronous Buck PWM converter features a fixed-frequency, voltage-mode control architecture and integrates an internal Type III compensation network. An LC filter is employed at the output, providing its characteristic resonant frequency.

$$f_O = \frac{1}{2\pi\sqrt{L_O C_O}} \tag{3}$$

Choose the resonant frequency f_O such that with the internal compensation, converter has sufficient phase margin and gain margin for the target bandwidth. For the best performance choose the LC filter such that the nominal f_O frequency falls in the 10kHz to 20kHz range. Suggest component value as charge current of 750kHz default switching frequency is shown in Table 1.

Table 1. Recommended Component Values for Rated Charge Current at 750kHz Default Switching Frequency

Charge Current	2A	3A	4A	6A	8A
Output Inductor	6.8μH or 8.2μH	5.6μH or 6.8μH	3.3μH or 4.7μH	3.3μH	2.2μH
Output Capacitor	20μF	20μF	20μF	30μF	40μF
Sense Resistor	10mΩ	10mΩ	10mΩ	10mΩ	10mΩ

Ceramic capacitors show a DC bias effect. The DC bias voltage of ceramic capacitors significantly reduces the effective capacitance of them especially at higher output voltages and for smaller size packages. Consider the proper capacitance derating for C_O based on the manufacturer recommendations. A rated voltage much higher than the operating voltage may be required to minimize such derating.

The SGM41535 integrates input current, charge current, ILIM charge current, and charge voltage regulation loops, which converge at a shared error amplifier. The highest output from the three loops determines the voltage at the error amplifier output (EAO). An internal saw-tooth ramp is then compared to the EAO signal to modulate the converter duty cycle. The ramp includes a 1.4V offset to permit a 0% duty cycle.

When the battery voltage approaches the input voltage, the converter enters 100% duty cycle switching. If the BTST-to-PHASE voltage drops below 3.5V, a refresh cycle is initiated by turning on the low-side N-MOSFET to recharge the bootstrap capacitor. This architecture supports duty cycles up to 99.5%

DETAILED DESCRIPTION (continued)

Discontinuous Conduction Mode (DCM)

When the high-side FET (HSFET) is turned off and the low-side FET (LSFET) is turned on, the inductor current decays. If this current reaches zero, the converter enters discontinuous conduction mode (DCM). To prevent the system voltage from being boosted by the HSFET body diode, under-current protection (UCP) activates, blocks reverse current by turning off the LSFET when the voltage across SRP and SRN drops below 6mV (corresponding to 0.6A through a 10mΩ sense resistor).

In DCM, the control-loop response automatically transitions to a single-pole control system, where the pole location varies with the load current.

In both CCM and DCM, the LSFET turns on synchronously each clock cycle. However, if the average charge current falls below 125mA (through a 10mΩ sense resistor) or the battery voltage drops below 2.5V, the LSFET is held off. The charger then enter non-synchronous mode, conducting current through the LSFET body diode. In this mode, the LSFET is pulsed on briefly only to refresh the BTST bootstrap capacitor.

Synchronous operation resumes when the average charge current exceeds 250mA (through a 10mΩ sense resistor), reducing power loss in the LSFET.

Input Over-Current Protection (ACOC)

The SGM41535 can no longer regulate the input current level at its value if the charge current has been already reduced to 0 and system is the only adapter load. After the system current continues increasing to the ACOC function threshold with ACOC deglitch time, the ACFET and RBFET are permanently latched off. To clear this latch-off state, the adapter must be removed and the system is shut down until V_{ACDET} drops below 0.6V, resetting the device. Once reset, the FETs can be turned on again. The ACOC threshold is programmable via SMBus using ChargeOption register bits [2:1] (ACOC Threshold Adjust). It can be set to 1.33×, 1.66×, or 2.22× of the input DPM current, or disabled entirely. The ACOC deglitch time is also configurable via ChargeOption register bit[3] (ACOC_DGL), with options of 2.15ms or 90μs.

Charge Over-Current Protection (CHGOCP)

By monitoring the voltage across SRP and SRN, cycle-by-cycle peak charge over-current protection is implemented to keep the charge current below OCP threshold. The gate driver of the HSFET turns off for the rest of the cycle when the over-current is detected until the beginning of the next cycle.

With a 10mΩ current sensing resistor, the charge OCP threshold is set to 5.5A, 8.5A or 11A automatically based on the charge current setting in the ChargeCurrent register command. This automatic setting prevents too low or too high OCP settings that can result in unwanted protection trigger or unsafe settings. Select an inductor value that avoids triggering over-current protection (OCP) from excessive current ripple during normal operation.

Battery Over-Voltage Protection (BATOVP)

If the sensed battery voltage on V_{SRN} rises 4% or more above regulation voltage set point, both MOSFET switches will be kept off. If this situation lasts for more than 30ms, the charger will be fully disabled. This ensures rapid over-voltage response, such as during the load or battery disconnect. After BATOVP event an internal small current sink (lasting about 30ms) is connected to SRN to discharge any stored energy in the output inductor and the output capacitors. When the charge regulation voltage is set below 4.6V, the small current is about 4mA. Otherwise, the small current is about 6mA.

Battery Shorted to Ground (BATLOWV)

If the battery voltage on SRN goes too low and drops below 2.5V (BATLOWV event), the charge current is limited to 0.5A when using a 10mΩ sense resistor, or to a lower value if programmed via register. With this feature, current overshoot is avoided that otherwise could cause inductor saturation and damage to the MOSFET. If BATLOWV continues, the LSFET remains off and only turns on for short pulses to refresh BTST capacitor.

Thermal Shutdown Protection (TSD)

The device TQFN package provides very good junction to ambient thermal conduction to keep the device cool.

To prevent thermal damage, the device enters shutdown if the junction temperature exceeds +155℃, turning off the converter. It remains off until the junction temperature falls below +135℃.

During thermal shutdown, the I_{REGN_LIM} is reduced to 13mA while the ACFET and RBFET stay on to maintain system power. Once the temperature drops below +135℃, charge charging resumes with a soft-start sequence.

DETAILED DESCRIPTION (continued)

EMI Switching Frequency Adjust

The switching frequency can be adjusted by ±18% via SMBus to address EMI concerns. This feature is controlled through the ChargeOption register:

- Disable: Set ChargeOption register bit [9] (EMI Switching Frequency Enable) = 0.
- Enable and adjust: Set EMI Switching Frequency Enable = 1, then set ChargeOption register bit [10] (EMI Switching Frequency Adjust) to 0 (reduce frequency) or 1 (increase frequency).

Note that reducing the frequency increases inductor current ripple for a given inductance. The inductor must be selected to avoid triggering cycle-by-cycle peak overcurrent protection under worst-case conditions (e.g., high input voltage, 50% duty cycle, minimum inductance, and lowest switching frequency).

Inductor Short, MOSFET Short Protection

The SGM41535 uses a unique short-circuit protection method by cycle-by-cycle current monitoring of the MOSFETs R_{DSON} voltage drops that are sensed after a short blanking time from the beginning of each cycle. A short-circuit condition in the MOSFETs or inductor is detected by dual comparators, each with a dedicated counter. After seven consecutive detections, the charger latches off: the ACFET and RBFET are disabled to disconnect the adapter, while the BATFET is enabled to connect the battery to the system. The latch-off state is cleared when V_{CC} falls below V_{UVLO} or when V_{ACDET} drops below 0.6V. This typically requires adapter removal and system shutdown. The short-circuit voltage-drop thresholds are independently configurable for the high-side and low-side MOSFETs. The low-side threshold is adjustable via SMBus. IFAULT_LO Comparator Threshold Adjust bit = 0, 1 set the low side MOSFET voltage drop comparator threshold 130mV and 240mV respectively, and is disabled by IFAULT_LO_DIS bit. The high-side MOSFET Short-Circuit voltage drop threshold can be adjusted via SMBus command. IFAULT_HI Comparator Threshold Adjust [1:0] = 00, 01, 10, or 11 set the HSFET voltage drop comparator threshold 500mV, 700mV, 900mV, and 1100mV respectively, and is disabled by IFAULT_HI_DIS bit.

The cycle-by-cycle charge over-current protection circuit may detect the over-current firstly and turn off the switch before the short-circuit protection circuit can detect it. It can happen due to the short-circuit detection blank time that is considered to avoid influence of MOSFET transient noises during turn-on. Note that the MOSFET is forced to turn off by the over-current protection before the end of blanking time and in this condition, the device cannot detect short-circuit and the counters may not reach 7 to latch off. Therefore, the charger keeps switching with very small duty cycle for cycle-by-cycle current limiting. Even in this situation the charger and MOSFETs remain in their safe operation area due to very short on-time. Due to the same reason (blanking times), during soft-start the short-circuit protection trigger may take much longer than 7 cycles.

DETAILED DESCRIPTION (continued)

Programming

SMBus write-word or read-word charger protocol commands are supported by SGM41535. The charger can be identified by the 16-bit ManufacturerID and DeviceID registers located at 0xFE and 0xFF respectively. All registers of the SGM41535 are 16-bit which are divided into a high byte and a low byte.

SMBus Interface

The SGM41535 is a slave device with the 7-bit address of 0x09 (0b0001 001). As a slave device, it will not initiate a communication on the bus. A host is needed to control and program communications through the SMBus. A simplified subgroup of the System Management Bus Specification V1.1 commands (available from www.smbus.org) is supported for communication with the smart battery using read-word and write-word protocols.

Both data (SDA) and clock (SCL) pins use Schmitt-trigger inputs to allow slow pulse edges. Use 10kΩ pull-ups on both lines to provide the required SMBus rise/fall times. The master (usually the host) starts a communication by creating a START condition on the bus and terminates it by creating a STOP condition. Then the bus will be free for a new transaction. START condition is created by an SDA high-to-low transition while SCL is high, and a STOP condition is issued by an SDA low-to-high transition while SCL is high. See Figure 3 and Figure 4 for the timing diagrams of the SMBus interface signals. The address, command, and data bytes are all exchanged between the START and STOP conditions. During transactions, the SDA state only can change when the SCL is low, except for the START and STOP conditions. Data is transmitted bit by bit starting from MSB to LSB and one byte (8-bits) at a time. Data bits are sampled from SDA line at the rising edges of the SCL. A 9th acknowledge bit is also transmitted by receiver, so nine clock cycles are required for transferring each byte. The write-word and read-word command protocols are provided in Table 2 and Table 3.

SMBus Write-Word and Read-Word Protocols

Table 2. Write-Word Format

Bits	S/SR	Slave Addr	Write Bit	ACK	Cmnd. Byte	ACK	Low Data Byte	ACK	High Data Byte	ACK	STOP (P)
Creator	MTR	MTR	MTR	SLV	MTR	SLV	MTR	SLV	MTR	SLV	MTR
# of Bits		7	1	1	8	1	8	1	8	1	
Order		MSB LSB			MSB LSB		MSB LSB		MSB LSB		

Table 3. Read-Word Format

Bits	S/SR	Slave Addr	Write Bit	ACK	Cmnd. Byte	ACK	S/SR	Slave Addr	Read Bit	ACK	Low Data Byte	ACK	High Data Byte	NCK	STOP (P)
Creator	MTR	MTR	MTR	SLV	MTR	SLV	MTR	MTR	MTR	SLV	SLV	MTR	SLV	MTR	MTR
# of Bits		7	1	1	8	1		7	1	1	8	1	8	1	
Order		MSB LSB			MSB LSB			MSB LSB			MSB LSB		MSB LSB		

NOTES:
1. MTR: Master, SLV: Slave.
2. S = START condition, SR = Repeated START condition, P = STOP condition.
3. Write bit ($\overline{W}$) and ACK are logic low.
4. Read bit (R) and NCK (Not acknowledge) are logic high.

DETAILED DESCRIPTION (continued)

Timing Diagrams

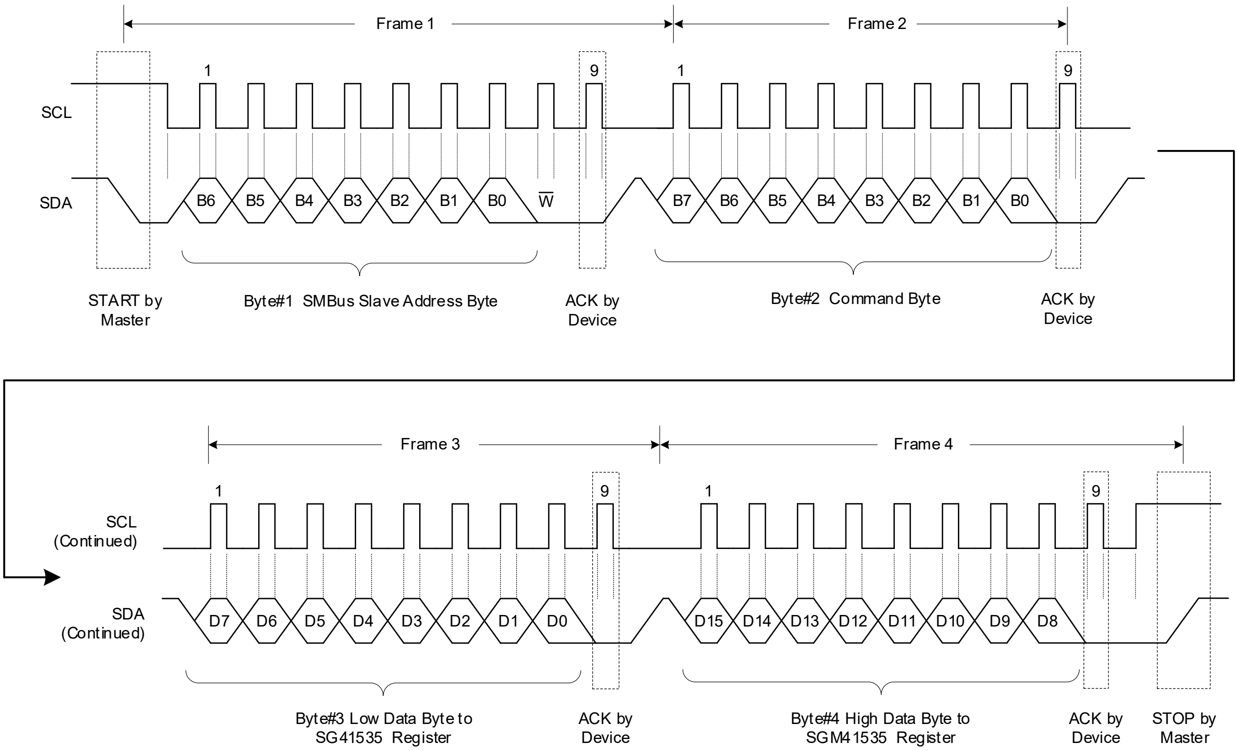


Figure 3. SMBus Write Timing

DETAILED DESCRIPTION (continued)

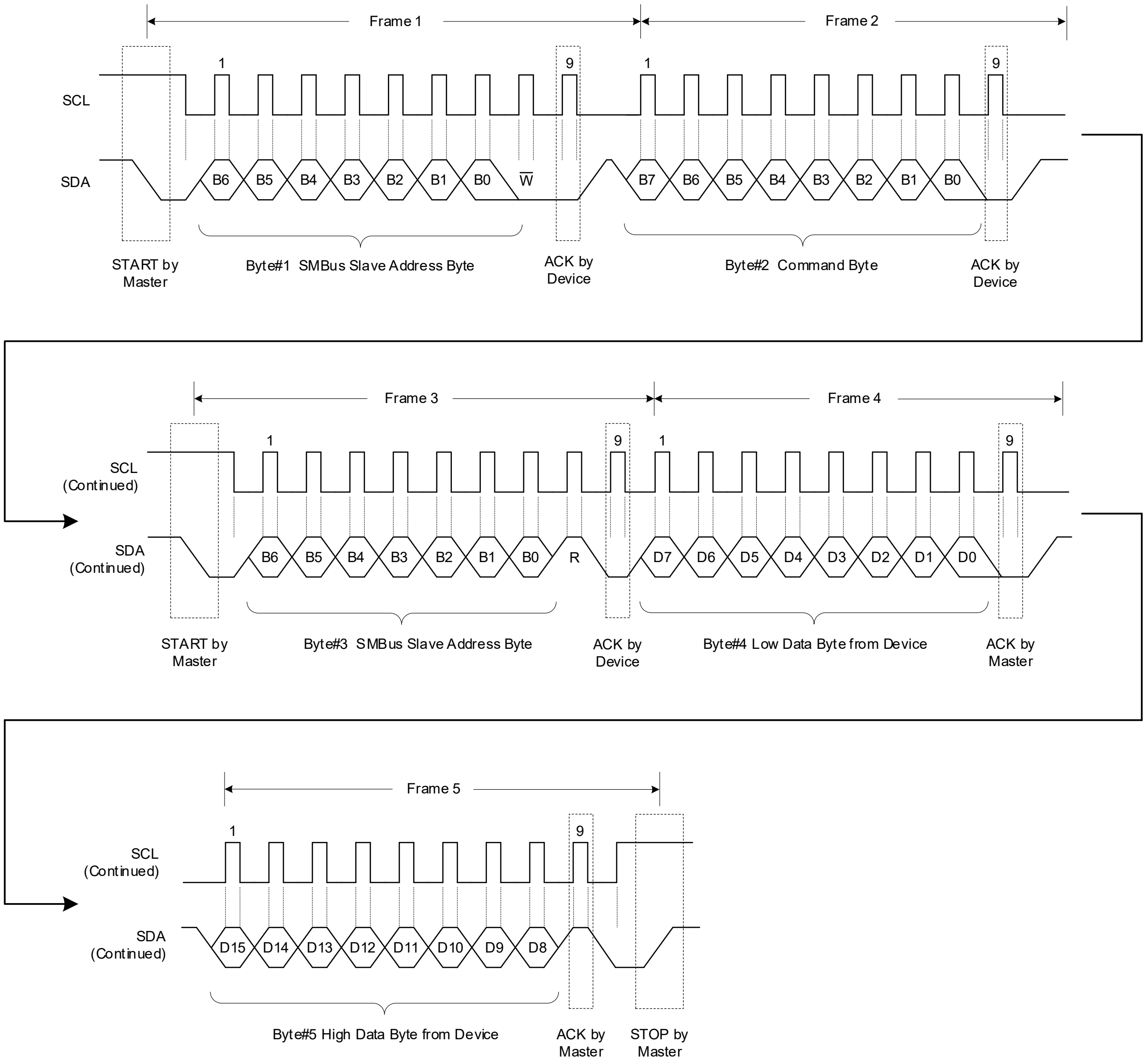


Figure 4. SMBus Read Timing

REGISTER MAPS

Battery-Charger Commands

The SGM41535 supports six battery-charger commands that use either Write-Word or Read-Word protocols, (a summary as shown). ManufacturerID and DeviceID Registers enable SGM41535 identification, with fixed return values of 0x0040 and 0x0008 for their respective commands.

Table 4. SGM41535 Battery Charger Command Register Summary

SMBus Address	Register Name	Description	POR State	Type	Links
0x12	ChargeOption Register	Charger Options Control	0x7904	R/W	Go
0x14	ChargeCurrent Register	7-Bit Charge Current Setting	0x0000	R/W	Go
0x15	ChargeVoltage Register	11-Bit Charge Voltage Setting	0x0000	R/W	Go
0x3F	InputCurrent Register	7-Bit Input Current Setting	0x1000	R/W	Go
0xFE	ManufacturerID Register	Manufacturer ID	0x0040	R	—
0xFF	DeviceID Register	Device ID	0x0008	R	—

REGISTER MAPS (continued)

Bit Types:
R/W: Read/Write bit(s)
R: Read only bit(s)
n: Parameter code formed by the bits as an unsigned binary number.

Setting Charger Options

After POR, the SGM41535 allows configuration of multiple charger options via the ChargeOption register command (0x12 or 0b0001 0010), as detailed in Table 5 and Table 6.

ChargeOption Register (SMBus Address = 0x12) [Reset = 0x7904]

Table 5. ChargeOption Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	ACOK Deglitch Time Adjust	0	R/W	Set ACOK Rising Edge Deglitch Time for the Adapter Input. To configure this option, VCC must be above the UVLO threshold to enable SMBus communication. Following a POR, the bit defaults to 0, resulting in an ACOK rising‑edge deglitch time of 140ms. 0 = ACOK rising edge deglitch time 140ms (default) 1 = ACOK rising edge deglitch time 1.1s
D[14:13]	WDTMR_ADJ[1:0]	11	R/W	Watchdog Timer Setting. Set the maximum time interval between two consecutive SMBus write commands for charge voltage or current to reset the timer and prevent watchdog reset. If the watchdog timer is enabled and the device receives no such write commands within the watchdog period, charging will be suspended. Once the watchdog timer expires and charging is suspended, the charging process will resume upon receipt of a subsequent SMBus write command for charge voltage or current. 00 = Disable Watchdog Timer 01 = Enabled, 38s 10 = Enabled, 76s 11 = Enable Watchdog Timer (152s) (default)
D[12:11]	BAT Depletion Comparator Threshold Adjust [1:0]	11	R/W	Battery Depletion (Over-Discharge) Detector Falling Threshold Setting. During LEARN cycle, the device turns off the BATFET and turns on the ACFET once the battery voltage falls below the depletion threshold, switching the system power source from the battery to the AC adapter. It is given as percentage of the voltage regulation setting in REG0x15. 00 = Falling Threshold = 60% of voltage regulation limit (~2.52V/cell) 01 = Falling Threshold = 63% of voltage regulation limit (~2.646V/cell) 10 = Falling Threshold = 67% of voltage regulation limit (~2.814V/cell) 11 = Falling Threshold = 72% of voltage regulation limit (~3.024V/cell) (default)
D[10]	EMI Switching Frequency Adjust	0	R/W	EMI Switching Frequency Adjust 0 = Reduce PWM switching frequency by 18% (default) 1 = Increase PWM switching frequency by 18%
D[9]	EMI Switching Frequency Enable	0	R/W	Enable EMI Switching Frequency Adjust 0 = Disable adjust PWM switching frequency (default) 1 = Enable adjust PWM switching frequency
D[8:7]	IFAULT_HI Comparator Threshold Adjust [1:0]	10	R/W	Short-Circuit protection HSFET voltage drop comparator threshold. 00 = 500mV 01 = 700mV 10 = 900mV (default) 11 = 1100mV

REGISTER MAPS (continued)

Table 6. ChargeOption Register Details (continued)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[6]	LEARN Enable	0	R/W	Enable Battery LEARN Mode Setting this bit to 1 initiates the battery LEARN cycle, during which the device turns off the ACFET and turns on the BATFET to discharge the battery. When the battery voltage reaches the threshold configured by by ChargeOption register bits [12:11], the BATFET is turned off and the ACFET is turned on, completing the LEARN cycle. The bit is then automatically cleared to 0. Setting this bit to 0 stops the LEARN cycle immediately, turning off the BATFET and turning on the ACFET. 0 = Disable LEARN cycle (default) 1 = Enable LEARN cycle
D[5]	IOUT Selection	0	R/W	IOUT Selection Setting 0 = IOUT is the 20× adapter current amplifier output (default) 1 = IOUT is the 20× charge current amplifier output
D[4]	AC Adapter Indication	0	R	Indicator Bit for Adapter Present 0 = AC adapter is not present (V_{ACDET} < 2.4V) (default) 1 = AC adapter is present (V_{ACDET} > 2.4V)
D[3]	ACOC_DGL	0	R/W	The deglitch time of voltage across input sense resistor rising to latch off ACFET/RBFET time. 0 = 2.15ms (default) 1 = 90μs
D[2:1]	ACOC Threshold Adjust [1:0]	10	R/W	ACOC Threshold Limit Setting 00 = Disable ACOC 01 = 1.33× of input current regulation limit 10 = 1.66× of input current regulation limit (default) 11 = 2.22× of input current regulation limit
D[0]	Charge Inhibit	0	R/W	Charge Inhibit Battery charging is enabled if this bit is 0 (If REG0x14 and REG0x15 values are valid) 0 = Enable charge (default) 1 = Inhibit charge

REGISTER MAPS (continued)

Setting the Charge Current

The charge current can be set by writing a 7-bit value in the 16-bit ChargeCurrent register (0x14 or 0b0001 0100) command with the format given in Table 7. The charge current can be set in the 128mA to 8.128A range in 64mA steps when a 10mΩ sense resistor is used. Writing 0 or 64mA to this register terminates the current charge cycle. The register resets to 0A upon POR or if ACOK goes low due to an invalid adapter condition (V_{ACDET} < 2.4 V).

For signal conditioning, place a 0.1µF ceramic capacitor between SRP and SRN for differential-mode filtering, a 0.1µF capacitor between SRN and GND for common-mode filtering, and a 0.1µF capacitor between SRP and GND for additional common-mode rejection. The total capacitance on SRP should not exceed 0.1µF to maintain accurate cycle-by-cycle under-current and over-current detection.

The SRP and SRN pins are used to measure the voltage drop across the charge current sense resistor (R_{SR}). The default R_{SR} value is 10mΩ, however, other values may also be used that will scale the currents in Table 7 by the 10mΩ/R_{SR} ratio. Generally, a larger resistor provides better measurement accuracy and regulation but increases the conduction losses. The current ripple peaks may also trigger over-current with a large R_{SR}. To reduce ripple and avoid unwanted over-current trigger, a larger inductance value or a lower current sense resistor value is needed. It is recommended to choose an R_{SR} not higher than 20mΩ.

As an additional protection level, user can set the maximum charge current by setting the ILIM pin voltage. The actual charge current limit will be the lower setting between ChargeCurrent register and the ILIM pin setting. This feature can be disabled by pulling ILIM above 1.625V externally. If ILIM voltage is pulled below 75mV, charge will be disabled. Use Equation 1 to set the ILIM pin value with respect to the preferred charge current limit:

$$V_{ILIM} = 20 \times (V_{SRP} - V_{SRN}) = 20 \times I_{CHG} \times R_{SR} \quad (1)$$

ChargeCurrent Register (SMBus Address = 0x14) [Reset = 0x0000]

Table 7. ChargeCurrent Register Details, Using 10mΩ Sense Resistor

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:13]	Reserved	000	R/W	Reserved and writing “1” is not recommended.
D[12]	Charge Current, DACICHG 6	0	R/W	0 = Add 0mA of charger current. 1 = Add 4096mA of charger current.
D[11]	Charge Current, DACICHG 5	0	R/W	0 = Add 0mA of charger current. 1 = Add 2048mA of charger current.
D[10]	Charge Current, DACICHG 4	0	R/W	0 = Add 0mA of charger current. 1 = Add 1024mA of charger current.
D[9]	Charge Current, DACICHG 3	0	R/W	0 = Add 0mA of charger current. 1 = Add 512mA of charger current.
D[8]	Charge Current, DACICHG 2	0	R/W	0 = Add 0mA of charger current. 1 = Add 256mA of charger current.
D[7]	Charge Current, DACICHG 1	0	R/W	0 = Add 0mA of charger current. 1 = Add 128mA of charger current.
D[6]	Charge Current, DACICHG 0	0	R/W	0 = Add 0mA of charger current. 1 = Add 64mA of charger current.
D[5:0]	Reserved	00 0000	R/W	Reserved and writing “1” is not recommended.

REGISTER MAPS (continued)

Setting the Charge Voltage

The output charge regulation voltage can be set by writing an 11-bit value in 16bit ChargeVoltage register (0x15 or 0b0001 0101) using the data format listed in Table 8. The charge regulation voltage can be set within the 1.024V to 27.600V range in 16mV steps. Writing a value below 1.024V or above 27.6V, the register is cleared and the current charge cycle is terminated. Upon POR, the charge voltage setting is 0V and the converter is off. Writing 0 to the ChargeVoltage register disables battery charging.

The SRN pin senses the battery voltage for regulation. This pin must be decoupled (0.1μF recommended) as close as possible to the device and connected close to the battery.

ChargeVoltage Register (SMBus Address = 0x15) [Reset = 0x0000]

Table 8. ChargeVoltage Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	Reserved	0	R/W	Reserved and writing “1” is not recommended.
D[14]	Charge Voltage, DACV 10	0	R/W	0 = Add 0mV of charger voltage. 1 = Add 16384mV of charger voltage.
D[13]	Charge Voltage, DACV 9	0	R/W	0 = Add 0mV of charger voltage. 1 = Add 8192mV of charger voltage.
D[12]	Charge Voltage, DACV 8	0	R/W	0 = Add 0mV of charger current. 1 = Add 4096mV of charger current.
D[11]	Charge Voltage, DACV 7	0	R/W	0 = Add 0mV of charger current. 1 = Add 2048mV of charger current.
D[10]	Charge Voltage, DACV 6	0	R/W	0 = Add 0mV of charger current. 1 = Add 1024mV of charger current.
D[9]	Charge Voltage, DACV 5	0	R/W	0 = Add 0mV of charger current. 1 = Add 512mV of charger current.
D[8]	Charge Voltage, DACV 4	0	R/W	0 = Add 0mV of charger current. 1 = Add 256mV of charger current.
D[7]	Charge Voltage, DACV 3	0	R/W	0 = Add 0mV of charger voltage. 1 = Add 128mV of charger voltage.
D[6]	Charge Voltage, DACV 2	0	R/W	0 = Add 0mV of charger voltage. 1 = Add 64mV of charger voltage.
D[5]	Charge Voltage, DACV 1	0	R/W	0 = Add 0mV of charger voltage. 1 = Add 32mV of charger voltage.
D[4]	Charge Voltage, DACV 0	0	R/W	0 = Add 0mV of charger voltage. 1 = Add 16mV of charger voltage.
D[3:0]	Reserved	0000	R/W	Reserved and writing “1” is not recommended.

REGISTER MAPS (continued)

Setting Input Current

System power has large fluctuations depending on the power requirements of the CPU and other subsystems and may vary from near zero (in sleep mode) to a maximum. Therefore, to optimize adapter rating, Dynamic Power Mode (DPM) is used in which the charge current is continuously adjusted based on the available adapter current and the system load. DPM allows the use of a lower-cost AC wall adapter by reducing the peak input current requirement.

The total input current drawn from the adapter (a wall cube or other DC source) equals the sum of the system supply current and the charger input current. When the input current attempts to exceed the programmed limit, the SGM41535 reduces charge current to prioritize the system load. If the system current demand continues to increase, the charge current linearly reduce to 0. Once charge current reaches zero, all available input current is allocated to the system load.

During DPM regulation, the total input current equals the sum of the device supply current I_{BIAS}, the charger input current, and the system load current I_{LOAD}, and can be estimated as follows:

$$I_{INPUT} = I_{LOAD} + \left[\frac{I_{BATTERY} \times V_{BATTERY}}{V_{IN} \times \eta}\right] + I_{BIAS} \quad (2)$$

η is the efficiency of the charger Buck converter.

The input current limit can be set by writing a 7-bit value in a 16-bit InputCurrent register command (0x3F or 0b0011 1111) using the data format listed in Table 9. The input current limit can be set within the 128mA to 8.128A range in 64mA steps when a 10mΩ sense resistor is used. The recommended minimum input current limit is 512mA. Writing a value below 128mA or above 8.128A, the register is cleared and the current charge cycle is terminated. Upon POR, the default input current limit is 4096mA.

The ACP and ACN pins measures the voltage drop across the input current sense resistor (R_{AC}). The default R_{AC} value is 10mΩ, however, other values may also be used that will scale the currents by the 10mΩ/R_{AC} ratio. A larger resistor provides better measurement accuracy and regulation but increases the conduction losses.

If input current rises exceed 107% of the programmable limit, the charger asserts shutdown to allow the input current drop. Once charging stops, the charger resumes with a slowly start if the adapter remains capable of supporting battery charging. This mechanism prevents system crash during high and fast load transients that would otherwise overload the adapter. The delay between shutdown and restart is determined by the natural response time of the input current limit loop.

REGISTER MAPS (continued)

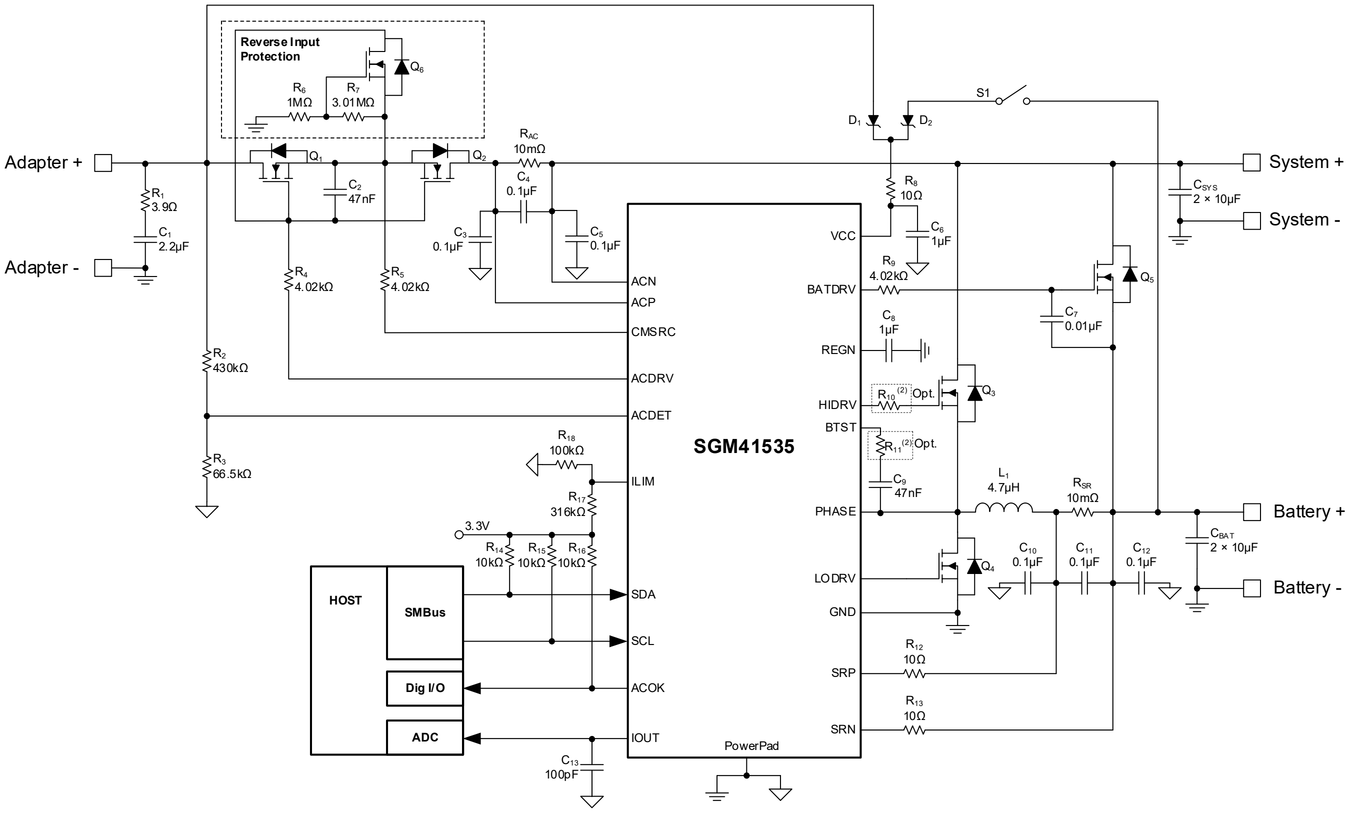
InputCurrent Register (SMBus Address = 0x3F) [Reset = 0x1000]

Table 9. InputCurrent Register Details, Using 10mΩ Sense Resistor

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:13]	Reserved	000	R/W	Reserved and writing "1" is not recommended.
D[12]	Input Current, DACIIN 6	1	R/W	0 = Add 0mA of input current. 1 = Add 4096mA of input current.
D[11]	Input Current, DACIIN 5	0	R/W	0 = Add 0mA of input current. 1 = Add 2048mA of input current.
D[10]	Input Current, DACIIN 4	0	R/W	0 = Add 0mA of input current. 1 = Add 1024mA of input current.
D[9]	Input Current, DACIIN 3	0	R/W	0 = Add 0mA of input current. 1 = Add 512mA of input current.
D[8]	Input Current, DACIIN 2	0	R/W	0 = Add 0mA of input current. 1 = Add 256mA of input current.
D[7]	Input Current, DACIIN 1	0	R/W	0 = Add 0mA of input current. 1 = Add 128mA of input current.
D[6]	Input Current, DACIIN 0	0	R/W	0 = Add 0mA of input current. 1 = Add 64mA of input current.
D[5:4]	Reserved	00	R/W	Reserved and writing "1" is not recommended.
D[3]	DIS_IOUT	0	R/W	Disable IOUT Pin Output Buffer 0 = Enable IOUT output (default) 1 = Disable IOUT output
D[2]	IFAULT_HI_DIS	0	R/W	Disable short-circuit protection HSFET voltage drop comparator. 0 = Enable (default) 1 = Disable
D[1]	IFAULT_LO Comparator Threshold Adjust	0	R/W	Short-Circuit protection LSFET voltage drop comparator threshold. 0 = 130mV (default) 1 = 240mV
D[0]	IFAULT_LO_DIS	0	R/W	Disable short-circuit protection LSFET voltage drop comparator. 0 = Enable (default) 1 = Disable

APPLICATION INFORMATION

TYPICAL APPLICATION



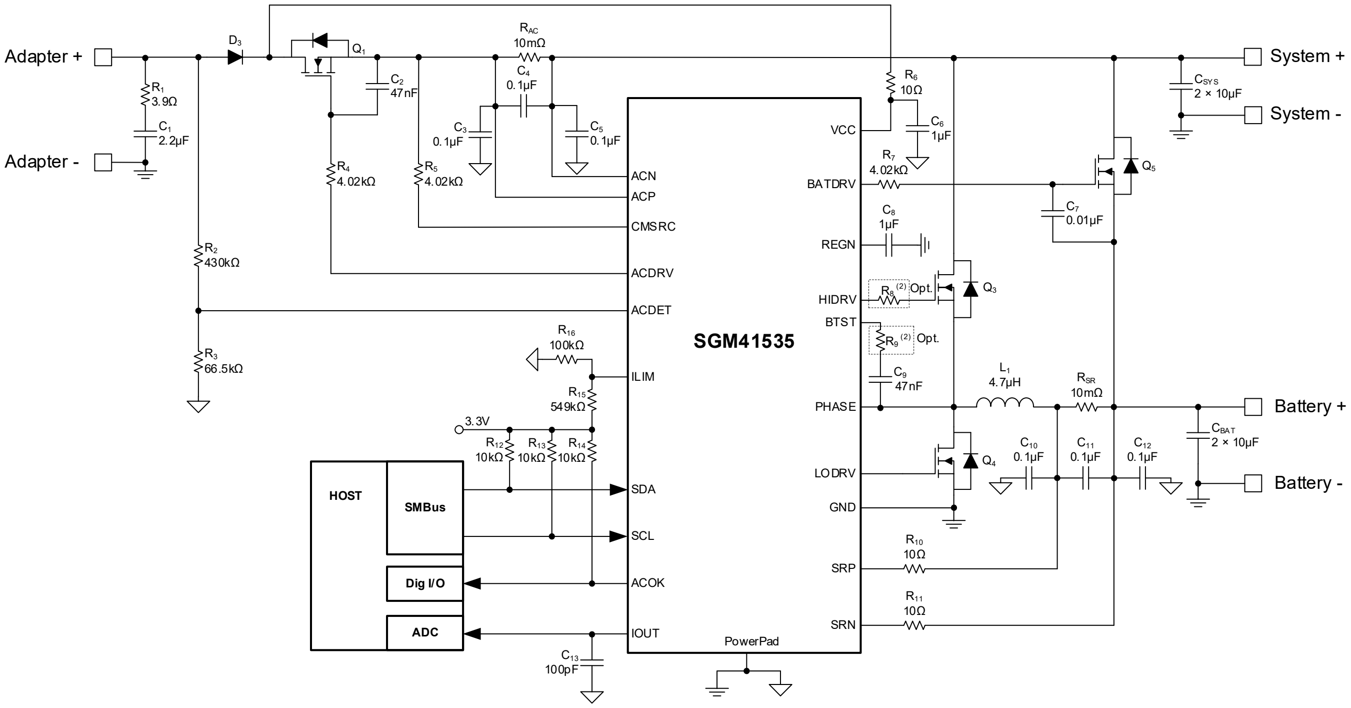
NOTES:

1. f_{SW} = 750kHz, V_{CHRG} = 12.592V, I_{ADPT} = 4.096A, I_{LIM} = 4A, I_{CHRG} = 2.944A, 90W adapter and 3S2P battery pack. See the application information about protection against negative output caused by a hard battery-to-ground short or reverse connection.

2. R_{10} and R_{11} are not present on the actual evaluation board, but is recommended for practical applications.

Figure 5. Typical SGM41535 Battery Charging Application with Two NMOS Selector

APPLICATION INFORMATION (continued)



NOTES:

1. f_{SW} =750kHz, V_{CHRG} = 12.592V, I_{ADPT} = 2.688A, I_{LIM} = 2.54A, I_{CHRG} = 1.984A, 65W adapter and 3S2P battery pack. See the application information about negative output voltage protection for hard shorts on battery to ground or battery reverse connection.

2. R_8 and R_9 are not present on the actual evaluation board, but is recommended for practical applications.

Figure 6. Typical SGM41535 Battery Charging Application with One NMOS Selector and Schottky Diode

APPLICATION INFORMATION (continued)

Table 10. Component List for Typical System Circuit of Figure 5

Item	Designator	QTY	Description
1	C_{SYS}, C_{BAT}	4	Ceramic Capacitor, 10μF, 35V, X5R, 0805
2	C_1	1	Ceramic Capacitor, 2.2μF, 35V, X5R, 0603
3	C_2	1	Ceramic Capacitor, 47nF,10V, X5R, 0603
4	C_3, C_5, C_{10}, C_{12},	4	Ceramic Capacitor, 100nF, 35V, X5R, 0402
5	C_4, C_{11}	2	Ceramic Capacitor, 100nF, 10V, X5R, 0603
6	C_6	1	Ceramic Capacitor, 1uF, 35V, X5R, 0603
7	C_7	1	Ceramic Capacitor, 10nF, 50V, X7R, 0603
8	C_8	1	Ceramic Capacitor, 1uF, 10V, X5R,0603
9	C_9	1	Ceramic Capacitor, 47nF, 50V, X5R, 0603
10	D_1, D_2	2	Diode, 75V, SOD323F,1N4148WS
11	L_1	1	Inductor, 4.7uH, I_{RMS} = 11.3A, I_{SAT} = 15A, DCR = 9.9mΩ, 1090
12	Q_1, Q_2, Q_3, Q_4, Q_5	5	NMOS, 30V, TDFN Package, SGMNM05330
13	Q_6	1	NMOS, 60V, SOT-23-3, 2N7002
14	R_{AC}, R_{SR}	2	Film Resistor, 10mΩ, 1%, 1W, 1206
15	R_1	1	Film Resistor, 3.9Ω, 5%, 0.5W, 1210
16	R_2	1	Film Resistor, 430kΩ, 1%, 0.1W, 0603
17	R_3	1	Film Resistor, 66.5kΩ, 1%, 0.1W, 0603
18	R_4, R_5, R_9	3	Film Resistor, 4.02kΩ, 1%, 0.1W, 0603
19	R_6	1	Film Resistor, 1MΩ 1%, 0.1W, 0603
20	R_7	1	Film Resistor, 3.01MΩ 1%, 0.1W, 0603
21	R_8	1	Film Resistor, 10Ω, 1%, 0.25W,1206
22	R_{12}, R_{13}	2	Film Resistor, 10Ω, 1%, 0.1W, 0603
23	R_{14}, R_{15}, R_{16}	3	Film Resistor, 10kΩ, 1%, 0.1W, 0603
24	R_{17}	1	Film Resistor, 316kΩ, 1%, 0.1W, 0603
25	R_{18}	1	Film Resistor, 100kΩ, 1%, 0.1W, 0603
26	U1	1	2-6 Cell Li+ Battery Charge Controller, TQFN-3.5×3.5-20L

Negative Output Voltage Protection

If by accident or a production failure the battery pack isinserted with reverse polarity or if a short occurs on the battery connections, negative voltages can appear on the SRP and SRN pins. When the output exhibits a negative voltage, it may forward-bias the internal ESD protection diodes (between GND and SRP/SN) and the anti-parallel diodes between SRP and SRN, resulting in high reverse current.

To limit this current, insert small resistors in series with SRP and SRN. Recommended values are 10Ω on SRP and SRN. With these resistors in place, a minimum pre-charge current of 192mA is recommended when using a 10mΩ sense resistor.

Reverse Input Voltage Protection

In Figure 5, Q_6, R_6 and R_7 protect the system and device against reverse adapter voltage. When adapter is connected correctly, Q_6 remains off due to the negative gate-source voltage (V_{GS}). If the adapter is connected in reverse polarity, the V_{GS} will be positive and Q_6 turns on and shorts Q_1/Q_2 (ACFET/RBFET) gate and source together and keeps it off. The body diode of Q_2 blocks the negative voltage from reaching to the device and the system. However, the CMSRC and ACDRV pins need current limiting resistors (R_5 and R_4) to limit their ESD diode currents caused by the negative voltage. A low V_{GS} threshold MOSFET should be selected for Q_6 with low Q_{GS} gate charge for quick turn-on (before Q_2) upon negative voltage connection.

APPLICATION INFORMATION (continued)

The R_5 and R_4 resistances must be small enough for quick response of ACFET/RBFET (to avoid slow turn-on/turn-off). R_5 and R_4 power rating must be large enough to dissipate losses at maximum adapter voltage without overheating. Figure 6 uses a Schottky diode (D_3) to provide reverse-adapter-voltage protection, eliminating the need for additional MOSFETs or resistors.

Reduce Battery Quiescent Current

When adapter is disconnected and VCC is powered from the battery (through a direct or indirect path resulting in $V_{VCC} > V_{UVLO}$), the internal BATFET charge pump will constantly run to drive the N-channel BATFET by keeping BATDRV voltage at 5.7V above V_{SRN}. The additional quiescent current caused by the charge pump is not necessary because BATFET does not need to be turned on at light load or shutdown state and its body diode can conduct the small system current without significant loss. To extend the system run time with battery, BATFET needs to be turned on only at high current to reduce the loss and voltage drop across its source and drain (channel conduction rather than body diode conduction). During a complete system shutdown, the internal BATFET charge pump can be disabled to minimize battery quiescent current. The battery power path can be disconnected by opening switch S1 on the VCC pin (see Figure 5). In this state, the host can still be powered through the BATFET body diode. Since the system load is minimal during shutdown, conduction loss across the body diode remains low.

Inductor Selection

The SGM41535 offers 3 selectable fixed switching frequency. Higher switching frequency reduces the required inductance and capacitances. The inductor saturation current must be higher than the highest peak current that is the sum of charging current (I_{CHG}) and half of the peak to peak ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + \frac{1}{2} I_{RIPPLE} \tag{4}$$

The inductor ripple is determined by the input voltage, duty cycle, switching frequency and inductance:

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{f_{SW} \times L} \tag{5}$$

The maximum inductor ripple current occurs at around 50% duty cycle (D = 0.5). For example, for a 3-cell pack the charge voltage varies from 9V to 12.6V and if a 20V adapter is used, the ripple is maximum when the battery voltage is around 10V. For a 4-cell battery, the voltage varies from 12V to 16.8V and 12V will generate the highest inductor current ripple with a 20V adapter.

For a reasonable tradeoff between size and efficiency, the inductor current ripple is usually considered in the range of 20% to 40% of the maximum charge current.

The UCP function monitors the current-sense resistor voltage on a cycle-by-cycle basis. The typical falling-edge threshold is 6mV, equivalent to 0.6A with a 10mΩ sense resistor. If the average charge current falls below 125mA (using a 10mΩ resistor), the low-side MOSFET is turned off and remains off except for BTST capacitor refresh pulses. During this off state, inductor current freewheels through the MOSFET body diode.

Input Capacitor

Input capacitor must be able to circulate all input current ripple and high frequency switching currents and keep them away from the input line and adapter. When the converter is providing charge current the resulting RMS ripple current in the input can be estimated from Equation 6. The worst case occurs around D = 50%. If the converter operates in a range away from 50% duty cycle, the worst case will be at the duty cycle which is closest to 50%:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \tag{6}$$

It is recommended to use low ESR ceramic capacitor like X7R or X5R for input decoupling. These capacitors must be placed close to the drain of the HSFET and source of the LSFET. DC bias voltage derating must be considered for the ceramic capacitors. For a 20V to 30V adapter, at least a 35V capacitor is needed. For a typical 3A to 4A charge current, a 10μF to 20μF ceramic capacitance is recommended for input capacitor.

DC bias effect can lead to significant capacitance drop, especially at higher input voltages and for small capacitor package sizes. It is recommended to refer to the capacitor datasheet to evaluate the DC bias performance. A higher voltage rating and larger capacitance value may be required to achieve the desired capacitance at the operating voltage.

APPLICATION INFORMATION (continued)

Output Capacitor

Output capacitor must also be able to carry the inductor ripple current and store enough energy for stable operation against system load transients. The output capacitor RMS current can be estimated from Equation 7:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{7}$$

The SGM41535 uses an internal compensator. For good loop stability, the output LC filter resonant frequency should be set between 10kHz to 20kHz. A 35V, X7R or X5R ceramic capacitor is recommended for the output capacitor. For a typical 3A to 4A charger, a 10μF to 20μF capacitance should be sufficient. C_{OUT} must be placed after R_{SR} resistor for the best accuracy in the charge current regulation.

Power MOSFETs Selection

Synchronous switching is implemented with two external N-channel MOSFETs. The internal gate drivers provide 6V gate drive voltage. Choose at least 40V MOSFETs for 20V to 30V input voltage rating.

Switching MOSFETs are usually selected based on a figure-of-merit (FOM) to tradeoff between the conduction and switching losses. For the HSFET, it is defined as the product of on-resistance (R_{DSON}) and the gate-to-drain charge (Q_{GD}). For the LSFET, it is defined as the product of the R_{DSON} and the total gate charge (Q_G).

$$FOM_{HS} = R_{DSON} \times Q_G \quad FOM_{LS} = R_{DSON} \times Q_G \tag{8}$$

A MOSFET with lower FOM value generates lower total loss. Lower R_{DSON} usually costs more with the same package size.

The HSFET loss can be estimated form Equation 9 in which t_{ON} is the turn-on time and turn-off time is represented by t_{OFF}:

$$P_{HS} = D \times I_{CHG}^{\,2} \times R_{DSON} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times \left(t_{ON} \times t_{OFF}\right) \times f_{SW} \tag{9}$$

Conduction and switching losses are represented by the first and second terms respectively. Note that R_{DSON} typically increases by 50% with +100°C rise in junction temperature. t_{ON} and t_{OFF} times can be estimated by Equation 10:

$$t_{ON} = \frac{Q_{SW}}{I_{ON}} \quad t_{OFF} = \frac{Q_{SW}}{I_{OFF}} \tag{10}$$

where I_{ON} and I_{OFF} are the turn-on and turn-off gate driving currents and Q_{SW} is the switching charge. If Q_{SW} is not given, Equation 11 can be used to estimate it based on the Q_{GD} and gate-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \tag{11}$$

Gate driving currents can also be estimated from REGN voltage (V_{REGN}), plateau voltage of the MOSFET (V_{PLT}), and the total gate driver turn-on and turn-off gate resistances (R_{ON} and R_{OFF}):

$$I_{ON} = \frac{V_{REGN} - V_{PLT}}{R_{ON}} \quad I_{OFF} = \frac{V_{PLT}}{R_{OFF}} \tag{12}$$

The LS MOSFET conduction loss is given by Equation 13 when operating in continuous synchronous conduction mode:

$$P_{BOTTOM} = \left(1 - D\right) \times I_{CHG}^{\,2} \times R_{DSON} \tag{13}$$

During non-synchronous operation, the LS MOSFET remains off, allowing inductor current to freewheel through its body diode. The body diode power loss is given by Equation 14, which depends on the diode forward voltage (V_F), the non-synchronous charging current ($I_{NONSYNC}$), and the duty cycle (D).

$$P_D = V_F \times I_{NONSYNC} \times (1 - D) \tag{14}$$

In non-synchronous mode, the maximum charging current is 0.25A (with a 10mΩ sense resistor), or 0.5A when the battery voltage is below 2.5V. The body diode power loss (PD) reaches its maximum at the minimum duty cycle, which occurs at the lowest battery voltage. It is recommended to choose a MOSFET with an internal Schottky diode or one with sufficient body diode rating to carry the maximum non-synchronous charge current.

Input Filter

An input filter is necessary to prevent damage to the device due to the voltage spikes cause by the adapter hot plug-in. These spikes are generated by resonance of the cable parasitic inductance and the input capacitor. This filter should be properly designed and tested to avoid over-voltage damage.

Various technics can be used for damping or limiting the voltage spikes during adapter hot plug, such that the peak is adequately less than the V_{CC} maximum voltage rating. One simple method is using a large electrolytic capacitor at the input. The high ESR of this kind of capacitors can damp the resonance and reduce the spike peak significantly. Another common method is using high current TVS Zener diodes for clamping the spikes to a safe level. These methods may need too much space and can be costly.

APPLICATION INFORMATION (continued)

A more cost-effective and compact solution is presented in Figure 7. The R_1 and C_1 form an RC network to damp the resonance and limit the spike to a safe level. D_1 is added to protect VCC pin from reverse voltage caused by oscillations. C_2 is placed as close as possible to VCC pin for decoupling and must be smaller than C_1 such that R_1 is the dominant component of the circuit equivalent ESR to get sufficient damping. R_2 limits the D_1 inrush current and protects D_1 during adapter hot plug-in. $R_2 \times C_2$ time constant should be around 10μs to limit the dV/dt of the VCC pin and the hot plug inrush current (R_1 carries the high inrush current). R_1 package size must be large enough (with minimal parasitic inductance) to tolerate the inrush current power loss (check the resistor datasheet). This filter must be tested in the real application for verification and any required adjustment after completing the design.

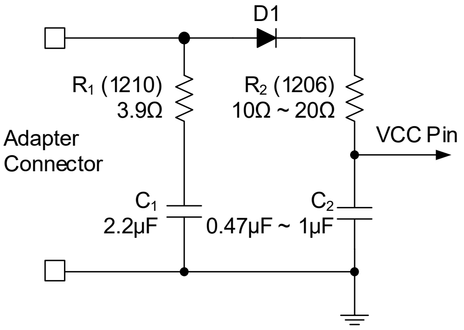


Figure 7. Input Filter

SGM41535 Design Guideline

Figure 8 shows the block diagram of the SGM41535 special short-circuit protection scheme. The RDSON voltage drop of the MOSFETs is monitored after a certain blanking time from the beginning of each cycle through the COMP1 and COMP2 comparators. If a MOSFET or inductor short occurs, the corresponding comparator will increment its counter. The charger will latch off if a counter reaches to 7 short-circuit detections and will not be released unless the adapter is removed and re-inserted.

In normal operation, the low-side MOSFET conducts current from source to drain. The resulting negative voltage drop prevents the over-current comparator from triggering. But if a short occurs across the high side MOSFET or the inductor, a large current will flow from the drain to the source of the low side MOSFET that can be detected by the low side MOSFET over-current comparator (COMP2). The low-side switch voltage drop is sensed through the PHASE and GND pins.

COMP1 detects a high-side MOSFET short by monitoring the voltage drop between the ACP and PHASE pins. Therefore, it monitors the total voltage drop on the high side MOSFET, R_{AC} (adapter sense resistor) and PCB traces from ACN pin of the R_{AC} to the high side MOSFET drain pin. There is usually a relatively long path from the R_{AC} sense resistor to the converter positive supply (high side MOSFET drain) and its effect must be minimized by a proper PCB layout.

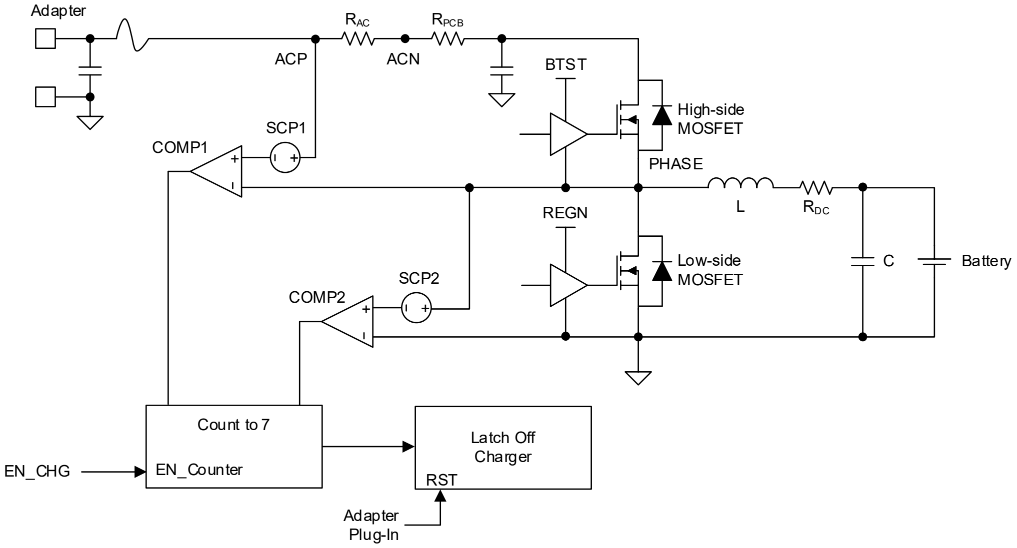


Figure 8. Block Diagram of SGM41535 Short-Circuit Protection

APPLICATION INFORMATION (continued)

To avoid unwanted shutdowns by false short-circuit detection, good PCB layout and careful R_{DSON} selection for MOSFETs are critical.

Figure 9 shows an improvement PCB layout example and its equivalent circuit. However, the system and charger input current paths are not separated after ACN, causing the PCB voltage drop from the system current to couple into the COMP1 sense voltage. In a bad layout, the system current is drawn at a point after the charger input point. In such case all voltage drops cause by system current are included in COMP1 over-current sensing. The worst-case condition occurs when the sum of the system current and charger input current equals the DPM current limit. If the system load increases further, the charger reduces the charge current to maintain the input current at the DPM limit.

Figure 10 shows the optimized PCB layout example. The system current and charger input current paths are separated and only the charger input current PCB voltage drops sensed by COMP1 will minimize the risk of charger shutdown due to false charger short-circuit detection. It also simplifies the layout design for applications with high system current.

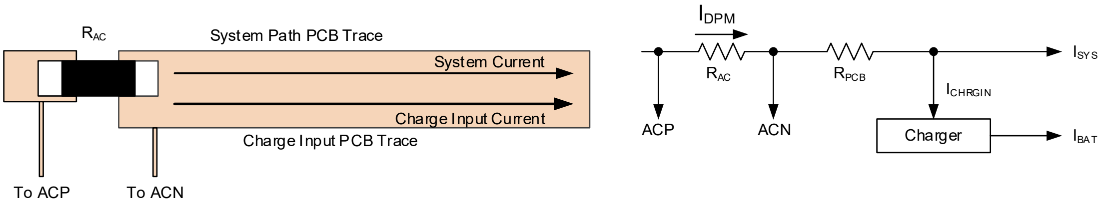
The total voltage drop sensed by the short-circuit comparator in Figure 9 can be express as the Equation 15.

$$V_{TOP} = R_{AC} \times I_{DPM} + R_{PCB} \times \left[I_{CHRGIN} + \left(I_{DPM} - I_{CHRGIN} \right) \times k \right] + R_{DSON} \times I_{PEAK} \tag{15}$$

R_{AC} is the input sense resistance (adapter current sense), I_{IN} is the input current, R_{PCB} is the PCB parasitic resistance between R_{AC} and the converter, I_{BUCK_IN} is the charger input current, R_{DSON} is the HS MOSFET on-resistance and I_{PEAK} is the peak inductor current. The k represents a PCB factor that varies from k = 0 for the well decoupled layout (Figure 10) in which the PCB traces for system and charge currents are completely separated, to k = 1 for the fully coupled layout (Figure 9) in which one trace carries both currents (whole I_{DMP} current). The total voltage drop (V_{HS}) must remain below the HS short-circuit comparator threshold to avoid false triggering of the short-circuit shutdown.

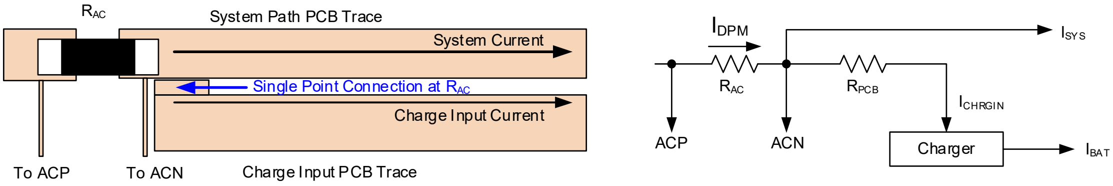
The LS comparator threshold can be disabled or set to 130mV and 240mV by programming the IFAULT_LO Comparator Threshold Adjust bit in the InputCurrent register to 0 or 1 respectively. The high-side MOSFET short-circuit voltage drop threshold can be adjusted via SMBus command. IFAULT_HI Comparator Threshold Adjust [1:0] = 00, 01, 10, or 11 set the HSFET voltage drop comparator threshold 500mV, 700mV, 900mV, and 1100mV respectively, and is disabled by IFAULT_HI_DIS bit.

Proper short-circuit detection thresholds should be programmed by the host when the PCB layout is known, to avoid false protection triggers.



(a) PCB Layout (b) Equivalent Layout

Figure 9. PCB Layout Example to Minimize False Short-Circuit Detection



(a) PCB Layout (b) Equivalent Layout

Figure 10. Optimized PCB Layout Example to Minimize False Short-Circuit Detection

LAYOUT INFORMATION

To reduce the switching losses, try to minimize the switching rise and fall times. By selecting component with right sizes, and proper placement and routing, the high frequency current path (loop) can be minimized as explained in Figure 11. At the same time, the switching node and connected conductors must have minimal areas to minimize radiation and electrical and magnetic coupling to the nearby traces and elements. For a proper PCB layout, follow the next guidelines in the specified priority order.

1. Place input ceramic capacitor as close as possible to switching MOSFETs (HS drain and LS source) with the shortest copper connections. MOSFETS and capacitor must be on the same layer of the PCB (Do not use vias for these connections).

2. Place the device close to the switching MOSFET gate pins to minimize the gate drive path. The device can be placed on the other side of the PCB.

3. Place one inductor terminal close to the MOSFETS switching node with a short and wide trace and minimum copper area to minimize radiation. Do not use multiple layer parallel traces for this connection. Try to minimize parasitic capacitance coupling from the switching node to any other trace, plane, or component.

4. Place the charging current sensing resistor right next to the inductor output terminal and route its sense leads with Kelvin connections, as shown in Figure 12, to the device on the same layer. Keep the sense traces close to each other to minimize loop area and do not route them through or shared with a high-current path. Place a decoupling capacitor on the sense traces next to the device.

5. Place output capacitor close to the sensing resistor output pin. Place its GND pin close to the low side switch and Input capacitor ground retunes.

6. Input and output capacitor ground connections must be tied together and connected to the same copper area before connection to the system ground.

7. Connect and tie charger power ground and analog ground only in a single point. Pour an analog ground plane under the device but keep it away from power pins to minimize inductive and capacitive noise coupling.

8. Always route analog and power grounds separately. Connect analog and power grounds only at one point either using the device power pad or with a tiny 0Ω jumper resistor (in the latter case, tie the power pad to the analog ground if possible).

9. Place any decoupling capacitor close to the respective device pin and device GND with the shortest trace lengths.

10. Soldering the device exposed power pad to the PCB ground is necessary. Consider enough thermal vias under the device, to connect it to other ground planes for better heat conduction and improved thermal performance.

11. Consider enough vias with proper sizes based on the maximum current in the path.

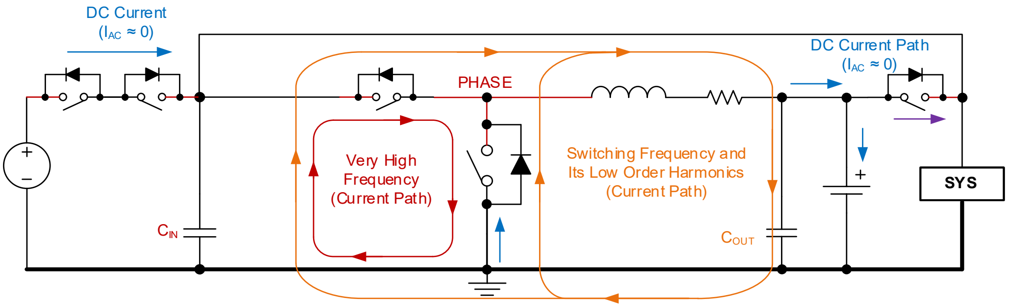


Figure 11. High Frequency Current Path

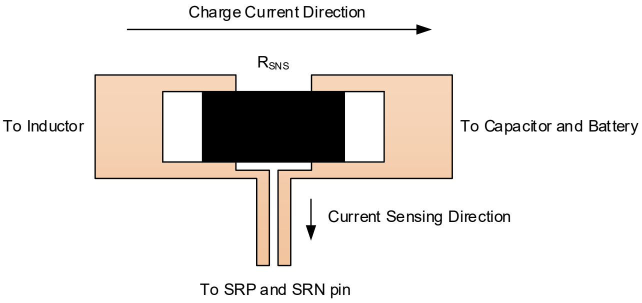


Figure 12. Sensing Resistor PCB Layout

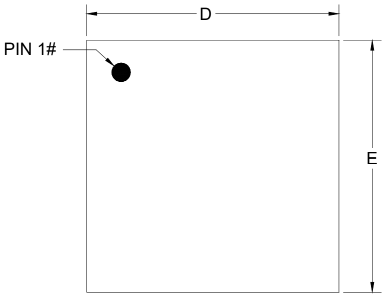
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

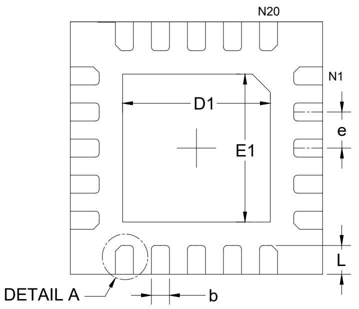
Changes from Original to REV.A (FEBRUARY 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

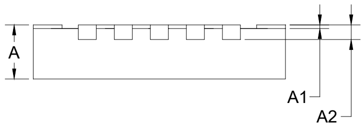
TQFN-3.5×3.5-20L



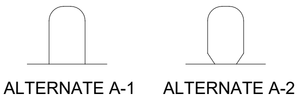
TOP VIEW



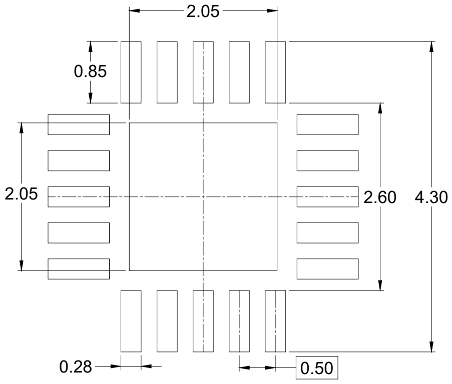
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTION



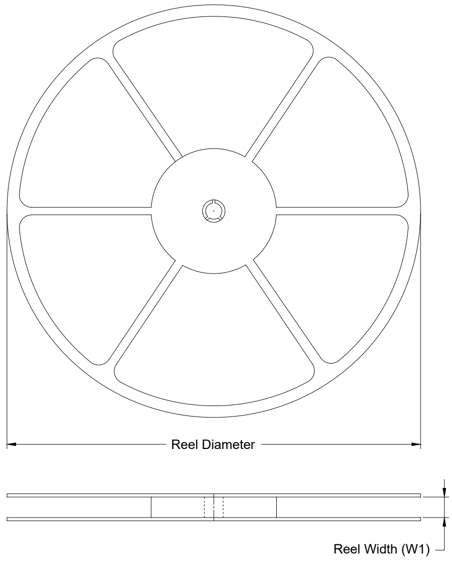
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	-	-	0.050
A2	0.203 REF		
D	3.450	3.500	3.550
D1	2.000	2.050	2.100
E	3.450	3.500	3.550
E1	2.000	2.050	2.100
b	0.200	0.250	0.300
e	0.500 BSC		
L	0.350	0.400	0.450

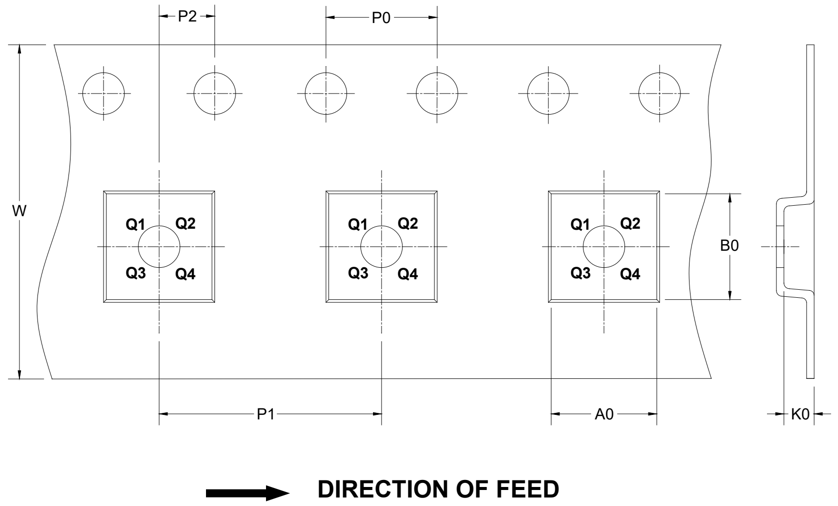
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



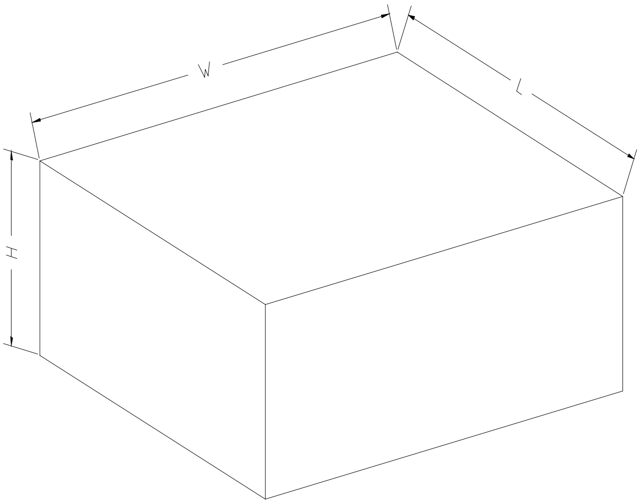
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3.5×3.5-20L	13"	12.4	3.80	3.80	0.95	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002