SGM61231
4.5V to 28V Input, 3A Output, Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61231 is a current mode controlled synchronous Buck converter with 4.5V to 28V input range and 3A rated output current. The quiescent current is 190μA (TYP) and the shutdown supply current is 1.2μA (TYP). Two MOSFETs with low R_{DSON} are integrated to improve the efficiency. Efficiency is maximized through power-save mode (PSM) at light loads. The SGM61231 has adjustable soft-start time for flexible application.

The UVLO level can be adjusted (increased) by an external resistor divider. Secure operation in overload conditions is ensured by cycle-by-cycle current limit, hiccup protection and thermal shutdown protection. The low-side MOSFET has sinking current limit to prevent excessive reverse current.

The SGM61231 is available in a Green SOIC-8 (Exposed Pad) package.

FEATURES

- **4.5V to 28V Input Voltage Range**
- **0.8V Internal Voltage Reference**
- **Typical 190μA Quiescent Current**
- **Typical 1.2μA Shutdown Current**
- **Integrated 125mΩ and 85mΩ MOSFETs Support up to 3A Continuous Output Current**
- **Adjustable Soft-Start**
- **Fixed 770kHz Frequency**
- **High Light-Load Efficiency**
- **Hiccup Mode Over-Current Protection**
- **Over-Voltage Protection**
- **Thermal Shutdown Protection**
- **Available in Green SOIC-8 (Exposed Pad) Package**

APPLICATIONS

Industrial Power Supplies
Distributed Power Bus Supplies
LCD Display
CPE Equipment
Set-Top Displays
Battery Chargers

SIMPLIFIED SCHEMATIC

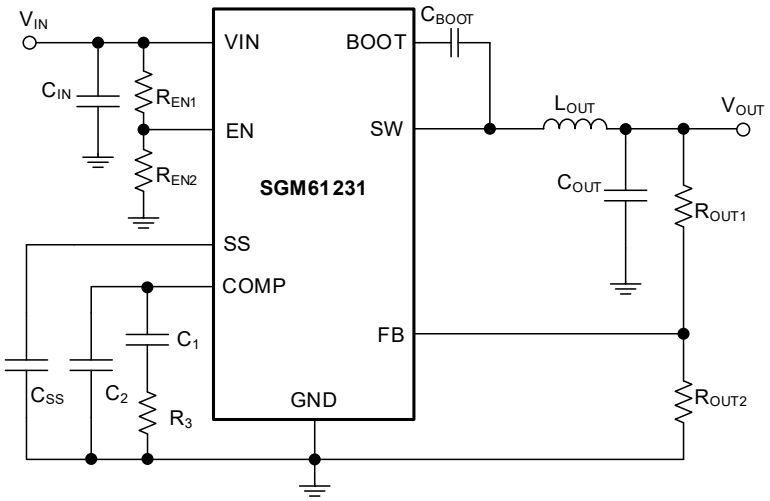


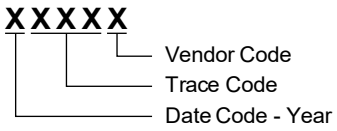
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61231	SOIC-8 (Exposed Pad)	-40℃ to +150℃	SGM61231TPS8G/TR	SGM 61231TPS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range ..... -0.3V to 30V
EN Voltage..... -0.3V to 6V
BOOT Voltage .....-0.3V to (V_{SW} + 6.5V)
FB, COMP, SS Voltages..... -0.3V to 6V
BOOT-SW Voltage .....0V to 6.5V
SW Voltage..... -0.3V to 30V
SW Voltage (10ns Transient)..... -3.5V to 30V
V_{DIFF}, (GND to Exposed Thermal Pad) .....-0.2V to 0.2V
Package Thermal Resistance
SOIC-8 (Exposed Pad), θ_{JA}..... 37.5℃/W
SOIC-8 (Exposed Pad), θ_{JB}..... 14.2℃/W
SOIC-8 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 48.2℃/W
SOIC-8 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 5.9℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM.....±4000V
CDM .....±2000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range .....4.5V to 28V
Output Current Range .....0A to 3A
Operating Junction Temperature Range.....-40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

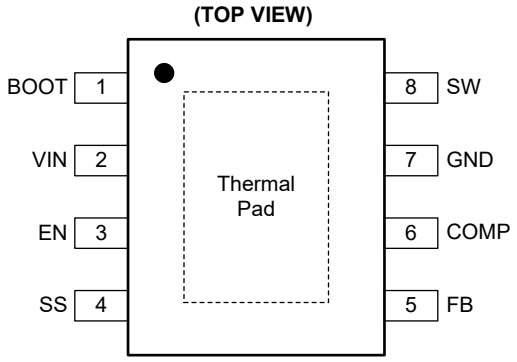
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	BOOT	O	Bootstrap Input. Connect it to SW pin with a 0.1μF ceramic capacitor. The MOSFET will turn off if the BOOT capacitor voltage drops below its BOOT-SW UVLO level to get the capacitor voltage refreshed.
2	VIN	P	Input Supply Voltage. Connect it to a 4.5V to 28V power source.
3	EN	I	Active High Enable Input. Float or pull up to enable, or pull down below 1.12V (TYP) to disable the device. VIN UVLO level can be programmed using a resistor divider from VIN pin.
4	SS	I	Soft-Start Programming Pin. Connect an external capacitor to SS pin to program the output rise time during startup.
5	FB	I	Transconductance (gm) Error Amplifier (EA) Inverting Input. It is used as the feedback input to sense and regulate V_{OUT}. Output voltage is set by a resistor divider from the output.
6	COMP	O	EA Output (internally connected to the PWM comparator input). Place the compensation network between COMP and GND. The EA output current is injected into this network to create the control voltage (V_C). It will be compared with the compensated sensed current signal to generate the switching pulses (set duty cycle).
7	GND	G	Ground.
8	SW	P	Switching Node of the Converter. Connect it to the bootstrap capacitor and the inductor.
Exposed Pad	GND	G	Thermal Pad. It helps to cool the device junction and must be connected to GND pin for proper operation.

NOTE: I = Input, O = Output, P = Power, G = GND.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +150℃, V_{IN} = 4.5V to 28V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage and UVLO (VIN Pin)						
Operating Input Voltage	V_{IN}		4.5		28	V
Input UVLO Threshold	V_{UVLO}	Rising V_{IN}		4.2	4.5	V
Input UVLO Hysteresis	V_{UVLO_HYS}			320	390	mV
VIN Pin Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V		1.2	14	μA
VIN Pin Operating Non-Switching Supply Current	I_Q	V_{REF} × 105%		190	290	μA
Enable (EN Pin)						
Enable Threshold	V_{EN_TH}	Rising		1.19	1.27	V
		Falling	1.03	1.12		V
Input Current	I_{EN}	V_{EN} = 1.1V		1.2		μA
Hysteresis Current	I_{HYS}	V_{EN} = 1.3V		3.7		μA
Voltage Reference						
Leakage Current into FB	I_{FB_LKG}	V_{FB} = 800mV		20	100	nA
Voltage Reference	V_{REF}	T_J = +25℃	0.785	0.8	0.812	V
		T_J = -40℃ to +150℃	0.782	0.8	0.815	
MOSFET						
High-side Switch Resistance (1)	R_{DSON_HS}	$V_{BOOT-SW}$ = 3.5V		135	250	mΩ
		$V_{BOOT-SW}$ = 5V		125	230	
Low-side Switch Resistance (1)	R_{DSON_LS}			85	170	mΩ
Error Amplifier						
Error-Amplifier Transconductance	gm_{EA}	-2μA < I_{COMP} < 2μA, V_{COMP} = 1V		155		μA/V
Error-Amplifier Source and Sink Current	I_{EA}	V_{COMP} = 1V, 100mV overdrive		14		μA
Start Switching Peak Current Threshold (2)	I_{gm}			0.8		A
COMP to I_{SWITCH} gm	gm_{PS}			9		A/V
Current Limit						
High-side Switch Current Limit Threshold	I_{LIM_HS}	V_{IN} = 12V, V_{OUT} = 5V, L = 6.8μH, T_J = +25℃	3.6	5.8	7.8	A
Low-side Switch Sourcing Current Limit	I_{LIM_LS}		3.0	4.4	5.9	A
Zero Cross Current	I_{LS_ZC}			20		mA
Thermal Shutdown						
Thermal Shutdown (2)	T_{SD}			165		℃
Thermal Shutdown Hysteresis (2)	T_{HYS}			20		℃
BOOT Pin						
BOOT-SW UVLO	$V_{UVLO\_BOOT-SW}$			3.2	3.6	V
Soft-Start						
Soft-Start Charge Current	I_{SS}			2.1		μA

NOTES:

1. Measured at pins.
2. Not production tested.

TIMING REQUIREMENTS

PARAMETER	MIN	TYP	MAX	UNITS
Current Limit				
Hiccup Wait Time		512		Cycles
Hiccup Time before Restart		16384		Cycles

SWITCHING CHARACTERISTICS

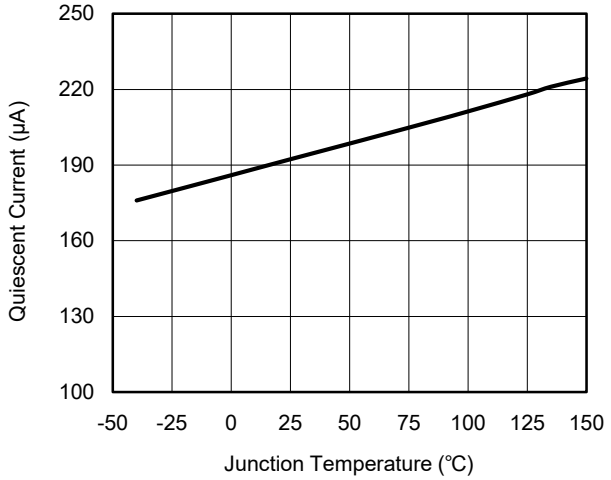
(All typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SW Pin					
Minimum On-Time	Measured at 90% to 90% of V_{IN}, I_{SW} = 2A		110		ns
Minimum Off-Time	$V_{BOOT-SW}$ ≥ 3.5V		90		ns
Switching Frequency					
Internal Switching Frequency			770		kHz

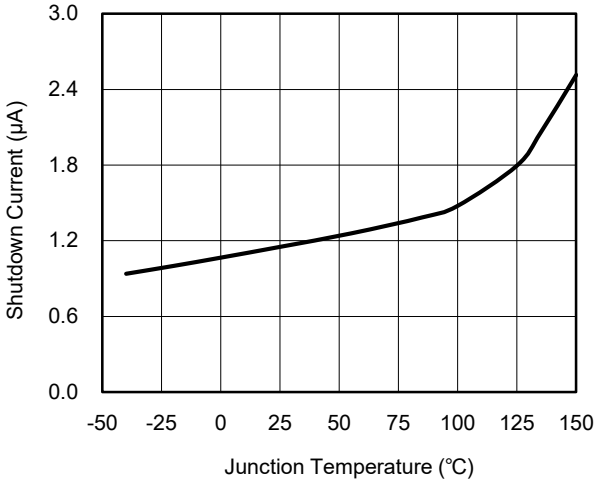
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, and the corresponding BOM can be found in Table 1, unless otherwise noted.

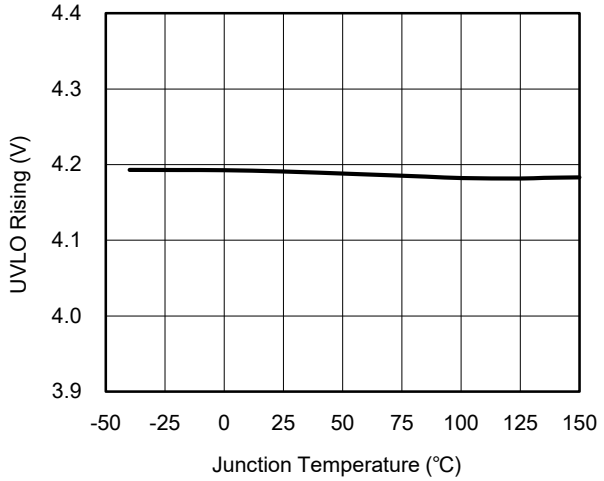
Quiescent Current vs. Junction Temperature



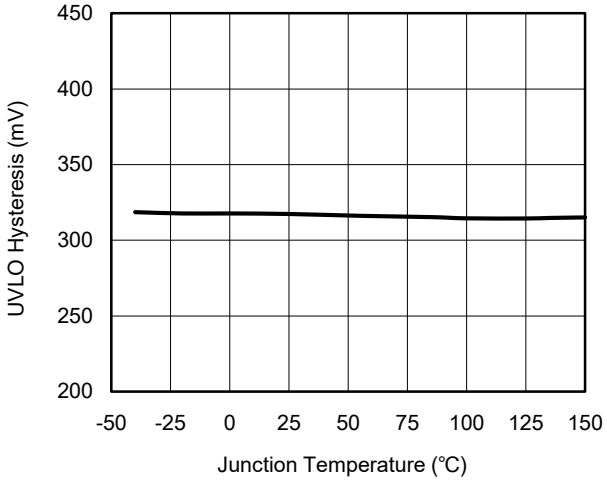
Shutdown Current vs. Junction Temperature



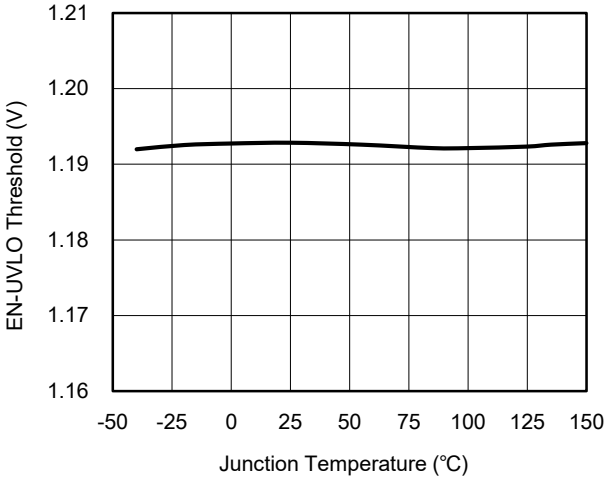
UVLO Rising vs. Junction Temperature



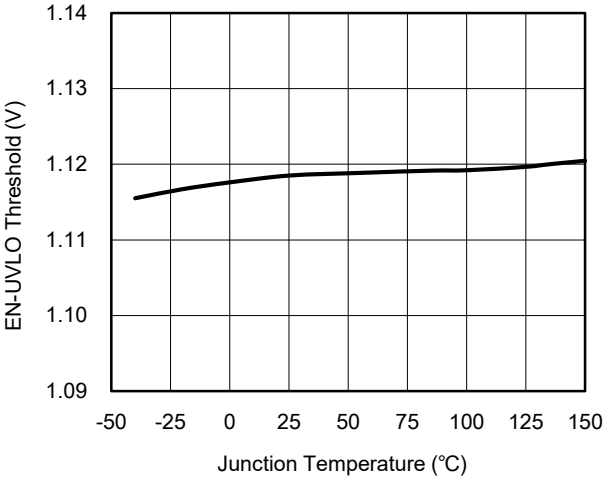
UVLO Hysteresis vs. Junction Temperature



EN-UVLO Rising Threshold vs. Junction Temperature



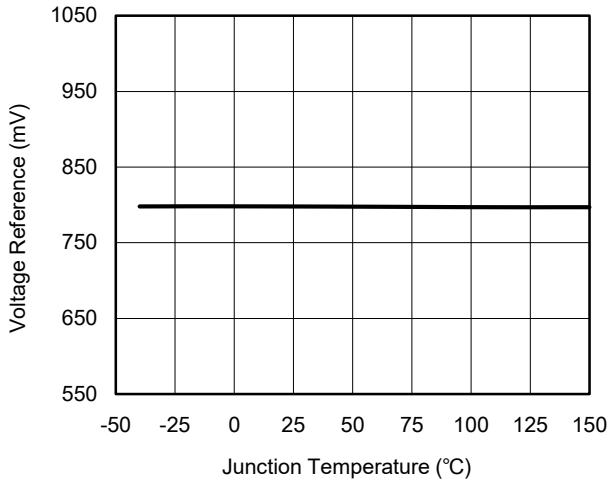
EN-UVLO Falling Threshold vs. Junction Temperature



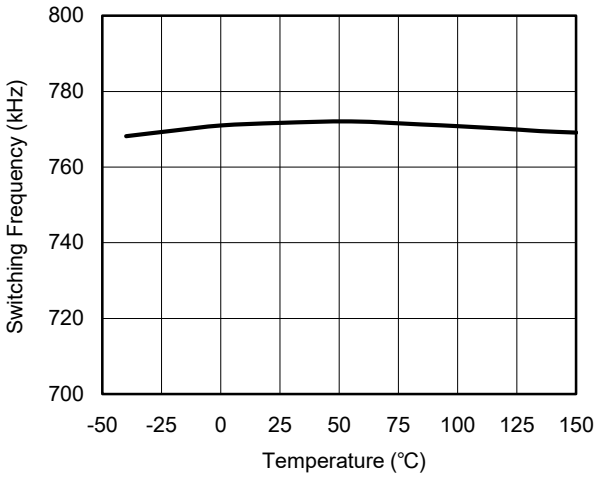
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, and the corresponding BOM can be found in Table 1, unless otherwise noted.

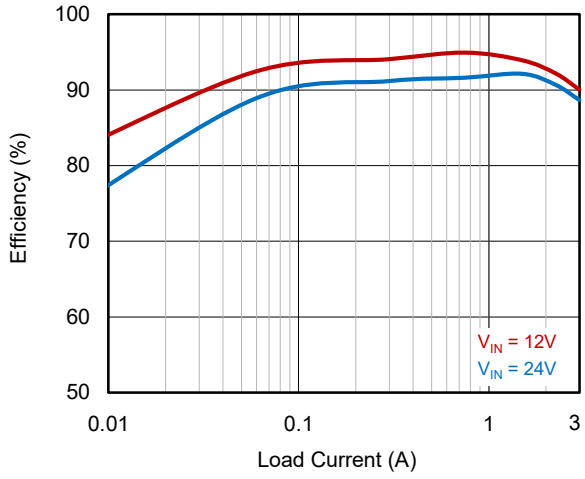
Voltage Reference vs. Junction Temperature



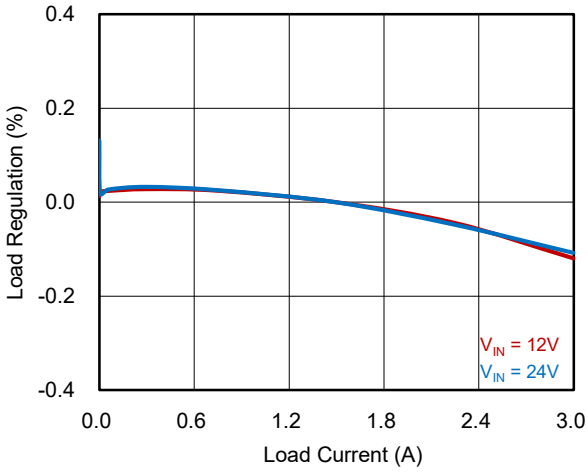
Switching Frequency vs. Temperature



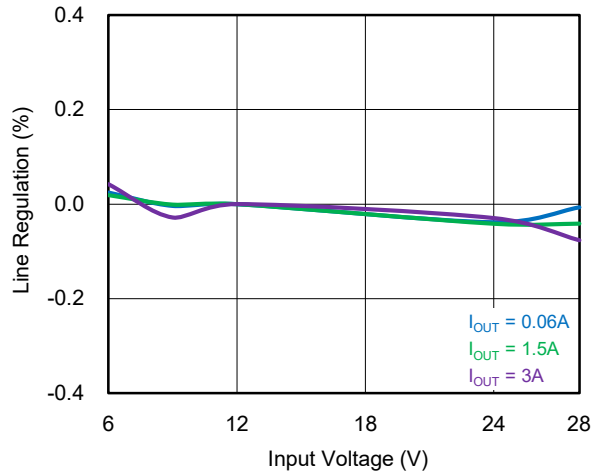
Efficiency vs. Load Current



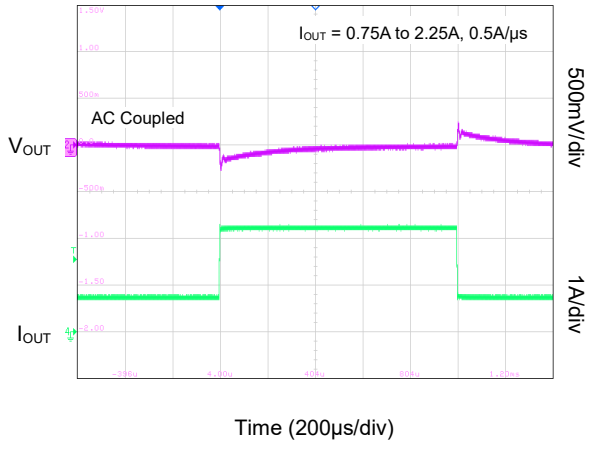
Load Regulation vs. Input Voltage



Line Regulation vs. Input Voltage



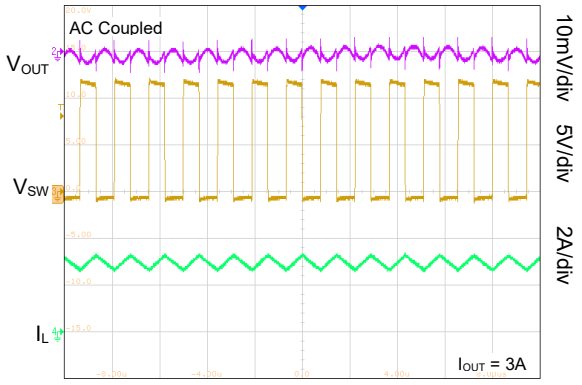
Load Transient



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

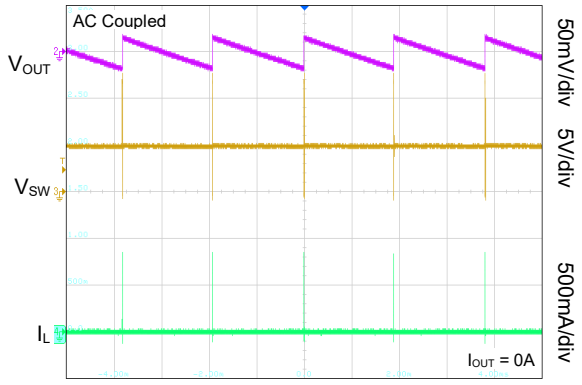
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, and the corresponding BOM can be found in Table 1, unless otherwise noted.

CCM Mode



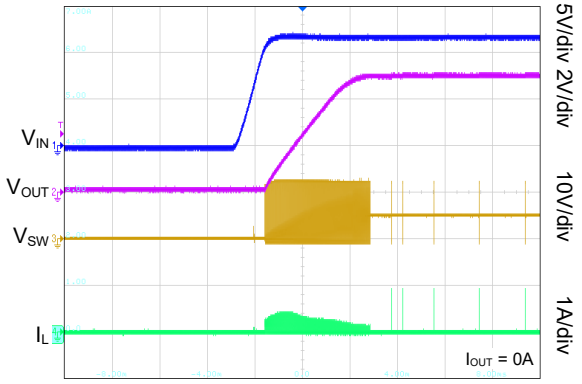
Time (2μs/div)

PSM Mode



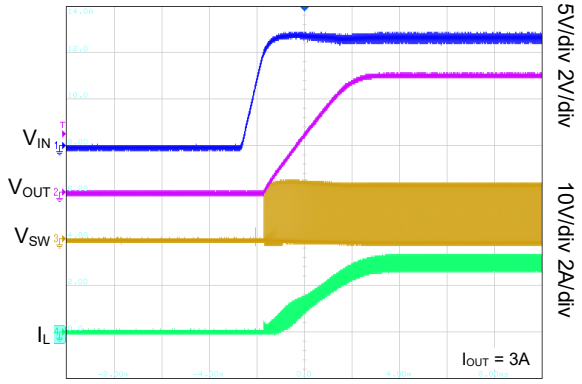
Time (1ms/div)

Start-Up by VIN



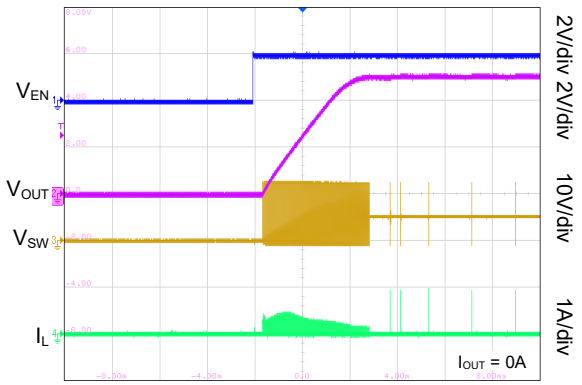
Time (2ms/div)

Start-Up by VIN



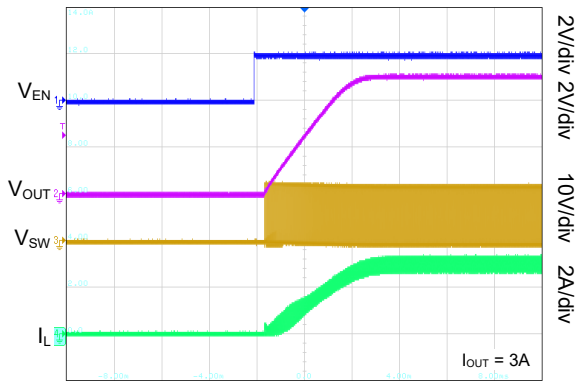
Time (2ms/div)

Start-Up by EN



Time (2ms/div)

Start-Up by EN

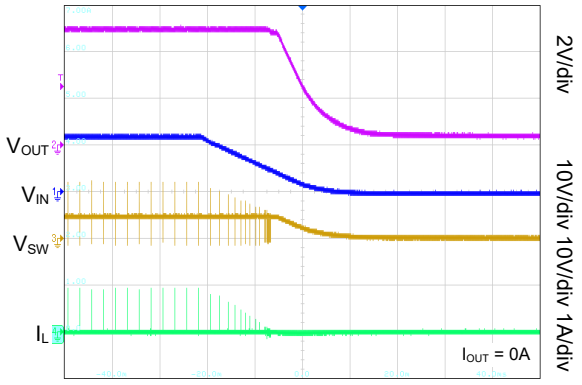


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

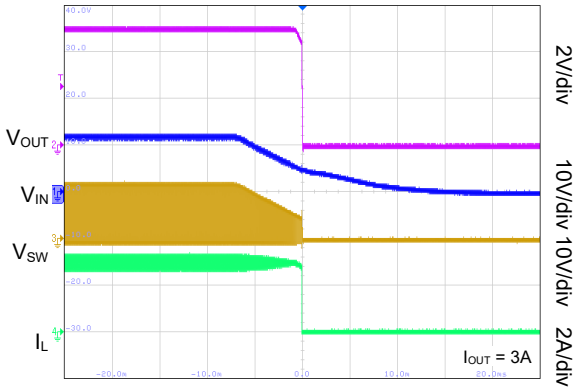
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, and the corresponding BOM can be found in Table 1, unless otherwise noted.

Shutdown by VIN



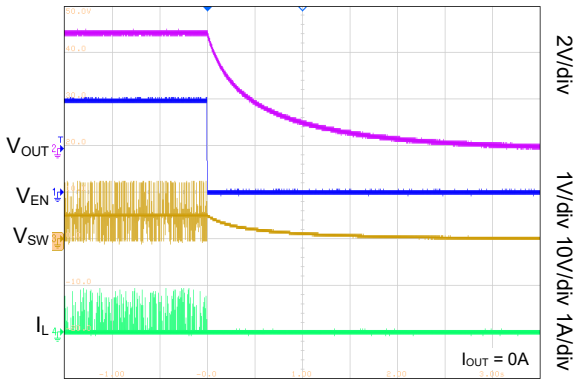
Time (10ms/div)

Shutdown by VIN



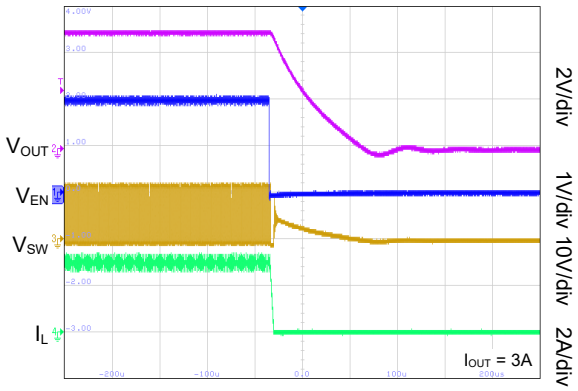
Time (5ms/div)

Shutdown by EN



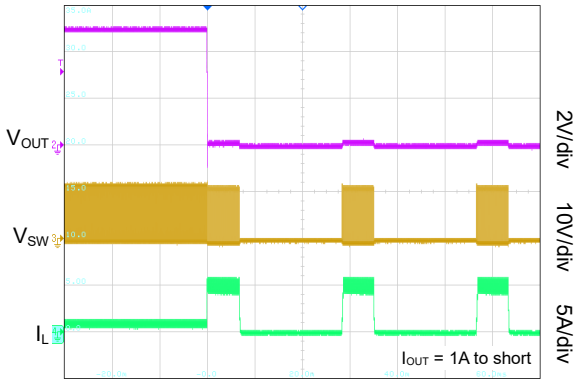
Time (500ms/div)

Shutdown by EN



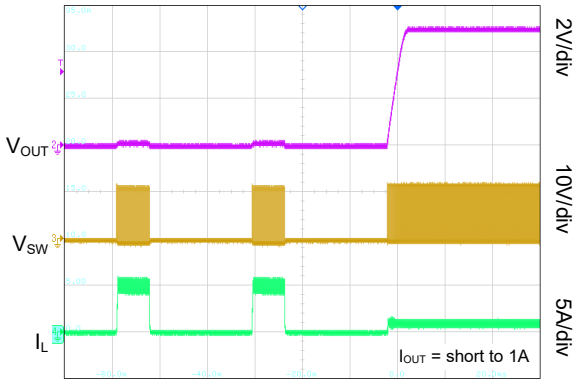
Time (50μs/div)

SCP Entry



Time (10ms/div)

SCP Recovery



Time (10ms/div)

FUNCTIONAL BLOCK DIAGRAM

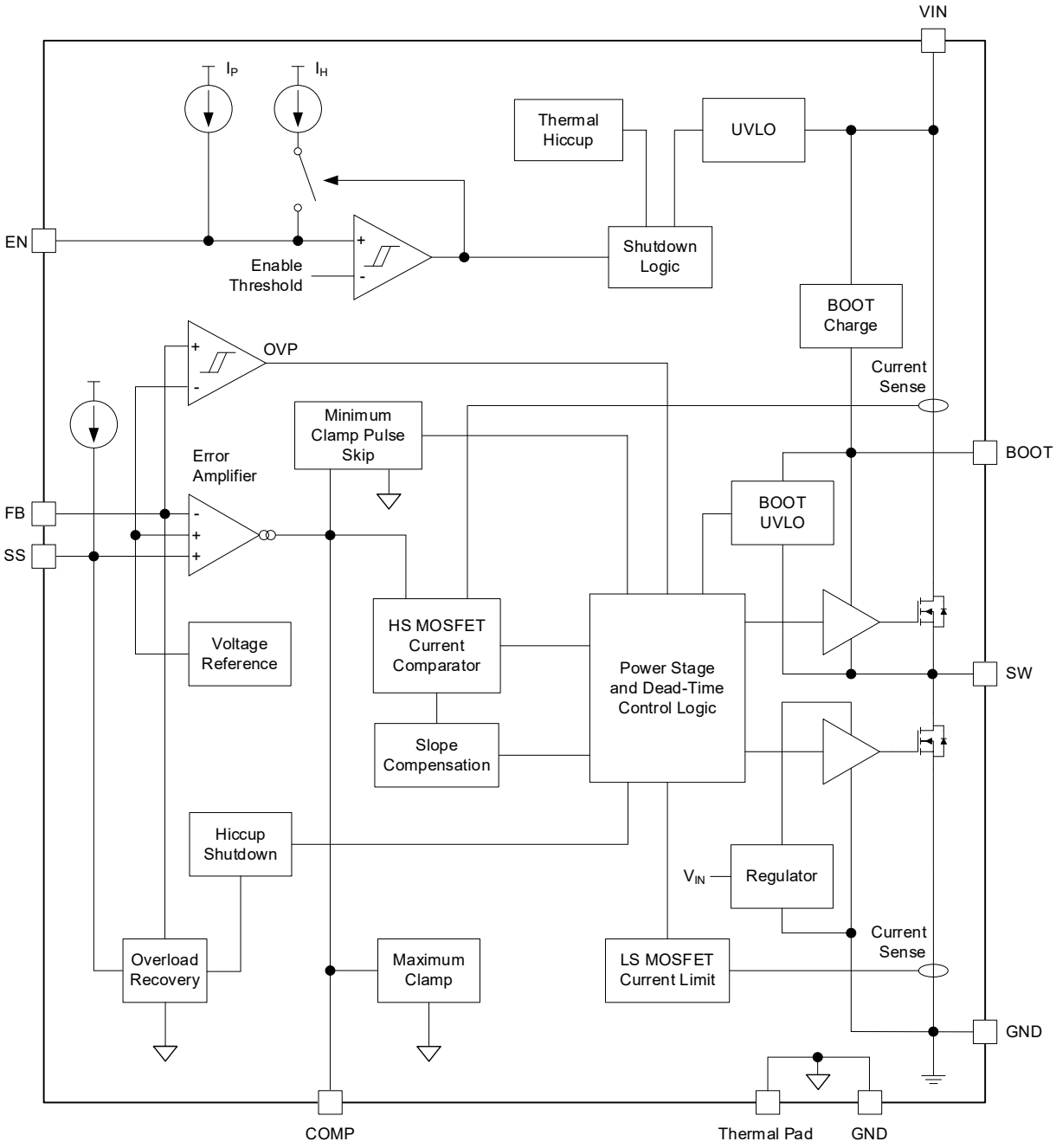


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61231 is a 28V synchronous Buck converter with two integrated N-MOSFETs and 3A continuous output current capability. Using peak current mode control provides the device good line and load transient responses with reduced output capacitance and simple compensation.

The minimum operating input voltage of the device is 4.5V. The output voltage can be set down to 0.8V (reference voltage). Typical no switching operating current is 190μA. The shutdown current is 1.2μA if the device is disabled. High efficiency is achieved through the integrated low R_{DSON} high-side switch (125mΩ) and low-side switch (85mΩ).

The EN pin is internally pulled up by a current source that can keep the device enable if EN pin is floating. It can also be used to increase the input UVLO threshold with a resistor divider.

The bootstrap diode is integrated and only a small capacitor (C_{BOOT}) between BOOT and SW pins is needed for the high-side MOSFET gate driving bias. A separate UVLO circuit monitors C_{BOOT} voltage and turns off the high-side switch if C_{BOOT} voltage falls below a preset threshold.

Additional features such as thermal shutdown, over-voltage protection, and short-circuit protection (hiccup mode) are also provided.

The SGM61231 has an internal current source on the SS pin that allows soft-start time to be adjusted with a small external capacitor. The device has a fixed 770kHz switching frequency.

Minimum Input Voltage (4.5V) and UVLO

The recommended minimum operating input voltage is 4.5V. It may operate with lower input voltages that are above the V_{IN} rising UVLO threshold (4.2V TYP). The V_{IN} UVLO threshold has a hysteresis of 320mV (TYP). If V_{IN} falls below the falling UVLO voltage, the device will stop switching. If the EN pin is left floating or pulled high and V_{IN} exceeds the rising UVLO threshold, the device will start up with a soft-start.

Enable Input and UVLO Adjustment

The EN pin is able to control the device on or off. An internal pull-up current source keeps the EN pin voltage at high state by default. The EN pin can be pulled up to a voltage above its rising threshold or left floating to enable the device. The device will be disabled if the EN voltage is pulled externally below the falling threshold voltage.

If an application requires increasing the V_{IN} turn-on threshold and adding hysteresis to the V_{IN} UVLO, a voltage divider as shown in Figure 3 is required. When EN voltage exceeds V_{ENH} = 1.19V (TYP), an additional 3.7μA current is injected to the divider to provide hysteresis and it will be removed when EN pin voltage is below V_{ENL} = 1.12V (TYP). Use Equation 1 and 2 to calculate these resistors. V_{START} is the input start (turn-on) threshold voltage and V_{STOP} is the input stop (turn-off) threshold voltage.

$$R_{EN1} = \frac{V_{START}\left(\frac{V_{ENL}}{V_{ENH}}\right) - V_{STOP}}{1.2\mu A \times \left(1 - \frac{V_{ENL}}{V_{ENH}}\right) + 3.7\mu A} \quad (1)$$

$$R_{EN2} = \frac{R_{EN1} \times V_{ENL}}{V_{STOP} - V_{ENL} + R_{EN1}(1.2\mu A + 3.7\mu A)} \quad (2)$$

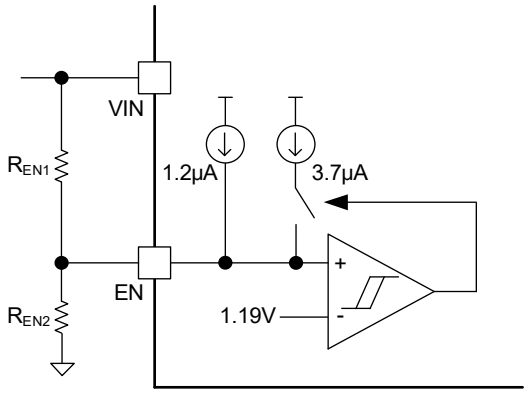


Figure 3. VIN UVLO Adjustment

Bootstrap Gate Driving (BOOT)

An internal regulator provides the bias voltage for gate driver using a 0.1μF ceramic capacitor. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor must have a 10V or higher voltage rating. When the voltage across the BOOT capacitor falls below the BOOT-SW UVLO (3.2V TYP), the high-side switch is turned off, and the low-side switch is turned on to recharge the BOOT capacitor.

DETAILED DESCRIPTION (continued)

SS Pin and Soft-Start Adjustment

The SGM61231 has an external soft-start (SS) pin for adjustable startup time. It is recommended to add a soft-start capacitor (C_{SS}) between SS pin and GND to set the soft-start time. The lower of the SS pin voltage V_{SS} and V_{REF} is applied to the error amplifier to regulate the output. The internal I_{SS} = 2.1μA (TYP) current charges C_{SS} and provides a linear voltage ramp on the SS pin. Use Equation 4 to calculate the soft-start time.

$$t_{SS}\ (ms) = \frac{C_{SS}\ (nF) \times V_{REF}\ (V)}{I_{SS}\ (\mu A)} \quad (4)$$

Error Amplifier (EA)

This device uses a transconductance amplifier as an error amplifier (EA) to compare the sensed output voltage (V_{FB}) with the internal reference. The gain of EA amplifier in normal operation is 155μA/V (TYP). The output current is injected into the frequency compensation network (between COMP and GND pins) to produce the control signal (V_C) for the PWM comparator.

Slope Compensation

Without implementing some slope compensation, the PWM pulse widths will be unstable and oscillatory at duty cycles above 50%. To avoid sub-harmonic oscillations in this device, an internal compensation ramp is added to the measured switch current before comparing it with the control signal by the PWM comparator.

Power-Save Mode

To increase light load efficiency, power-save mode (PSM) feature is included in the SGM61231. When the COMP pin voltage (V_C) is lower than 0.545V (TYP), the device will enter power-save mode. In this mode, the MOSFET switching is inhibited when V_C falls below 0.545V. The device will exit PSM if V_C rises above 0.545V.

Low Dropout

As input voltage drops, the difference between input voltage and output voltage decreases, causing off-time of the high-side MOSFET to approach its minimum possible value. Dropout occurs when input voltage falls below the required minimum for the regulator to maintain output voltage. To maintain output voltage at nominal value, SGM61231 will decrease its switching frequency and increase duty cycle.

Over-Current Protection

Over-current protection (OCP) is naturally provided by current mode control. In each cycle, the high-side (HS) current sensing starts a short time (blanking time) after the HS switch is turned on. The sensed HS switch current is continuously compared with the HS current limit threshold and when the HS current reaches to that threshold, the HS switch is turned off.

While the low-side (LS) switch is turned on, the conduction current is monitored by the internal circuitry. In each cycle, the sensed LS switch current is compared to the internally LS current limit threshold only when the HS current limit threshold is triggered. If the sensed LS switch current is higher than the LS current limit threshold during LS conduction, the HS does not turn on and the LS stays on when the clock signal comes. When the sensed LS switch current is below the LS current limit threshold, the HS switch turns on again at the next clock.

In addition, if an output overload condition occurs for more than 512 switching cycles, then the device shuts down and restarts after 16384 cycles.

Over-Voltage Protection

When an overload or an output fault condition is removed, large overshoot may occur on the output. The SGM61231 includes a protection circuit to reduce such over-voltage transients. If the voltage at the FB pin exceeds 115% of the V_{REF} threshold, the high-side switch is turned off. When it returns below 105% of the V_{REF}, the high-side switch is allowed to turn on again.

Thermal Shutdown (TSD)

If the junction temperature (T_J) exceeds +165℃, the TSD protection circuit will stop switching to protect the device from overheating. The device will automatically restart with a power up sequence when the die temperature drops below +145℃ (TYP).

APPLICATION INFORMATION

The design method and component selection for the SGM61231 Buck converter are explained in this section. A typical application circuit for the SGM61231 is shown in Figure 4. It is used for converting a 7V to 28V supply voltage to a lower 5V output voltage with a maximum output current of 3A.

The external components are designed based on the application requirements and device stability. Some suitable parameters for different output voltages are provided in Table 1 to simplify the selection of components. The C_{OUT} values in Table 1 are actual derating values. Higher nominal values are used for ceramic capacitors.

Typical Application

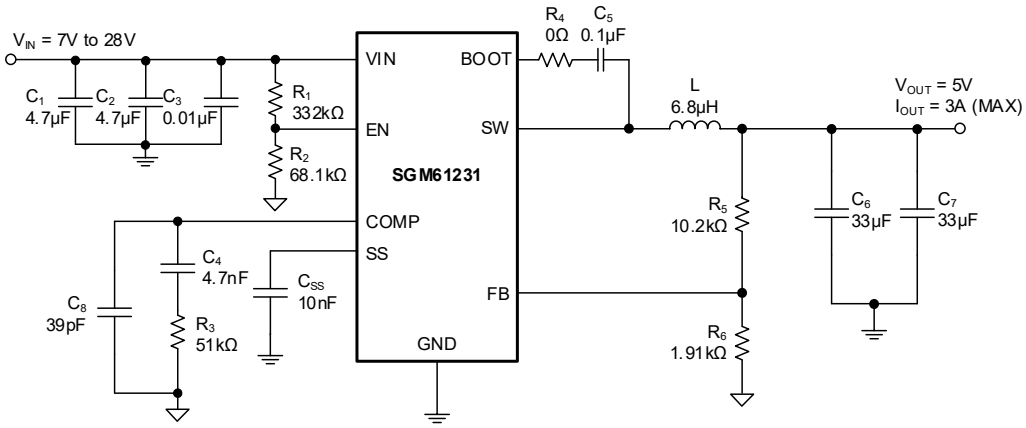


Figure 4. SGM61231 Typical Application Circuit

Table 1. Some Typical Parameters for Stable Operation

f_{SW} (kHz)	V_{OUT} (V)	L (μH)	C_{OUT} (μF)	R_5 (kΩ)	R_6 (kΩ)	R_3 (kΩ)	C_4 (nF)	C_8 (pF)
770	3.3	4.7	94	10.2	3.24	68	1	6.8
770	5	6.8	66	10.2	1.91	51	4.7	39
770	24	15	18.8	332	11.3	100	2.2	4.7

Requirements

The design parameters required for the design example are given in Table 2.

Table 2. Design Parameters

Design Parameter	Example Value
Input Voltage	12V nominal
Start Input Voltage (Rising V_{IN})	7V
Stop Input Voltage (Falling V_{IN})	6V
Input Ripple Voltage	360mV, 3% of V_{IN_NOM}
Output Voltage	5V
Output Ripple Voltage	50mV, 1% of V_{OUT}
Output Current Rating	3A
Transient Response 1.5A to 3A Load Step	250mV, 5% of V_{OUT}
Operating Frequency	770kHz

Input Capacitors Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61231. At least 3μF of effective capacitance (after derating) is needed at the input. In some applications, additional bulk capacitance may also be required for the input, for example, when the SGM61231 is more than 5cm away from the input source. The input capacitor ripple current rating must also be greater than the maximum input current ripple. The input current ripple can be calculated using Equation 5 and the maximum value occurs at 50% duty cycle. Using the design example values, I_{OUT} = 3A, yields an RMS input ripple current of 1.5A.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (5)$$

For this design, a ceramic capacitor with at least 50V voltage rating is required to support the maximum input voltage. Therefore, a 10μF/50V capacitor is selected for VIN to cover all DC bias, thermal and aging derating. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 6.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (6)$$

It is recommended to place an additional small size 0.1μF ceramic capacitor right beside VIN and PGND pins for high frequency filtering.

APPLICATION INFORMATION (continued)

Inductor Design

Equation 7 is conventionally used to calculate the output inductance of a Buck converter. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor (K_{IND} = $\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions. For peak current mode converter, selecting an inductor with saturation current must be above the switch current limit. Typically, a 20% to 40% current ripple is selected (K_{IND} = 0.2 ~ 0.4).

$$L = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (7)$$

In this example, the calculated inductance will be 5.7μH with K_{IND} = 0.3, so the nearest larger inductance of 6.8μH is selected. The ripple, RMS and peak inductors current calculations are summarized in Equations 8, 9 and 10 respectively.

$$\Delta I_L = \frac{V_{IN\_MAX} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (8)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (9)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (10)$$

Output Capacitor Design

There are three main criteria that must be considered when designing the output capacitor (C_{OUT}): (1) the converter pole location, (2) the output voltage ripple, (3) the transient response to a large change in load current. The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of V_{OUT} in response to a large load step. Transient response is usually the more stringent criteria in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect and respond to the output change.

Another requirement may also be expressed as desired hold-up time in which the output capacitor must hold the output voltage above a certain level for a specified period if the input power is removed. It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step). Equation 11 can be used to calculate the minimum output capacitance that is needed to supply a current step (ΔI_{OUT}) for at least 2 cycles until the control loop responds to the load change with a maximum allowed output transient of ΔV_{OUT} (overshoot or undershoot).

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (11)$$

where:

- ΔI_{OUT} is the change in output current.
- ΔV_{OUT} is the allowable change in the output voltage.

For example, if the acceptable transient from 1.5A to 3A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V and ΔI_{OUT} = 1.5A, the minimum required capacitance will be 15μF. Note that the impact of output capacitor ESR on the transient is not considered in Equation 11. For ceramic capacitors, the ESR is generally small enough to ignore its impact on the calculation of ΔV_{OUT} transient.

The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high to low load current. The energy stored in the inductor can produce an output voltage overshoot when the load current rapidly decreases. The excess energy absorbed in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 12 calculates the minimum capacitance required to keep the output-voltage overshoot to a desired value.

$$C_{OUT} > L \times \frac{I_{OUT\_H}^2 - I_{OUT\_L}^2}{\left(V_{OUT} + \Delta V_{OUT}\right)^2 - V_{OUT}^2} \quad (12)$$

where:

- I_{OUT_H} is the output current under heavy loads.
- I_{OUT_L} is the output current under light loads.

APPLICATION INFORMATION (continued)

For example, if the acceptable transient from 3A to 1.5A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V, the minimum required capacitance will be 17.9μF.

Equation 13 can be used for the output ripple criteria and finding the minimum output capacitance needed. V_{OUT_RIPPLE} is the maximum acceptable ripple. In this example, the allowed ripple is 50mV that results in minimum capacitance of 1.67μF.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \quad (13)$$

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 13. For a specific output capacitance value, use Equation 14 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement.

$$ESR_{COUT} < \frac{V_{OUT\_RIPPLE}}{\Delta I_L} - \frac{1}{8 \times f_{SW} \times C_{OUT}} \quad (14)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, a 2 × 33μF/16V X5R ceramic capacitor with 3mΩ of ESR is used. The amount of ripple current that a capacitor can handle without damage or overheating is limited. The inductor ripple is bypassed through the output capacitor. Equation 15 calculates the RMS current that the output capacitor must support.

$$I_{COUT\_RMS} = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{\sqrt{12} \times V_{IN\_MAX} \times L \times f_{SW}} \quad (15)$$

Bootstrap Capacitor Selection

Use a 0.1μF high-quality ceramic capacitor (X7R or X5R) with 10V or higher voltage rating for the bootstrap capacitor (C_4). It is recommended to add a resistor R_4 in series with C_4 to slow down switch-on speed of the HS switch and improve radiated EMI problems. For most applications, R_4 is less than 10Ω. Too high values for R_4 may cause insufficient C_4 charging in high duty-cycle applications. Slower switch switch-on speed will also increase switch losses and reduce efficiency.

UVLO Setting

The input UVLO can be programmed using an external voltage divider on the EN pin of the SGM61231. In this design, R_1 is connected between VIN and the EN pins and R_2 is connected between EN and AGND pins (see Figure 4). The UVLO has two thresholds (hysteresis), one for power-up (turn-on) when the input voltage is rising and one for power-down or brownout (turn-off) when the voltage is falling. In this design, the turn-on (enable to start switching) occurs when V_{IN} rises above 7V (UVLO rising threshold). When the regulator is working, it will not stop switching until the input falls below 6V (UVLO falling threshold). Equations 1 and 2 are provided to calculate the resistors. For this example, the nearest standard resistor values are R_1 = 332kΩ and R_2 = 68.1kΩ.

Feedback Resistors Setting

Use resistor dividers (R_5 and R_6) to set the output voltage through Equation 16 and 17.

$$R_6 = \frac{R_5 \times V_{REF}}{V_{OUT} - V_{REF}} \quad (16)$$

$$V_{OUT} = V_{REF} \times \left(\frac{R_5}{R_6} + 1\right) \quad (17)$$

It is recommended to choose R_5 around 10.2kΩ and calculate R_6 from Equation 16. Use accurate and stable resistors (1% or better) to enhance output accuracy. For this example, the selected values are R_5 = 10.2kΩ and R_6 = 1.91kΩ, resulting in a 5.072V output voltage.

Compensation Network Setting

Several techniques are used by engineers to compensate a DC/DC regulator. The method presented here uses simple calculations and generally results in high phase margins.

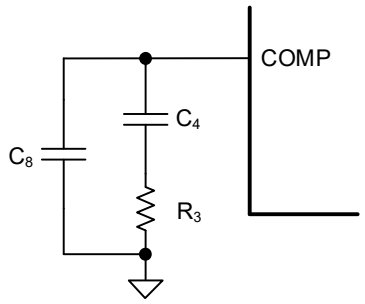


Figure 5. SGM61231 Typical Application Circuit

APPLICATION INFORMATION (continued)

One pole of the system is determined by the converter (C_{OUT} and R_{LOAD}), as given in Equation 18:

$$f_{P1} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}} \quad (18)$$

where R_{LOAD} is the load resistor and C_{OUT} is the output capacitor.

The system has two zeros. One is generated by the large ESR of C_{OUT} (ESR_{COUT}) and the other by the compensator (C_3 and R_3), as given in Equation 19 and Equation 20:

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR_{COUT}} \quad (19)$$

$$f_{Z1} = \frac{1}{2\pi \times C_3 \times R_3} \quad (20)$$

If the ESR of the output capacitor is large, the effect of this zero can be compensated by adding C_7 to the compensation network that places a third pole at:

$$f_{P3} = \frac{1}{2\pi \times C_7 \times R_3} \quad (21)$$

The main goal of the compensation network is to adjust the shape of the converter transfer function to get a desired loop gain. The crossover frequency at which the loop gain is 1 (0dB) is an important factor that determines the bandwidth. Setting the crossover at a frequency that too high will lead to system instability.

At the beginning of the design, the crossover frequency is initially set to approximately 10% of the switching frequency (0.1 × f_{SW}), and then the following steps are taken to design the compensation network with sufficient phase margin.

1. Select R_3 based on the desired crossover frequency (f_C):

$$R_3 = \frac{2\pi \times C_{OUT} \times f_C}{gmEA \times gmps} \times \frac{V_{OUT}}{V_{REF}} \quad (22)$$

where gmEA is the error-amplifier transconductance (gmEA = 155μA/V) and gmps is the current-sense transconductance (gmps = 9A/V).

2. Select C_4 to get sufficient phase margin. In the applications using typical inductor values, placing the compensation zero (f_{Z1}) at f_{Z1} < 0.25 × f_C would be sufficient and C_3 can be calculated as:

$$C_4 > \frac{4}{2\pi \times R_3 \times f_C} \quad (23)$$

3. Use C_8 if the ESR zero is located below $f_{SW}/2$. This condition is valid if Equation 24 is true:

$$\frac{1}{2\pi \times C_{OUT} \times ESR_{COUT}} < \frac{f_{SW}}{2} \quad (24)$$

In this case, choose C_8 from Equation 25 to set a pole (f_{P3}) over the ESR zero:

$$C_8 = \frac{C_{OUT} \times ESR_{COUT}}{R_3} \quad (25)$$

LAYOUT INFORMATION

Layout Considerations

The layout has been shown to bring good results, although other layout designs may also obtain good performance.

- Bypass the VIN pin to PGND pin with low-ESR ceramic capacitors and place them as close as possible to the device.
- Share the same PGND connection point with the input and output capacitors.
- Connect the device PGND to the PCB ground plane right at the PGND pin.
- Minimize the length and the area of the connection route from SW pin to the inductor to reduce the noise coupling from this area.
- Consider sufficient ground plane area on the top side for proper heat dissipation. Connect the large internal or back-side ground planes to the top-side ground near the device with thermal vias for better heat dissipation.

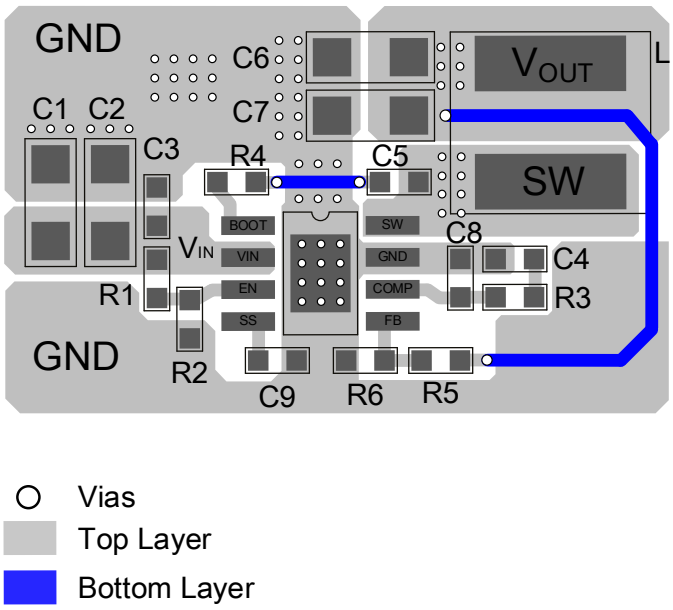


Figure 6. Layout Example

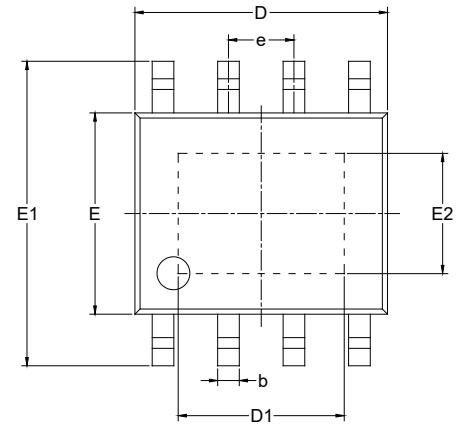
REVISION HISTORY

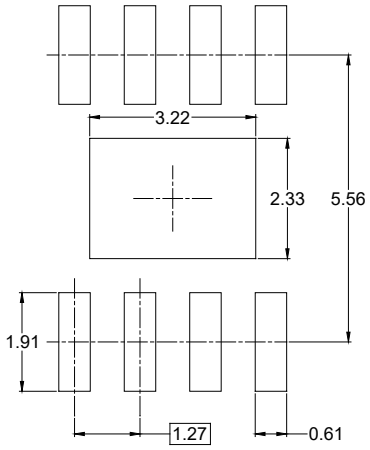
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (OCTOBER 2025)	Page
Changed from product preview to production data	All

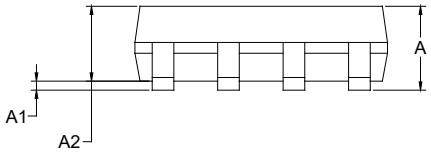
PACKAGE OUTLINE DIMENSIONS

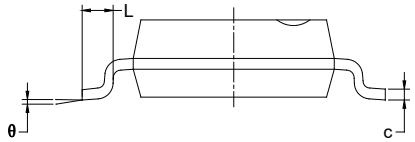
SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)





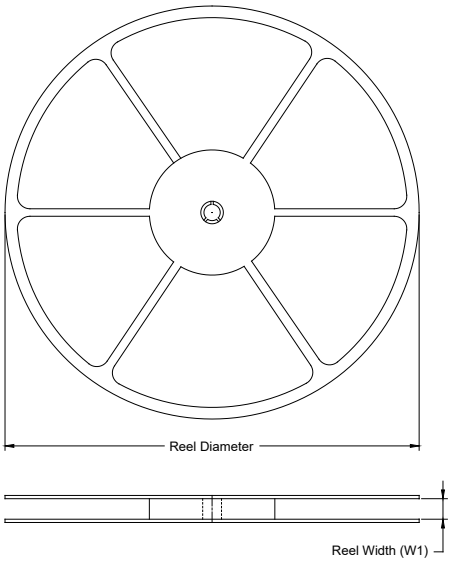
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°

NOTES:

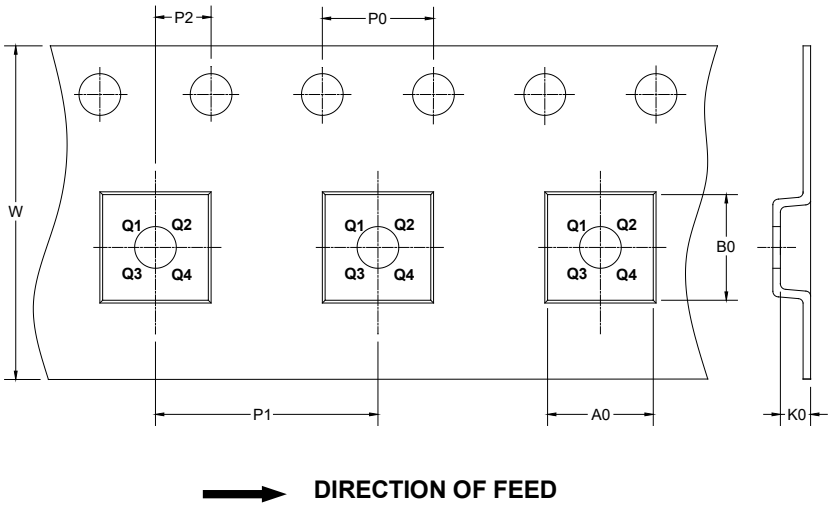
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



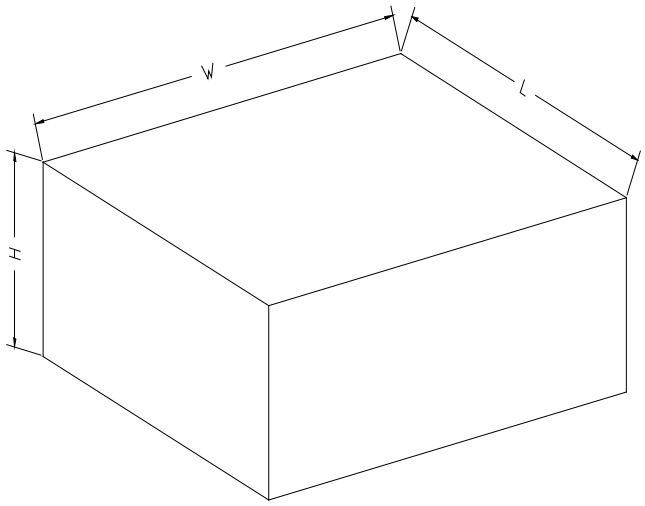
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002