SGM41295
DC Bias Controller for EML

GENERAL DESCRIPTION

The SGM41295 provides DC bias for the laser diode, EA bias, and MPD bias monitor circuits, and it also provides an unregulated negative output generated by an inverting charge pump which is equal to negative input voltage.

The SGM41295 is available in a Green TQFN-3×3-16L package. It operates over an ambient temperature range of -40℃ to +105℃.

APPLICATIONS

EML Fiber Modules
AOC and Transponders for Telecom and Data Center Interconnection

FEATURES

- **Negative Charge Pump Output (-1×) with 150mA Maximum Loading Current**
- **Digitally Programmable EAM Bias and LD Driving Current Source**
- **Voltage Sources for EAM Bias (-0.2V to -3.2V, 12.5mV/Step) with 100mA Maximum Loading Current**
- **Current Sources for LD (0mA to 239.5mA, 0.5mA/Step or 0mA to 119.75mA, 0.25mA/Step)**
- **Backside MPD Current Monitoring (0mA to 3mA)**
- **Support I^2C Interface and up to 1MHz I^2C Clock Frequency**
- **No Inrush Current during Startup**
- **Charge Pump Output Short Protection**
- **LD Short/Open and EAM Short Monitoring**
- **+135℃ Over-Temperature Alert Bit**
- **+155℃ Over-Temperature Shutdown**
- **Available in a Green TQFN-3×3-16L Package**

TYPICAL APPLICATION

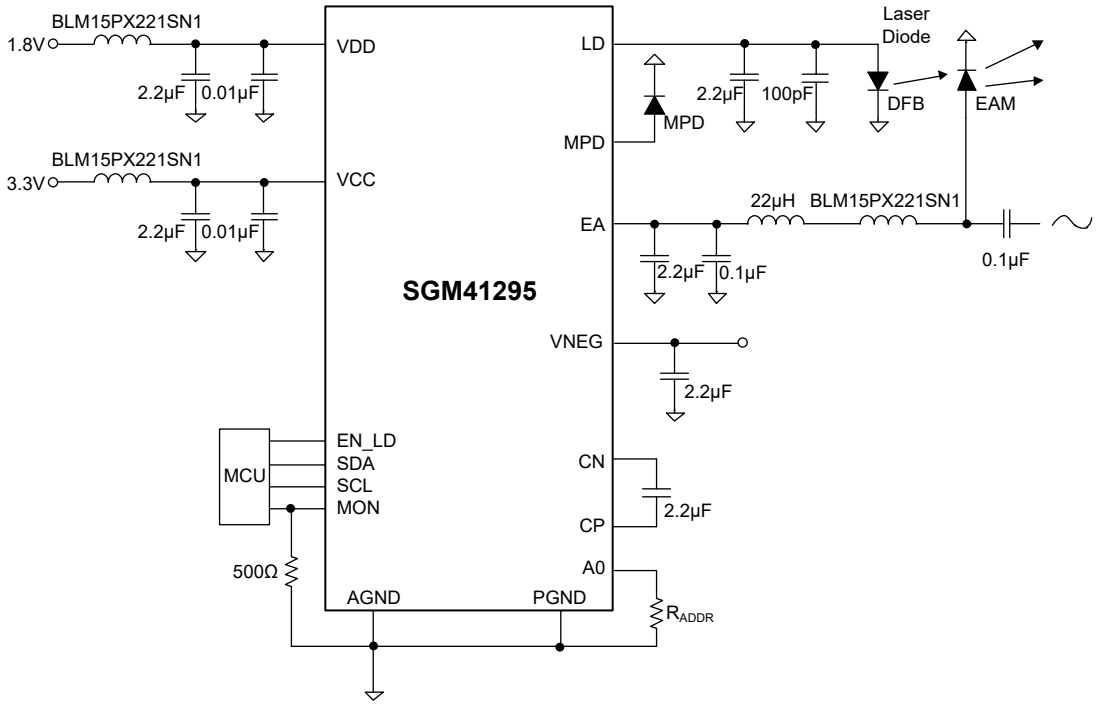


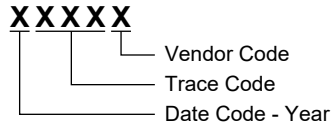
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41295	TQFN-3×3-16L	-40℃ to +105℃	SGM41295GTQ16G/TR	CB2TQ XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{DD}, SDA, SCL ..... -0.3V to 6V
V_{NEG} ..... -6V to 0.3V
MON, V_{CP}, EN_LD, A0 ..... -0.3V to V_{CC} + 0.3V
MPD, V_{EA}, V_{CN} ..... V_{NEG} - 0.3V to 0.3V
LD ..... -0.3V to V_{DD} + 0.3V
Package Thermal Resistance
TQFN-3×3-16L, θ_{JA} ..... 40℃/W
TQFN-3×3-16L, θ_{JB} ..... 13.9℃/W
TQFN-3×3-16L, $\theta_{JC\ (TOP)}$ ..... 42.7℃/W
TQFN-3×3-16L, $\theta_{JC\ (BOT)}$ ..... 3.2℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

V_{CC} ..... 2.85V to 5.5V
V_{DD} ..... 1.5V to 5.5V
MON Current Output Range ..... 0mA to 3mA
MON Voltage Output Range ..... 0V to 3.3V
SCL, SDA Pull-Up Voltage ..... 2.5V (MIN)
Operating Junction Temperature Range ..... -40℃ to +125℃
Operating Ambient Temperature Range ..... -40℃ to +105℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

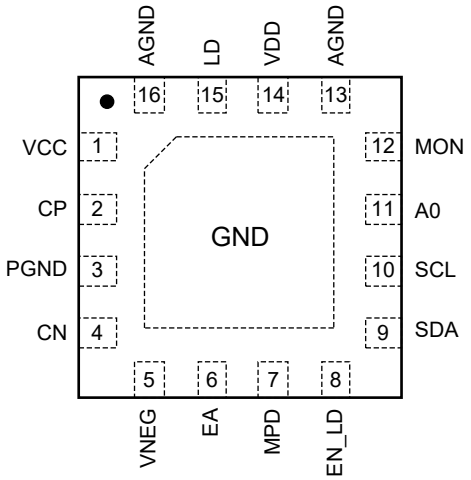
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×3-16L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	VCC	P	Power Supply for the Chip.
2	CP	I/O	Fly Capacitor Positive Connection.
3	PGND	G	Power Ground.
4	CN	I/O	Fly Capacitor Negative Connection.
5	VNEG	O	Charge Pump Output.
6	EA	O	EAM Biasing Output. The output voltage of EA is programmable via the I^2C interface.
7	MPD	I	MPD Current Monitor Input. Cathode of MPD is connected to ground and anode of MPD is connected to this pin.
8	EN_LD	I	Laser Bias Enable. Logic low disables the laser bias only (not EAM bias). Logic high enables the laser bias. Don't leave it floating.
9	SDA	IO	Data for the I^2C Compatible Interface.
10	SCL	IO	Clock for the I^2C Compatible Interface.
11	A0	O	Slave Address Programming. To program the address, a resistor is connected between this pin and ground.
12	MON	O	Multiplexed Monitor Output. There are three monitor signals selected via I^2C interface.
13, 16	AGND	G	Analog Ground.
14	VDD	P	Power Supply for Laser Diode Current Source.
15	LD	O	Laser Biasing Output. The current of LD is programmable via the I^2C interface.
–	Exposed Pad	G	Exposed Pad. Used for circuit ground connection.

NOTE: I: input, O: output, I/O: input or output, G: ground, P: power for the circuit.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V, V_{DD} = 1.8V, Full = -40℃ to +105℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETERS	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Power Supply							
Supply Voltage Range	V_{CC}		Full	2.85		5.5	V
V_{CC} Under-Voltage Lockout Threshold	V_{UVLO_R}	V_{CC} rising	+25℃	2.55	2.67	2.80	V
	V_{UVLO_F}	V_{CC} falling	+25℃		2.5		
Power-Up Blanking Time	t_{BLANK}		+25℃		10		ms
Operating Quiescent Current	I_Q	I_{LD} and EA disabled, no switching (test mode)	+25℃		100	150	μA
LD Current Source							
Maximum Output Current	I_{LD_MAX}	V_{LD} = 1.5V	+25℃		239.5		mA
Current Programming Resolution	I_{RES_MAX}	V_{LD} = 1.5V, LD current gain = 1, 8-bit DAC programming	+25℃	0.1	0.5	0.9	mA
		V_{LD} = 1.5V, LD current gain = 1/2, 8-bit DAC programming	+25℃	0.05	0.25	0.45	
LD Current Source Accuracy		V_{LD} = 1.5V, I_{LD} = 100mA	+25℃	-3		3	%
LD Current Source Noise	I_{NOISE}	V_{LD} = 1.5V, I_{LD} = 100mA, 10Hz to 10kHz	+25℃		2.6		$μA_{RMS}$
LD Current Source Output DC Impedance		V_{LD} = 1.2V to 1.5V, I_{LD} = 100mA	+25℃		10		kΩ
LD Current Source Full Temperature Drift		I_{LD} = 100mA	Full		12		μA/℃
LD Current Source Headroom Voltage	V_{LD_ROOM}	V_{DD} = 1.8V, I_{LD} = 239.5mA	+25℃		0.13	0.2	V
LD Current Source Soft-Start Time	t_{SS_LD}		+25℃		280	500	μs
LD Current Source Open Detection Threshold	V_{LD_OPEN}	V_{DD} - V_{LD} falling	+25℃		50		mV
LD Current Source Short Detection Threshold	V_{SHORT_LD}	V_{LD} falling	+25℃	0.55	0.6	0.65	V
EAM Negative Voltage Bias							
EA Output Voltage Range	V_{EA}	8-bit DAC programming	Full	V_{NEG} + 0.25		-0.2	V
EA Output Voltage DAC Accuracy		V_{EA} = -2V	+25℃	-1		1	%
Voltage Difference between EA and VNEG			Full	0.25		4	V
EA Output Voltage DAC Resolution			+25℃	0	12.5	25	mV
EA Output Voltage Full Temperature Drift		V_{EA} = -2V	Full		53		μV/℃
EA Maximum Output Current	I_{EA_MAX}		+25℃	100			mA
EA Noise	V_{NOISE}	V_{EA} = -2V, I_{EA} = 50mA, 10Hz to 10kHz	+25℃		65		$μV_{RMS}$
EA Short Detection Threshold	V_{SHORT_EAM}	V_{EA} rising	+25℃		-100		mV
EA DC Impedance		V_{EA} = -2V, I_{EA} = 0mA to 100mA	+25℃		0.05		Ω
EA Voltage Change Slew Rate			+25℃		3.3		mV/μs
Negative Charge Pump							
Switching Frequency	f_S	I_{OUT} = 100mA	+25℃		1.75		MHz
Maximum Load Current	I_{NEG_MAX}		+25℃	150			mA
Output Impedance		I_{OUT} = 100mA	+25℃		1.6		Ω
MPD Pin							
Current Range			+25℃	0		3	mA
Voltage Range			+25℃	V_{NEG} + 1		0	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.3V, V_{DD} = 1.8V, Full = -40℃ to +105℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETERS	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Multiplexed Monitor Output (EA current sampling ratio 40:1 or 20:1. LD voltage sampling ratio 2:1. TX MPD current sampling ratio 1:1.)							
MON Pin Current Accuracy		I_{EA} = 60mA, sampling ratio = 40:1	+25℃	-5		5	%
		I_{EA} = 60mA, sampling ratio = 20:1	+25℃	-5		5	
		I_{MPD} = 3mA	+25℃	-5		5	
		I_{MPD} = 250μA (1:8)	+25℃	-5		5	
MON Pin Current Full Temperature Drift		I_{EA} = 60mA, sampling ratio = 40:1	Full	-1		1	%
		I_{EA} = 60mA, sampling ratio = 20:1	Full	-1		1	
		I_{MPD} = 3mA	Full	-0.5		0.5	
		I_{MPD} = 250μA (1:8)	Full	-0.5		0.5	
MON Pin Current Noise		I_{EA} = 60mA, sampling ratio = 40:1	+25℃		0.015		μA_{RMS}
		I_{EA} = 60mA, sampling ratio = 20:1	+25℃		0.025		
		I_{MPD} = 3mA	+25℃		0.02		
MON Pin Leakage Current	I_{MON_LEAK}	Monitor function disabled, forcing 1V on MON pin	+25℃		0.01	0.2	μA
Logic EN_LD, SDA, SCL							
Input High Threshold	V_{IH}		Full	2.2			V
Input Low Threshold	V_{IL}		Full			0.8	V
Output Low Voltage	V_{OL}	I_{SINK} = 200μA	Full			0.4	V
Thermal Detection							
Thermal Alert Threshold					135		℃
Thermal Shutdown Threshold					155		℃
Thermal Shutdown Hysteresis					20		℃

I²C INTERFACE TIMING CHARACTERISTICS (1)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard mode	+25℃			100	kHz
		Fast mode	+25℃			400	kHz
		Fast mode plus	+25℃			1	MHz
LOW Period of the SCL Clock	t_{LOW}	Standard mode	+25℃	4.7			μs
		Fast mode	+25℃	1.3			μs
		Fast mode plus	+25℃	0.5			μs
HIGH Period of the SCL Clock	t_{HIGH}	Standard mode	+25℃	4.0			μs
		Fast mode	+25℃	600			ns
		Fast mode plus	+25℃	260			ns
Bus Free Time between a STOP and a START Conditions	t_{BUF}	Standard mode	+25℃	4.7			μs
		Fast mode	+25℃	1.3			μs
		Fast mode plus	+25℃	0.5			μs
Hold Time for a Repeated START Condition	$t_{hd;STA}$	Standard mode	+25℃	4.0			μs
		Fast mode	+25℃	600			ns
		Fast mode plus	+25℃	260			ns
Setup Time for a Repeated START Condition	$t_{su;STA}$	Standard mode	+25℃	4.7			μs
		Fast mode	+25℃	600			ns
		Fast mode plus	+25℃	260			ns
Data Setup Time	$t_{su;DAT}$	Standard mode	+25℃	250			ns
		Fast mode	+25℃	100			ns
		Fast mode plus	+25℃	50			ns
Data Hold Time	$t_{hd;DAT}$	Standard mode	+25℃	0.05		3.45	μs
		Fast mode	+25℃	0.05		0.9	μs
		Fast mode plus	+25℃	0			μs
Rise Time of SCL Signal after a Repeated START Condition and after an Acknowledge Bit	t_{RCL1}	Standard mode	+25℃	$20 + 0.1C_B$		1000	ns
		Fast mode	+25℃	$20 + 0.1C_B$		1000	ns
		Fast mode plus	+25℃			120	ns
Rise Time of SCL Signal	t_{RCL}	Standard mode	+25℃	$20 + 0.1C_B$		1000	ns
		Fast mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode plus	+25℃			120	ns
Fall Time of SCL Signal	t_{FCL}	Standard mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode plus	+25℃			120	ns
Rise Time of SDA Signal	t_{RDA}	Standard mode	+25℃	$20 + 0.1C_B$		1000	ns
		Fast mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode plus	+25℃			120	ns
Fall Time of SDA Signal	t_{FDA}	Standard mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode plus	+25℃			120	ns

I²C INTERFACE TIMING CHARACTERISTICS (1) (continued)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Setup Time for STOP Condition	$t_{su;STO}$	Standard mode	+25℃	4.0			μs
		Fast mode	+25℃	600			ns
		Fast mode plus	+25℃	260			ns
Capacitive Load for SDA and SCL	C_B		+25℃			0.4	nF

NOTE:
1. Industry standard I²C timing characteristics according to I²C-Bus Specification. Not tested in production.

I²C INTERFACE TIMING DIAGRAM

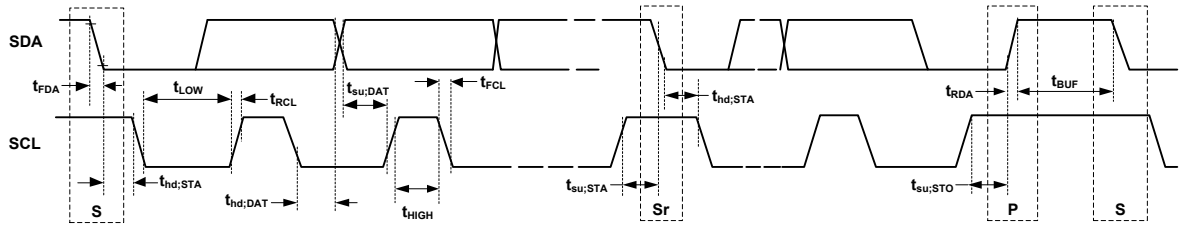
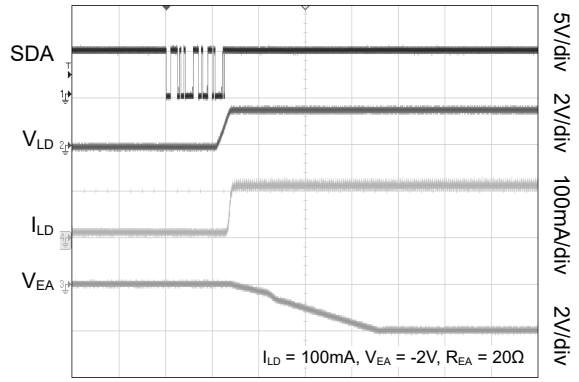


Figure 2. Serial Interface Timing for F/S-Mode

TYPICAL PERFORMANCE CHARACTERISTICS

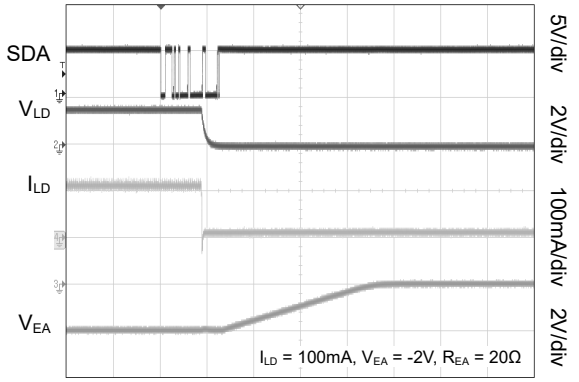
T_J = +25℃, V_{CC} = 3.3V, V_{DD} = 1.8V, unless otherwise noted.

I_{LD} and V_{EA} Startup



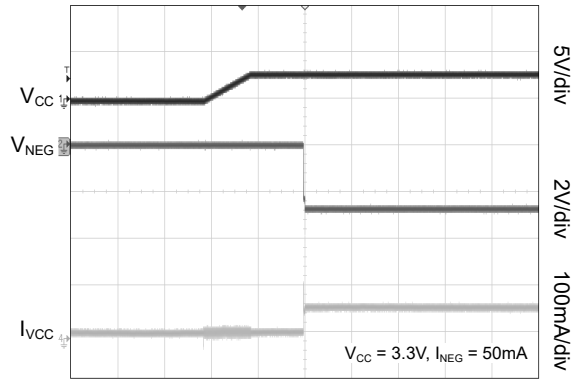
Time (200μs/div)

I_{LD} and V_{EA} Shutdown



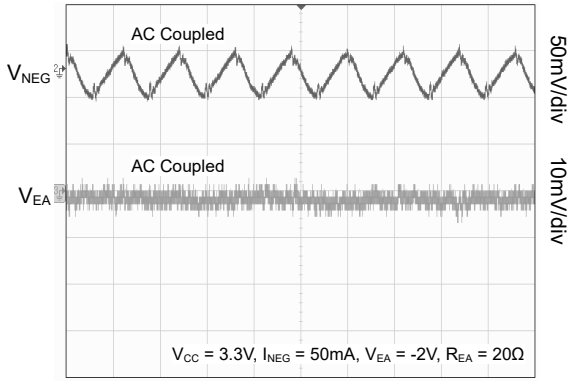
Time (200μs/div)

Charge Pump Power Up



Time (10ms/div)

Charge Pump and V_{EA} Ripple

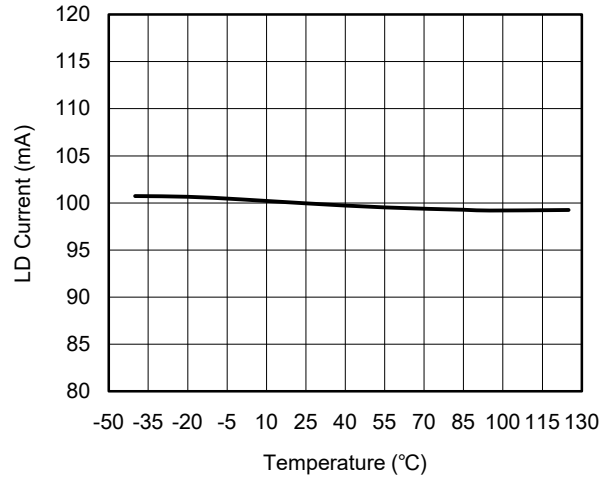


Time (500ns/div)

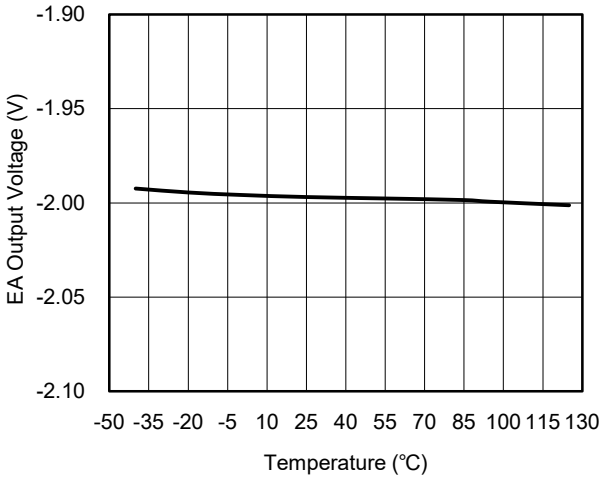
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{CC} = 3.3V, V_{DD} = 1.8V, unless otherwise noted.

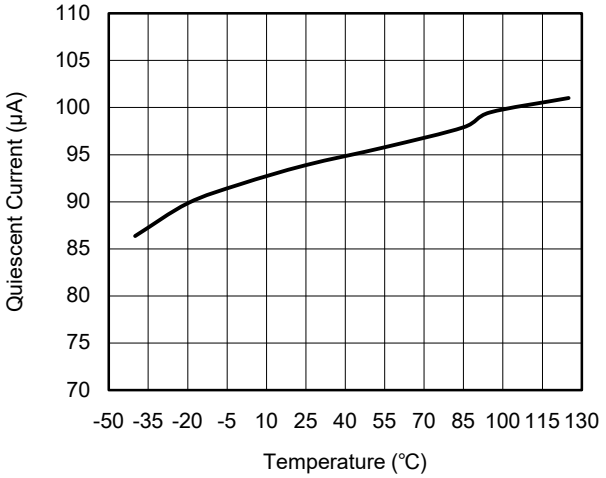
I_{LD} vs. Temperature



V_{EA} vs. Temperature



I_{Q_VCC} vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

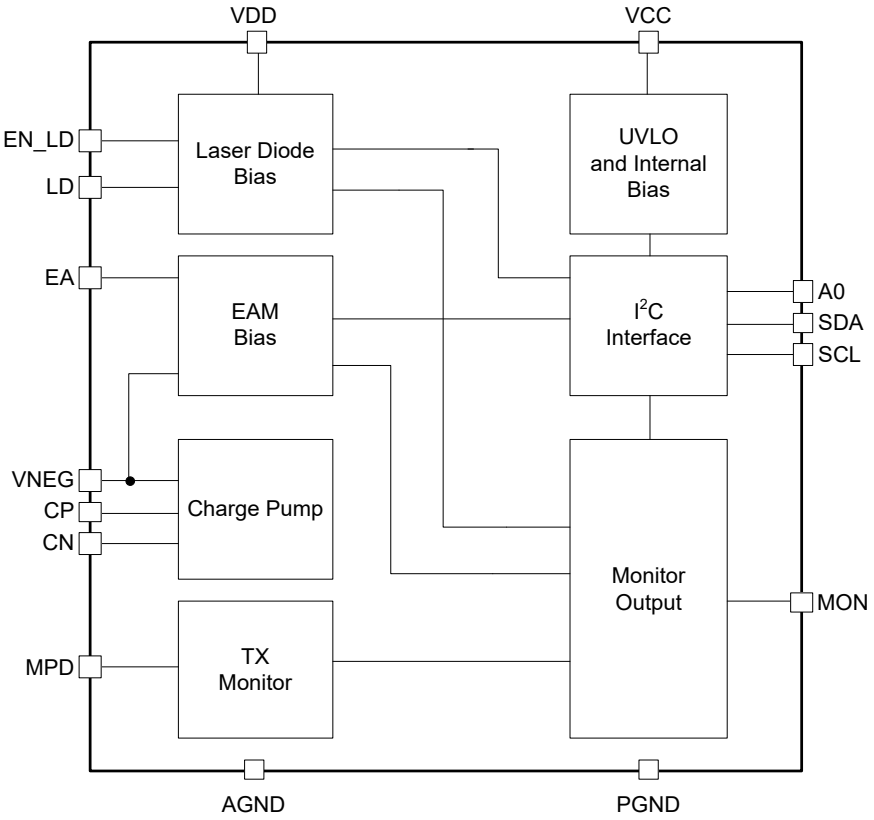


Figure 3. Block Diagram

DETAILED DESCRIPTION

The SGM41295 provides DC bias for the laser diode, EA bias, and MPD bias monitor circuits, and it also provides an unregulated negative output generated by an inverting charge pump which is equal to negative input voltage. This chip supports I^2C interface and other features such as Laser Diode (LD) open/short monitor, EAM short monitor, over-temperature alert, over-temperature protection and so on.

Negative Charge Pump

The SGM41295 uses a switched capacitor charge pump to get an unregulated negative voltage with an absolute value of V_{CC}. The switching signal, which drives the charge pump, is created by an integrated oscillator within the control circuit block. The charge pump switching frequency is from 50kHz to 1.75MHz. The SGM41295 will automatically adjust the frequency according to V_{CC} and V_{NEG} voltage gap. The oscillator frequency increases with load increase. The higher frequency will compensate the output ripple at heavy load condition. When the absolute value of V_{NEG} is smaller than 0.7 × V_{CC}, the charge pump will treat it as over current condition. SGM41295 will limit the input current. The equivalent output resistance of the charge pump is about 1.6Ω.

Enable and Disable

In order to enable the LD current source, 3 conditions have to be met:

1. VCC voltage is higher than UVLO threshold for longer than 10ms.
2. Logic high on EN_LD pin.
3. Setting LD_EN = '1', by enabling the corresponding bit of the register 0x03h Bit[0].

Pulling EN_LD pin low, setting LD_EN = '0', or setting VCC voltage lower than UVLO threshold can disable the LD current source.

It is recommended that the VCC is powered on after the VDD.

In order to enable the EA, 2 conditions have to be met:

1. VCC voltage is higher than UVLO threshold for longer than 10ms.
2. Setting EA_EN = '1', by enabling the corresponding bit of the register 0x03h Bit[1].

Either setting EA_EN = '0' or VCC voltage lower than UVLO threshold can disable the EA.

Programming LD Current Source

The LD current source is programmed with 8-bit DAC. The added offset current is 112mA, 96mA, 80mA, 64mA, 48mA, 32mA, 16mA or 0mA respectively, which is set by Bit[2:0] in register 0x05h. The LD current is calculated with the following equation:

$$I_{LD} = k \times (I_{OFFSET} + 128 \times (Code/256)) \quad (1)$$

where k is the LD current gain (1 or 1/2), the I_{OFFSET} is the added offset current, and Code is from 0 to 255.

For example, setting Bit[7:0] = 00000010 in register 0x05h and Bit[7:0] =10001000 in register 0x20h can set I_{LD} = 100mA. When V_{CC} is lower than 3V, the recommended maximum set current of LD current source is 200mA.

Programming EA Voltage

The EA voltage is programmed with 8-bit linear coded DAC and is calculated with the following equation:

$$V_{EA} = -3.2 \times (Code/256) \quad (2)$$

where Code is from 0 to 255.

For example, setting Bit[7:0] = 10100000 in register 0x21h (Code = A0) can set V_{EA0} = -2V.

MPD Pin Application

EML backside MPD current is monitored by sinking current to VNEG through MPD pin. Please refer to Figure 4 for more detail.

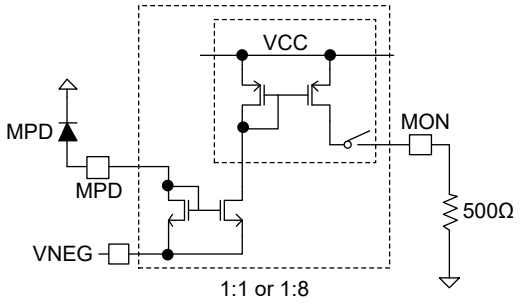


Figure 4. MPD Pin Application

DETAILED DESCRIPTION (continued)

Multiplexed Monitor Output

There are three monitor signals multiplexed for output, and they are selected via the I²C interface. One of those analog values monitored is selected by setting the register 0x06h, and the selected one is transferred to the MON pin.

EAM Current Sampling

EAM current is sampled and converted into current source in 40:1 or 20:1 ratio. Connecting a resistor between MON pin and GND to convert the sampled current into voltage for ADC conversion. The transfer function is shown below:

$$I_{MONx} = \frac{I_{EA}}{S} \quad (3)$$

where, I_{MONx} is the MON pin output current. S is the sampling ratio which can be set by I²C interface. Figure 5 shows the typical application circuit of EAM bias.

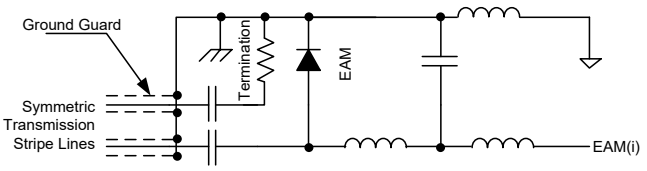


Figure 5. Typical Application Circuit of EAM Bias

FAULT Flag and OT Status Read

LD open status can be read through Bit[4] in register 0x01h. LD current source short status can be read through Bit[5] in register 0x01h. EA pin short status can be read through Bit[3] in register 0x01h. OT_Alert status can be read through Bit[2] in register 0x01h.

When any abnormal event occurs, including LD open, LD current source short, EA pin short and over-temperature alert, the shared flag is set to high, which then can be read through the Fault bit (Bit[1] in register 0x01h).

Under-Voltage Lockout (UVLO)

The SGM41295 integrates an under-voltage lockout block. When VCC voltage is higher than UVLO threshold for longer than 10ms, the device is enabled. The device will be disabled as soon as the VCC voltage falls below the UVLO threshold, and then the device stops responding to any instruction sent to it.

I²C Reset

Setting Bit[2] in register 0x00h to high can reset all digital settings to defaults.

I²C Serial Interface Description

The SGM41295 communicates through an industry standard I²C compatible interface, to receive data in slave mode. I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification).

The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices are connected to the I²C bus through open-drain I/O pins, SDA and SCL pins. A master device, usually a microcontroller or a digital signal processor, controls the bus.

The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The SGM41295 works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification: standard mode (100kbps), fast mode (400kbps) and fast-mode plus (1000kbps). The data transfer protocols for standard mode, fast mode and fast-mode plus are exactly the same, therefore they are referred to as F/S-mode plus in this document. The SGM41295 supports 7-bit addressing, and the LSB enables the write or read function (see Table 1).

DETAILED DESCRIPTION (continued)

The device that initiates the communication is called a master, and the devices controlled by the master are slaves. The master generates the serial clock on SCL, controls the bus access, and generates START and STOP conditions (see Figure 6). A START initiates a new data transfer to a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. A STOP condition ends a data transfer to slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/$\overline{W}$ on the SDA line. During all transmissions, the master ensures that the data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 7). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an Acknowledgment, ACK, (see Figure 8) by pulling the SDA line low during the entire high period of the SCL cycle. Upon detecting this ACK, the master knows that communication link with a slave has been established.

This device could be programmed for eight slave addresses by connecting a resistor R_{ADDR} between the A0 pin and ground, which is shown as Table 1. And ±5% accuracy resistor is suitable for most applications.

The master generates further SCL cycles to either transmit data to the slave (R/$\overline{W}$ bit = 0) or receive data from the slave (R/$\overline{W}$ bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an ACK signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit ACK can continue as long as necessary. To terminate the data transfer, the master generates a STOP condition by pulling the SDA line from low to high while the SCL line is high (see Figure 9). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the STOP condition. Upon the receipt of a STOP condition, all devices know that the bus is released, and they wait for a START condition followed by a matching address.

Table 1. SGM41295 Slave Address Byte

(MSB)			SGM41295 ADDRESS				(LSB)	8-Bit Write Value (Hex)	R_{ADDR} (kΩ)
0	0	1	1	0	0	0	R/$\overline{W}$	0x30	0
0	0	1	1	0	0	1	R/$\overline{W}$	0x32	4.64
0	0	1	1	0	1	0	R/$\overline{W}$	0x34	9.1
0	0	1	1	0	1	1	R/$\overline{W}$	0x36	15.4
0	0	1	1	1	0	0	R/$\overline{W}$	0x38	25.5
0	0	1	1	1	0	1	R/$\overline{W}$	0x3A	44.2
0	0	1	1	1	1	0	R/$\overline{W}$	0x3C	86.6
0	0	1	1	1	1	1	R/$\overline{W}$	0x3E	300

DETAILED DESCRIPTION (continued)

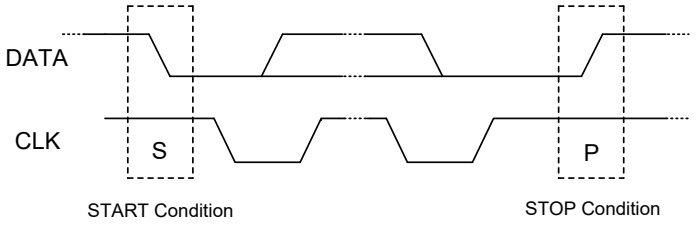


Figure 6. START and STOP Conditions

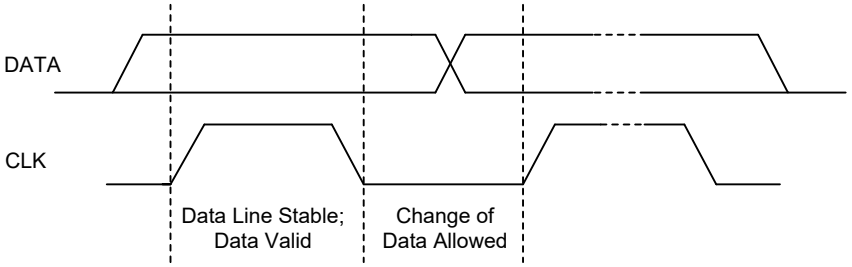


Figure 7. Bit Transfer on the Serial Interface

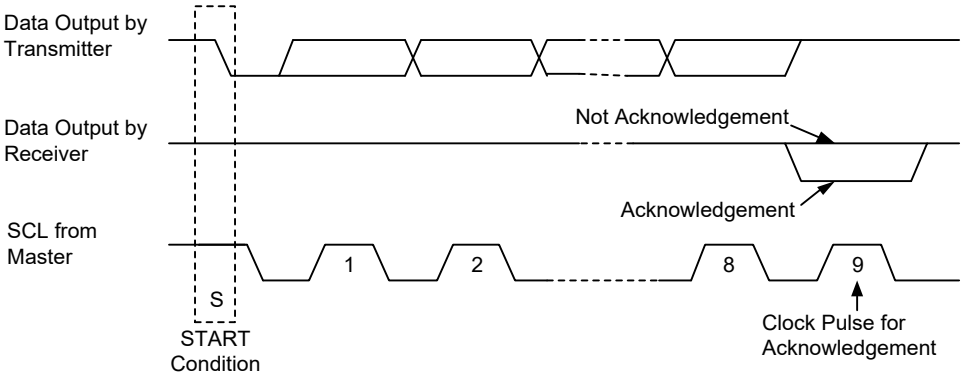


Figure 8. Acknowledgement on the I^2C Bus

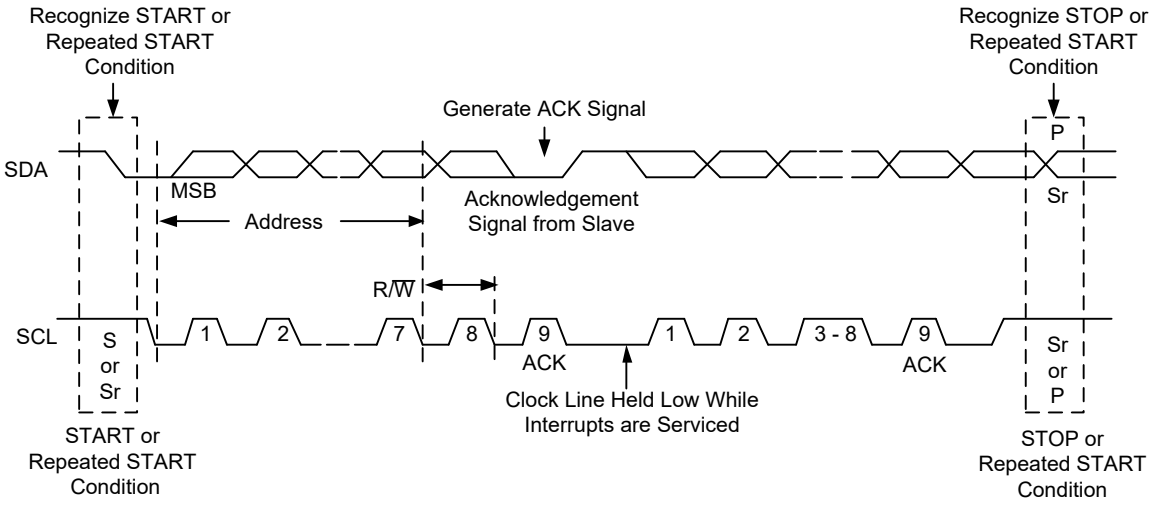


Figure 9. Bus Protocol

CONTROLS AND LOGIC DIAGRAMS

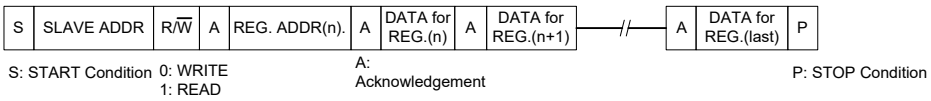


Figure 10. Write Data in F/S-Mode with Register Address Auto-Increment

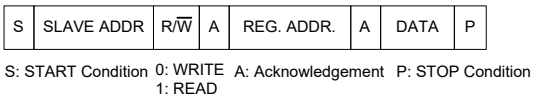


Figure 11. I^2C Transfer Format Writing into a Single Register

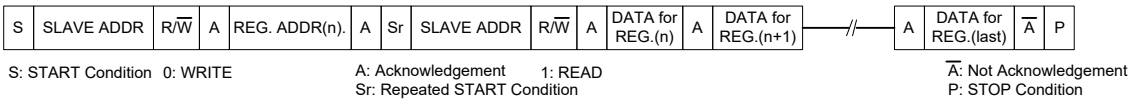


Figure 12. Read Data in F/S-Mode with Register Address Auto-Increment

REGISTER MAP

Addr	Byte Name	Bit No.	Default Hex	RW	Function
0x00h	Soft Reset	7:3	00	RW	Reserved.
		2	0	RW	1: Generate Reset. Reset all digital settings to defaults.
		1:0	0	RW	Reserved.
0x01h	Status	7:6	0	R	Reserved.
		5	0	R	LD Short Flag. This flag will be set high when LD is shorted to GND.
		4	0	R	LD Open Flag. This flag will be set high when LD is open.
		3	0	R	V_{EA} Short Flag. This flag will be set high when V_{EA} is shorted to GND.
		2	0	R	OT_Alert (Over-Temperature Alert). The flag will be set high when die temperature is higher than +135℃. Fault flag will be also set high when OT_Alert is high.
		1	0	R	Fault Flag. The flag will be set high when certain abnormal events happen.
		0	x	R	EN_LD Pin Status.
0x02h	IEA Sample Ratio	7:1	00	RW	Reserved.
		0	0	RW	1 for 40:1 (I_{EA}/I_{MON}). 0 for 20:1 (I_{EA}/I_{MON}).
0x03h	LD_EN/ VEA_EN	7:2	00	RW	Reserved.
		1	1	RW	Enable V_{EA} Voltage Source. 1: Enable, 0: Disable.
		0	1	RW	Enable LD Current Source. 1: Enable, 0: Disable.
0x04h	MPD Range Selection	7:1	00	R	Reserved.
		0	0	RW	MPD Range Selection. The selection of monitoring range for MPD. This bit is to select the range of MPD monitoring current. 0: The monitoring range for MPD is 250μA ~ 2mA (mirror ratio = 1:1). 1: The monitoring range for MPD is 50μA ~ 250μA (mirror ratio = 1:8).
0x05h	LD Gain and Offset Ctrl	7:4	00	R	Reserved.
		3	0	RW	LD Current Gain Selection. 0: gain = 1 (0mA ~ 239.5mA). 1: gain = 1/2 (0mA ~ 119.75mA).
		2:0	0	RW	LD Pin Offset Selection. 000: The I_{LD} offset current is 0mA. 001: The I_{LD} offset current is 16mA. 010: The I_{LD} offset current is 32mA. 011: The I_{LD} offset current is 48mA. 100: The I_{LD} offset current is 64mA. 101: The I_{LD} offset current is 80mA. 110: The I_{LD} offset current is 96mA. 111: The I_{LD} offset current is 112mA.
0x06h	Multiplex Monitoring Output Selection	7:2	00	RW	Reserved.
		1:0	3	RW	Multiplex Monitoring Output Channel Selection (1). This register is used to select channels to MON pin.
DAC registers (Reg 0x20h ~ 0x21h) All data written to these registers are immediately copied to the DAC registers and the DAC output updates.					
0x20h	ILD	7:0	00	RW	8-bit Laser Bias for Channel 0. $I_{LD} = k \times (I_{OFFSET} + 128 \times (Code/256))$.
0x21h	VEA	7:0	00	RW	8-bit EAM Bias for Channel 0. $V_{EA} = -3.2 \times (Code/256)$.

NOTE:

1. Multiplex Monitoring Output Selection

Multiplex Selection (2-Bit Hex)	Input
0	VEA Monitor Current.
1	MPD Monitor Current.
2	LD Monitor Voltage (1/2).

APPLICATION INFORMATION

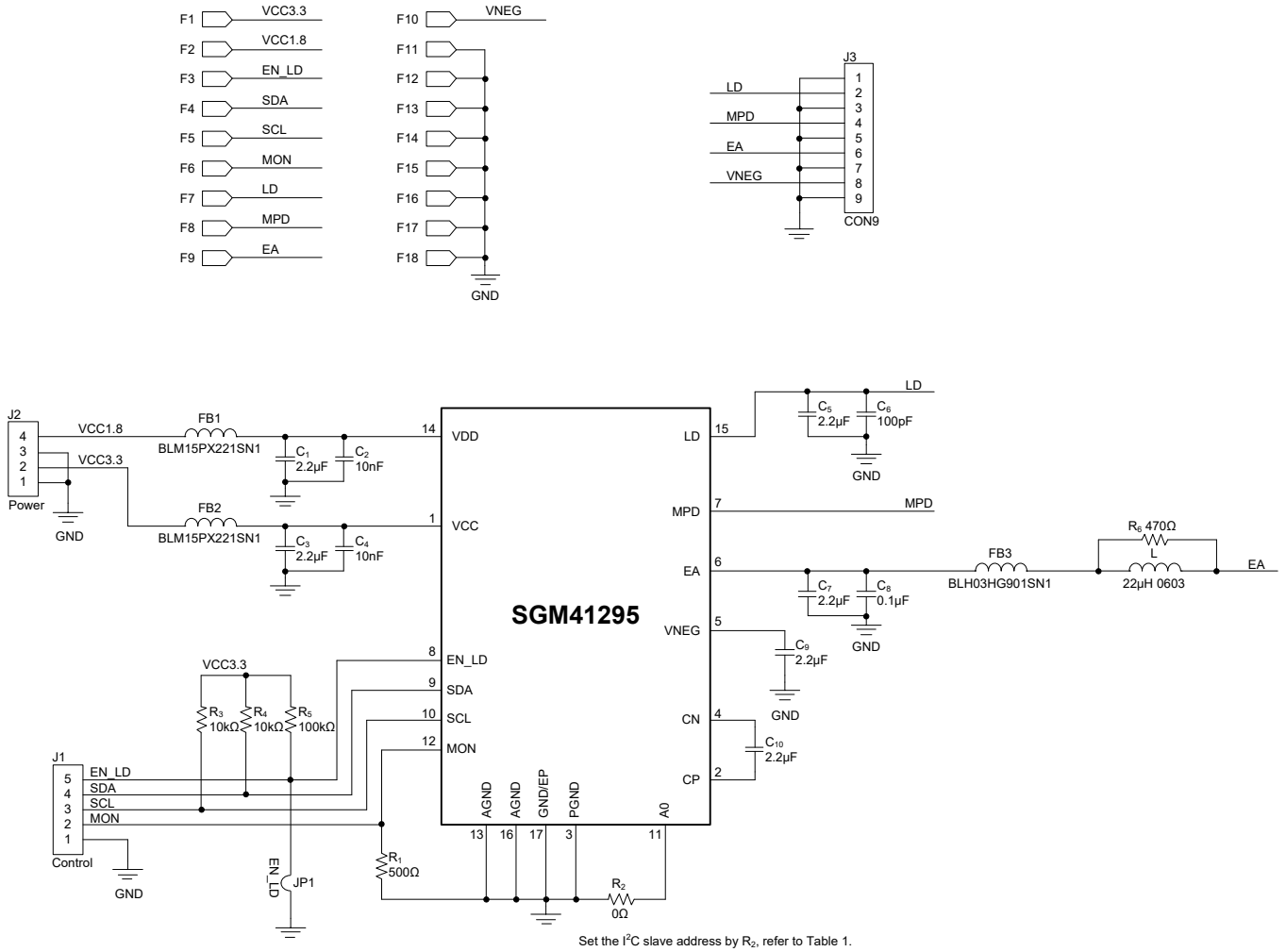


Figure 13. SGM41295 Demo Board Circuits

PCB Layout Guideline

A good PCB layout is critical for stable operation of the SGM41295. Follow these guidelines for the best results:

- The SGM41295 charge pump has high di/dt switching loop, which is formed by the VCC (pin 1), CP (pin 2), CN (pin 4), VNEG (pin 5) and PGND (pin 3). It is critical to put the C_{VCC} (C_3, C_4), C_{FLY} (C_{10}) and C_{VNEG} (C_9) capacitors as close to their respective device pins and PGND pin as possible, which minimizes the parasitic inductance and the VCC pin voltage spike.
- It is recommended to connect the PGND (pin 3) and the bottoms of C_{VCC} (C_3, C_4) and C_{VNEG} (C_9) as close as possible, away from others to avoid the PGND high di/dt current flows through the SGM41295 exposed pad (EP) and AGND (pin 13 and pin 16).
- The VDD (pin 14) is not a high di/dt switching pin. It is recommended to put C_{VDD} (C_1, C_2) as close to VDD (pin 14) and AGND (pin16, pin13 and EP) as possible for better noise decoupling.
- The LD (pin 15) is not a high di/dt switching pin. It is recommended to put C_{LD} (C_5, C_6) as close to LD pin and AGND (pin 16, pin 13 and EP) as possible for better noise decoupling.

APPLICATION INFORMATION (continued)

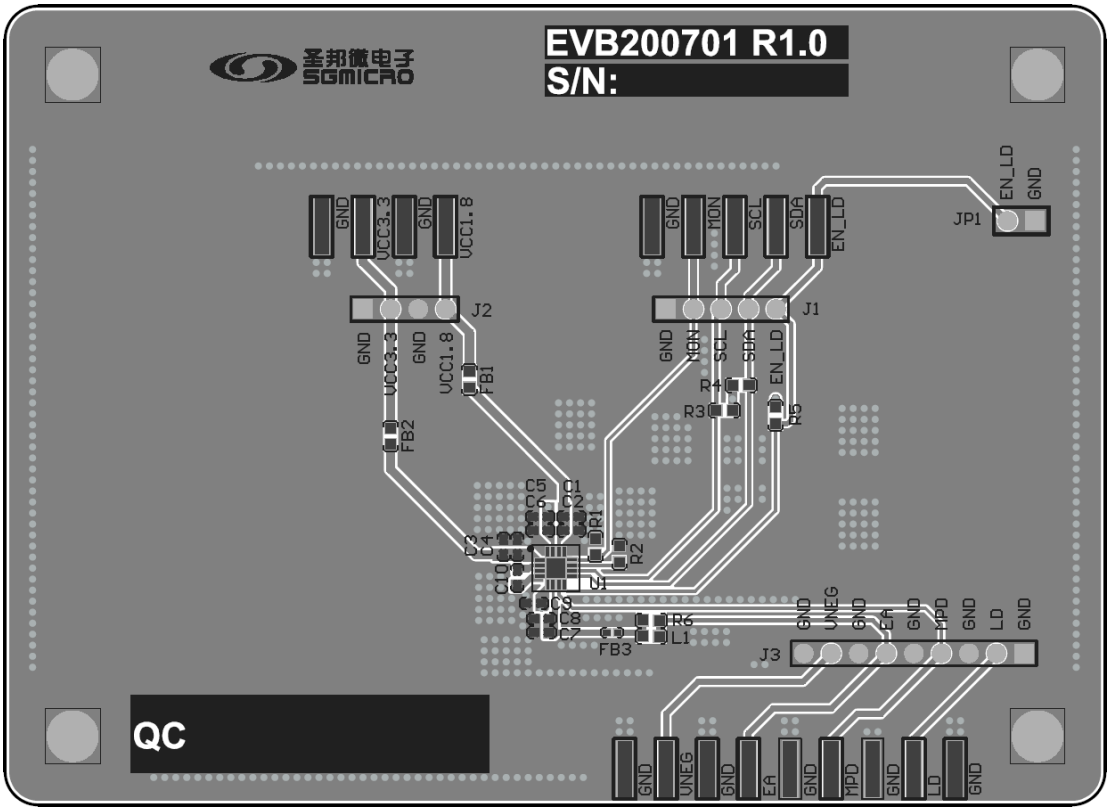


Figure 14. Top Layer

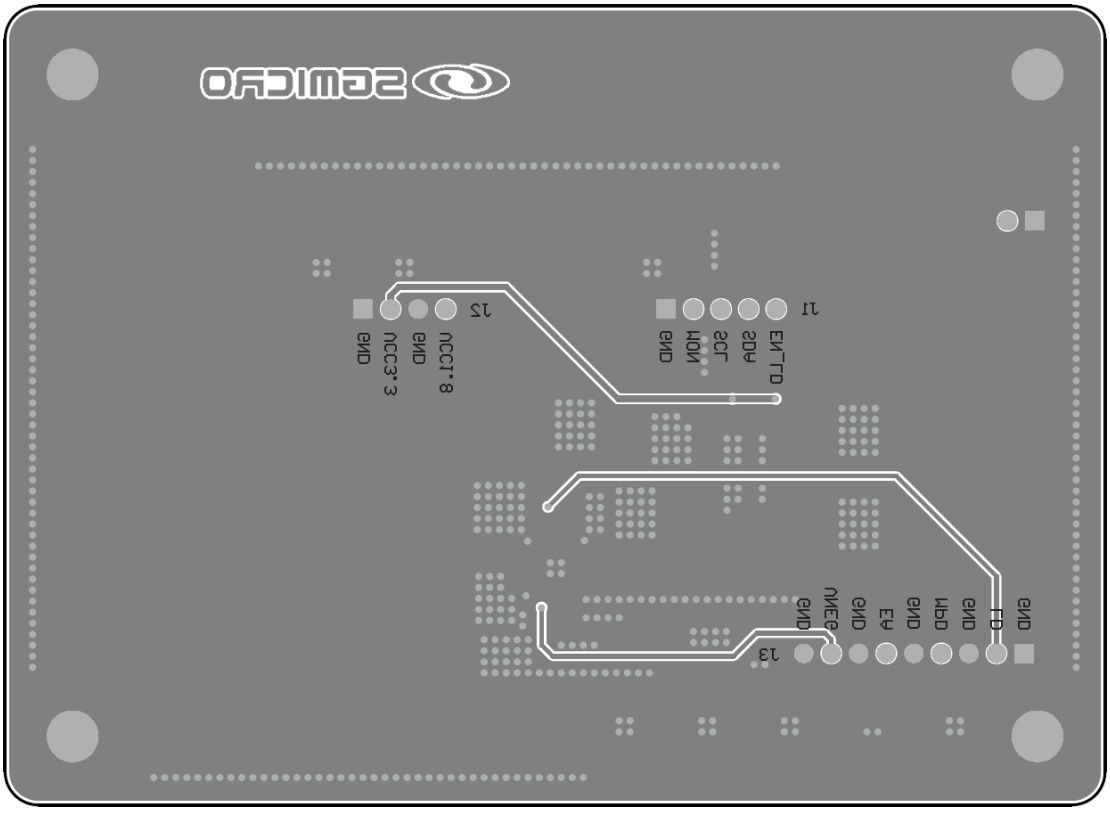


Figure 15. Bottom Layer

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JULY 2024 – REV.B to REV.B.1	Page
Added Package Thermal Resistance section	2
Updated Package Outline Dimensions	20

NOVEMBER 2023 – REV.A.4 to REV.B	Page
Updated the Register Map section	16

JUNE 2023 – REV.A.3 to REV.A.4	Page
Updated Electrical Characteristics and I^2C Interface Timing Characteristics sections	5-7

DECEMBER 2022 – REV.A.2 to REV.A.3	Page
Updated the Enable and Disable section	10

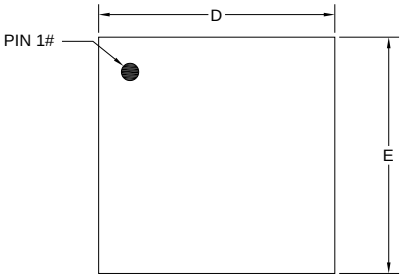
SEPTEMBER 2021 – REV.A.1 to REV.A.2	Page
Added the PCB layout guideline section	16-17

JANUARY 2020 – REV.A to REV.A.1	Page
Updated the I^2C INTERFACE TIMING CHARACTERISTICS (1)	6

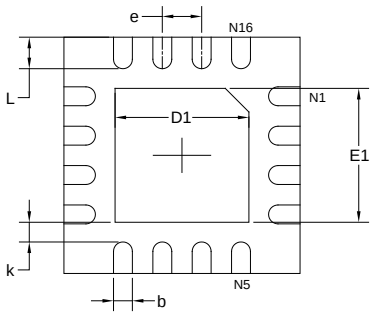
Changes from Original (JULY 2019) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

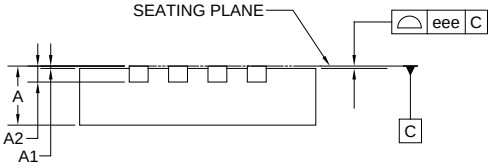
TQFN-3×3-16L



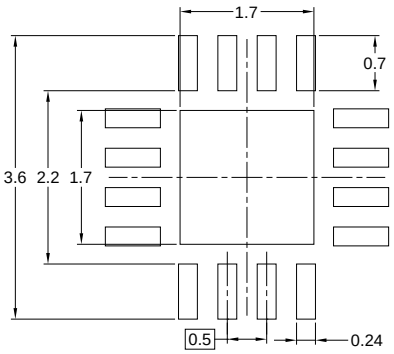
TOP VIEW



BOTTOM VIEW



SIDE VIEW



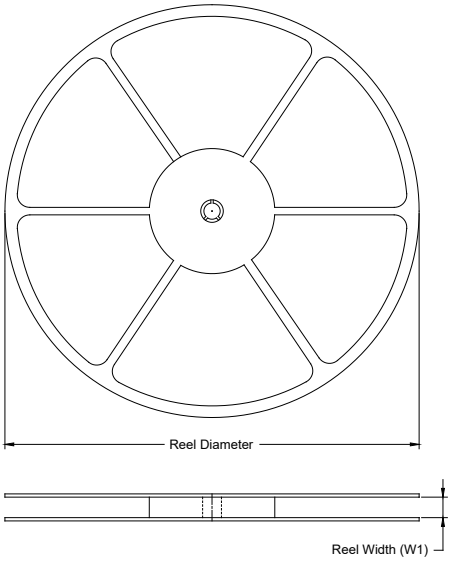
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020
eee	0.080		0.003	

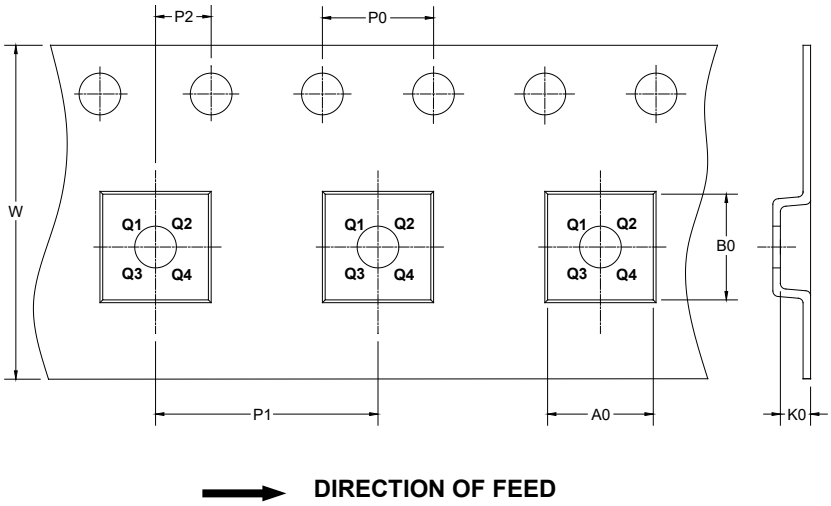
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



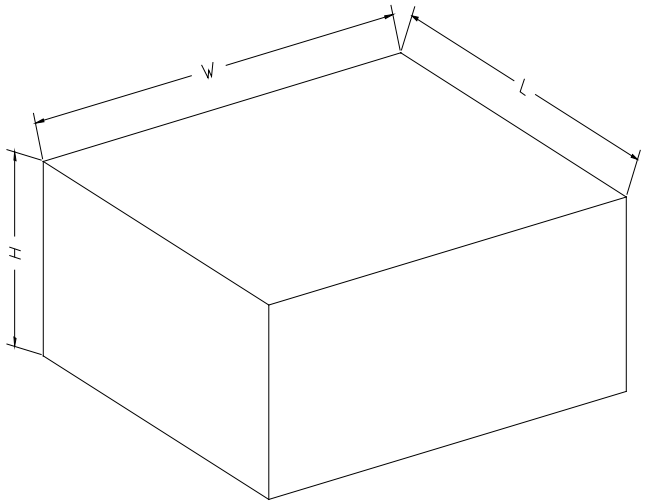
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-16L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002