SGM41664A
Efficient I²C Power Backup Manager with High Current Bidirectional DC/DC Converter and Capacitor Measurement Capability

GENERAL DESCRIPTION

The SGM41664A is a programmable power management IC with I²C interface and integrated analog-to-digital converter (ADC) for applications that need backup power or energy storage capability such as solid-state drivers (SSD). For example, in an SSD the power is needed for a few milliseconds after an unexpected supply loss to complete any remaining write action. The integrated efficient bidirectional synchronous Buck converter/Boost charger is capable of charging storage capacitors to as high as 36V from a 2.8V to 16V input source. A quasi-fixed frequency and constant off-time controller provides fast transient response and excellent converter stability.

An integrated reverse blocking MOSFET (BLKFET) in the input allows blocking of energy leaking back to the removed source. The BLKFET has a programmable current limit in the range of 1.2A to 6.2A. BUS over-voltage protection threshold is selected based on the input source nominal voltage (3.3V, 5V or 12V) by strapping the OVP pin. The I²C interface is used to set the input current limit, switching frequency, Boost peak current limit and for measuring the storage capacitance and ESR. It is also used to monitor system variables and statuses, such as input voltage, input current, BUS voltage and storage voltage.

The SGM41664A is available in a Green TQFN-4×4-25L package to allow compact layout design and better space saving for higher SSD memory capacity.

APPLICATIONS

Solid-state Drivers

Power Backup Systems

FEATURES

- **Wide 2.8V to 16V Input Voltage Range**
- **Up to 36V Programmable Storage Voltage**
- **Up to 6.2A Programmable Input Current Limit**
- **Efficient Bidirectional DC/DC Converter**
- **Low R_{DSON} for Internal MOSFETs**
  - **Input Reverse Blocking MOSFET (BLKFET): 14mΩ**
  - **High-side/Low-side MOSFETs: 45mΩ/47mΩ**
  - **STR Disconnect MOSFET (STRFET): 35mΩ**
- **Adjustable BLKFET Turn-On Delay and Soft-Start**
- **Adjustable Quasi-Fixed Frequency: 0.25MHz to 1.5MHz**
- **Constant Off-Time Control in Steady State**
- **Programmable Boost Charging Peak Current**
- **Autonomous or I²C Modes for Optimal Operation**
- **Complete Voltage and Current ADC Conversion**
- **Selectable Input Over-Voltage Protection**
- **Input Reverse Blocking to Block Leakage Current**
- **Short-Circuit Protection at Energy Storage Side**
- **Storage Capacitance Measurement**
- **Abnormal ESR Detection**

TYPICAL APPLICATION

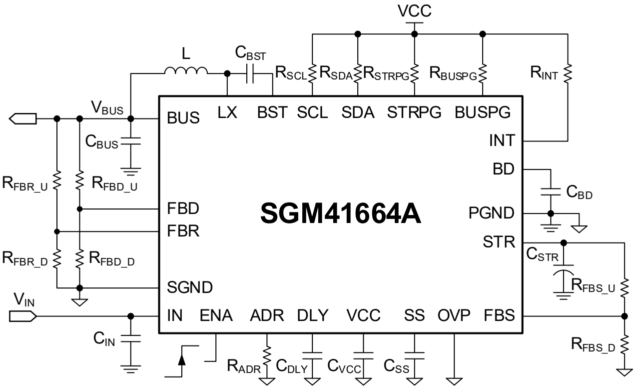


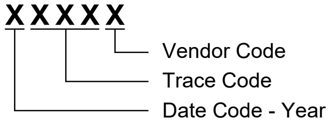
Figure 1. SGM41664A Typical Application

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41664A	TQFN-4×4-25L	-40℃ to +125℃	SGM41664AXTRQ25G/TR	1SS XTRQ25 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range
STR, BD, LX, BST, FBS.................................. -0.3V to 38V
LX (10ns transient).. -5V to 38V
IN, BUS, BUSPG, OVP, STRPG, ADR, FBD, FBR, ENA, BD - STR, INT... -0.3V to 18V
IN, BUS, BUSPG, OVP, STRPG, ADR, ENA, INT (100ns transient)... -0.3V to 22V
SCL, SDA, DLY, SS.. -0.3V to 6V
VCC, BST - LX.. -0.3V to 4V
Package Thermal Resistance
TQFN-4×4-25L, θ_{JA}.. 59℃/W
Junction Temperature...+150℃
Storage Temperature Range........................-65℃ to +150℃
Lead Temperature (Soldering, 10s)............................+260℃
ESD Susceptibility
HBM..2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

STR, BD, LX, BST, FBS Voltages .... -0.3V to 36V
IN, BUS, BUSPG, OVP, STRPG, ADR, FBD, FBR, ENA, BD - STR, INT Voltages.................................... -0.3V to 16V
SCL, SDA, DLY, SS Voltages.............................. -0.3V to 5V
VCC, BST - LX Voltages.................................. -0.3V to 3.3V
Operating Junction Temperature Range.......-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

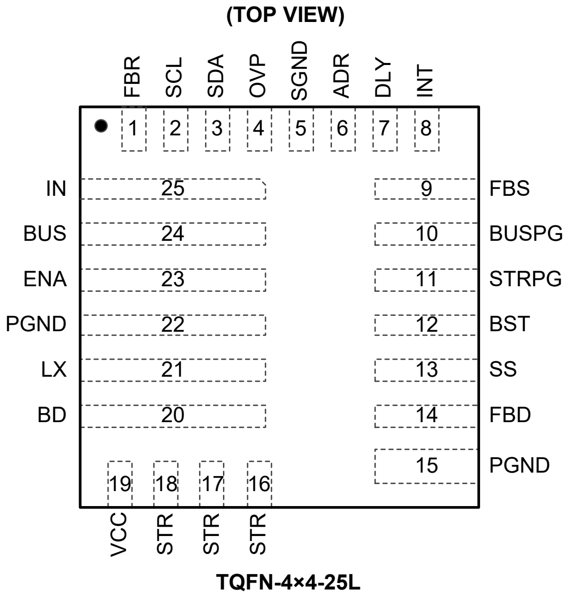
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



TQFN-4×4-25L

PIN DESCRIPTION

<table>
<tr><th>NUMBER</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>FBR</td><td>Voltage Feedback Pin for Buck Mode Regulation. Use a resistor divider to set the Buck mode voltage (V_{REF} = 0.61V).</td></tr>
<tr><td>2</td><td>SCL</td><td>I^2C Interface Clock Pin.</td></tr>
<tr><td>3</td><td>SDA</td><td>I^2C Interface Data Pin.</td></tr>
<tr><td>4</td><td>OVP</td><td>Input Over-Voltage Threshold Selection Pin (selected based on the input source voltage). Use the following table to select the input OVP threshold and the OVP logic will be latched after the power-on reset (POR) is completed. It is recommended to decoupling this pin with a 0.1μF capacitor when OVP logic is High. This pin also determines the minimum input voltage that turns on the device (POR threshold).
<table>
<tr><th rowspan="2">OVP Pin State</th><th rowspan="2">Input Source Voltage</th><th>V_{IN} OVP Threshold</th></tr>
<tr><th>TYP</th></tr>
<tr><td>Low (OVP = GND)</td><td>3.3V</td><td>3.8V</td></tr>
<tr><td>High (OVP = IN)</td><td>5V</td><td>6.1V</td></tr>
<tr><td>OVP Floating</td><td>12V</td><td>14.1V</td></tr>
</table></td></tr>
<tr><td>5</td><td>SGND</td><td>Signal Ground Pin.</td></tr>
<tr><td>6</td><td>ADR</td><td>I^2C Address Pin. Pull ADR up by a resistor to IN pin to select address 0x59. Pull it low by a resistor to SGND to select 0x5A. Float it to select address 0x5B. The I^2C Address will be latched after the POR is completed.</td></tr>
<tr><td>7</td><td>DLY</td><td>Turn-On Delay Time Program Pin for the Reverse Blocking MOSFET (BLKFET). Connect DLY with a capacitor (C_{DLY} > 10nF) to SGND to program this delay time: $t_{DLY}\ (ms) = \frac{C_{DLY}(nF) \times 1V}{4\mu A}$ or float it for the default 1ms delay.</td></tr>
<tr><td>8</td><td>INT</td><td>Open-Drain Interrupt Indicator Pin. INT goes high to indicate a fault condition.</td></tr>
<tr><td>9</td><td>FBS</td><td>Voltage Feedback Pin for Energy Storage Capacitor. Use a resistor divider to set the storage voltage. If R_5 resistor is between STR and FBS and R_6 between FBS and GND, $V_{STR} = 1.205V \times (1 + R_5/R_6)$.</td></tr>
<tr><td>10</td><td>BUSPG</td><td>Open-Drain Power Good Output Pin for BUS Voltage. BUSPG is pulled low if FBD pin voltage drops below 0.605V, and is released to go high when the FBR pin voltage exceeds 0.635V.</td></tr>
<tr><td>11</td><td>STRPG</td><td>Open-Drain Power Good Output Pin for STR Voltage. STRPG is pulled low if FBS pin voltage drops below 1V, and is released to go high when the FBS voltage exceeds 1.05V.</td></tr>
<tr><td>12</td><td>BST</td><td>Bootstrap pin. It supplies the high-side gate driver of the bidirectional converter. Connect a 0.1μF or larger ceramic capacitor between this pin and LX.</td></tr>
<tr><td>13</td><td>SS</td><td>Soft-Start Program Pin for the Reverse Blocking MOSFET. Use an external capacitor to set this soft-start time.</td></tr>
<tr><td>14</td><td>FBD</td><td>Feedback Pin for Buck Mode Detection. The converter goes to Buck mode if the FBD voltage falls below 0.605V. Use a feedback resistor divider on BUS voltage to set the BUS low voltage detection level and start Buck mode.</td></tr>
<tr><td>15, 22</td><td>PGND</td><td>Power Ground Pins.</td></tr>
<tr><td>16, 17, 18</td><td>STR</td><td>Energy Storage Capacitor Connection Pins. Connect the storage capacitors between STR and PGND.</td></tr>
<tr><td>19</td><td>VCC</td><td>3.3V Internal LDO Output Pin. Decouple VCC to GND with at least 2.2μF ceramic capacitor (X5R or better).</td></tr>
<tr><td>20</td><td>BD</td><td>Drain Pin of the STR Disconnect FET (STRFET) and the Input of the Buck Converter. BD must be decoupled to PGND with at least a 2.2μF ceramic capacitor (X5R or better).</td></tr>
<tr><td>21</td><td>LX</td><td>Converter Switching Node Pin. Connect it to the inductor and bootstrap capacitor.</td></tr>
<tr><td>23</td><td>ENA</td><td>Enable Control Pin for the BLKFET with an internal 1MΩ pull-down resistor. Logic high enables the BLKFET.</td></tr>
<tr><td>24</td><td>BUS</td><td>BUS Output Pin. It must be decoupled to PGND with at least 22μF ceramic capacitor (X5R or better).</td></tr>
<tr><td>25</td><td>IN</td><td>Power Supply Input Pin. Decouple it to PGND with at least 0.1μF ceramic capacitor.</td></tr>
</table>

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V, V_{BUS} = 5V, L = 4.7µH, V_{BD} = V_{STR} = 12V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Device Power Supply (IN)						
Input Voltage Range	V_{IN}		2.8		16	V
Input Rising for Activating I^2C	V_{IN4C}	V_{IN} rising		2.5	2.8	V
Power-On Reset (POR) Rising Threshold (V_{IN})	V_{PORR}	OVP = low		2.5	2.8	V
		OVP = high		3.5	3.7	
		OVP = floating		8.4	9	
POR Falling Threshold (V_{IN})	V_{PORF}	OVP = low	2.0	2.4		V
		OVP = high	3.1	3.3		
		OVP = floating	7.6	8		
On-Resistance of BLKFET	R_{DSON_R}			14	25	mΩ
Reverse Blocking Leakage Current	I_{RBLK}	V_{IN} = 0V, V_{BUS} = 16V, V_{ENA} = 0V		0.1	2	µA
		V_{IN} = 16V, V_{BUS} = 0V, V_{ENA} = 0V		0.1	2	
Input Supply Current Before POR	I_{IN_POR}	V_{IN} rises to 8V, OVP = floating, ENA = high			267	µA
Bias Current (IN)	I_{BIAS}	V_{IN} = 5V, OVP = high, DC/DC converter is disabled		1400		µA
Reverse Blocking Range	V_{RB}				16	V
Input Over-Voltage Threshold (1)	V_{OVP}	OVP = low, internal accuracy	3.67	3.8	3.90	V
		OVP = high, internal accuracy	5.91	6.1	6.23	
		OVP = floating, internal accuracy	13.77	14.1	14.45	
Input Over-Voltage Threshold Hysteresis	V_{OVPHYS}	OVP = low		150		mV
		OVP = high		200		
		OVP = floating		400		
BLKFET Turn-On Delay Time	t_{DLY}	C_{DLY} = 10nF (1)		2.5		ms
Soft-Start Time	t_{SS}	C_{SS} = 100nF (2)		16.5		ms
Current Limit Program Range	I_{LIM}		1.2		6.2	A
Current Limit Accuracy		LSP[5:3] = 011	-9		9	%
BUSPG Threshold (1)	V_{BUSPGH}	V_{FBR} rising, internal accuracy	0.611	0.635	0.655	V
	V_{BUSPGL}	V_{FBD} falling, internal accuracy	0.590	0.605	0.619	V
Internal LDO Output Voltage	V_{VCC}	V_{IN} > 3.3V		3.3		V
		V_{IN} ≤ 3.3V		V_{IN}		
ENA Logic Voltage	V_{ENAH}		1.1			V
	V_{ENAL}				0.5	V
OVP Pin Logic Voltage	V_{OVPH}		1.1			V
	V_{OVPL}				0.5	V
Bidirectional DC/DC Converter						
BUS Side Operation Voltage Range	V_{BUSOP}		2.8		16	V
STR Side Buck Operation Voltage Range	V_{STROP}		2.8		36	V
Boost Minimum Peak Current	I_{PMIN}			250		mA
Switching Frequency	f_{SWBST}	SF[1:0] = 01		500		kHz
Minimum LSFET On-Time	t_{OFF_MINL}	During Boost/Buck mode		110		ns
Minimum HSFET On-Time	t_{ON_MIN}	During Boost/Buck mode		110		ns
Boost CV Mode Voltage Reference	V_{REF_BST}	T_J = +25℃, internal accuracy	1.188	1.205	1.222	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V, V_{BUS} = 5V, L = 4.7μH, V_{BD} = V_{STR} = 12V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{FBS} Boost Burst Mode Stop Switching Threshold	V_{BRT_R}	V_{FBS} rising		1.2		V
V_{FBS} Boost Burst Mode Switching Resume Threshold	V_{BRT_F}	V_{FBS} falling		1.17		V
V_{FBS} Boost Burst Mode Threshold Accuracy			-3.0		5.0	%
V_{FBD} Buck Detection Voltage Reference (1)	V_{BUCK_DET}	V_{FBD} falling, internal accuracy	0.590	0.605	0.619	V
V_{FBR} Buck Regulation Voltage Reference (1)	V_{BUCK_REG}	Internal accuracy	0.592	0.610	0.624	V
Maximum Cycle-by-Cycle Buck Peak Current	I_{PK_BK}	V_{STR} = 28V, V_{BUS} = 8.6V, T_J = +25℃	7.5	8.4		A
V_{FBS} STRPG Threshold	V_{STRPGH}	V_{FBS} rising		1.05		V
	V_{STRPGL}	V_{FBS} falling		1.00		V
STR Short-Circuit Detection Threshold in Pre-charge	V_{STRSC}	V_{FBS} value		0.7		V
Pre-charge Current	I_{PRECHG}	V_{STR} = 7.5V, V_{BD} = 15V		150		mA
R_{DSON} of High-side FET	R_{DSON_H1}			45	74	mΩ
R_{DSON} of Low-side FET	R_{DSON_L1}			47	76	mΩ
R_{DSON} of STR Disconnect FET	R_{DSON_D}			35	59	mΩ
STR Capacitor Measurement						
Capacitance Measurement Discharge Current	I_{DIS}	DCP[7:6] = 10		9.5		mA
Internal Counter Clock	f_{CLK}			500		Hz
Abnormal ESR Detection Discharge Current	I_{ESR}			1		A
I^2C and Logic Interfaces (SDA, SCL, ADR, INT)						
High State Input Voltage	V_{IH}	SDA and SCL pins	1.5			V
Low State Input Voltage	V_{IL}	SDA and SCL pins			0.4	V
Low State Output Voltage	V_{OL}	Sink 4mA, INT pin			0.5	V
ADR Pin Logic Voltage	V_{ADRH}		1.1			V
	V_{ADRL}				0.5	V
ADC						
ADC Reference Voltage	V_{REF_ADC}			1		V
ADC Resolution				8		Bits
ADC Conversion Time		For one variable		40		μs
Thermal Protection						
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Recovery Hysteresis	T_{HYS}			25		℃
Thermal Warning Threshold	T_{WRN}			125		℃

NOTES:

1. These values are guaranteed by FT.
2. Recommended Delay Time Program Table

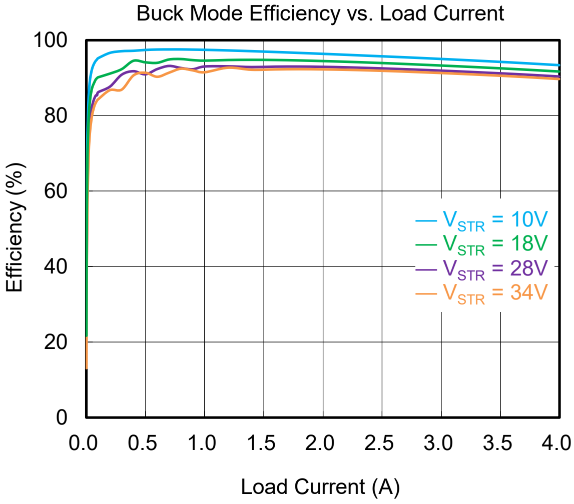
C_{DLY} (nF)	None	10	47	100
Delay Time (ms)	1.0	2.5	11.8	25.0

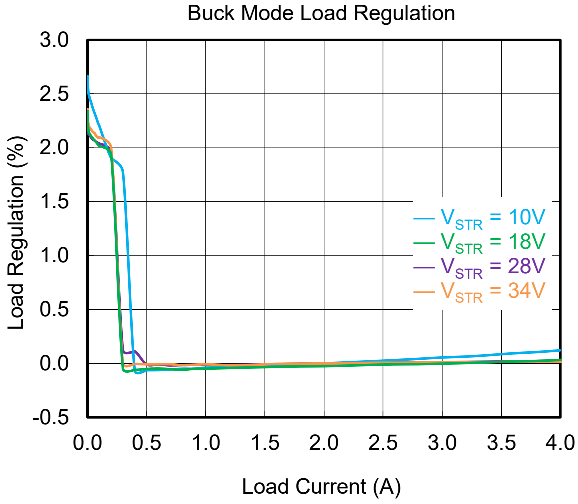
3. Recommended Soft-Start Time Program Table

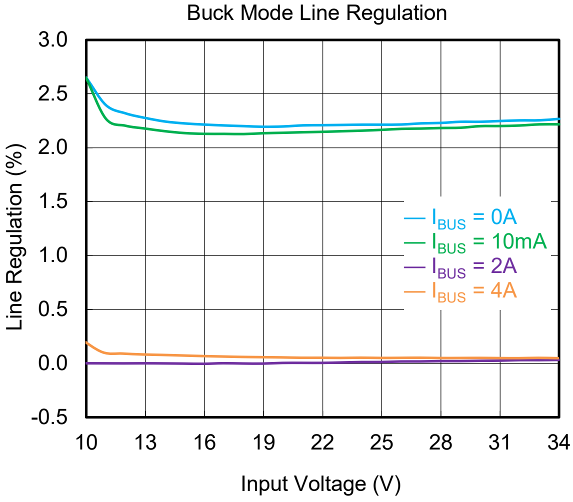
C_{SS} (nF)	None	10	47	100
Rise Time (ms)	1.0	1.7	7.7	16.5

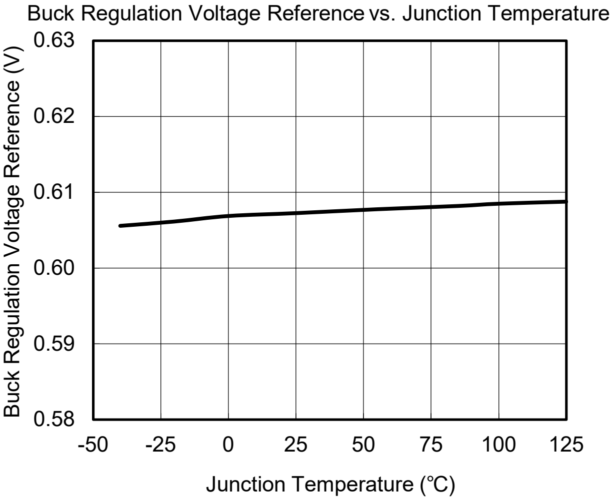
TYPICAL PERFORMANCE CHARACTERISTICS

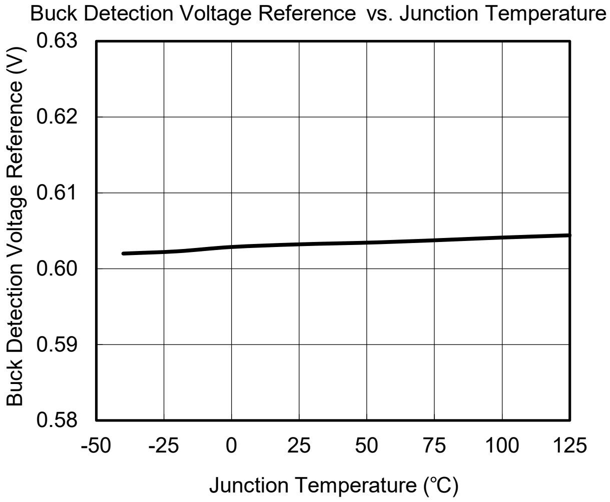
V_{IN} = 12V, V_{BUS_REG} = 8.7V, V_{BUS_DET} = 8.5V, OVP floating, L = 4.7μH, V_{BD} = V_{STR} = 31V, unless otherwise noted.

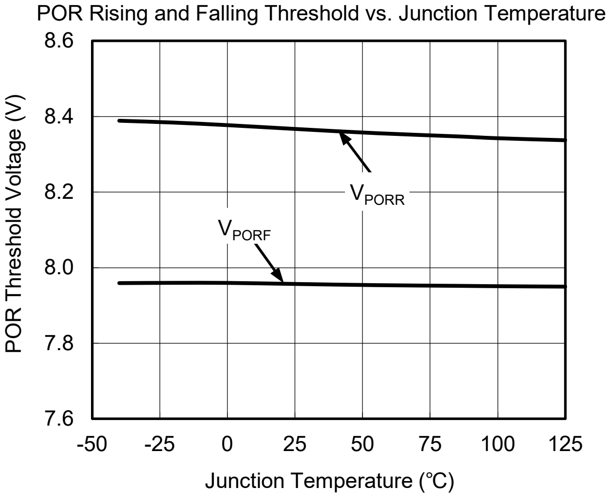








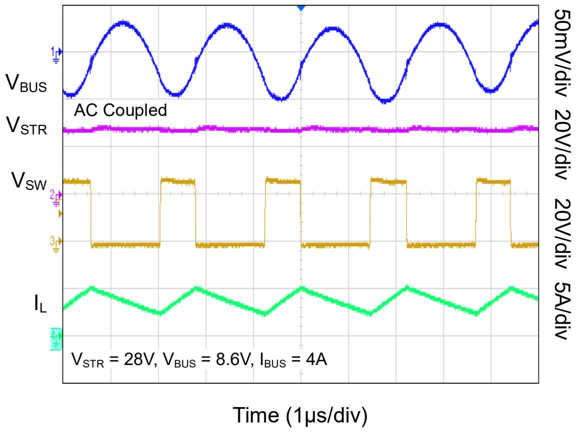




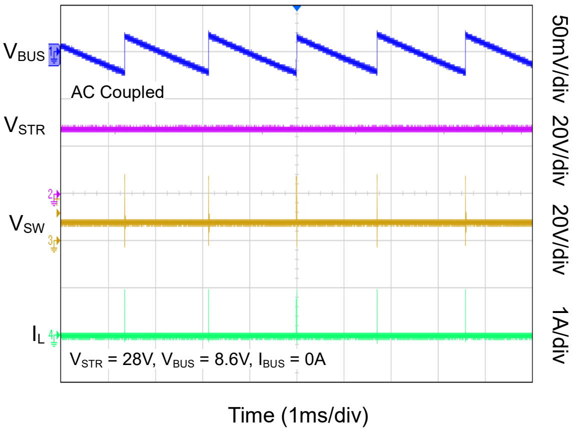
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{BUS_REG} = 8.7V, V_{BUS_DET} = 8.5V, OVP floating, L = 4.7μH, V_{BD} = V_{STR} = 31V, unless otherwise noted.

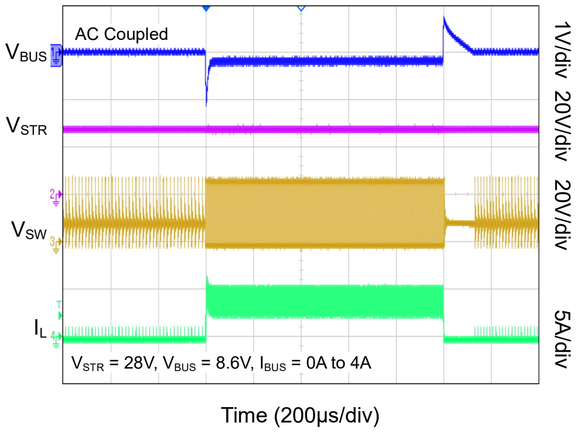
Buck Mode CCM Switching Waveform



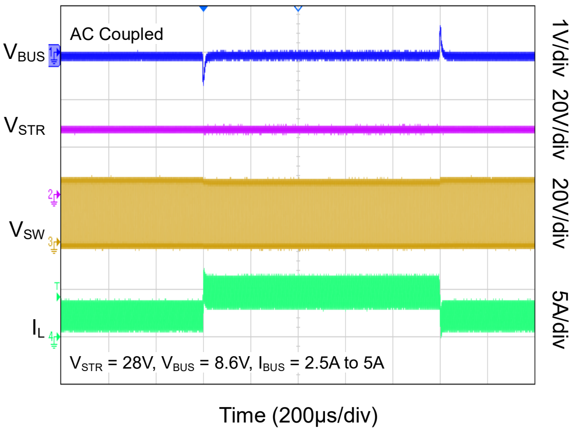
Buck Mode PFM Switching Waveform



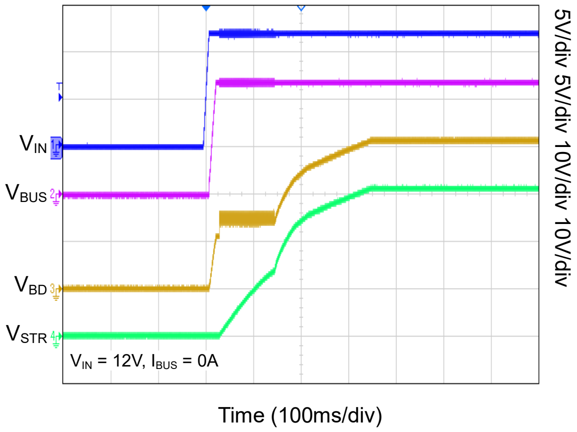
Buck Mode Load Transient



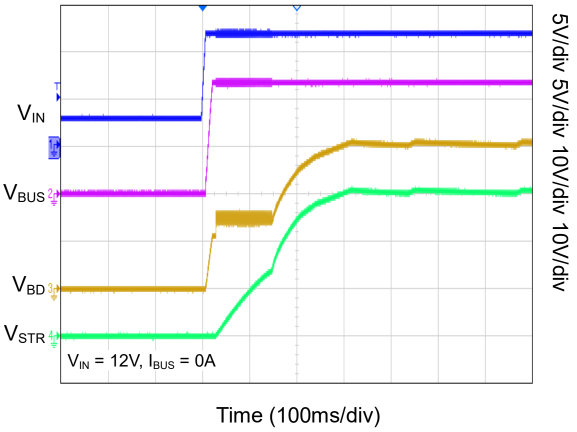
Buck Mode Load Transient



Startup by VIN (CV Mode)



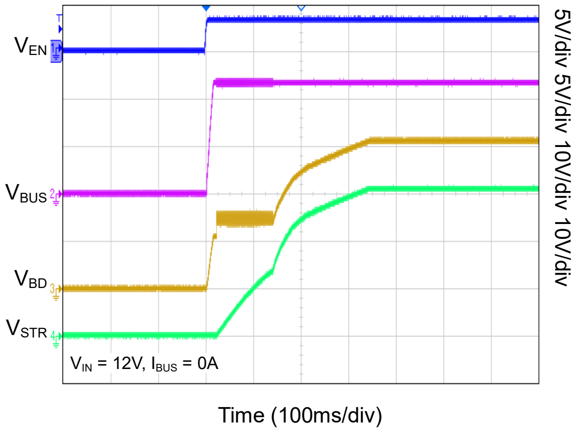
Startup by VIN (Burst Mode)



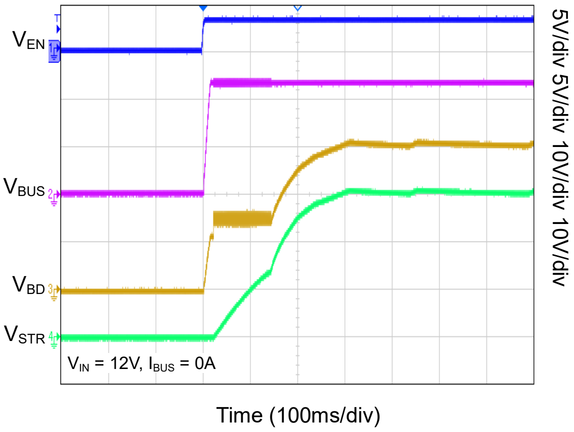
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{BUS_REG} = 8.7V, V_{BUS_DET} = 8.5V, OVP floating, L = 4.7μH, V_{BD} = V_{STR} = 31V, unless otherwise noted.

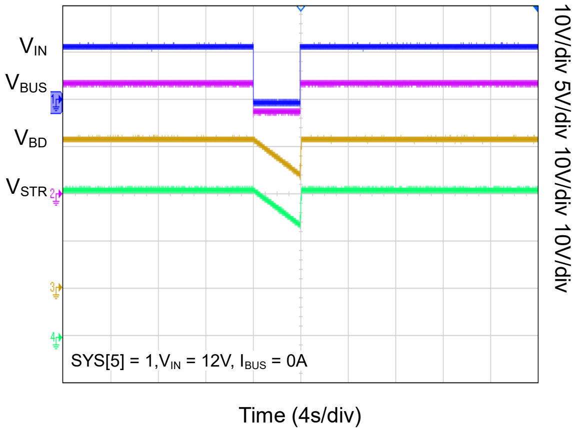
Startup by EN (CV Mode)



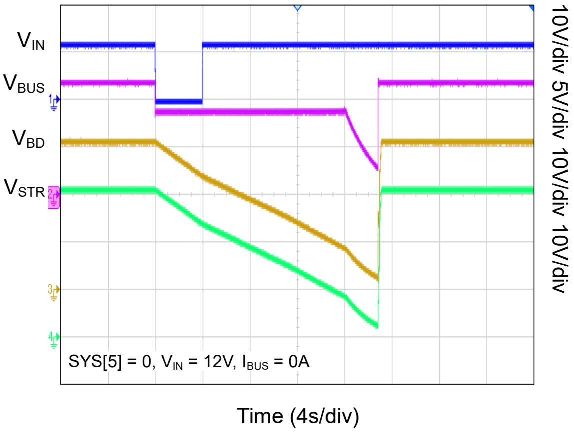
Startup by EN (Burst Mode)



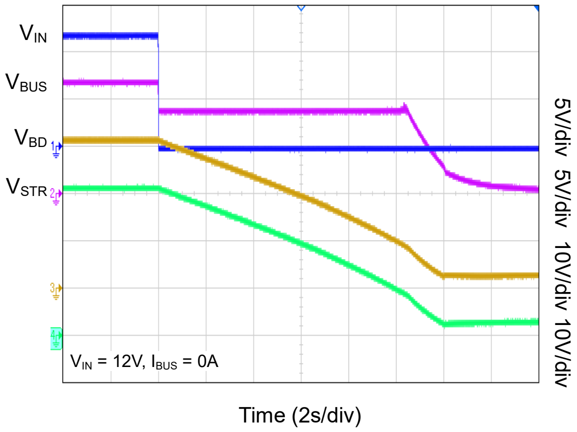
Input Recovery



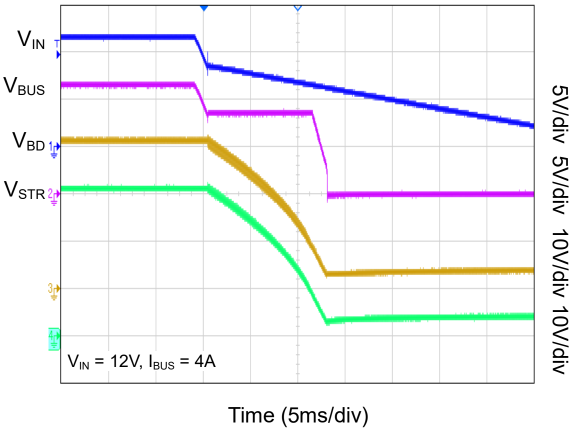
Input Recovery



Shutdown by VIN



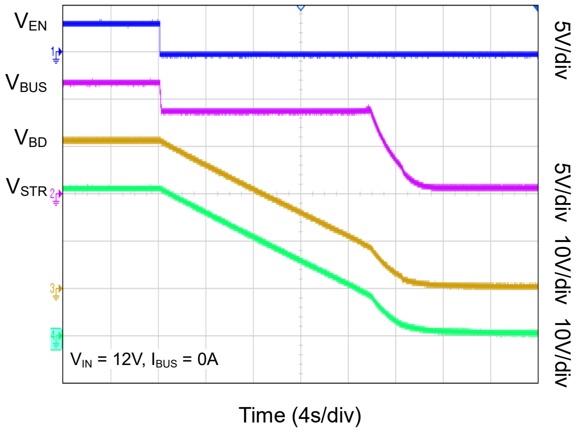
Shutdown by VIN



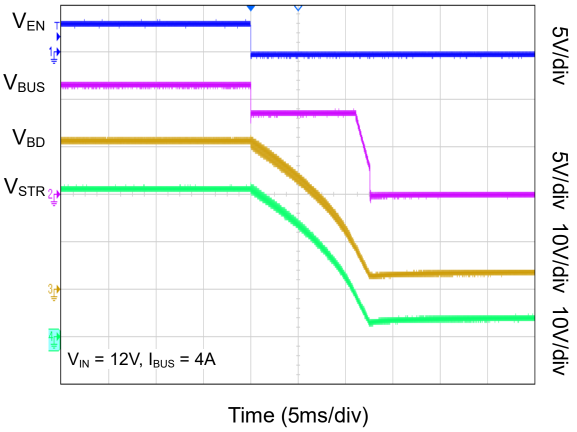
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{BUS_REG} = 8.7V, V_{BUS_DET} = 8.5V, OVP floating, L = 4.7μH, V_{BD} = V_{STR} = 31V, unless otherwise noted.

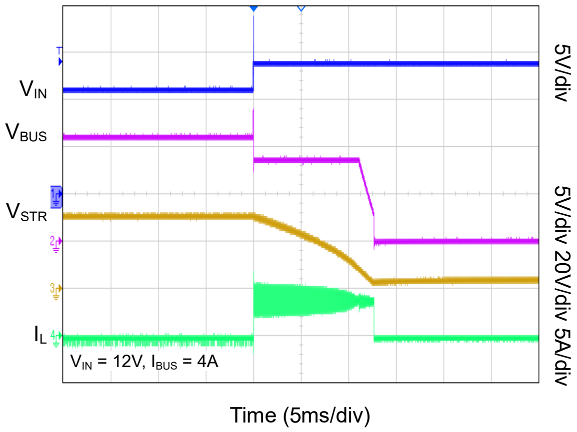
Shutdown by EN



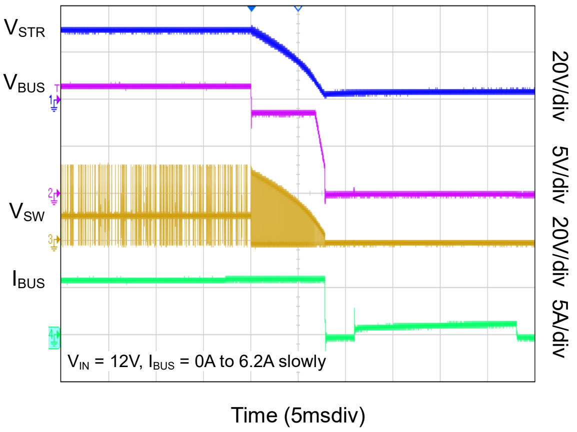
Shutdown by EN



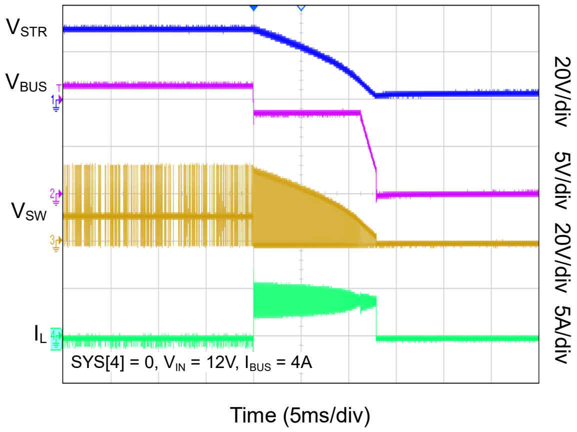
VIN OVP



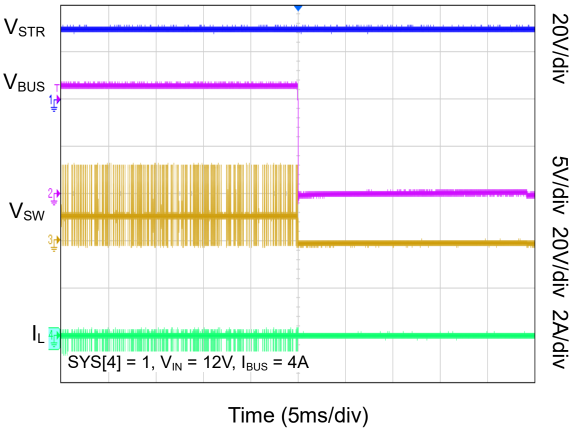
BLKFET OCP



Thermal Shutdown



Thermal Shutdown



REGISTER ADDRESS MAPING (17, 8-Bit Registers)

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).
Slave Device Address is selectable: 0x59, 0x5A or 0x5B.

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE
DEVICE_REV	—	—	—	0x00[5:3]	—
VIN_OVP	—	0x0F[7]	0x0E[7]	—	0x01[7]
ILIM_IN	—	0x0F[6]	0x0E[6]	0x01[5:3]	—
BLKFET	0x10[0]	—	—	—	0x01[0]
IDIS_CSTR	—	—	—	0x02[7:6]	—
CSTR_MEAS	0x07[7:0] & 0x08[7:0]	0x0F[3]	0x0E[3]	0x04[7:0] & 0x05[7:0]	0x06[5]
ESR_DET	0x09[0]	0x0F[3]	0x0E[3]	0x06[3:2]	0x06[5]
STR_SCP	—	0x0F[5]	0x0E[5]	—	—
STR_OVP	—	0x10[3]	—	0x0B[4:0]	—
FSW_SET	—	—	—	0x06[1:0]	—
BOOST	—	—	—	0x02[3:1] & 0x06[4]	0x02[0]
BUCK	—	—	—	—	0x02[0]
BUCK_OFF	—	—	—	0x03[7:0]	—
RECOVER_MODE	—	—	—	0x10[5]	
RB_PROT	—	0x0F[4]	0x0E[4]	—	0x06[6]
THERMAL	—	0x0F[1] & 0x0F[0]	0x0E[1] & 0x0E[0]	0x10[4]	—
VBUS_PG	—	0x10[2]	—	—	—
VIN_PG	—	0x10[1]	—	—	—
ADC	—	0x0F[2]	0x0E[2]	—	0x10[7]
IIN_ADC	0x09[7:2]	—	—	—	—
VBUS_ADC	0x0A[7:0]	—	—	—	—
VIN_ADC	0x0C[7:0]	—	—	—	—
VSTR_ADC	0x0D[7:0]	—	—	—	—

REGISTER DESCRIPTION

Bit Types:

R: Read only bit

R/W: Read or write bit

R/WC: Read or write bit. Writing a ‘1’ clears the bit. Writing a ‘0’ has no effect.

REG0x00: Vendor ID Register Address (reset = 0x00)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	CTRL[7]	0	R	Reserved	
D[6]	CTRL[6]	0	R	Reserved	
D[5]	CTRL[5]	0	R	Device Revision Bits 000 = SGM41664A	
D[4]	CTRL[4]	0	R		
D[3]	CTRL[3]	0	R		
D[2]	CTRL[2]	0	R	Reserved	
D[1]	CTRL[1]	0	R	Reserved	
D[0]	CTRL[0]	0	R	Reserved	

REG0x01: BLKFET Control Parameter Programming Register Address (reset = 0x39)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	LSP[7]	0	R/W	V_{IN} OVP Enable Bit 0 = OVP function is enabled (default) 1 = OVP function is disabled	
D[6]	LSP[6]	0	R	Reserved	
D[5]	LSP[5]	1	R/W	Input Current Limit Threshold 000 = 1.2A 001 = 2A 010 = 2.5A 011 = 3A 100 = 3.5A 101 = 4A 110 = 4.5A 111 = 6.2A (default)	
D[4]	LSP[4]	1	R/W		
D[3]	LSP[3]	1	R/W		
D[2]	LSP[2]	0	R	Reserved	
D[1]	LSP[1]	0	R	Reserved	
D[0]	LSP[0]	1	R/W	ENA Bit 0 = BLKFET is disabled 1 = BLKFET is enabled (default)	

REGISTER DESCRIPTION (continued)

REG0x02: DC/DC Converter Control Parameter Programming Register Address (reset = 0xC9)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	DCP[7]	1	R/W	C_{STR} Measurement Discharge Current 00 = 2mA 01 = 5mA 10 = 9.5mA 11 = 20mA (default)	
D[6]	DCP[6]	1	R/W		
D[5]	DCP[5]	0	R	Reserved	
D[4]	DCP[4]	0	R	Reserved	
D[3]	DCP[3]	1	R/W	Boost Peak Current 000 = 300mA 001 = 500mA 010 = 600mA 011 = 800mA 100 = 1A (default) 101 = 1.5A 110 = 2A 111 = 2.5A	
D[2]	DCP[2]	0	R/W		
D[1]	DCP[1]	0	R/W		
D[0]	DCP[0]	1	R/W	ENCON, DC/DC Converter Enable Bit 0 = DC/DC converter is disabled 1 = DC/DC converter is enabled (default)	

REG0x03: Buck-Off Voltage Programming Register Address (reset = 0x37)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	OFF[7]	0	R/W	Buck-Off Voltage Programming	Default: 0x37. V_{BUCK_OFF} = 2.64V V_{BUCK_OFF} = OFF[7:0] × 0.048V The V_{BUCK_OFF} program range is 2.64V to 12V. Example: If OFF[7:0] = 0x37, then $V_{BUCK\_OFF} = (3 \times 16^1 + 7 \times 16^0) \times 0.048 = 2.64V$.
D[6]	OFF[6]	0	R/W		
D[5]	OFF[5]	1	R/W		
D[4]	OFF[4]	1	R/W		
D[3]	OFF[3]	0	R/W		
D[2]	OFF[2]	1	R/W		
D[1]	OFF[1]	1	R/W		
D[0]	OFF[0]	1	R/W		

REG0x04: VDIS1 Programming Register Address (reset = 0xA6)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	VDIS1[7]	1	R/W	V_{DIS1} Threshold Programming (For C_{STR} measurement)	Default: 0xA6. V_{DIS1} = 24.9V V_{DIS1} = VDIS1[7:0] × 0.15V The V_{DIS1} voltage program range is 1.5V to 36V. Example: If VDIS1[7:0] = 0xA6, then $V_{DIS1} = (10 \times 16^1 + 6 \times 16^0) \times 0.15 = 24.9V$.
D[6]	VDIS1[6]	0	R/W		
D[5]	VDIS1[5]	1	R/W		
D[4]	VDIS1[4]	0	R/W		
D[3]	VDIS1[3]	0	R/W		
D[2]	VDIS1[2]	1	R/W		
D[1]	VDIS1[1]	1	R/W		
D[0]	VDIS1[0]	0	R/W		

REGISTER DESCRIPTION (continued)

REG0x05: VDIS2 Programming Register Address (reset = 0x8F)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	VDIS2[7]	1	R/W	V_{DIS2} Threshold Programming (For C_{STR} measurement)	Default: 0x8F. V_{DIS2} = 21.45V V_{DIS2} = VDIS2[7:0] × 0.15V The V_{DIS2} voltage program range is 1.5V to 36V. Example: If VDIS2[7:0] = 0x8F, then $V_{DIS2} = (8 \times 16^1 + 15 \times 16^0) \times 0.15 = 21.45V$.
D[6]	VDIS2[6]	0	R/W		
D[5]	VDIS2[5]	0	R/W		
D[4]	VDIS2[4]	0	R/W		
D[3]	VDIS2[3]	1	R/W		
D[2]	VDIS2[2]	1	R/W		
D[1]	VDIS2[1]	1	R/W		
D[0]	VDIS2[0]	1	R/W		

REG0x06: Switching Frequency, C_{STR} Measuring, Reverse Block and CV Mode Program Register Address (reset = 0x01)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	SF[7]	0	R	Reversed	
D[6]	SF[6]	0	R/W	Reverse Block Enable Bit 0 = BLKFET turns off once the reverse current exceeds 0.5A 1 = BLKFET unchanged if the reverse current exceeds 0.5A	
D[5]	SF[5]	0	R/W	C_{STR} Measurement Enable Default: 0	Capacitance measurement starts when SF[5] changes from 0 to 1.
D[4]	SF[4]	0	R/W	Boost Operation Mode 0 = CV mode (Default) 1 = Burst mode	In Burst mode, it is recommended to use a BST capacitor with a relatively small capacitance value to accelerate the recharge speed, such as 47nF.
D[3]	SF[3]	0	R/W	C_{STR} ESR Detection Threshold 00 = 50mV (default) 01 = 100mV 10 = 150mV 11 = 200mV	
D[2]	SF[2]	0	R/W		
D[1]	SF[1]	0	R/W	Switching Frequency 00 = 250kHz 01 = 500kHz (default) 10 = 1MHz 11 = 1.5MHz	
D[0]	SF[0]	1	R/W		

REG0x07: C_{STR} Discharge Timer High Byte Register Address (reset = 0x00)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	TIMH[7]	0	R	1 = 65536ms	Capacitor Discharge Timer Reading Range: 0 - 131070ms
D[6]	TIMH[6]	0	R	1 = 32768ms	
D[5]	TIMH[5]	0	R	1 = 16384ms	
D[4]	TIMH[4]	0	R	1 = 8192ms	
D[3]	TIMH[3]	0	R	1 = 4096ms	
D[2]	TIMH[2]	0	R	1 = 2048ms	
D[1]	TIMH[1]	0	R	1 = 1024ms	
D[0]	TIMH[0]	0	R	1 = 512ms	

REGISTER DESCRIPTION (continued)

REG0x08: C_{STR} Discharge Timer Low Byte Register Address (reset = 0x00)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	TIML[7]	0	R	1 = 256ms	Capacitor Discharge Timer Reading Range: 0 - 131070ms
D[6]	TIML[6]	0	R	1 = 128ms	
D[5]	TIML[5]	0	R	1 = 64ms	
D[4]	TIML[4]	0	R	1 = 32ms	
D[3]	TIML[3]	0	R	1 = 16ms	
D[2]	TIML[2]	0	R	1 = 8ms	
D[1]	TIML[1]	0	R	1 = 4ms	
D[0]	TIML[0]	0	R	1 = 2ms	

REG0x09: ADC I_{IN} Data and ESR Detection Status Register Address (reset = 0x00)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	LSC[7]	0	R	1 = 4.8A	Input Current ADC Results Reading Range: 0 - 9.45A 6 bits (0 - 63) × 0.15A resolution
D[6]	LSC[6]	0	R	1 = 2.4A	
D[5]	LSC[5]	0	R	1 = 1.2A	
D[4]	LSC[4]	0	R	1 = 0.6A	
D[3]	LSC[3]	0	R	1 = 0.3A	
D[2]	LSC[2]	0	R	1 = 0.15A	
D[1]	LSC[1]	0	R	Reserved	
D[0]	LSC[0]	0	R	Detected ESR Status (ESR_{CSTR}) 0 = ESR normal 1 = ESR error	Error is detected if the ΔV_{STR} (= ESR × I_{ESR}) is higher than the threshold set in SF[3:2] bits.

REG0x0A: ADC V_{BUS} Data Register Address (reset = 0x00)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	BUS[7]	0	R	1 = 8.192V	V_{BUS} ADC Results Reading Range: 0 - 16.32V 8 bits (0 - 255) × 64mV resolution
D[6]	BUS[6]	0	R	1 = 4.096V	
D[5]	BUS[5]	0	R	1 = 2.048V	
D[4]	BUS[4]	0	R	1 = 1.024V	
D[3]	BUS[3]	0	R	1 = 0.512V	
D[2]	BUS[2]	0	R	1 = 0.256V	
D[1]	BUS[1]	0	R	1 = 0.128V	
D[0]	BUS[0]	0	R	1 = 0.064V	

REG0x0B: STR Over-Voltage Protection Programming Register Address (reset = 0x1D)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	OVP[7]	0	R	Reserved	
D[6]	OVP[6]	0	R	Reserved	
D[5]	OVP[5]	0	R	Reserved	
D[4]	OVP[4]	1	R/W	V_{STR} OVP Threshold Programming	Default: 0x1D, V_{STROVP} = 36V The V_{STROVP} voltage program range is 7V to 38V. V_{STROVP} = OVP[4:0] × 1V+ 7V Example: if OVP[4:0] = 0x1D, then $V_{STROVP} = (1 \times 16^1 + 13 \times 16^0 + 7) \times 1 = 36V$.
D[3]	OVP[3]	1	R/W		
D[2]	OVP[2]	1	R/W		
D[1]	OVP[1]	0	R/W		
D[0]	OVP[0]	1	R/W		

REGISTER DESCRIPTION (continued)

REG0x0C: ADC V_{IN} Data Register Address (reset = 0x00)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	IN[7]	0	R	1 = 8.192V	V_{IN} ADC Results Reading Range: 0 - 16.32V 8 bits (0 - 255) × 64mV resolution
D[6]	IN[6]	0	R	1 = 4.096V	
D[5]	IN[5]	0	R	1 = 2.048V	
D[4]	IN[4]	0	R	1 = 1.024V	
D[3]	IN[3]	0	R	1 = 0.512V	
D[2]	IN[2]	0	R	1 = 0.256V	
D[1]	IN[1]	0	R	1 = 0.128V	
D[0]	IN[0]	0	R	1 = 0.064V	

REG0x0D: ADC V_{STR} Data Register Address (reset = 0x00)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	STR[7]	0	R	1 = 19.2V	V_{STR} ADC Results Reading Range: 0 - 38.25V 8 bits (0 - 255) × 0.15V resolution
D[6]	STR[6]	0	R	1 = 9.6V	
D[5]	STR[5]	0	R	1 = 4.8V	
D[4]	STR[4]	0	R	1 = 2.4V	
D[3]	STR[3]	0	R	1 = 1.2V	
D[2]	STR[2]	0	R	1 = 0.6V	
D[1]	STR[1]	0	R	1 = 0.3V	
D[0]	STR[0]	0	R	1 = 0.15V	

REG0x0E: Interrupt (INT Pin Output Signal) Mask Control Register Address (reset = 0x00)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
All		0	R/W	0 = event can assert interrupt 1 = event cannot interrupt but its flag bit is set	
D[7]	MASK[7]	0	R/W	Mask V_{IN} OVP Interrupt	If V_{IN} OVP function is enabled in LSP[7].
D[6]	MASK[6]	0	R/W	Mask Input OCP Interrupt	
D[5]	MASK[5]	0	R/W	Mask C_{STR} SCP Interrupt	
D[4]	MASK[4]	0	R/W	Mask Reverse Blocking Protection Interrupt	If the RB protection is enabled in SF[6].
D[3]	MASK[3]	0	R/W	Mask C_{STR} Measurement Complete Interrupt	Measuring starts if SF[5] rises from 0 to 1.
D[2]	MASK[2]	0	R/W	Mask ADC Complete Interrupt	ADC starts when SYS[7] rises from 0 to 1.
D[1]	MASK[1]	0	R/W	Mask High Junction Temperature Warning Interrupt	
D[0]	MASK[0]	0	R/W	Mask Thermal Shutdown Interrupt	

REGISTER DESCRIPTION (continued)

REG0x0F: Interrupt Flag Register Address (reset = 0x00)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
All		0	R/WC	0 = event has not occurred 1 = event has occurred To reset flag and interrupt, write 1 to the bit after the event is cleared.	
D[7]	FLAG[7]	0	R/WC	V_{IN} OVP Event Flag Bit (V_{IN} OVP exceeded)	If V_{IN} OVP function is enabled in LSP[7].
D[6]	FLAG[6]	0	R/WC	Input OCP Event Flag Bit (Input current limit exceeded)	
D[5]	FLAG[5]	0	R/WC	C_{STR} SCP Event Flag Bit (V_{STR} fell below the short-circuit threshold)	
D[4]	FLAG[4]	0	R/WC	Reverse Blocking Protection Event Flag Bit (BUS to IN current passed the reverse current threshold).	If the RB protection is enabled in SF[6].
D[3]	FLAG[3]	0	R/WC	C_{STR} Measurement Complete Event Flag Bit	Measuring starts if SF[5] rises from 0 to 1.
D[2]	FLAG[2]	0	R/WC	ADC Conversion Complete Event Flag Bit	ADC starts if SYS[7] rises from 0 to 1.
D[1]	FLAG[1]	0	R/WC	High Junction Temperature Warning Event Flag Bit (T_J > +125℃)	
D[0]	FLAG[0]	0	R/WC	Thermal Shutdown Event Flag Bit (T_J > +150℃)	

REG0x10: System Control Register Address (reset = 0x02)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	COMMENT
D[7]	SYS[7]	0	R/W	ADC Conversion Enable Default: 0	ADC starts if SYS[7] rises from 0 to 1.
D[6]	SYS[6]	0	R	Reserved	
D[5]	SYS[5]	0	R/W	Converter Mode After V_{IN} Recovery 0 = Run and continue in Buck mode until V_{STR} goes below V_{BUCK_OFF}. 1 = Exit Buck mode and charge C_{BUS} from V_{IN} (if already in Buck mode)	
D[4]	SYS[4]	0	R/W	After Detecting Thermal Shutdown 0 = Force to Buck mode 1 = Turn off all circuits immediately	
D[3]	SYS[3]	0	R/WC	V_{STR} OVP Flag Bit and Interrupt 0 = No V_{STR} OVP event occurred 1 = V_{STR} passed the V_{STROVP} threshold. An interrupt is asserted. To reset the flag and interrupt, write 1 to the bit after the event is cleared.	
D[2]	SYS[2]	0	R/WC	V_{BUS} Power Fail Flag Bit and Interrupt 0 = No V_{BUS} power fail event occurred 1 = V_{FBD} fell below V_{BUCK_DET} threshold. An interrupt is asserted. To reset the flag and interrupt, write 1 to the bit after the event is cleared.	
D[1]	SYS[1]	1	R	V_{IN} Power Good Flag Bit and Interrupt 0 = V_{IN} source not good. An interrupt is asserted. This flag is automatically set to 1 and interrupt is reset after a good V_{IN} is detected. 1 = Good V_{IN} source is detected	
D[0]	SYS[0]	0	R	BLKFET Status Flag Bit 0 = BLKFET is off 1 = BLKFET is on	

FUNCTIONAL BLOCK DIAGRAM

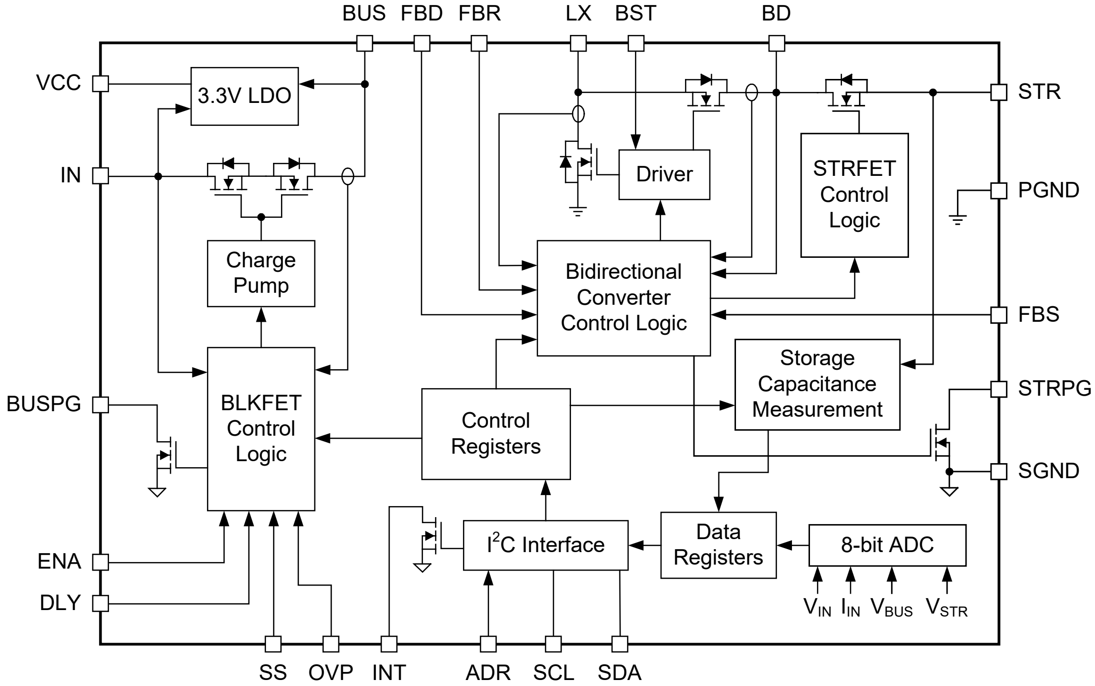


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM41664A is a cost effective power management device for applications that need power backup or energy storage. The stored energy can be delivered to system to complete urgent tasks if the input source has failed. For example, an SSD can complete its write after unexpected power removal. This device includes a synchronous bidirectional Buck converter that in the reverse direction (Boost) acts as an efficient charger for energy storage capacitors (STR) and in the forward direction (Buck) releases energy from the storage capacitors into the BUS. An I^2C interface and an ADC are also integrated for monitoring the parameters, system status and flexible device configuration.

The input power supply and the load (system) are connected to the input (IN) and the BUS, respectively. Normally, the source (IN) directly connects to the BUS through the integrated reverse blocking MOSFET (BLKFET). The BUS is linked to the storage capacitors on the STR pin through the bidirectional DC/DC converter BD port and a disconnecting switch (STRFET). When V_{IN} is normal, the STR capacitors are kept charged at a high voltage level using the bidirectional converter in Boost mode. In case of a sudden source shutdown like V_{IN} removal, the converter acts in Buck mode and discharges the backup capacitors to the BUS to hold the V_{BUS} voltage up and disconnects the BLKFET to avoid leaking energy to the failed input.

Startup Sequence

The startup has several steps. It is started when the V_{IN} exceeds the 2.5V threshold. The internal LDO and bias circuits are turned on and the I^2C interface is initialized for communication. All 17 registers will also reset to their default values. If the input voltage drops below 2.4V, the LDO, bias circuits and I^2C interface will be turned off.

The host can access the registers after the power-on reset (POR) is completed. POR has 3 steps for input:

1. LDO (VCC) Power up.
2. Poor Source Qualification.
3. Turning BLKFET on to connect V_{IN} to BUS.

To allow BLKFET turn-on, the source voltage and current supply capabilities must qualify the following criteria:

1. $V_{IN} > V_{PORR}$ when pulling 20mA for a period of t_{DLY}.
2. $V_{IN} < V_{OVP}$.

DETAILED DESCRIPTION (continued)

V_{OVP} and V_{PORR} are programmed by strapping OVP to SGND, IN or leaving OVP floating, depending on the application input voltage (3.3V, 5V or 12V). If an OVP fault is detected ($V_{IN} > V_{OVP}$), the device waits until this condition is cleared and then recovers automatically. If a poor source is detected (condition1), the source qualification routine is repeated every 300ms.

After input qualification for t_{DLY}, the BLKFET turn-on process starts if $V_{IN} > V_{BUS}$ and both ENA pin and ENA bit are set, that is:

1. External ENA = H (ENA pin is pulled high).
2. Internal ENA bit is set, LSP[0] = 1 (default).
3. $V_{IN} > V_{BUS}$.

If all above conditions are valid, the BLKFET gradually turns on and charges the BUS capacitors from 0V to V_{IN} with a controlled rate (soft-start, t_{SS}). The soft-start time is set by the C_{SS} capacitor on the SS pin and the input current limit is set by LSP[5:3] bits. When the SS pin voltage reaches 1.4V, the Boost converter can be enabled by the DCP[0] bit for charging the backup capacitors. The capacitor on the BD pin is also charged during the soft-start period.

After the soft-start time, if the converter-enable bit DCP[0] is set, the pre-charge period will start when $V_{FBR} > 0.635V$. In this period, the Boost output (BD voltage) is regulated in the range of 120% to 135% of the V_{BUS} and the STR capacitors are charged with a pre-charge current near 150mA. The pre-charge period ends when the STRFET voltage (between BD and STR) is almost 0V. At this time the STRFET is fully turned on and the Boost converter starts to regulate the FBS voltage.

The DLY pin is provided to set t_{DLY}. If it is floating, the t_{DLY} is about 1ms. If a capacitor (C_{DLY}) is connected to DLY pin, it will be charged with a 4μA current source and the time between 0V and 1V determines the t_{DLY} time, estimated by Equation 1:

$$t_{DLY}\ (\text{ms}) = \frac{C_{DLY}(\text{nF}) \times 1\text{V}}{4\mu\text{A}} \tag{1}$$

After the t_{DLY} time, the V_{BUS} soft-start time (t_{SS}) begins. The SS pin programs this time. If the SS pin is left floating, t_{SS} is about 1ms. If a capacitor (C_{SS}) is connected to the SS pin, it will be charged by a 8.5μA current source and the time between 0V and 1.4V determines the t_{SS} time, estimated by Equation 2:

$$t_{SS}\ (\text{ms}) = \frac{C_{SS}(\text{nF}) \times 1.4\text{V}}{8.5\mu\text{A}} \tag{2}$$

Converter Control in Charger Mode (Boost)

After completing the BLKFET soft-start, and $V_{FBR} > 0.635V$, the bidirectional converter starts to operate as a Boost charger with constant off-time peak current control. The peak is programmed in the DCP[3:1] bits through the I^2C interface.

At the beginning of each cycle in Boost mode, the low-side MOSFET (LSFET) is turned on and the inductor current starts to rise until it reaches the programmed peak value. At this point the LSFET turns off and HSFET turns on. The inductor current starts to decrease while flowing through the STRFET to the STR capacitor. After a fixed off time, the LSFET is turned on again and the next cycle starts. The STR voltage is set by the divider resistor connected to the FBS feedback pin.

The Boost operation can be set to the high efficiency burst mode (SF[4] = 1) or the low-ripple constant voltage (CV) mode (SF[4] = 0). In burst mode, the Boost charger stops switching when the FBS voltage reaches 1.2V and starts again when it falls below 1.17V. In CV mode, the LSFET turns on for a new cycle only if the V_{FBS} is below the 1.205V reference. Otherwise, it remains off until V_{FBS} falls below 1.205V.

The default peak current for Boost mode is set to 1A (DCP[3:1] bits = 100) but it can be programmed to 7 other values between 0.3A and 2.5A. The SGM41664A also includes current foldback to help fully charge the STR capacitor. When V_{STR} rises above 58% of its nominal output level, the peak current is stepped down from its setting value I_{BT_PEAK} to min (600mA, I_{BT_PEAK}). Taking 1.5A for I_{BT_PEAK} as an example, the actual peak current limit is shown in Figure 3, so that the STR capacitor can be fully charged till V_{STR} reaches its intended level with only a minute current flowing into the capacitor, which means the voltage drop across the internal ESR is negligible. If the Boost switching peak current is programmed lower than 0.8A (0.3A, 0.5A or 0.6A), the HSFET will not turn on in the off-time (only the body diode conducts) to reduce the negative peak current of the inductor. Even for the peak currents above 0.8A, the inductor current can go negative due to the minimum on-time of the HSFET that may result in the STR voltage not reaching the programmed voltage at high conversion ratios. Therefore, higher peak currents ($I_{PEAK} > \Delta I_L/2$) are recommended. The typical t_{ON_MIN} for the HSFET is 110ns. The following equation can be used to choose the proper Boost peak current setting.

$$I_{PEAK}(\text{A}) \geq \frac{V_{STR}(\text{V}) - V_{IN}(\text{V})}{2 \times L(\mu\text{H})} \times 110(\text{ns}) \tag{3}$$

DETAILED DESCRIPTION (continued)

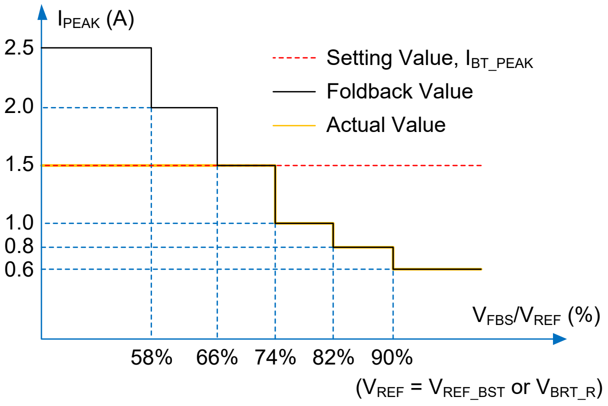


Figure 3. Boost Mode Peak Current Limit Foldback

Converter Control in Buck Mode

After completing the BLKFET soft-start and the IC is in normal operation, the Buck mode is activated as soon as a significant V_{BUS} drop is detected (V_{FBD} falling below 0.605V) to use the backup energy. Upon detection of $V_{FBD} < 0.605V$, the converter starts operating as a Buck and the BLKFET is turned off to block negative current from V_{BUS} to V_{IN}. The SYS[0] is also set to 0 to show the BLKFET shutdown status. In Buck mode, the energy stored in the STR capacitors is transferred to the BUS capacitors using a quasi-fixed frequency constant off-time control scheme for faster response. In Buck mode, the BUS regulation voltage is set by FBR pin. The maximum peak current in Buck mode is internally clamped to 8.4A. When the STR voltage falls below the Buck-off threshold (V_{BUCK_OFF}) programmed in OFF[7:0] bits, switching stops and the Buck shuts down. The detailed shutdown process waveforms and transfer of the stored energy to the BUS after an unexpected input removal is shown in Figure 4.

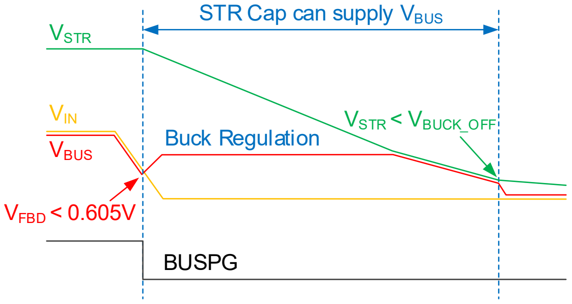


Figure 4. Use of Backup Energy to Keep the System Powered for a Short Time before Shutdown after an Unexpected Input Removal

Startup after Input Recovery

SYS[5] bit can be used to select the recovery mode when V_{IN} returns to normal. If SYS[5] = 0, after input recovery, the converter temporarily continues in Buck mode to discharge any remaining charge in the STR capacitor and waits for V_{STR} to drop below V_{BUCK_OFF}. Then a new startup sequence with POR will start.

If SYS[5] = 1, the source qualification is performed if $V_{IN} > V_{PORR}$. After qualification, the V_{IN} power good flag (SYS[1]) is set to 1 and the SGM41664A fully turns on BLKFET again and exits Buck converter mode if all of the following conditions are true, even though the interrupt signal is not cleared.

1. ENA pin = H (pulled high).
2. ENA bit (LSP[0]) = 1.
3. $V_{BUS} < V_{IN} < V_{OVP}$.
4. $V_{BUS} > V_{BUCK\_DET}$.
5. $T_J < +125$℃ (thermal shutdown occurred) or $T_J < +150$℃ (thermal shutdown not occurred).

The input POR falling/rising thresholds (V_{PORF}/V_{PORR}) and the input OVP threshold (V_{OVP} and V_{OVPHYS}) are set by strapping the OVP pin (SGND, IN or floating).

Control of the Reverse Blocking FET

The BLKFET unit controls the input current limiting, over-voltage (OV) protection and reverse blocking (RB) functions. If any of the following 8 conditions occurs, the BLKFET is softly turned off, the SYS[0] bit is set to 0, and the converter enters Buck mode:

1. V_{IN} voltage falls below V_{PORF}.
2. ENA bit (LSP[0]) = 0 or ENA pin = L (pulled low).
3. V_{FBD} falls below 0.605V.
4. Reverse current from BUS to IN exceeds 500mA if reverse block enable bit (SF[6]) is 0.
5. Input OV triggers if V_{IN} OVP enable bit (LSP[7]) is 0.
6. Input current exceeds I_{LIM} threshold.
7. Thermal shutdown is detected if thermal shutdown mode setting bit SYS[4] is 0.
8. Converter operates in Buck mode.

Device Enable and Disable

The ENA pin and the ENA bit (LSP[0]) can enable or disable the device. The internal circuits are enabled if both of them are high. It is recommended to pull up the ENA pin by a 100kΩ resistor to IN pin.

DETAILED DESCRIPTION (continued)

VCC Output

The internal circuits are powered from the LDO that is supplied from the higher of V_{IN} or V_{BUS}. A 2.2μF or larger ceramic capacitor is required on the LDO output (VCC pin) for decoupling. The normal VCC voltage is 3.3V. If the device is powered from a 3.3V or lower source, the VCC will follow V_{IN} due to the required headroom. In this condition, any external loading on VCC such as a small BUSPG pull-up resistor can pull the VCC down and cause startup issues. Therefore, use 100kΩ pull-up resistors for BUSPG, STRPG and INT or pull them up to the BUS pin instead, if V_{BUS} is 5V or less.

BUS Power Good (BUSPG)

The BUSPG is an open-drain output pin with 4mA pull-down capability. If V_{FBD} drops below 0.605V or V_{IN} drops below V_{PORF} or V_{IN} OVP is triggered, the BUSPG is pulled low. When V_{FBR} exceeds 0.635V, it is released to go high. Pull the BUSPG up with a 100kΩ resistor to BUS (if $V_{BUS} \le 5V$) or VCC.

STR Power Good (STRPG)

The STRPG is an open-drain output pin with 4mA pull-down capability. If V_{FBS} pin falls below 1V, the STRPG is pulled low and when V_{FBS} exceeds 1.04V, it is released to go high. Pull the STRPG up with a 100kΩ resistor to BUS (if $V_{BUS} \le 5V$) or VCC.

Internal ADC

An integrated 8-bit analog-to-digital converter (ADC) can measure the V_{IN}, I_{IN}, V_{BUS} and V_{STR}. The A/D conversion is started by setting the SYS[7] bit from 0 to 1. When the conversions are complete, the FLAG[2] bit is set to 1. An interrupt signal is also asserted if it is not masked.

See the ADC register descriptions for details.

The SGM41664A enters Buck mode as soon as any of the following events occurs during the A/D conversion:

1. V_{IN} drops below V_{PORF}.
2. Disabling the device (LSP[0] = 0 or ENA pulled low).
3. V_{FBD} falls below 0.605V.
4. Input OVP event (if V_{IN} OVP is enabled, LSP[7] = 0).
5. I_{IN} exceeds I_{LIM} threshold.
6. BUS to IN reverse current exceeds 500mA (if the reverse block is enabled, SF[6] = 0).
7. Thermal shutdown (if the thermal shutdown mode setting bit, SYS[4], is 0).

Measuring the Storage Capacitor

The SGM41664A can measure the C_{STR} capacitance and ESR by two internal current sinks as shown in Figure 5. The ESR detection current (I_{ESR}) is almost 1A, and the C_{STR} detection current (I_{DIS}) can be set to 2mA, 5mA, 9.5mA or 20mA (default) by DCP[7:6] bits. The measuring steps are as follows with ESR measured first:

1. The C_{STR} measurement-complete-interrupt bit must be unmasked by setting MASK[3] to 0.
2. The host initiates the measurement by writing a 0 to 1 transition in the SF[5] bit.
3. C_{STR} is charged until V_{FBS} reaches 1.2V.
4. C_{STR} is discharged by I_{ESR} for 15μs and V_{STR} is measured just before and after turning I_{ESR} off. The voltage difference will be equal to ESR × I_{ESR}.
5. If the difference is higher than the programmed ESR detection threshold set by SF[3:2] bits, an ESR error is identified and the LSC[0] is set to 1. See Figure 6 for the ESR detection process.

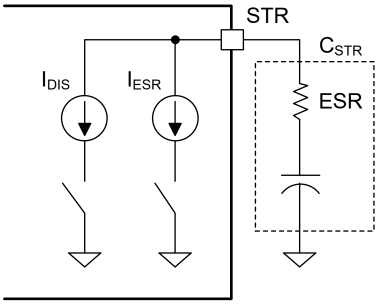


Figure 5. Capacitance and ESR Measuring Circuit

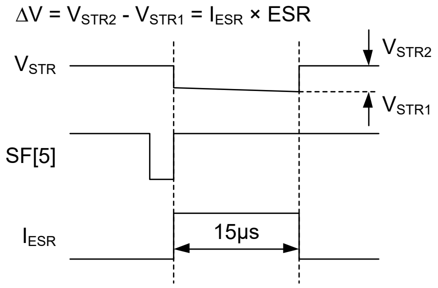


Figure 6. ESR Measurement Process

6. After completing the ESR detection, the I_{DIS} current sink is turned on to discharge C_{STR}.
7. After completing the measurement, Boost charging function is restarted automatically and FLAG[3] is set to 1. An interrupt is also asserted if it is unmasked.

DETAILED DESCRIPTION (continued)

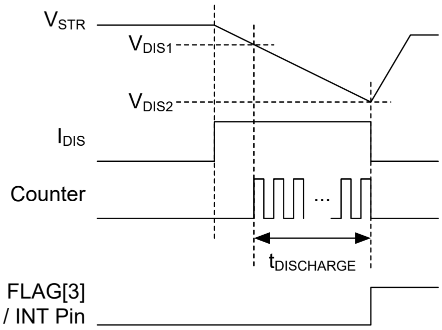


Figure 7. Measuring Capacitance with 500kHz Counter

8. To reset the FLAG[3], a ‘1’ must be written to it.
9. $t_{DISCHARGE}$ is read from the registers REG0x07 and REG0x08 to calculate the C_{STR} from Equation 4:

$$C_{STR}=\frac{I_{DIS}\times t_{DISCHARGE}}{V_{DIS1}-V_{DIS2}} \tag{4}$$

For example, if REG0x07 = 01h and REG0x08 = 23h, then $t_{DISCHARGE}$ = 291 (0123h) × 2 = 582ms. If V_{DIS1} = 24.9V, V_{DIS2} = 21.45V and I_{DIS} = 20mA, The C_{STR} will be 3374μF:

$$C_{STR}=\frac{I_{DIS}t_{DISCHARGE}}{V_{DIS1}-V_{DIS2}}=\frac{20\text{mA}\times 582\text{ms}}{24.9\text{V}-21.45\text{V}}=3374\mu\text{F}$$

V_{DIS1} and V_{DIS2} must be larger than V_{IN}.

The device will switch to Buck mode if any of the following events occurs during measurement. The STR capacitor cannot be measured in Buck mode.

1. V_{IN} drops below V_{PORF}.
2. Disabling the device (LSP[0] = 0 or ENA pulled low).
3. V_{FBD} falls below 0.605V.
4. Input OVP (if V_{IN} OVP is enabled, LSP[7] = 0).
5. I_{IN} exceeds I_{LIM} threshold.
6. BUS to IN reverse current exceeds 500mA (if the reverse block is enabled, SF[6] = 0).
7. Thermal shutdown (if the thermal shutdown mode setting bit, SYS[4], is 0.)

Interrupt and Event Sequence Control

The INT pin is an open-drain output. A 100kΩ pull-up resistor to BUS pin (if $V_{BUS} \leq 5V$) or VCC is recommended. It goes high if a fault condition occurs and is not masked. The interrupt informs the host that a fault has occurred. The INT remains high until it is reset by the host. If a new interrupt occurs before reset, it remains high until all events are reset by the host as shown in Figure 8.

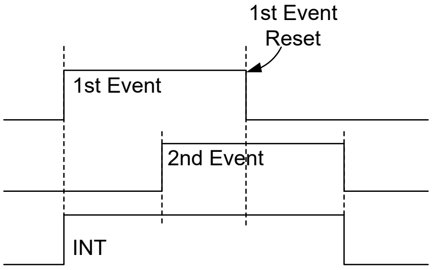


Figure 8. Interrupt Control Sequence

Table 1 summarizes the fault events and the actions that happen after their interrupts.

Input Over-Voltage Protection (OVP)

The OVP pin can be tied to SGND, IN, or left floating to select one of the 3 input OVP thresholds (V_{OVP}). Refer to the PIN DESCRIPTION table for details.

If the V_{IN} OVP detection is enabled (LSP[7] = 0), then a V_{IN} OVP fault is detected when V_{IN} exceeds the V_{OVP} threshold. Upon OVP detection, the BLKFET is turned off and the Buck converter starts to operate to maintain the V_{BUS} power from the stored energy in the STR capacitor. FLAG[7] holds the V_{IN} OVP status until it is reset by the host. The OVP asserts an interrupt if it is not masked and BUSPG is pulled low. When Buck mode is finished, a new startup sequence with POR will start.

Input Over Current Protection (OCP)

The input current limit controls the current that flows through the BLKFET, and thus it avoids inrush current from IN to BUS. The SS external capacitor sets the soft-start time to control the charge rate of the BUS capacitors and limits the inrush current. The input current limit is set by LSP[5:3] bits. When the input is qualified, the current starts to ramp from 0A and is kept below the programmed input current limit during the soft-start time.

If the I_{IN} reaches the OCP threshold, the BLKFET is turned off and the Buck converter starts to maintain V_{BUS} from the storage capacitors. An interrupt is asserted if it is not masked and the input OCP event flag (FLAG[6]) is set to record the OCP event status. When Buck mode is finished, a new startup sequence with POR will start.

DETAILED DESCRIPTION (continued)

BUS and STR Short-Circuit Protection (SCP)

If a short-circuit happens on the BUS during normal operation, the BLKFET will shut down immediately and the converter enters Buck mode to discharge the storage capacitor with maximum peak current. The BUS power fail event flag (SYS[2]) is also set to record the event and an interrupt is asserted.

If a BUS short-circuit occurs before POR is completed, while V_{BUS} is below 90% of V_{IN} and soft-start time is completed, the BLKFET is turned off and an interrupt signal is asserted. The SYS[2] flag is also set to record the event. Then the BLKFET waits for $8 \times t_{SS}$ before a new soft-start begins automatically.

STR voltage is continuously checked from 56ms after the pre-charge process begins. In the pre-charge period, an STR short-circuit is identified, if V_{STR} cannot exceed 0.7V. Upon detection of an STR short, the STRFET is turned off and the converter stops switching. Also, the C_{STR} SCP event flag (FLAG[5]) is set to record the SCP event and an interrupt is asserted (if not masked). After an STR short, the converter latches off and a new power-on cycle (and POR) will automatically restart.

During the fast charge period, an STR short event is identified if the V_{STR} drops below 0.7V or V_{BUS} - 0.2V. When the converter is in Buck mode, the STR to BUS voltage drop detection is disabled.

Reverse Blocking Protection (RBP)

The BLKFET reverse blocking protection is activated when the current from BUS to VIN reaches 500mA if the reverse block enable bit, SF[6], is set to 0. The BLKFET is also turned off and the Buck converter starts to maintain V_{BUS}. The SYS[0] bit is also set to 0 to record the BLKFET shutdown status and the RBP flag, FLAG[4], is set to record this event. An interrupt is also asserted if it is not masked. RBP is disabled if SF[6] = 1. When Buck mode is finished, a new startup sequence with POR will start.

STR Over-Voltage Protection (STR OVP)

When V_{STR} exceeds the threshold set by OVP[4:0] bits, an STR OVP occurs and the Boost charger stops switching. The STR OVP event flag, SYS[3], is set and an interrupt is asserted. The Boost charger is restarted when the V_{STR} drops 1V below the STR OVP threshold.

Thermal Warning and Shutdown

A thermal warning feature is implemented in the device to avoid thermal runaway. If the die temperature (T_J) exceeds +125℃, the high T_J warning flag (FLAG[1]) is set to 1 and an interrupt is asserted (if it is not masked). Writing a 1 to this bit resets the interrupt after T_J falls below +100℃.

Similarly, if the junction temperature reaches +150℃, the thermal shutdown bit (FLAG[0]) is set to 1 and an interrupt is asserted if it is unmasked.

Two thermal shutdown response types can be selected by SYS[4] bit. If SYS[4] = 1, all circuits will turn off immediately. If SYS[4] = 0, the device is forced into Buck mode with BLKFET in off state and discharges the C_{STR} into C_{BUS} until V_{STR} falls below V_{BUCK_OFF} and the Buck is turned off. The device will recover automatically when T_J falls below +125℃ similar to a V_{IN} recovery. Writing 1 to the FLAG[0] resets the interrupt after T_J drops below +125℃. If the junction temperature rises to +165℃, all circuits will turn off.

Default Register Values

All control registers have a fixed default value that is loaded after power-on reset. They can be modified after power-on through the I^2C interface and by the host to meet the system requirements. The device I^2C address can be set by the ADR pin. Refer to the PIN DESCRIPTION table for more details.

DETAILED DESCRIPTION (continued)

Table 1. Fault Events and Responses

Event	Flag Bit	Indicator(s)	Power Action After Event
Input Over Voltage	V_{IN} OVP Flag FLAG[7] bit	INT pin goes high BUSPG pin goes low	V_{IN} OVP is enabled by LSP[7] bit. BLKFET turns off and IC enters Buck mode.
Input Over Current	Input OCP Flag FLAG[6] bit	INT pin goes high	BLKFET turns off. IC enters Buck mode.
C_{STR} Short Circuit	C_{STR} SCP Flag FLAG[5] bit	INT pin goes high STRPG pin goes low	STRFET turns off. Converter switching stops.
Reverse Current (From BUS to IN)	Reverse Blocking Protection Flag FLAG[4] bit	INT pin goes high	Reverse blocking protection is enabled by SF[6] bit. BLKFET turns off and IC enters Buck mode.
C_{STR} Measurement Complete	C_{STR} Measurement Complete Flag FLAG[3] bit	INT pin goes high	No action
ADC Complete	ADC Conversion Complete Flag FLAG[2] bit	INT pin goes high	No action.
Junction High Temperature	High T_J Warning Flag FLAG[1] bit	INT pin goes high	No action.
Junction Over Temperature	Thermal Shutdown Flag FLAG[0] bit	INT pin goes high	BLKFET turns off. If SYS[4] is 0, IC enters Buck mode. Otherwise all circuits are turned off.
V_{STR} Over Voltage	V_{STR} OVP Flag SYS[3] bit	INT pin goes high	Converter stops switching.
V_{BUS} Power Fail	V_{BUS} Power Fail Flag SYS[2] bit	INT pin goes high BUSPG pin goes low	BLKFET turns off. IC enters Buck mode.
V_{IN} Power Fail	V_{IN} Power Fail Flag SYS[1] bit	INT pin goes high BUSPG pin goes low	BLKFET turns off. IC enters Buck mode.

APPLICATION INFORMATION

Selecting Feedback Resistors

The SGM41664A enters Buck mode and regulates the BUS voltage at V_{BUS_REG} when V_{BUS} falls below V_{BUS_DET} as shown in Figure 9. The BUSPG output will be low in Buck mode. Figure 10 shows how the V_{BUS_DET} and V_{BUS_REG} values can be adjusted by R_1 - R_2 and R_3 - R_4 resistor dividers, respectively. It is recommended to set V_{BUS_DET} lower than V_{BUS_REG}.

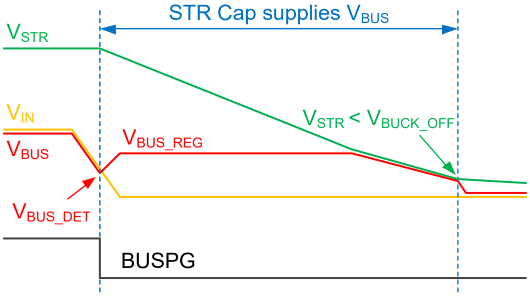


Figure 9. Buck Mode Waveforms

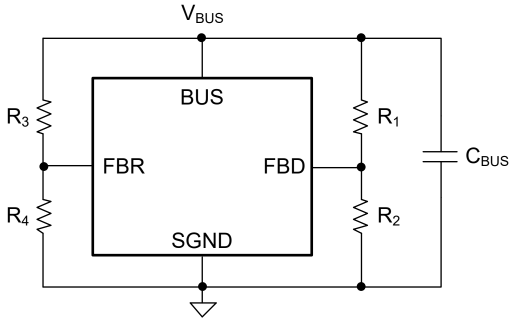


Figure 10. V_{BUS} Feedback Resistors

It is recommended to choose 1% precision resistors for R_1, R_2, R_3 and R_4 in the 10kΩ to 1MΩ range to minimize the loss and for good light load efficiency. Equations 5 and 6 can be used to select the resistors.

$$V_{BUS\_DET} = \frac{R_1 + R_2}{R_2} \times 0.605V \tag{5}$$

$$V_{BUS\_REG} = \frac{R_3 + R_4}{R_4} \times 0.61V \tag{6}$$

The Boost charger stops working in burst mode, when V_{FBS} exceeds 1.2V and restarts again when V_{FBS} falls below 1.17V. Figure 11 shows how R_5 and R_6 set the maximum voltage (V_{STR_MAX}) in burst mode. 1% resistors in the 10kΩ to 1MΩ range are recommended for R_5 and R_6. Use Equation 7 to select R_5 and R_6.

$$V_{STR\_MAX} = \frac{R_5 + R_6}{R_6} \times 1.2V \tag{7}$$

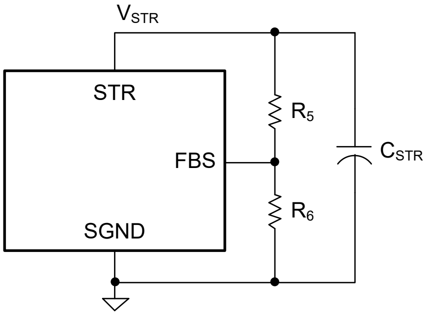


Figure 11. V_{STR} Feedback Resistor Divider

If the Boost charger operates in CV mode, Equation 8 can be used to set the desired V_{STR}.

$$V_{STR} = \frac{R_5 + R_6}{R_6} \times 1.205V \tag{8}$$

Input Capacitor Selection (C_{IN})

Two factors are considered for selecting C_{IN}:

1. It should tolerate the maximum input surge voltage with adequate margin.
2. The input peak current should be minimized to reduce the input noise. An extra 0.1μF or larger low ESR ceramic capacitor must be placed close to the IN pin for bypass.

The ceramic capacitors DC bias derating must be considered. Choose the X5R, X7R or better dielectrics for better DC bias and temperature stability. The DC bias effect is more significant for smaller sizes and choosing the largest possible size such as 1206 or 1210 is recommended. Consider a large margin for the voltage rating to cover the worst-case transients.

BUS Capacitor Selection (C_{BUS})

The C_{BUS} is the input capacitor of the Boost charger and also the output capacitor of the converter in Buck mode. The main factor for C_{BUS} selection is the stability of the control loop. Low ESR capacitors must be chosen for low ripple and small load step voltage transients.

For most applications, a 66μF or larger X5R or higher grade ceramic capacitor provides stable performance. Consider the actual capacitance value after bias voltage and temperature deratings.

APPLICATION INFORMATION (continued)

BD Capacitor Selection (C_{BD})

The C_{BD} stores energy during Boost pre-charge and releases that into C_{STR} when $V_{STR} < V_{BD}$. It is also the input port of the Buck converter. A 2.2μF or larger low ESR ceramic capacitor is recommended for decoupling of the BD pin to PGND. Consider at least 20% higher voltage margin above the targeted storage voltage after capacitance derating.

STR Capacitor Selection (C_{STR})

The STR capacitor stores energy from V_{IN} during normal operation and releases it to the C_{BUS} when V_{IN} is lost. A general purpose electrolytic or a low profile POS capacitor is satisfactory in most applications. Consider 20% or more margin for the rated voltage. An additional 0.1μF or larger low ESR ceramic capacitor close to STR pin is necessary for decoupling. The C_{STR} bulk value is designed based on the required hold time for the application. The required storage capacitance can be calculated from Equation 9:

$$C_{STR} = \frac{2 \times V_{BUS\_REG} \times I_{BUS} \times t_{HOLD}}{\eta \times \left(V_{STR}^2 - V_{BUS\_REG}^2\right)} \quad (9)$$

I_{BUS} is the BUS required current when it is regulated at V_{BUS_REG}.

V_{STR} is the storage voltage.

t_{HOLD} is the required hold time.

η is the energy-releasing efficiency of the Buck mode.Consider the converter losses for C_{STR} design.For example, if I_{BUS} = 3A, t_{HOLD} = 20ms, V_{STR} = 28V, V_{BUS_REG} = 7.5V, and η = 90%, then C_{STR} (bulk) = 1374μF.

Inductor Selection (L)

An inductor is necessary for the bidirectional DC/DC converter. Since the Buck mode current is higher, the inductor is designed for the Buck mode. If the maximum storage voltage is V_{STR_MAX}, the BUS regulation voltage is V_{BUS_REG} and the Buck switching frequency is f_{SW}. The inductance is given by Equation 10:

$$L = \frac{V_{BUS\_REG}}{\Delta I_L f_{SW}} \left(1 - \frac{V_{BUS\_REG}}{V_{STR\_MAX}}\right) \quad (10)$$

where ΔI_L is the peak-to-peak inductor ripple current and is typically selected between 20% and 40% of the full load current. The inductor saturation current should be higher than the inductor peak current with some margin.

Bootstrap Capacitor (C_{BST})

A bootstrap capacitor C_{BST} is needed for upper switch gate driver. A 0.1μF low ESR ceramic capacitor is recommended between BST and LX pins.

Power-On Reset Delay Time

A 10nF or larger capacitor connected to the DLY pin sets the power-on reset delay time. If the DLY pin is left floating, a default delay, around 1.0ms will be applied. Table 2 lists the recommended capacitor values and the corresponding delay time.

Table 2. Recommended C_{DLY} values for POR Delay t_{DLY}

C_{DLY} (nF)	None	10	47	100
t_{DLY} (ms)	1.0	2.5	11.8	25.0

BLKFET Soft-Start Time

A 10nF or larger capacitor connected to SS pin sets the BLKFET soft-start time. If the SS pin is left floating, a 1ms default delay will apply. Table 3 lists the recommended capacitor values and the corresponding soft-start time.

Table 3. Recommended C_{SS} Values and Soft-Start Time

C_{SS} (nF)	None	10	47	100
t_{SS} (ms)	1.0	1.7	7.7	16.5

PCB Layout Guidelines

A good PCB layout is critical for a stable design. Follow the following guidelines to design a good layout for SGM41664A.

1. Use short, wide, and direct traces for high-current connections (IN, BUS, LX, BD, STR and PGND).
2. Keep the switching node (LX) trace short and away from BUS and feedback network traces.
3. Use decoupling capacitors close to the BUS and PGND pins.
4. Use decoupling capacitors close to the STR and PGND pins. If a bulk capacitor is used, add an additional 1μF ceramic capacitor or larger value as close as possible to the STR and PGND pins.
5. Use decoupling capacitors close to the VCC and AGND pins.
6. Place the feedback resistors close to the feedback pins that are sensitive to noise (FBD/FBR/FBS).
7. Keep the BST trace as short as possible to the device.
8. Connect all signal grounds together and connect them at only one point to the PGND.

APPLICATION INFORMATION (continued)

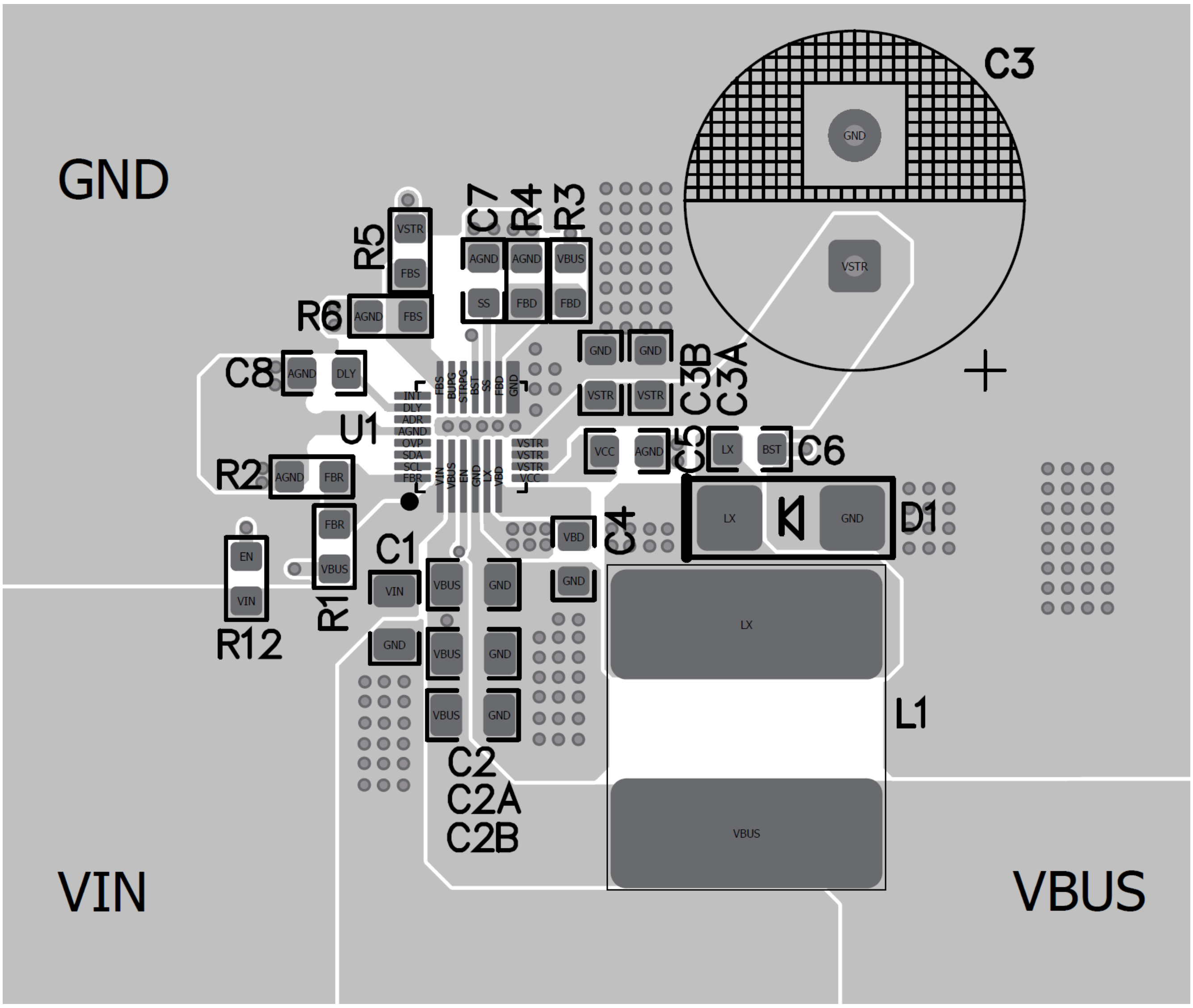


Figure 12. PCB Layout Guide

TYPICAL APPLICATION CIRCUIT

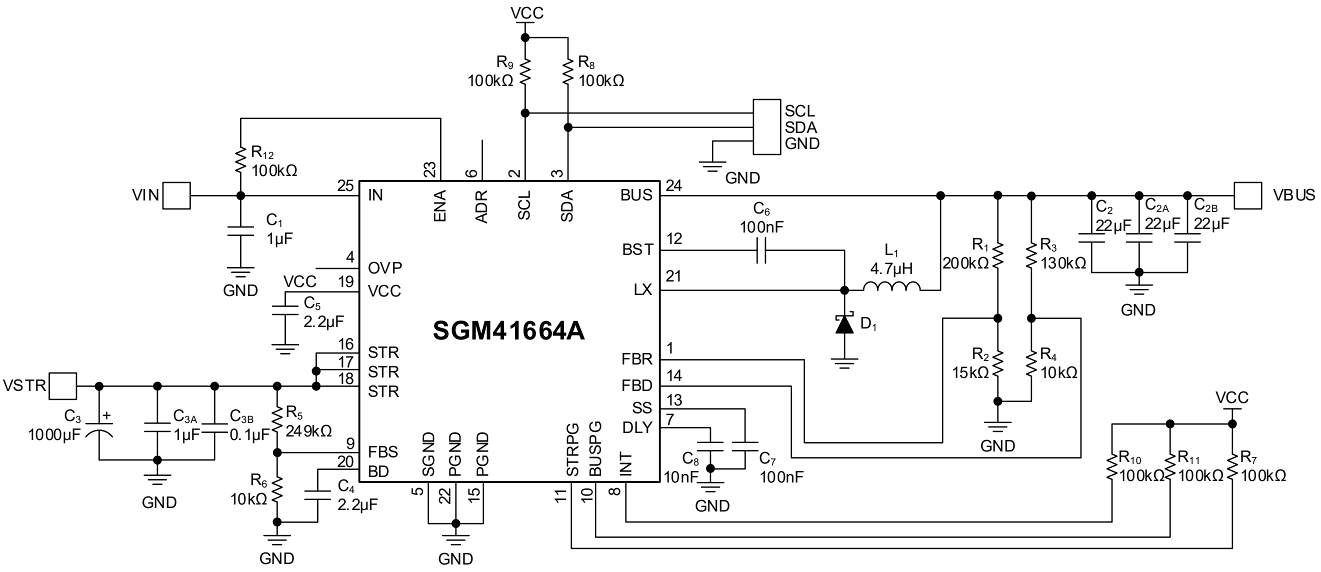


Figure 13. A Typical Power Backup Application Circuit with 12V Input and 31V Storage Voltage

Table 4 is a design example following the application information.

Table 4. Design Example

Input Voltage (V)	Buck Regulation Voltage (V)	Buck Detection Voltage (V)	Buck Output Current (A)	Storage Voltage (V)	L_1 (μH)	
					MIN	TYP
3.3	2.9	2.7	0 - 5	31	2.2	3.3
5	3.6	3.4	0 - 5	31	3.3	4.7
12	8.7	8.5	0 - 5	31	4.7	4.7

See Figure 13 for a detailed 12V application schematic. The waveforms are shown in the Typical Performance Characteristics section.

REVISION HISTORY

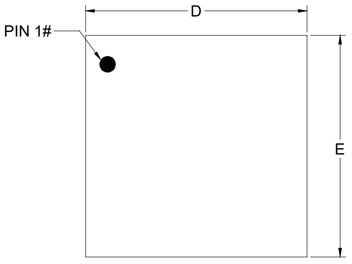
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

MARCH 2025 – REV.A to REV.A.1	Page
Updated Package/Ordering Information section	2
Changed I_{DIS} value at DCP[7:6] = 10	6, 13, 21

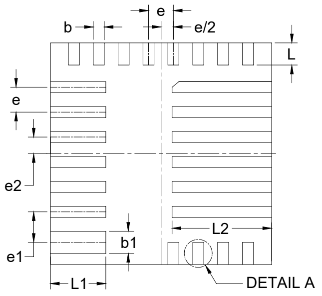
Changes from Original (AUGUST 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

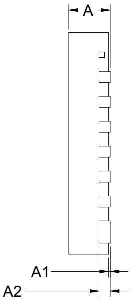
TQFN-4×4-25L



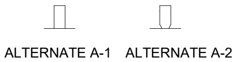
TOP VIEW



BOTTOM VIEW

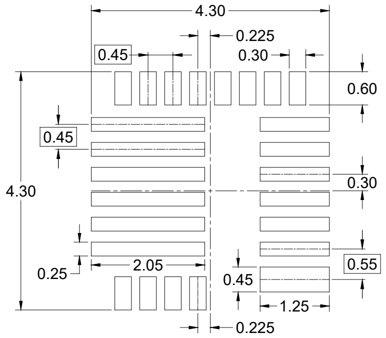


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



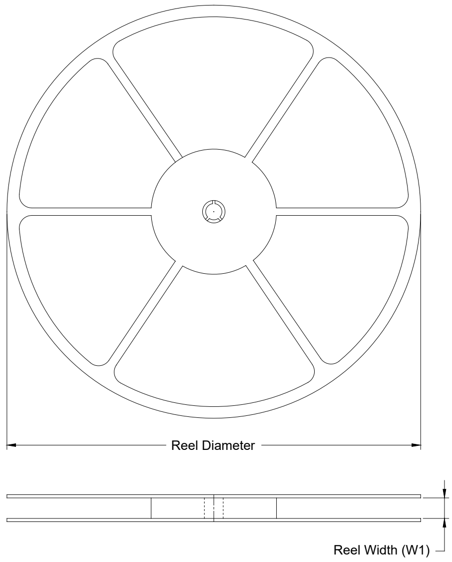
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	**NOM**	**MAX**
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A2	0.203 REF		
b	0.150	0.200	0.250
b1	0.350	0.400	0.450
D	4.000 BSC		
E	4.000 BSC		
e	0.450 BSC		
e1	0.550 BSC		
e2	0.300 BSC		
L	0.300	0.400	0.500
L1	0.900	1.000	1.100
L2	1.700	1.800	1.900

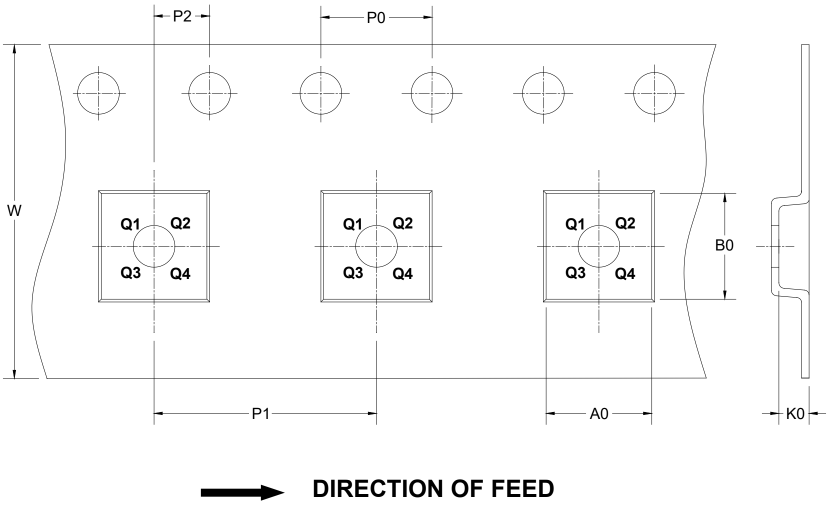
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



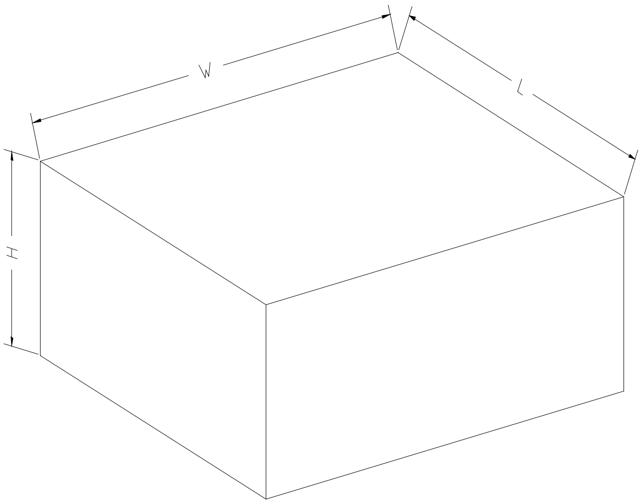
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-25L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002