



# SGM41604

## I<sup>2</sup>C Controlled, Single-Cell 8A Switched Cap Parallel Battery Charger with Bypass Mode and Dual-Input Selector

### GENERAL DESCRIPTION

The SGM41604 is an efficient 8A switched-capacitor battery charging device with I<sup>2</sup>C control that can operate either in charge-pump voltage divider mode or in bypass mode. It can charge single-cell Li-Ion or Li-polymer battery in a wide 3.6V to 12V input voltage range (VBUS) from smart wall adapters or power banks. The switched-capacitor architecture is optimized for 50% duty cycle to cut the input current to one-half of the battery current and reduce the wiring drops, losses and temperature rise in the application.

The SGM41604 is equipped with the capability to facilitate a 5A bypass mode charge, formerly known as battery switch charge, via its built-in MOSFETs. The R<sub>DS(ON)</sub> value for the charging path in bypass mode is kept under 17mΩ (TYP) to accommodate high current operations. This integrated bypass mode ensures that a 5V fast charging adapter can be used to charge a single-cell battery, thereby maintaining backward compatibility.

The SGM41604 is designed to support a dual input setup using an integrated multiplexer control and driver for external OVPFETs. Additionally, it also supports single input without OVPFET or with just a single OVPFET.

The SGM41604 is available in a Green WLCSP-2.65×2.65-36B-A package.

### APPLICATIONS

Smartphone, Tablet

### FEATURES

- **Efficiency Optimized Switched-Capacitor Architecture**
  - ◆ Up to 8A Output Current
  - ◆ 3.6V to 12V Input Voltage Range
  - ◆ 187.5kHz to 1.5MHz Switching Frequency Setting
  - ◆ Above 98% Voltage Divider Mode Efficiency (when V<sub>BAT</sub> = 4V, I<sub>BAT</sub> = 2A)
- **Dual-Input Power Mux Controller for Source Selection**
- **Integrated Programmable Protection Features for Safe Operation**
  - ◆ Input Over-Voltage Protection (VBUS\_OVP)
  - ◆ Battery Over-Voltage Protection (VBAT\_OVP)
  - ◆ Input Over-Current Protection (IBUS\_OCP)
  - ◆ Battery Over-Current Protection (IBAT\_OCP)
  - ◆ Input Under-Current Protection (IBUS\_UCP)
  - ◆ Input Short-Circuit Protection (VBUS\_SCP)
  - ◆ Output Over-Voltage Protection (VOUT\_OVP)
  - ◆ Battery and Cable Connector Temperature Monitoring (TSBAT\_FLT and TSBUS\_FLT)
  - ◆ Die Over-Temperature Protection (TDIE\_OTP)
- **Up to 13A Charging Current with Synchronized Dual SGM41604 for Parallel Charging**
- **10-Channel 16-Bit (Effective) ADC Converter**
  - ◆ VAC1, VAC2, VBUS, IBUS, VOUT, VBAT, IBAT, TSBUS, TSBAT, TDIE for Monitoring

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with Integrated Protection and Dual-Input Selector**

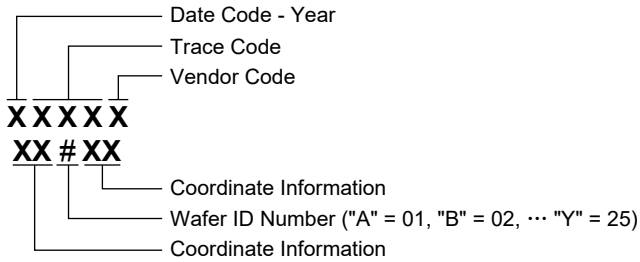
**SGM41604**

**PACKAGE/ORDERING INFORMATION**

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41604	WLCSP-2.65×2.65-36B-A	-40°C to +85°C	SGM41604YG/TR	SGM 41604 XXXXX XX#XX	Tape and Reel, 3000

**MARKING INFORMATION**

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

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**SGM41604**

## ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)	
VAC1, VAC2 (Converter not Switching)	-0.3V to 35V
VBUS (Converter not Switching)	-0.3V to 22V
PMID (Converter not Switching)	-0.3V to 22V
ACDRV1/ACDRV2 to VBUS	-22V to 6V
PMID to VBUS	-0.3V to 6V
CFL1, CFL2	-0.3V to 6V
CFH1, CFH2 while CFHx - VOUT = 6V (MAX)	-0.3V to 12V
VOUT	-0.3V to 6V
BATP, REGN, nINT, SDA, SCL, CDRVL_ADDRMS, SRN_SYNCIN, TSBAT_SYNCOUT, TSBUS	-0.3V to 6V
CDRVH	-0.3V to 22V
SRP_BATN	-0.3V to 1.8V
Package Thermal Resistance	
WLCSP-2.65×2.65-36B-A, $\theta_{JA}$	42.3°C/W
WLCSP-2.65×2.65-36B-A, $\theta_{JB}$	6.9°C/W
WLCSP-2.65×2.65-36B-A, $\theta_{JC}$	9.7°C/W
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility <sup>(1) (2)</sup>	
HBM	±2000V
CDM	±1000V

### NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

## RECOMMENDED OPERATING CONDITIONS

Input Voltage at VAC1 and VAC2, VAC1, VAC2	
.....	12V (MAX)
Input Voltage at VBUS	
.....	12V (MAX)
Input Voltage at PMID	
.....	12V (MAX)
Voltage across Q <sub>CH1</sub> , Q <sub>CH2</sub>	
PMID-CFH1, PMID-CFH2	5.5V (MAX)
Voltage across Q <sub>DH1</sub> , Q <sub>DH2</sub>	
CFH1-VOUT, CFH2-VOUT	5.5V (MAX)
Voltage across Q <sub>CL1</sub> , Q <sub>CL2</sub>	
VOUT-CFL1, VOUT-CFL2	5.5V (MAX)
Voltage across Q <sub>DL1</sub> , Q <sub>DL2</sub>	
CFL1, CFL2	5.5V (MAX)
Charging Current, I <sub>CHG</sub>	
.....	8A (MAX)
Junction Temperature Range	
.....	-40°C to +125°C

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

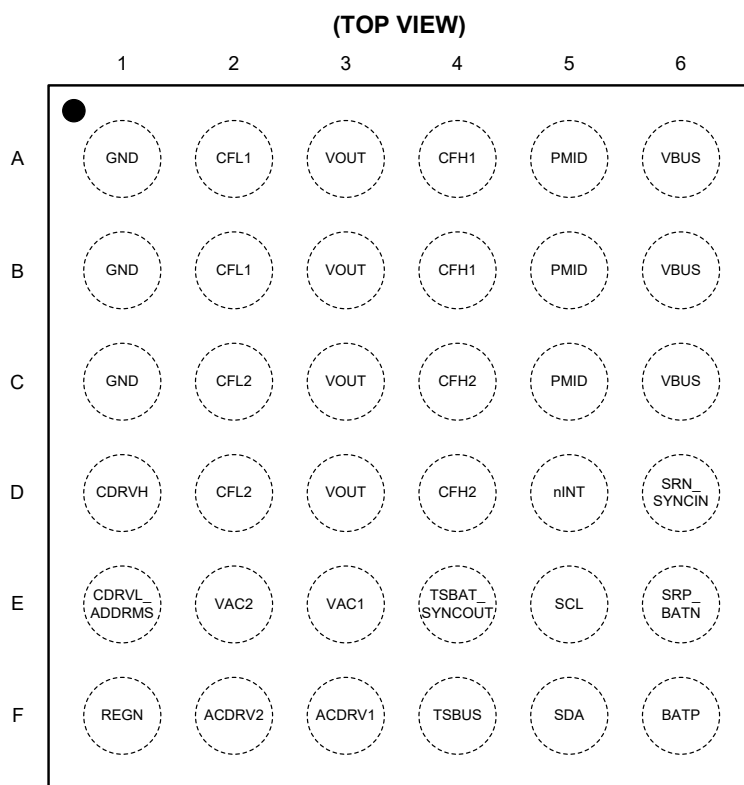
## ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION



**WLCSP-2.65×2.65-36B-A**

## PIN DESCRIPTION

PIN	NAME	TYPE <sup>(1)</sup>	FUNCTION
A1, B1, C1	GND	P	Power Ground Pins.
A2, B2	CFL1	P	Channel-1 Flying Capacitor Negative Pins. Connect 2~4 22μF parallel capacitors between CFH1 and CFL1 as close as possible to the device.
A3, B3, C3, D3	VOUT	P	Device Output Pins. Connect it to the battery pack positive terminal. A 22μF capacitor between VOUT and GND pins is recommended.
A4, B4	CFH1	P	Channel-1 Flying Capacitor Positive Pins. Connect 2~4 22μF parallel capacitors between CFH1 and CFL1 as close as possible to the device.
A5, B5, C5	PMID	P	Power Stage Supply Input Pins. Bypass them with at least a 10μF ceramic capacitor to GND.
A6, B6, C6	VBUS	P	Device Power Input Pins. Use a 1μF or larger ceramic capacitor between VBUS and GND pins close to the device.
C2, D2	CFL2	P	Channel-2 Flying Capacitor Negative Pins. Connect 2~4 22μF parallel capacitors between CFH2 and CFL2 as close as possible to the device.
C4, D4	CFH2	P	Channel-2 Flying Capacitor Positive Pins. Connect 2~4 22μF parallel capacitors between CFH2 and CFL2 as close as possible to the device.
D1	CDRVH	AIO	Charge Pump for Gate Drive. Connect a 0.22μF MLCC capacitor between CDRVH and CDRVL_ADDRMS.
D5	nINT	DO	Open-Drain Interrupt Output Pin. Use a 10kΩ pull-up to the logic high rail. It is normally high but generates a low 256μs pulse when a charge status or fault occurs to inform the host.

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**SGM41604**

**PIN DESCRIPTION (continued)**

PIN	NAME	TYPE <sup>(1)</sup>	FUNCTION
D6	SRN_SYNCIN	AI	Battery Current Sensing Negative Input and SYNCIN for Secondary Configuration. Place a 2mΩ or 5mΩ (R <sub>SNS</sub> ) shunt resistor between SRP_BATN and SRN_SYNCIN pins. Short SRP_BATN and SRN_SYNCIN together to GND if not used. If configured as a secondary IC for parallel charging, this pin functions as SYNCIN, and connect it to TSBAT_SYNCOUT of the primary IC, as well as connect a 1kΩ pull-up resistor from this pin to REGN.
E1	CDRVL_ADDRMS	AIO	Charge Pump for Gate Drive. Connect a 0.22μF MLCC capacitor between CDRVH and CDRVL_ADDRMS. During POR, this pin is also used to assign the I <sup>2</sup> C address of the device and the mode of the device as standalone, primary, or secondary.
E2	VAC2	AI	VAC2 Voltage Sense Input Pin. Connect it to VBUS if ACFET2 and RBFET2 are not used.
E3	VAC1	AI	VAC1 Voltage Sense Input Pin. Connect it to VBUS if ACFET1 and RBFET1 are not used.
E4	TSBAT_SYNCOUT	AI	Battery Temperature Sense Input and SYNCOUT for Primary Configuration. Connect it to the battery NTC thermistor and the external resistor divider that is pulled up to REGN. See the TSBAT section for choosing the resistor divider values. If configured as a primary IC for parallel charging, this pin functions as SYNCOUT, and is connected to SRN_SYNCIN of the secondary IC.
E5	SCL	DI	I <sup>2</sup> C Interface Clock Input Line. The device I <sup>2</sup> C controller block is forced to reset when receiving 9 clock pulses on the SCL line.
E6	SRP_BATN	AI	Battery Voltage Sensing Negative Input or Battery Current Sensing Positive Input. Connect a 100Ω resistor between this pin and negative terminal of the battery pack. Place a 2mΩ or 5mΩ (R <sub>SNS</sub> ) shunt resistor between this pin and SRN_SYNCIN pin. Short this pin and SRN_SYNCIN together if R <sub>SNS</sub> is not used.
F1	REGN	AO	Internal 5V LDO Output. Connect a 4.7μF MLCC capacitor between this pin and GND. In Primary/Secondary mode, connect through 1kΩ resistor to the TSBAT_SYNCOUT pin and SRN_SYNCIN pin. Do not use this pin for any other function.
F2	ACDRV2	P	External Dual N-MOSFET Gate Control Pin. Connect it to the gate of the external back-to-back N-MOSFET in the port2 charging path, or connect it to ground if the back-to-back N-MOSFET is not used.
F3	ACDRV1	P	External Dual N-MOSFET Gate Control Pin. Connect it to the gate of the external back-to-back N-MOSFET in the port1 charging path, or connect it to ground if the back-to-back N-MOSFET is not used.
F4	TSBUS	AI	BUS Temperature Sense Input. Connect it to the cable connector NTC thermistor and the external resistor divider that is pulled up to REGN. See the TSBUS section for choosing the resistor divider values.
F5	SDA	DIO	I <sup>2</sup> C Interface Data Line. The SDA line is forced to release when the 25ms I <sup>2</sup> C timeout fault occurs.
F6	BATP	AI	Battery Voltage Sensing Positive Input. Connect a 100Ω resistor between BATP and positive terminal of the battery pack.

NOTE:

1. P = power, AIO = analog input/output, AI = analog input, DO = digital output, AO = analog output, DIO = digital input/output.

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## ELECTRICAL CHARACTERISTICS

(T<sub>J</sub> = -40°C to +85°C, typical values are at T<sub>J</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Supply Currents</b>						
Battery Only Quiescent Current	I <sub>Q_BAT</sub>	ADC disabled, charge disabled, VBUS, VAC1, VAC2 not present		13	23	μA
		ADC enabled (slowest mode), charge disabled, VBUS, VAC1, VAC2 not present		1100	1800	
VAC Quiescent Current	I <sub>Q_VAC</sub>	ADC disabled, charge disabled, ACDRV disabled, EN_HIZ = 1, V <sub>VAC1</sub> or V <sub>VAC2</sub> = 8V		34		μA
		ADC disabled, charge disabled, ACDRV disabled, V <sub>VAC1</sub> or V <sub>VAC2</sub> = 8V		670		
		ADC disabled, charge disabled, ACDRV enabled, V <sub>VAC1</sub> or V <sub>VAC2</sub> = 8V		950		
VAC UVLO Rising Threshold	V <sub>AC_UVLO_R</sub>	V <sub>VAC1</sub> or V <sub>VAC2</sub> rising, for active I <sup>2</sup> C	3.1	3.35	3.6	V
VAC UVLO Falling Threshold	V <sub>AC_UVLO_F</sub>	V <sub>VAC1</sub> or V <sub>VAC2</sub> falling	2.9	3.15	3.4	V
VAC UVLO Hysteresis	V <sub>AC_UVLO_HYS</sub>			200		mV
VBUS UVLO Rising Threshold	V <sub>BUS_UVLO_R</sub>	V <sub>VBUS</sub> rising, for active I <sup>2</sup> C	3	3.3	3.6	V
VBUS UVLO Falling Threshold	V <sub>BUS_UVLO_F</sub>	V <sub>VBUS</sub> falling	2.5	2.8	3.1	V
VBUS UVLO Hysteresis	V <sub>BUS_UVLO_HYS</sub>			500		mV
VBUS Present Rising Threshold	V <sub>BUS_PRESENT_R</sub>	V <sub>VBUS</sub> rising to allow user to set CHG_EN = 1	3	3.3	3.6	V
VBUS Present Falling Threshold	V <sub>BUS_PRESENT_F</sub>	V <sub>VBUS</sub> falling	2.8	3.1	3.4	V
VBUS Present Hysteresis	V <sub>BUS_PRESENT_HYS</sub>			200		mV
VOOUT UVLO Rising Threshold	V <sub>OUT_UVLO_R</sub>	V <sub>VOOUT</sub> rising, for active I <sup>2</sup> C	2.2	2.45	2.7	V
VOOUT UVLO Falling Threshold	V <sub>OUT_UVLO_F</sub>	V <sub>VOOUT</sub> falling	2	2.25	2.5	V
VOOUT UVLO Hysteresis	V <sub>OUT_UVLO_HYS</sub>			200		mV
VOOUT Present Rising Threshold	V <sub>OUT_PRESENT_R</sub>	V <sub>VOOUT</sub> rising to allow user to set CHG_EN = 1	2.8	3.05	3.3	V
VOOUT Present Falling Threshold	V <sub>OUT_PRESENT_F</sub>	V <sub>VOOUT</sub> falling	2.7	2.95	3.2	V
VOOUT Present Hysteresis	V <sub>OUT_PRESENT_HYS</sub>			100		mV
<b>External OVP Control</b>						
VAC Present Rising Threshold	V <sub>AC_PRESENT_R</sub>	V <sub>VAC1</sub> or V <sub>VAC2</sub> rising to turn on ACFET- RBFET	3.1	3.35	3.6	V
VAC Present Falling Threshold	V <sub>AC_PRESENT_F</sub>	V <sub>VAC1</sub> or V <sub>VAC2</sub> falling	2.9	3.15	3.4	V
VAC Present Hysteresis	V <sub>AC_PRESENT_HYS</sub>			200		mV
VAC Present Rising Threshold Deglitch Time	t <sub>VAC_IN_DEG</sub>	Deglitch between V <sub>VAC</sub> rising above V <sub>AC_PRESENT_R</sub> and starting external OVPFET turn-on		5		ms
VAC OVP Rising Threshold Range	V <sub>AC_OVP_R</sub>	V <sub>VAC1</sub> or V <sub>VAC2</sub> rising	6.5		18	V
VAC OVP Threshold Accuracy	V <sub>AC_OVPR_ACC</sub>	V <sub>AC1_OVP_R</sub> or V <sub>AC2_OVP_R</sub> = 6.5V		6.5		V
		V <sub>AC1_OVP_R</sub> or V <sub>AC2_OVP_R</sub> = 10.5V		10.5		
		V <sub>AC1_OVP_R</sub> or V <sub>AC2_OVP_R</sub> = 12V		12		
		V <sub>AC1_OVP_R</sub> or V <sub>AC2_OVP_R</sub> = 18V		18		
VAC Over-Voltage Hysteresis	V <sub>AC_OVP_HYS</sub>			3		%
VAC OVP Rising Deglitch Time	t <sub>VAC_OVPR_DEG</sub>	Deglitch between V <sub>VAC1</sub> or V <sub>VAC2</sub> rising above V <sub>AC_OVP_R</sub> and triggering the protection action		100		ns
VAC OVP Resume Time	t <sub>VAC_OVP_RSM</sub>			64		μs
VAC Pull-Down Resistance	R <sub>PDN_VAC</sub>	V <sub>VAC1</sub> or V <sub>VAC2</sub> = 10V (Clamp to 35mA)		350		Ω
VBUS Pull-Down Resistance	R <sub>PDN_VBUS</sub>	V <sub>VBUS</sub> = 10V		5.5		kΩ
<b>REGN LDO</b>						
REGN LDO Output Voltage	V <sub>REGN</sub>	V <sub>VBUS</sub> = 8V, I <sub>REGN</sub> = 20mA		5		V
REGN LDO Current Limit	I <sub>REGN</sub>	V <sub>VBUS</sub> = 8V, V <sub>REGN</sub> = 4.5V	20			mA

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SGM41604 with Integrated Protection and Dual-Input Selector**

**ELECTRICAL CHARACTERISTICS (continued)**

(T<sub>J</sub> = -40°C to +85°C, typical values are at T<sub>J</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Switched Cap Chargers</b>							
VBUS to VOUT Resistance	R <sub>DROPOUT</sub>	Bypass mode		17		mΩ	
R <sub>DSON</sub> of Reverse Blocking FET	R <sub>DS_QRB</sub>	V <sub>VBUS</sub> = 8V		5.3		mΩ	
R <sub>DSON</sub> of Q <sub>CH1</sub>	R <sub>DS_QCH1</sub>	V <sub>PMID</sub> = 8V		20		mΩ	
R <sub>DSON</sub> of Q <sub>DH1</sub>	R <sub>DS_QDH1</sub>	V <sub>CFLY</sub> = 4V		12		mΩ	
R <sub>DSON</sub> of Q <sub>CL1</sub>	R <sub>DS_QCL1</sub>	V <sub>VOUT</sub> = 4V		12		mΩ	
R <sub>DSON</sub> of Q <sub>DL1</sub>	R <sub>DS_QDL1</sub>	V <sub>CFLY</sub> = 4V		12		mΩ	
R <sub>DSON</sub> of Q <sub>CH2</sub>	R <sub>DS_QCH2</sub>	V <sub>PMID</sub> = 8V		20		mΩ	
R <sub>DSON</sub> of Q <sub>DH2</sub>	R <sub>DS_QDH2</sub>	V <sub>CFLY</sub> = 4V		12		mΩ	
R <sub>DSON</sub> of Q <sub>CL2</sub>	R <sub>DS_QCL2</sub>	V <sub>VOUT</sub> = 4V		12		mΩ	
R <sub>DSON</sub> of Q <sub>DL2</sub>	R <sub>DS_QDL2</sub>	V <sub>CFLY</sub> = 4V		12		mΩ	
<b>Protection</b>							
nINT Low Pulse Duration when a Protection Occurs	t <sub>INT</sub>			256		μs	
VBUS OVP Rising Threshold Range	V <sub>BUS_OVP_R</sub>	Voltage divider mode	I <sup>2</sup> C programmable, 50mV per step, 8.9V by default	7	12.25	V	
		Bypass mode	I <sup>2</sup> C programmable, 25mV per step, 4.45V by default	3.5	6.5		
VBUS OVP Accuracy	V <sub>BUS_OVPR_ACC</sub>	V <sub>BUS_OVP_R</sub> = 4.45V		-2	2	%	
		V <sub>BUS_OVP_R</sub> = 9V		-1	1	%	
VBUS OVP Rising Deglitch Time	t <sub>VBUS_OVPR_DEG</sub>	Deglitch between V <sub>VBUS</sub> rising above V <sub>BUS_OVP_R</sub> and triggering protection action			1	μs	
VBUS OVP Alarm Rising Threshold Range	V <sub>BUSOVP_ALM_R</sub>	Voltage divider mode	I <sup>2</sup> C programmable, 50mV per step, 8.7V by default	7	13.35	V	
		Bypass mode	I <sup>2</sup> C programmable, 25mV per step, 4.35V by default	3.5	6.675		
VBUS OVP Alarm Hysteresis	V <sub>BUSOVP_ALM_HYS</sub>	V <sub>BUSOVP_ALM_R</sub> = 8V			100	mV	
VBUS OVP Alarm Accuracy	V <sub>BUSOVP_ALM_ACC</sub>	V <sub>BUSOVP_ALM_R</sub> = 4V		-3.1	3.5	%	
		V <sub>BUSOVP_ALM_R</sub> = 8V		-2.9	3.3	%	
IBUS OCP Threshold Range	I <sub>BUS_OCP</sub>	I <sup>2</sup> C programmable, 250mA per step, 4.25A by default			1	6.5	A
IBUS OCP Threshold Accuracy	I <sub>BUS_OCP_ACC</sub>	I <sub>BUS_OCP</sub> = 3.0A			-4	4	%
IBUS OCP Deglitch Time	t <sub>IBUS_OCP_DEG</sub>	Deglitch between I <sub>BUS</sub> rising above I <sub>BUS_OCP</sub> and trigger protection action			80	μs	
IBUS OCP Alarm Threshold Range	I <sub>BUSOCP_ALM_R</sub>	I <sup>2</sup> C programmable, 250mA per step, 3.5A by default			1	8.75	A
IBUS OCP Alarm Accuracy	I <sub>BUSOCP_ALM_ACC</sub>	I <sub>BUSOCP_ALM_R</sub> = 3.0A, initial accuracy, T <sub>J</sub> = +25°C			-5	5	%
IBUS UCP Threshold	I <sub>BUS_UCP</sub>	I <sub>BUS_UCP_R</sub> = 250mA, BUSUCP = 1			250	mA	
		I <sub>BUS_UCP_R</sub> = 500mA, BUSUCP = 0			500		
		I <sub>BUS_UCP_F</sub> = 125mA, BUSUCP = 1			125		
		I <sub>BUS_UCP_F</sub> = 250mA, BUSUCP = 0			250		
IBUS UCP Deglitch time	t <sub>IBUS_UCP_DEG</sub>	Deglitch between I <sub>BUS</sub> falling below I <sub>BUS_UCP</sub> and trigger protection action. I <sup>2</sup> C programmable, 0.01ms by default.			0.01	150	ms
VOUT OVP Rising Threshold Range	V <sub>OUT_OVP_R</sub>	I <sup>2</sup> C programmable, 0.1V per step, 5V by default			4.7	5	V
VOUT OVP Threshold Accuracy	V <sub>OUT_OVP_ACC</sub>	V <sub>OUT_OVP_R</sub> = 5V			4.7	5.2	V
VOUT OVP Rising Deglitch Time	t <sub>VOUT_OVP_DEG</sub>	Deglitch between V <sub>VOUT</sub> rising above V <sub>OUT_OVP_R</sub> and triggering protection action			4	μs	
VBAT OVP Rising Threshold Range	V <sub>BAT_OVP_R</sub>	I <sup>2</sup> C programmable, 10mV per step, 4.4V by default			3.5	4.77	V
VBAT OVP Threshold Accuracy	V <sub>BAT_OVP_ACC</sub>	V <sub>BAT_OVP_R</sub> = 4.4V			-0.9	0.9	%

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**ELECTRICAL CHARACTERISTICS (continued)**

(T<sub>J</sub> = -40°C to +85°C, typical values are at T<sub>J</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBAT OVP Alarm Rising Threshold Range	V <sub>BATOVP_ALM_R</sub>	I <sup>2</sup> C programmable, 10mV per step, 4.2V by default	3.5		4.77	V
VBAT OVP Alarm Hysteresis	V <sub>BATOVP_ALM_HYS</sub>			40		mV
VBAT OVP Alarm Accuracy	V <sub>BATOVP_ALM_ACC</sub>	V <sub>BATOVP_ALM_R</sub> = 4.4V	-1.2		1.2	%
IBAT OCP Threshold Range	I <sub>BAT_OCP</sub>	I <sup>2</sup> C programmable, 7.1A by default, 100mA per step for 2A to 8.5A range, and 300mA per step for 8.5A to 11.2A range	2		11.2	A
IBAT OCP Threshold Accuracy	I <sub>BAT_OCP_ACC</sub>	I <sub>BAT_OCP</sub> = 2A, R <sub>SNS</sub> = 2mΩ, initial accuracy, T <sub>J</sub> = +25°C	-5		5	%
		I <sub>BAT_OCP</sub> = 8A, R <sub>SNS</sub> = 2mΩ, initial accuracy, T <sub>J</sub> = +25°C	-1.2		1.2	%
IBAT OCP Deglitch Time	t <sub>BAT_OCP_DEG</sub>	Deglitch between I <sub>BAT</sub> rising above I <sub>BAT_OCP</sub> and triggering protection action		640		μs
IBAT OCP Alarm Rising Threshold Range	I <sub>BATOCP_ALM_R</sub>	I <sup>2</sup> C programmable, 100mA per step, 7A by default, R <sub>SNS</sub> = 2mΩ	0		12.7	A
IBAT OCP Alarm Threshold Accuracy	I <sub>BATOCP_ALM_ACC</sub>	I <sub>BATOCP_ALM_R</sub> = 2A, R <sub>SNS</sub> = 2mΩ, initial accuracy, T <sub>J</sub> = +25°C	-5		5	%
		I <sub>BATOCP_ALM_R</sub> = 8A, R <sub>SNS</sub> = 2mΩ, initial accuracy, T <sub>J</sub> = +25°C	-2		2	%
IBAT UCP Alarm Threshold Range	I <sub>BATUCP_ALM_F</sub>	I <sup>2</sup> C programmable, 50mA per step, 2A default, R <sub>SNS</sub> = 2mΩ	0		4.5	A
IBAT UCP Alarm Threshold Accuracy	I <sub>BATUCP_ALM_ACC</sub>	I <sub>BATUCP_ALM_F</sub> = 4.5A, R <sub>SNS</sub> = 2mΩ, initial accuracy, T <sub>J</sub> = +25°C	-3.5		3.5	A
VBUS_HI Rising Threshold	V <sub>BUS_HI_FALL</sub>	V <sub>BUS</sub> /(2 × V <sub>VOULT</sub> ) in voltage divider mode, V <sub>BUS</sub> /V <sub>VOULT</sub> in bypass mode		1.175		V/V
VBUS_HI Falling Threshold	V <sub>BUS_HI_RISE</sub>	V <sub>BUS</sub> /(2 × V <sub>VOULT</sub> ) in voltage divider mode, V <sub>BUS</sub> /V <sub>VOULT</sub> in bypass mode		1.2		
VBUS_LO Falling Threshold	V <sub>BUS_LO_FALL</sub>	V <sub>BUS</sub> /(2 × V <sub>VOULT</sub> ) in voltage divider mode, V <sub>BUS</sub> /V <sub>VOULT</sub> in bypass mode		1		
VBUS_LO Rising Threshold	V <sub>BUS_LO_RISE</sub>	V <sub>BUS</sub> /(2 × V <sub>VOULT</sub> ) in voltage divider mode, V <sub>BUS</sub> /V <sub>VOULT</sub> in bypass mode		1.0125		
TSBUS Percentage Fault Threshold Range	TS <sub>BUS_FLT_F</sub>	I <sup>2</sup> C programmable, 0.19531% per step, 4.10151% by default	0		49.8041	%
TSBUS Percentage Fault Accuracy	TS <sub>BUSFLT_ACC</sub>	TS <sub>BUS_FLT_F</sub> = 20.12%	19.7	20.12	20.9	%
TSBAT Percentage Fault Threshold Range	TS <sub>BAT_FLT_F</sub>	I <sup>2</sup> C programmable, 0.19531% per step, 4.10151% by default	0		49.8041	%
TSBAT Percentage Fault Accuracy	TS <sub>BATFLT_ACC</sub>	TS <sub>BAT_FLT_F</sub> = 20.12%	19.7	20.12	20.9	%
TDIE OTP Rising Threshold Range	T <sub>DIE_OTP_R</sub>	I <sup>2</sup> C programmable, 20°C per step, 140°C by default	80		140	°C
TDIE OTP Threshold Accuracy	T <sub>DIE_OTP_ACC</sub>		-6		6	°C
TDIE OTP Threshold Hysteresis	T <sub>DIE_OTP_HYS</sub>			30		°C
TDIE OTP Alarm Rising Threshold Range	T <sub>DIEOTP_ALM_R</sub>	I <sup>2</sup> C programmable, 0.5°C per step, 125°C by default	25		150	°C
TDIE OTP Alarm Threshold Accuracy	T <sub>DIEOTP_ALM_ACC</sub>		-6		6	°C
TDIE OTP Alarm Threshold Hysteresis	T <sub>DIEOTP_ALM_HYS</sub>			30		°C
<b>ADC Specification</b>						
ADC Conversion Time for Each Channel	t <sub>ADC_CONV</sub>	ADC_SAMPLE[1:0] = 00		16		ms
		ADC_SAMPLE[1:0] = 01		8		
		ADC_SAMPLE[1:0] = 10		4		
		ADC_SAMPLE[1:0] = 11		2		
ADC Resolution	ADC <sub>RES</sub>	ADC_SAMPLE[1:0] = 00		15		bit
		ADC_SAMPLE[1:0] = 01		14		
		ADC_SAMPLE[1:0] = 10		13		
		ADC_SAMPLE[1:0] = 11		11		
ADC IBUS Current Readable in REG0x25 and REG0x26	I <sub>BUS_ADC</sub>	Effective Range	0		7	A
		LSB		1		mA



# I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger

SGM41604

with Integrated Protection and Dual-Input Selector

## ELECTRICAL CHARACTERISTICS (continued)

(T<sub>J</sub> = -40°C to +85°C, typical values are at T<sub>J</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IBUS_ADC Accuracy	I <sub>BUS_ADC_ACC</sub>	I <sub>BUS</sub> = 2A, ADC_SAMPLE[1:0] = 00, initial accuracy, T <sub>J</sub> = +25°C	-3.5		3.5	%
		I <sub>BUS</sub> = 3A, ADC_SAMPLE[1:0] = 00, initial accuracy, T <sub>J</sub> = +25°C	-3.5		3.5	%
ADC VBUS Voltage Readable in REG0x27 and REG0x28	V <sub>BUS_ADC</sub>	Effective Range	0		16.39	V
		LSB		1		mV
VBUS_ADC Accuracy	V <sub>BUS_ADC_ACC</sub>	V <sub>VBUS</sub> = 4V, ADC_SAMPLE[1:0] = 00, initial accuracy, T <sub>J</sub> = +25°C	-1		1	%
		V <sub>VBUS</sub> = 8V, ADC_SAMPLE[1:0] = 00, initial accuracy, T <sub>J</sub> = +25°C	-1		1	%
ADC VAC1 Voltage Readable in REG0x29 and REG0x2A	V <sub>VAC1_ADC</sub>	Effective Range	0		14	V
		LSB		1		mV
VAC1_ADC Accuracy	V <sub>VAC1_ADC_ACC</sub>	V <sub>VAC1</sub> = 4V, ADC_SAMPLE[1:0] = 00, initial accuracy, T <sub>J</sub> = +25°C	-1		1	%
		V <sub>VAC1</sub> = 8V, ADC_SAMPLE[1:0] = 00, initial accuracy, T <sub>J</sub> = +25°C	-1		1	%
ADC VAC2 Voltage Readable in REG0x2B and REG0x2C	V <sub>VAC2_ADC</sub>	Effective Range	0		14	V
		LSB		1		mV
VAC2_ADC Accuracy	V <sub>VAC2_ADC_ACC</sub>	V <sub>VAC2</sub> = 4V, ADC_SAMPLE[1:0] = 00, initial accuracy, T <sub>J</sub> = +25°C	-1		1	%
		V <sub>VAC2</sub> = 8V, ADC_SAMPLE[1:0] = 00, initial accuracy, T <sub>J</sub> = +25°C	-1		1	%
ADC VOUT Voltage Readable in REG0x2D and REG0x2E	V <sub>OUT_ADC</sub>	Effective Range	0		6	V
		LSB		1		mV
VOUT_ADC Accuracy	V <sub>OUT_ADC_ACC</sub>	V <sub>VOUT</sub> = 4V, ADC_SAMPLE[1:0] = 00, initial accuracy, T <sub>J</sub> = +25°C	-0.5		0.5	%
		V <sub>VOUT</sub> = 4.4V, ADC_SAMPLE[1:0] = 00, initial accuracy, T <sub>J</sub> = +25°C	-0.5		0.5	%
ADC VBAT Voltage Readable in REG0x2F and REG0x30	V <sub>BAT_ADC</sub>	Effective Range	0		6	V
		LSB		1		mV
VBAT_ADC Accuracy	V <sub>BAT_ADC_ACC</sub>	V <sub>BAT</sub> = 4V, ADC_SAMPLE[1:0] = 00, initial accuracy, T <sub>J</sub> = +25°C	-0.3		0.3	%
		V <sub>BAT</sub> = 4.4V, ADC_SAMPLE[1:0] = 00, initial accuracy, T <sub>J</sub> = +25°C	-0.3		0.3	%
ADC IBAT Current Readable in REG0x31 and REG0x32	I <sub>BAT_ADC</sub>	Effective Range	0		12	A
		LSB		1		mA
IBAT_ADC Accuracy	I <sub>BAT_ADC_ACC</sub>	I <sub>BAT</sub> = 6A, R <sub>SNS</sub> = 2mΩ, ADC_SAMPLE[1:0] = 00	-1.6		1.6	%
		I <sub>BAT</sub> = 8A, R <sub>SNS</sub> = 2mΩ, ADC_SAMPLE[1:0] = 00	-1.4		1.4	%
ADC TSBUS Pin Percentage Readable in REG0x33 and REG0x34	TS <sub>BUS_ADC</sub>	Effective Range	0		50	%
		LSB		0.0977		%
TSBUS_ADC Accuracy	TS <sub>BUS_ADC_ACC</sub>	TSBUS = 20% of V <sub>REGN</sub> , ADC_SAMPLE[1:0] = 00	19.1	20	20.5	%
ADC TSBAT Pin Percentage Readable in REG0x35 and REG0x36	TS <sub>BAT_ADC</sub>	Effective Range	0		50	%
		LSB		0.0977		%
TSBAT_ADC Accuracy	TS <sub>BAT_ADC_ACC</sub>	TSBAT = 20% of V <sub>REGN</sub> , ADC_SAMPLE[1:0] = 00	19.1	20	20.5	%
ADC DIE Temperature Readable in REG0x37 and REG0x38	T <sub>DIE_ADC</sub>	Effective Range	-40		150	°C
		LSB		0.5		°C

**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

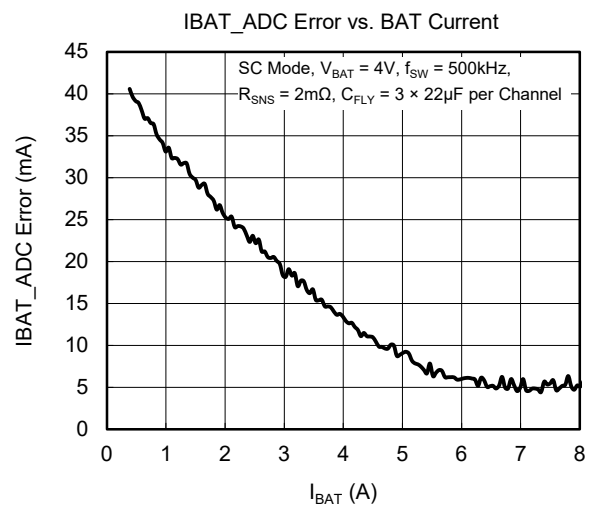
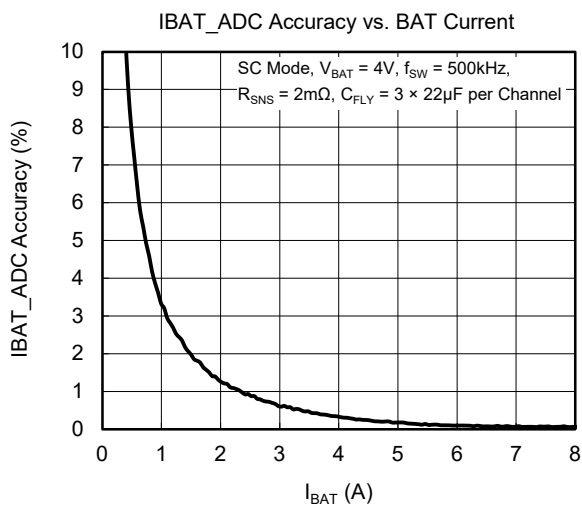
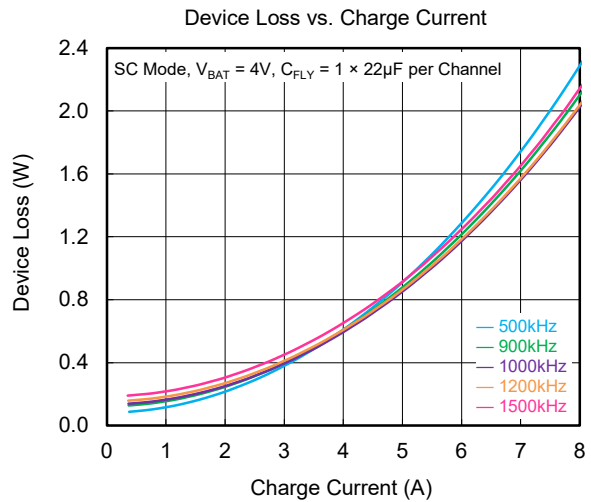
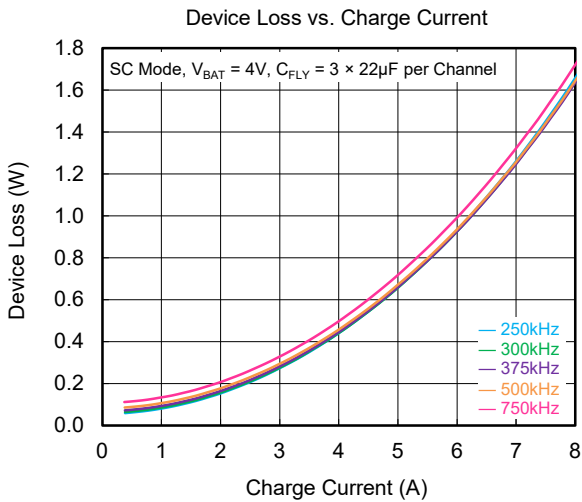
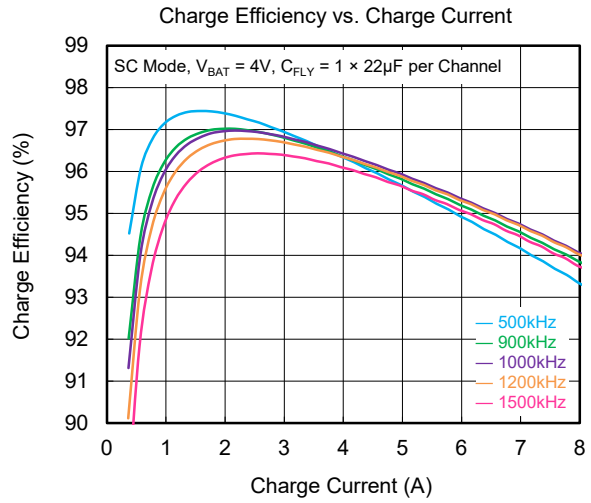
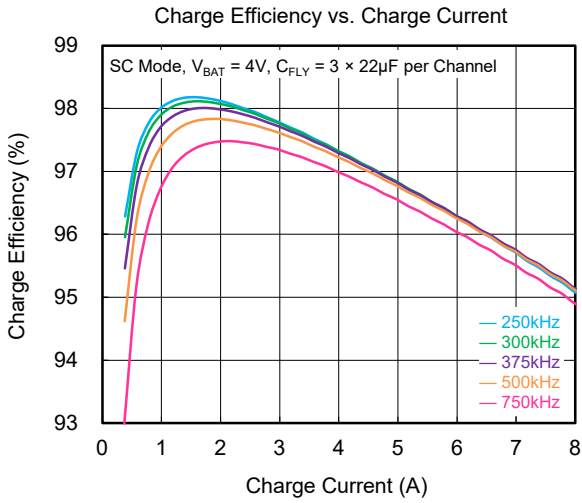
**SGM41604**

**ELECTRICAL CHARACTERISTICS (continued)**

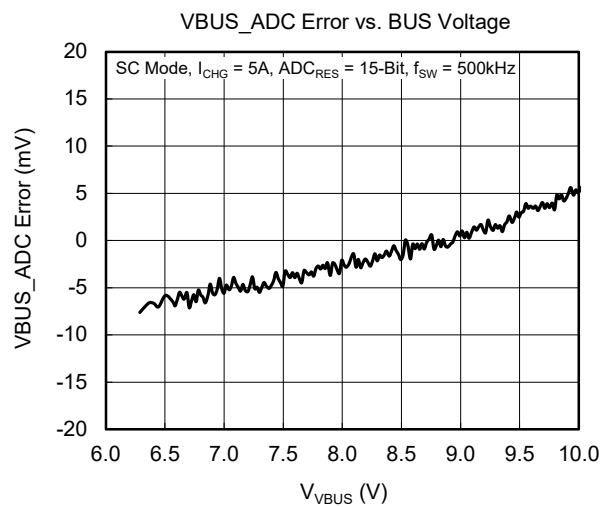
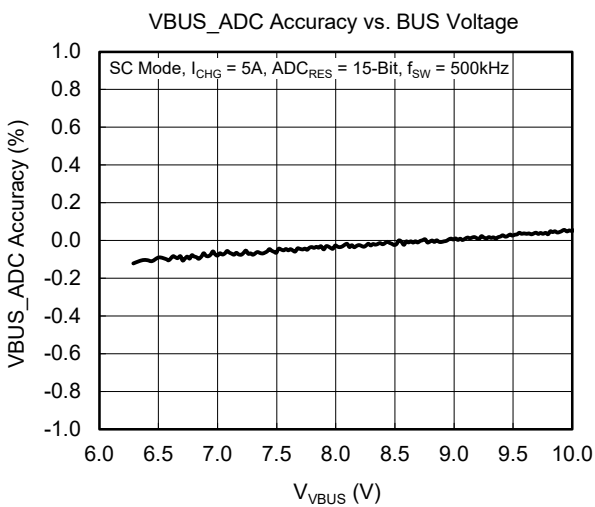
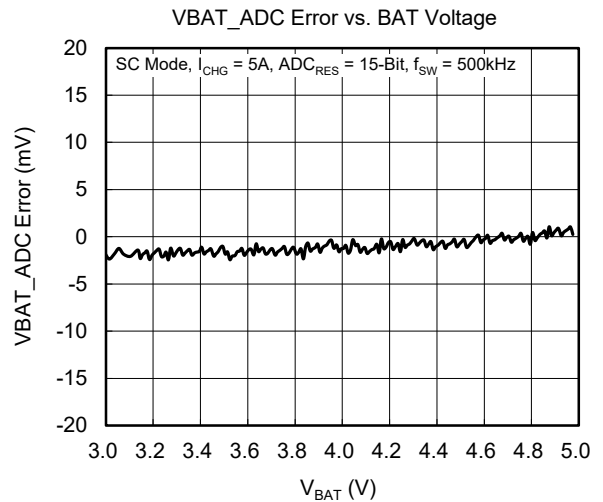
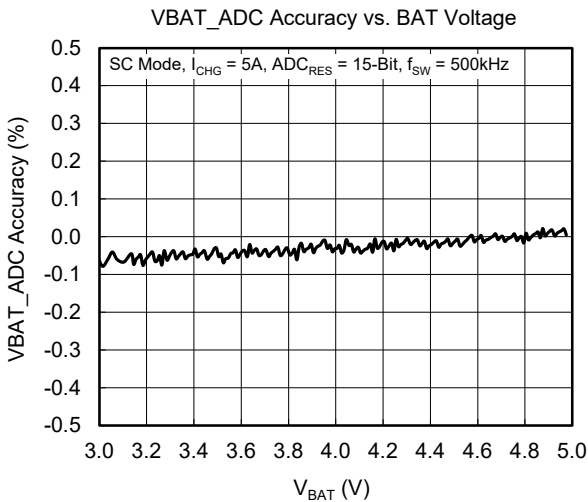
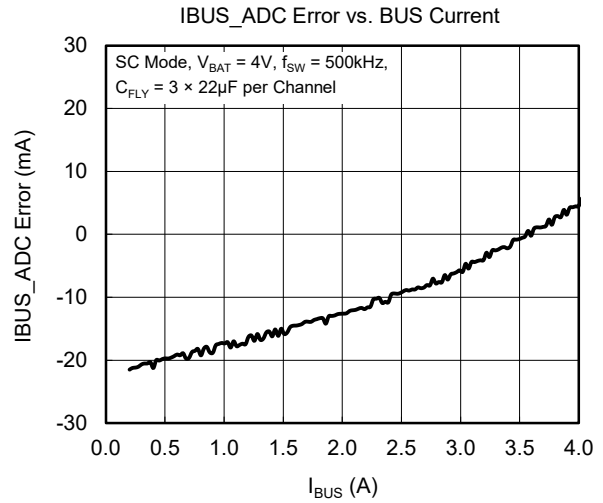
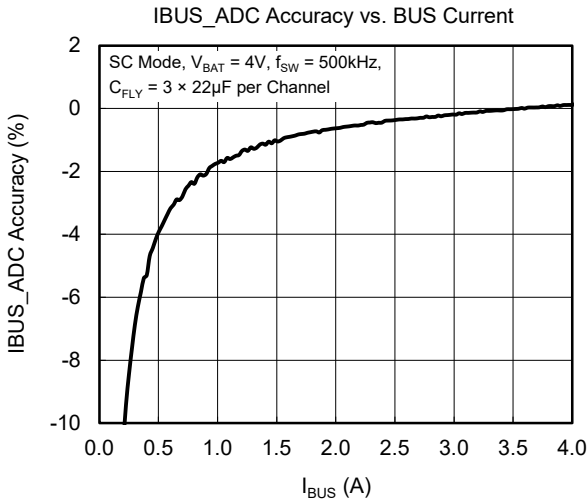
(T<sub>J</sub> = -40°C to +85°C, typical values are at T<sub>J</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>I<sup>2</sup>C Interface (SCL and SDA Pins)</b>						
High Level Input Voltage	V <sub>IH_I2C</sub>	SCL and SDA pins	0.825			V
Low Level Input Voltage	V <sub>IL_I2C</sub>	SCL and SDA pins			0.4	V
Low Level Output Voltage	V <sub>OL_SDA</sub>	Sink 5mA, SDA pin			0.4	V
High-Level Leakage Current	I <sub>LKG_I2C</sub>	Connected to 1.2V			1	μA
SCL Clock Frequency	f <sub>CLK</sub>				1000	kHz
<b>Logic Output Pin (nINT, TSBAT_SYNCOUT)</b>						
Low Level Output Voltage, nINT Pin	V <sub>OL_INT</sub>	Sink 5mA			0.4	V
High-Level Leakage Current, nINT Pin	I <sub>LKG_nINT</sub>	Connected to 1.2V			1	μA
Low Level Output Voltage, TSBAT_SYNCOUT Pin	V <sub>OL_TSBAT_SYNCOUT</sub>	Sink 5mA			0.4	V
High-Level Leakage Current, TSBAT_SYNCOUT Pin	I <sub>LKG_TSBAT_SYNCOUT</sub>	Connected to 1.2V			1	μA
<b>Logic Input Pin (SRN_SYNCIN)</b>						
High Level Input Voltage, SRN_SYNCIN Pin	V <sub>IH_SRN_SYNCIN</sub>		0.825			V
Low Level Input Voltage, SRN_SYNCIN Pin	V <sub>IL_SRN_SYNCIN</sub>				0.4	V
High-Level Leakage Current, SRN_SYNCIN Pin	I <sub>LKG_SRN_SYNCIN</sub>	Connected to 1.8V			1	μA
<b>Timing Requirement</b>						
Time between Consecutive Faults for ALM Indication	t <sub>ALM_DEBOUNCE</sub>			120		ms

**TYPICAL PERFORMANCE CHARACTERISTICS**



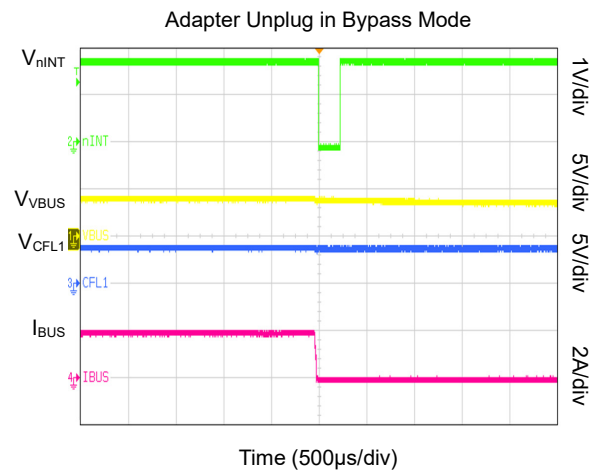
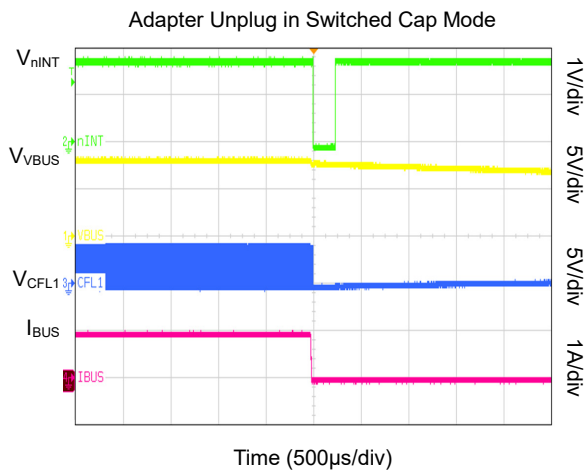
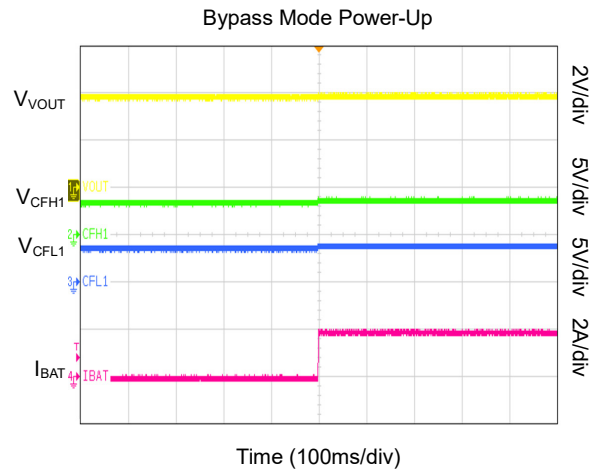
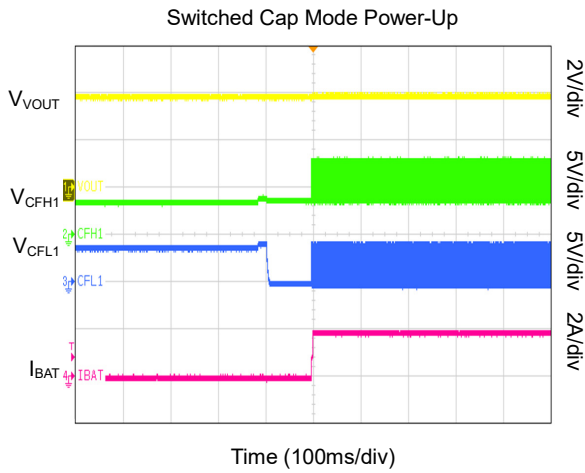
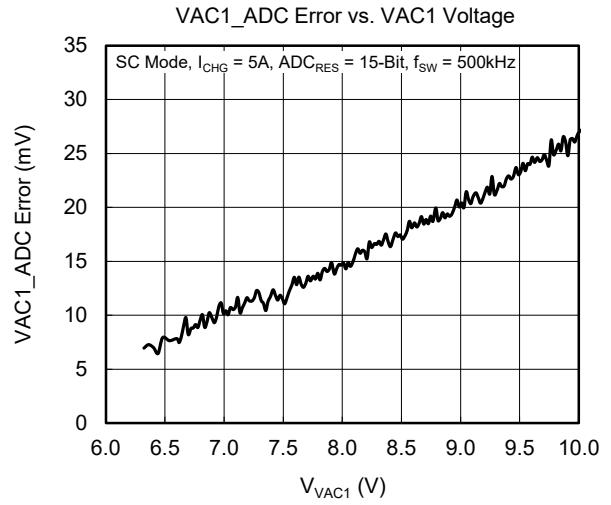
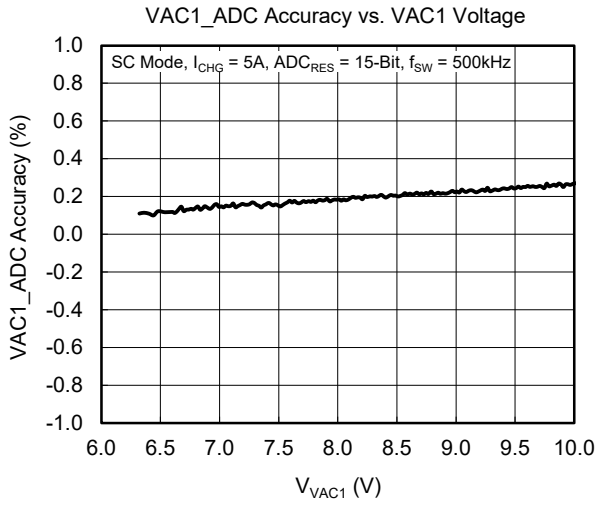
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**



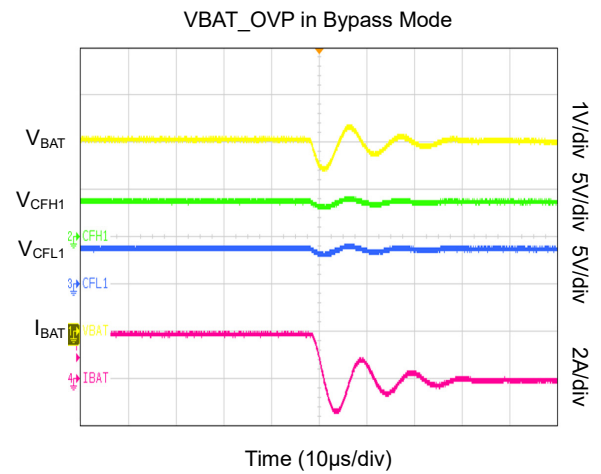
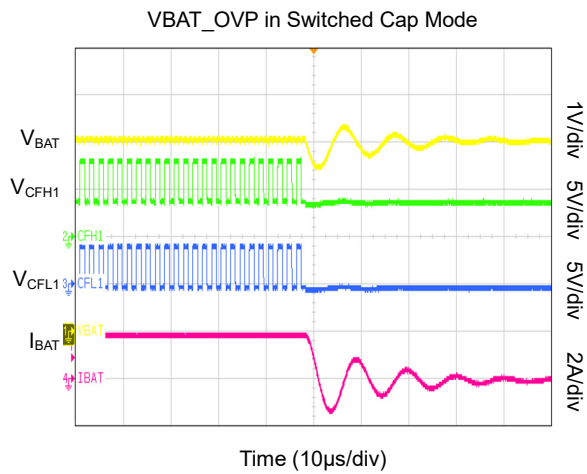
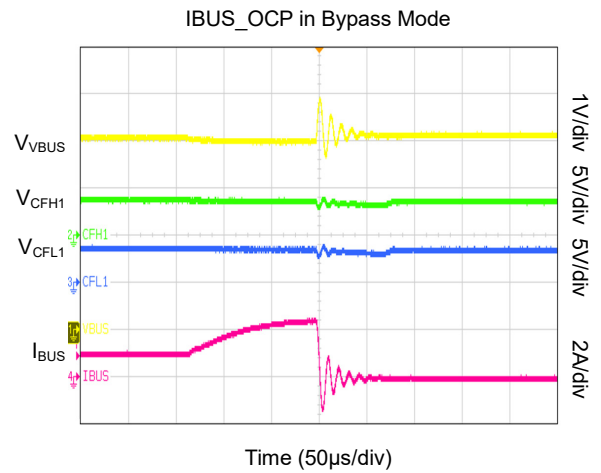
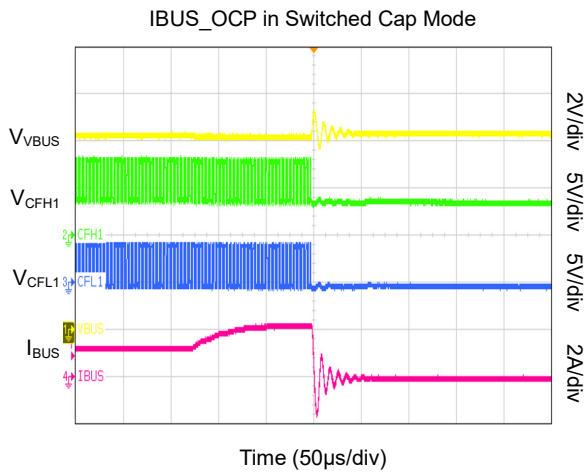
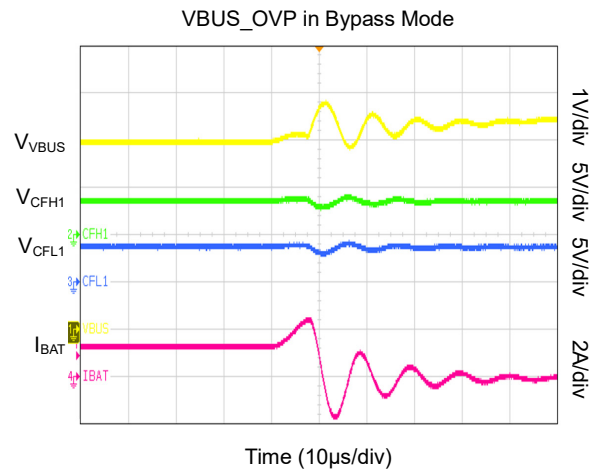
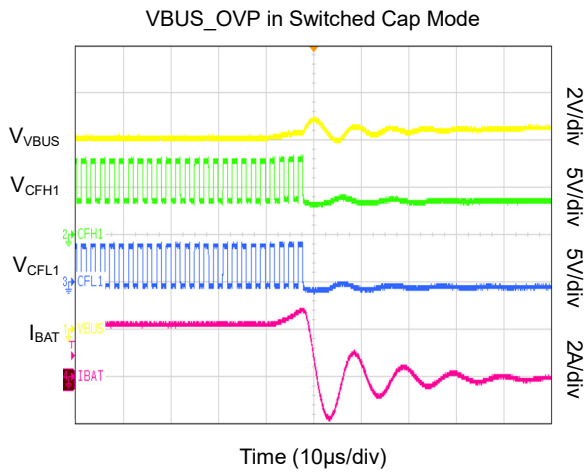
I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector

SGM41604

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

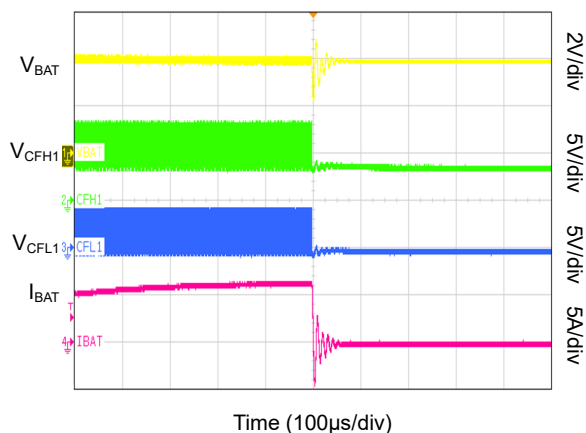


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

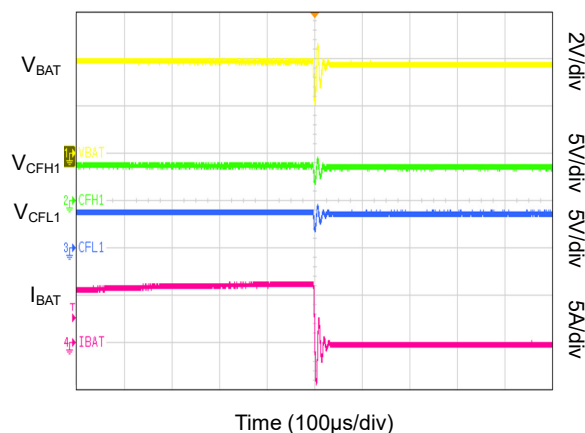


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

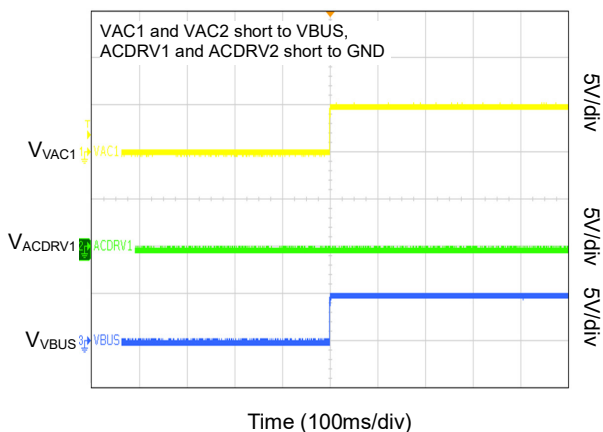
IBAT\_OCP in Switched Cap Mode



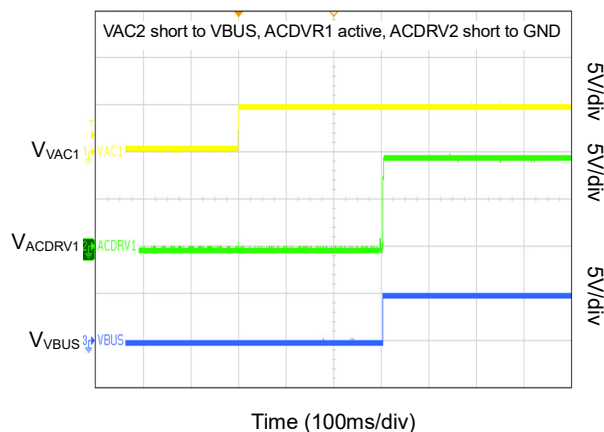
IBAT\_OCP in Bypass Mode



Power-Up without ACFET



Power-Up from VAC1



# I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger with Integrated Protection and Dual-Input Selector

**SGM41604**

## TYPICAL APPLICATION CIRCUITS

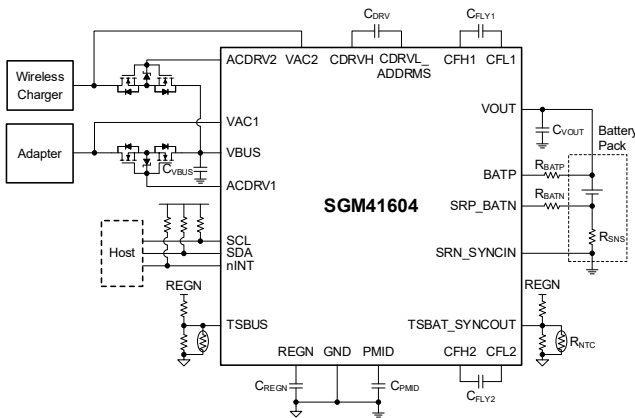


Figure 1. Typical Application Circuit with Dual Input

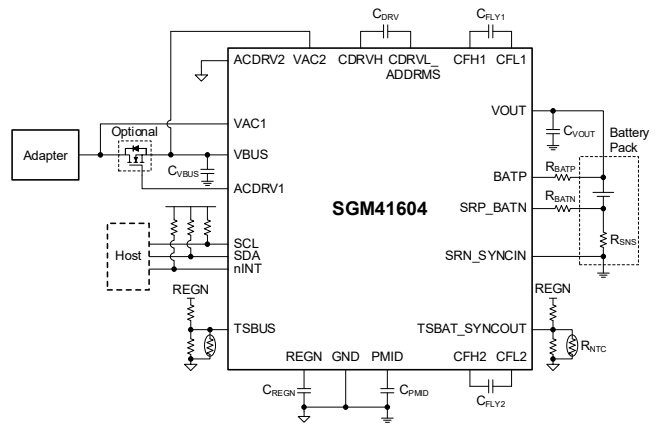


Figure 2. Typical Application Circuit with Single Input

## FUNCTIONAL BLOCK DIAGRAM

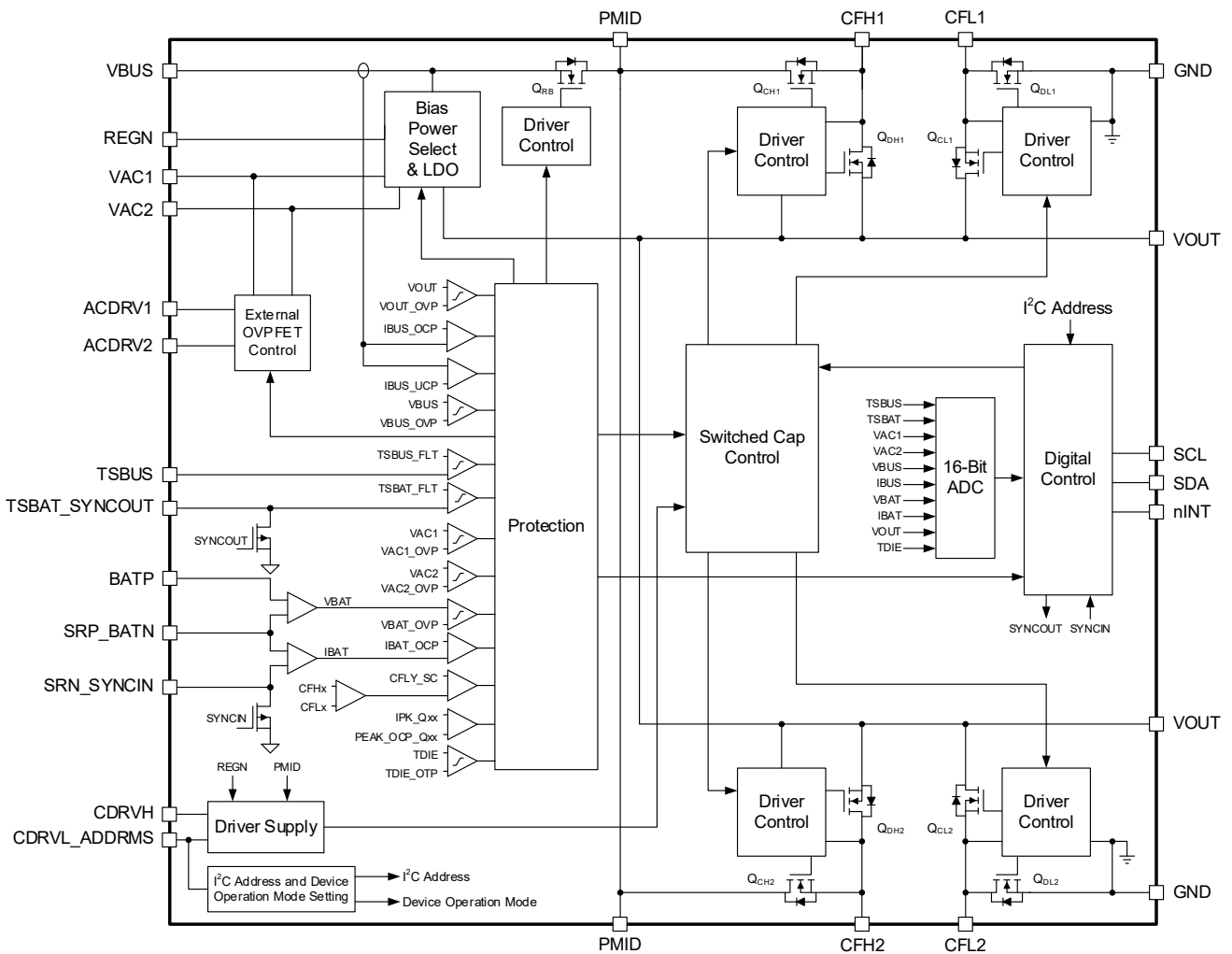


Figure 3. Functional Block Diagram



# I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger with Integrated Protection and Dual-Input Selector

SGM41604

## DETAILED DESCRIPTION

The SGM41604 is an efficient 8A switched-capacitor battery charging device with I<sup>2</sup>C control that can operate either in charge-pump voltage divider mode or in bypass mode. It can charge 1-cell Li-Ion or Li-polymer battery in a wide 3.6V to 12V input voltage range (VBUS) from smart wall adapters or wireless charger. The switched-capacitor architecture is optimized for 50% duty cycle to cut the input current to one-half of the battery current and reduce the wiring drops, losses and temperature rise in the application.

A two-channel switched-capacitor topology is used to reduce the required input capacitors, improve efficiency and minimize the output ripple. It supports dual input configuration through integrated MUX control and driver for external OVPFETs. It also allows single input with no external OVPFET or single OVPFET. Moreover, it supports two devices in parallel for higher power systems.

A high speed 16-bit ADC converter is also included to provide bus voltage, bus current, battery voltage, battery current, battery and cable connector temperature, and die temperature information for the charge management host via I<sup>2</sup>C serial interface.

### Charge-Pump Voltage Divider Mode

The charge-pump voltage divider mode operates with a fixed 50% duty cycle. Taking one of the two channels in the switched-capacitor as an example, the basic principle of operation is shown in Figure 4. In period 1, Q1 and Q3 are tuned on and V<sub>PMID</sub> charges the C<sub>FLY</sub> and the battery (in series) such that:

$$V_{CFLY} = V_{PMID} - V_{BAT} \quad (1)$$

In period 2, Q2 and Q4 are turned on and C<sub>FLY</sub> appears in parallel with the battery:

$$V_{CFLY} = V_{BAT} \quad (2)$$

Ignoring the small fluctuation of the capacitor and battery voltages in period 1 and 2 in steady state operation, Equation 1 and 2 can be combined to calculate capacitor voltage:

$$V_{CFLY} = V_{BAT} = V_{PMID}/2 \quad (3)$$

Ignoring small energy loss in each switching period, the input and output cycle-average powers are equal. Therefore,

$$V_{PMID} \times I_{BUS} = V_{BAT} \times I_{BAT} \quad (4)$$

or

$$I_{BUS} = I_{BAT}/2 \quad (5)$$

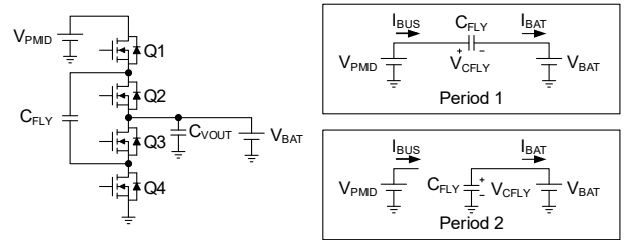


Figure 4. Voltage Divider Charger Operating Principle

Assuming no charge leakage path and considering R<sub>EFF</sub> as the effective input to output resistance (due to the switch on-resistances and C<sub>FLY</sub> losses), the divider can be modeled as shown in Figure 5. Using this model, the output voltage is half of the input voltage under no load conditions as explained before. The SGM41604 has two channels of such architecture operating at f<sub>sw</sub> frequency with 180° phase difference. Each channel provides I<sub>OUT</sub>/2 at the V<sub>OUT</sub> node, so:

$$V_{VOUT} = \frac{1}{2}V_{PMID} - \frac{1}{2}R_{EFF} \times I_{VOUT} \quad (6)$$

At low switching frequencies the capacitor charge sharing losses are dominant and R<sub>EFF</sub> ≈ 1/(4f<sub>sw</sub>C<sub>FLY</sub>). As frequency increases, R<sub>EFF</sub> finally approaches (R<sub>DS\_QCH</sub> + R<sub>DS\_QDH</sub> + R<sub>DS\_QCL</sub> + R<sub>DS\_QDL</sub>)/2.

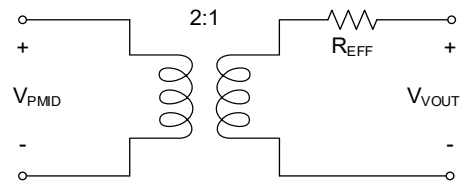


Figure 5. Model of Voltage Divider

The two-channel interleaved operation ensures a smooth input current and simplifies the noise filtering. The V<sub>OUT</sub> ripple can be estimated by first order approximation of C<sub>FLY</sub> voltage drop due to the discharge in the half period, plus the discharge drop during the short dead time.

Selecting high quality C<sub>FLY</sub> capacitors and proper switching frequency are the key factors for a well performing capacitor voltage divider. Switching frequency selection is a trade-off between efficiency and capacitor size. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance (R<sub>EFF</sub>). An optimum switching frequency can be found for any selected C<sub>FLY</sub> capacitor to minimize losses.

**DETAILED DESCRIPTION (continued)**

**Bypass Mode**

The SGM41604 is designed to operate in bypass mode when  $V_{VBUS}$  is close to the  $V_{VOUT}$ . When such valid voltage is present on VBUS, the device can enable bypass mode by setting  $EN\_BYPASS = 1$  and all switches between VBUS and VOUT are fully turned on while the other switches are kept off. When  $V_{VBUS}$  is near  $V_{VOUT}$ , the bypass mode offers the best efficiency and the device is capable of sourcing up to 5A. The bypass mode switched-capacitor charger is showed in Figure 6.

The output voltage is close to the  $V_{VBUS}$  minus a voltage drop caused by the on-resistances of the RBFET plus the two high-side switches of the two channels in parallel:

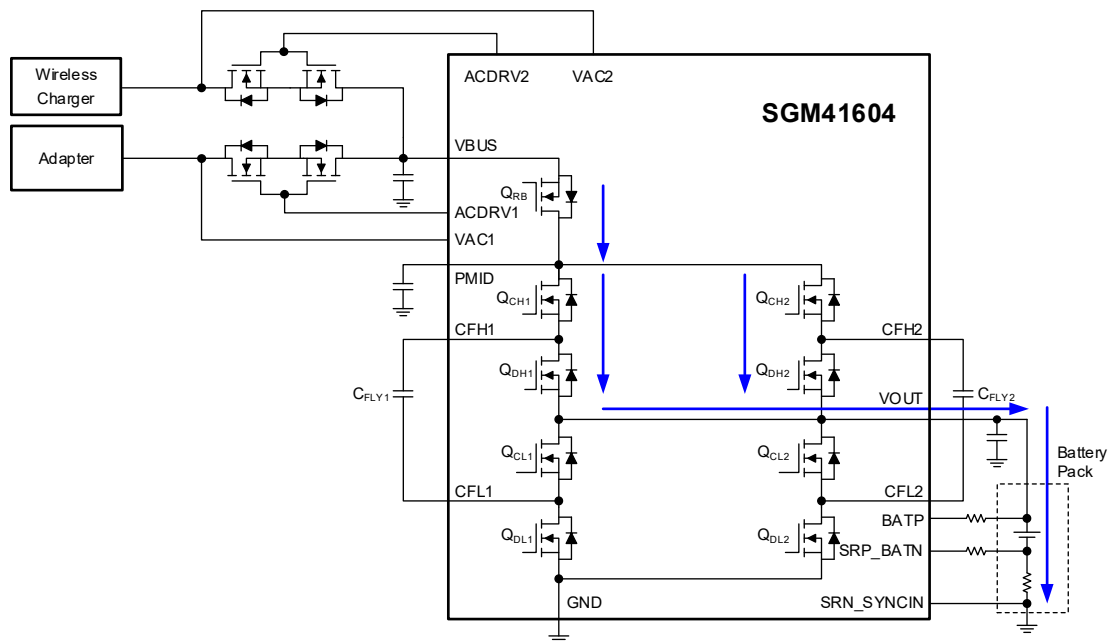
$$R_{EFF} \text{ (Bypass mode)} \approx R_{DS\_QRB} + (R_{DS\_QCH1} + R_{DS\_QDH1}) \parallel (R_{DS\_QCH2} + R_{DS\_QDH2}) \quad (7)$$

where  $R_{DS\_QXX}$  is the on-resistance of the switch  $Q_{XX}$ .

**Charging System**

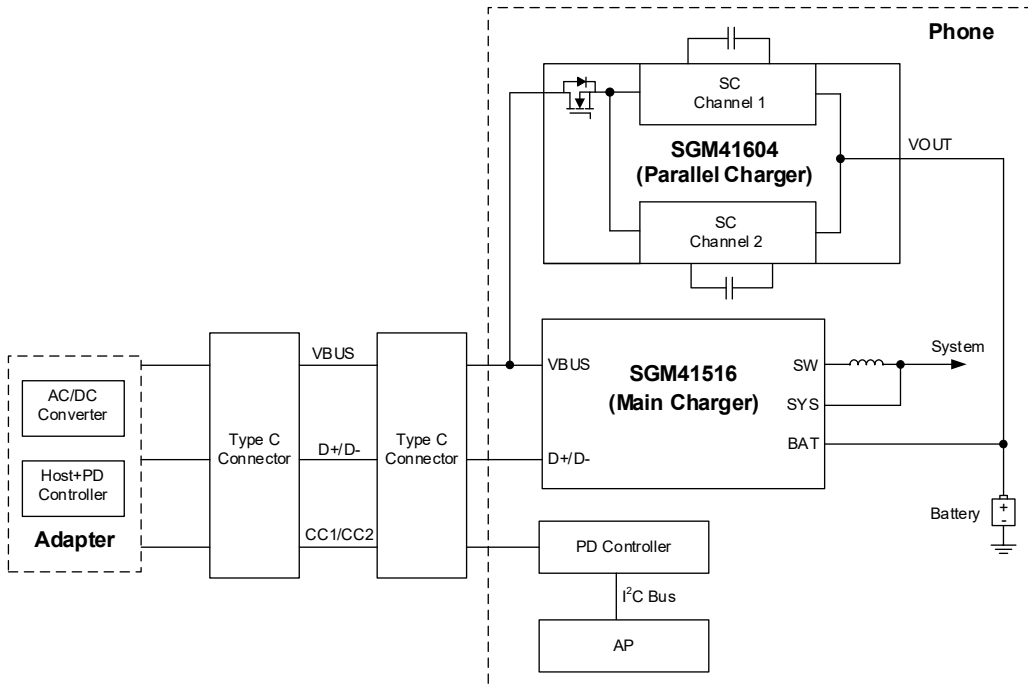
The SGM41604 is a slave charger device and needs a host. The host must set up all protection functions and disable the main charger before enabling the SGM41604. The host must monitor the nINT interrupts especially during high current charging. It must also communicate with the wall adapter to control the charge current.

Figure 7 shows the block diagram of a charge system using the SGM41604 along with other devices. In this system, the PD controller is used to communicate with adapter by PD protocol. When the smart wall adapter is inserted, the AP unit controls the switching charger (SGM41516) that powers the load system and the switched capacitor charger (SGM41604) that provides high current charging. The communication between those devices is through I<sup>2</sup>C interface.

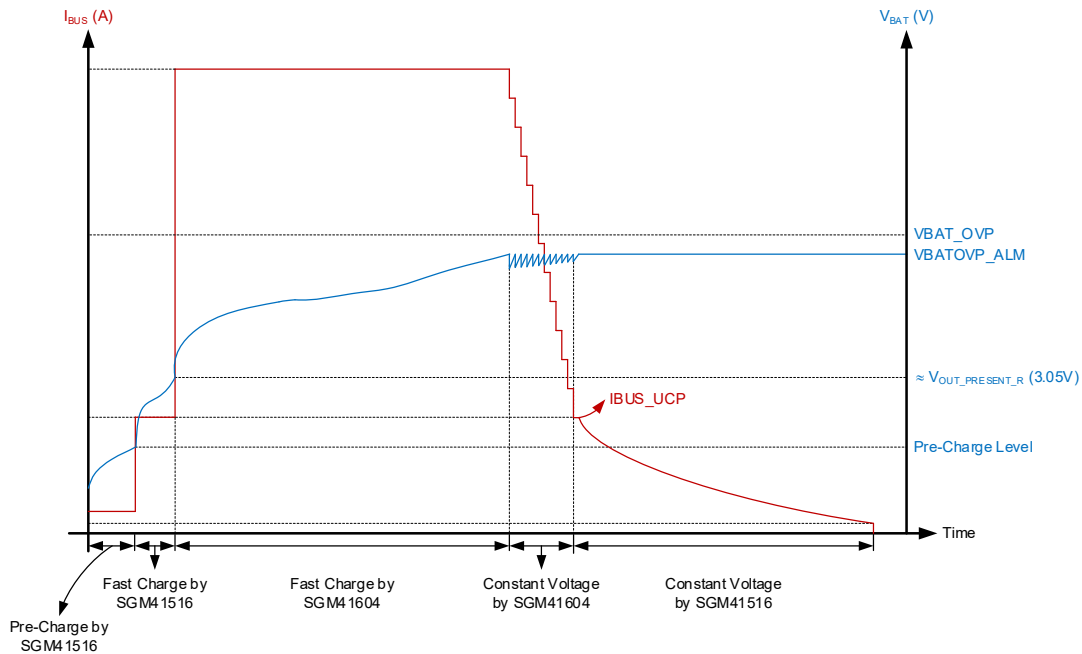


**Figure 6. SGM41604 Bypass Mode**

**DETAILED DESCRIPTION (continued)**



**Figure 7. SGM41604 Charging System Diagram**



**Figure 8. SGM41604 System Charging Profile**

## DETAILED DESCRIPTION (continued)

A typical charge profile for a high-capacity battery using switching charger and switched capacitor charger together is shown in Figure 8. During the trickle charge and pre-charge, the charging is controlled by the switching charger. Once the battery voltage reaches  $V_{OUT\_PRESENT\_R}$  (3.05V, TYP), the adapter can negotiate for a higher bus voltage and enable the SGM41604 for charging (bypass or voltage divider mode). Once the battery voltage approaches the  $V_{BATOV\_ALM}$  point, the SGM41604 will notify the AP to reduce the IBUS current, and the AP will negotiate with adapter for a lower bus voltage to effectively taper the current until a point where the IBUS current ramps down below  $I_{BUS\_UCP}$ .

### Startup Sequence

The SGM41604 is powered from the greater of VAC1, VAC2, VBUS or VOUT (VAC1 and VAC2 are used as sense inputs for adapter voltages as well). When  $V_{VOUT}$  rises above  $V_{OUT\_UVLO\_R}$ , or  $V_{VAC1}$ ,  $V_{VAC2}$  or  $V_{VBUS}$  rises above their respective UVLO rising threshold, the I<sup>2</sup>C interface is ready for communication and all the registers are reset to default values.

The device does not start charging after power-up, because by default the charger is disabled but the ADC can be enabled and the AP can read the system parameters before enabling charge. The charge can be enabled only if  $V_{VBUS} > V_{BUS\_PRESENT\_R}$  and  $V_{VOUT} > V_{OUT\_PRESENT\_R}$ .

### Device Power-Up from Battery without Input Source

To reduce the quiescent current and maximize the battery run time when it is the only available source, the REGN LDO and most of the sensing circuits are turned off, except VAC1\_PRESENT, VAC2\_PRESENT, BUS\_PRESENT and VOUT\_PRESENT functions.

### Device Power-Up from Input Source

When an input source is plugged-in and the conditions of  $V_{VBUS} > V_{BUS\_PRESENT\_R}$  and  $V_{VOUT} > V_{OUT\_PRESENT\_R}$  are valid, the AP must initialize all protections to the desired thresholds before enabling charge. The protection thresholds that need

to be set are VAC1\_OVP, VAC2\_OVP, VBUS\_OVP, IBUS\_OCP, IBUS\_UCP, VOUT\_OVP, VBAT\_OVP, IBAT\_OCP, TSBUS\_FLT, TSBAT\_FLT and TDIE\_OTP. If one of the protection trigger conditions is met, the charger stops switching. It will also be turned off the corresponding external OVPFETs when VAC1\_OVP or VAC2\_OVP or VBUS\_SCP event occurs.

After setting protections, the VBUS voltage is checked to be between VBUS\_ERRLO and VBUS\_ERRHI to allow forward charge mode operation. When the AP configures bypass or voltage divider mode by setting EN\_BYPASS = 1 or 0 and then set CHG\_EN = 1, charging is enabled and current flows into the battery, and CONV\_ACTIVE\_STAT bit is set to 1 to indicate charging is active. Then raising the VBUS voltage will increase the battery charge current. When the converter is on, any command to change the charge mode is ignored. To do so, the charging must be disabled first, and then the charge mode can be changed by I<sup>2</sup>C serial interface.

### Device HIZ State

The HIZ mode is activated when the AP sets EN\_HIZ bit from 0 to 1. When the SGM41604 enters HIZ mode, the charging stops, ADC conversion discontinues, ACDRV and REGN LDO are turned off regardless of the presence of the adapter or absence of any fault conditions. To exit HIZ mode, the AP should set EN\_HIZ to 0, or the device POR occurs.

### REGN Management

REGN provides the power required for the analog section. When  $V_{VBUS}$  rises above  $V_{BUS\_PRESENT\_R}$ , REGN is powered up and ramps up to 5V (TYP). A 4.7μF or larger capacitor is required on the REGN pin.

When the faults, including VBUS\_OVP, VBAT\_OVP, VOUT\_OVP, IBUS\_OCP, IBAT\_OCP, IBUS\_UCP, VBUS\_SCP, VAC1\_OVP, VAC2\_OVP, TSBUS\_FLT, TSBAT\_FLT and TDIE\_OTP, are triggered, the converter switching stops and CHG\_EN bit is reset to 0, but the REGN LDO remains powered up. Refer to the device protection section for more details.

## DETAILED DESCRIPTION (continued)

### Dual Input Power Path Management

The SGM41604 features two ACDRV pins to drive two sets of back-to-back N-channel MOSFETs, which select and manage the input power from two different input sources (such as wired and wireless input sources). Each set of back-to-back N-channel FETs consists of an input N-channel MOSFET (ACFET) and a reverse-blocking N-channel MOSFET (RBFET). During POR procedure, the internal bias circuit detects whether the ACDRVx pin is shorted to GND to sense whether the ACFET-RBFET are connected, and then updates the ACRB1\_CONFIG\_STAT and ACRB2\_CONFIG\_STAT bits to indicate the connection status of ACFET-RBFET. If the external back-to-back N-channel FETs are not populated in the schematic, then tie corresponding VAC pin to VBUS and short ACDRVx to GND. The device supports 4 input configurations: single input without any external FET, single input with only one ACFET, dual input with one set of ACFET-RBFET, and dual input with two sets of ACFET-RBFET. Detailed descriptions of the power-up sequences for different applications are provided below.

### ACDRV Turn-on Condition

For most of the 4 configurations, the ACDRV controls the input power path for both SGM41604 and main charger. When one or both input power sources are plugged in (not in OTG mode), the ACDRV can be turned on when all of the following conditions are met:

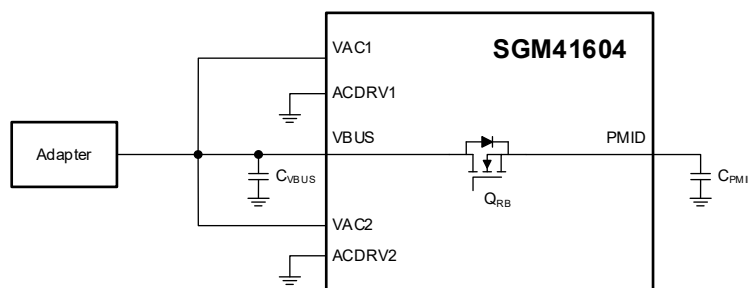
1. The corresponding ACFET-RBFET is populated: VAC is connected to the input power and ACDRV is not short to GND.
2.  $V_{VAC}$  exceeds  $V_{AC\_PRESENT\_R}$  and not higher than  $V_{AC\_OVP}$  thresholds.
3. DIS\_ACDRV\_BOTH is not set to 1.
4. Not in HIZ mode: EN\_HIZ is not set to 1.
5.  $V_{VBUS}$  is below  $V_{BUS\_PRESENT\_F}$  threshold.

### Single Input without ACFET-RBFET

In this configuration, the SGM41604 is not responsible for controlling the external OVPFET. VAC1 and VAC2 are both connected to VBUS directly, while ACDRV1 and ACDRV2 are both shorted to GND. The following table summarizes the related pin connections and the control function of relevant registers, as well as the status bits.

**Table 1. Single Input without External OVPFET**

Input Configuration	Single Input
External FET Connection	No external FET
Input Sense Pin Connection	VAC1 and VAC2 tied to VBUS
ACDRV Pin Connection	ACDRV1 and ACDRV2 short to GND
ACDRV1_STAT	0
ACDRV2_STAT	0
DIS_ACDRV_BOTH	1
ACRB1_CONFIG_STAT	0 = ACFET1-RBFET1 is not placed
ACRB2_CONFIG_STAT	0 = ACFET2-RBFET2 is not placed
EN_HIZ	No impact on ACDRV



**Figure 9. Single Input without ACFET-RBFET**

**DETAILED DESCRIPTION (continued)**

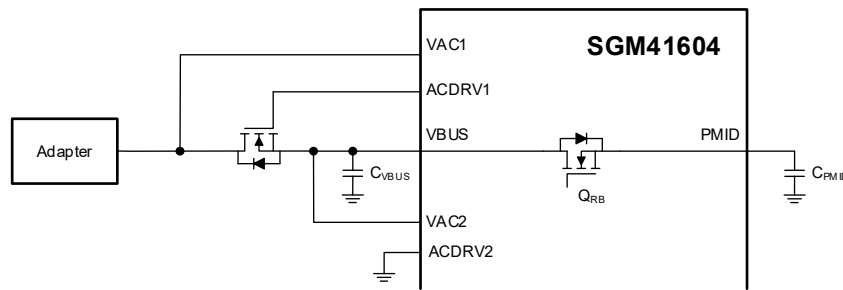
**Single Input with ACFET1**

In this configuration, only one input N-channel MOSFET for VAC1 (ACFET1) is placed. RBFET1 and ACFET2-RBFET2 are not used. VAC1 and ACDRV1 are connected to the drain and the gate of ACFET1, respectively. VAC2 is tied to VBUS,

and ACDRV2 is shorted to GND. This structure supports single input from VAC1. The following table summarizes the related pin connections and the control function of relevant registers, as well as the status bits.

**Table 2. Single Input with Single OVPFET**

Input Configuration	Single Input
External FET Connection	Only ACFET1, no RBFET1 and ACFET2-RBFET2
Input Sense Pin Connection	VAC1 tied to the input source, VAC2 short to VBUS
ACDRV Pin Connection	ACDRV1 tied to the gate of ACFET1, ACDRV2 short to GND
ACDRV1_STAT	1 = ACDRV1 is ON 0 = ACDRV1 is OFF
ACDRV2_STAT	0
DIS_ACDRV_BOTH	1 = Force ACDRV1 OFF 0 = ACDRV1 can be turned on when the activation conditions of ACDRV are valid
ACRB1_CONFIG_STAT	1 = ACFET1 is placed
ACRB2_CONFIG_STAT	0 = ACFET2-RBFET2 is not placed
EN_HIZ	1 = Enter HIZ mode, force ACDRV1 OFF 0 = Exit HIZ mode, ACDRV1 can be turned on when the activation conditions of ACDRV are valid



**Figure 10. Single Input with ACFET1**

## DETAILED DESCRIPTION (continued)

### Dual Input with ACFET1-RBFET1

In this configuration, only one set of back-to-back N-MOSFET for VAC1 is placed. VAC1 is connected to the drain of ACFET1. ACDRV1 is connected to the common gate of ACFET1-RBFET1. VAC2 is tied to VBUS and ACDRV2 is shorted to GND. This structure is able to support single input from VAC1. The following table summarizes the related pins connection and the control function of relevant registers, as well as the status bits.

### Input Source Swap with ACFET1-RBFET1

To switch the input source from VAC1 to wireless input, the AP should turn off ACDRV1 by setting DIS\_ACDRV\_BOTH = 1 to avoid that the two input sources are shorted together. After the ACFET1-RBFET1 is turned off and  $V_{VBUS}$  drops below  $V_{BUS\_PRESENT\_F}$ , the AP can enable the wireless input.

To switch the input source from wireless input to VAC1, the AP should remove or disable the wireless input first, and then set DIS\_ACDRV\_BOTH = 0 to turn on ACDRV1 after  $V_{VBUS}$  drops below  $V_{BUS\_PRESENT\_F}$ .

Table 3. Dual Input with ACFET1-RBFET1

Input Configuration	Dual Input
External FET Connection	ACFET1-RBFET1, no ACFET2-RBFET2
Input Sense Pin Connection	VAC1 tied to the input source, VAC2 short to VBUS
ACDRV Pin Connection	ACDRV1 tied to the common gate of ACFET1-RBFET1, ACDRV2 short to GND
ACDRV1_STAT	1 = ACDRV1 ON 0 = ACDRV1 OFF
ACDRV2_STAT	0
DIS_ACDRV_BOTH	1 = Force ACDRV1 OFF 0 = ACDRV1 can be turned on when the activation conditions of ACDRV are valid
ACRB1_CONFIG_STAT	1 = ACFET1-RBFET1 is placed
ACRB2_CONFIG_STAT	0 = ACFET2-RBFET2 is not placed
EN_HIZ	1 = Enter HIZ mode, force ACDRV1 OFF 0 = Exit HIZ mode, ACDRV1 can be turned on when the activation conditions of ACDRV are valid

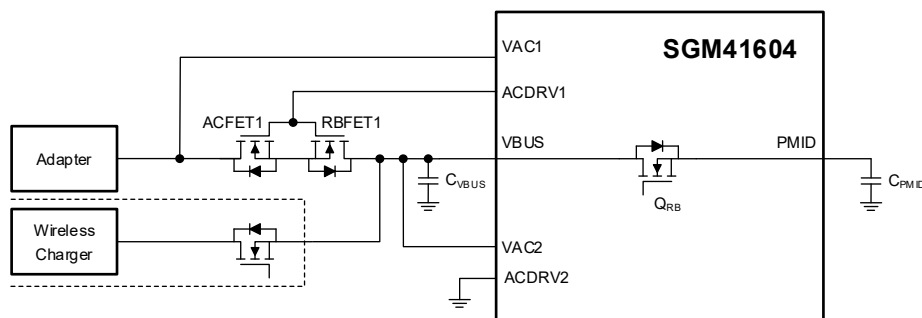


Figure 11. Dual Input with ACFET1-RBFET1

### Dual Input with ACFET1-RBFET1 and ACFET2-RBFET2

In this configuration, both sets of back-to-back N-MOSFET for VAC1 and VAC2 are placed and SGM41604 supports dual input source from VAC1 and VAC2. The following table summarizes the related pin connections and the control function of relevant registers, as well as the status bits.

### Input Source Swap with ACFET1-RBFET1 and ACFET2-RBFET2

Three examples are provided below to illustrate the process of swapping the input source from VAC1 to VAC2 (the procedure for swapping from VAC2 to VAC1 is similar).

#### VAC2 is plugged in after VAC1 is removed

1. When VAC1 is removed and  $V_{VAC1}$  drops below  $V_{AC\_PRESENT\_F}$ , ACDRV1 will be turned off automatically, and  $V_{VBUS}$  will slowly drop below  $V_{BUS\_PRESENT\_F}$ . The AP can write 1 to the VBUS pull-down resistor enable bit (VBUS\_PDN\_EN) as needed to expedite the discharge for VBUS.

# I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger with Integrated Protection and Dual-Input Selector

**SGM41604**

## DETAILED DESCRIPTION (continued)

2. After VAC1 is removed, VAC2 is plugged in, and then the device will turn on ACDRV2 until V<sub>VBUS</sub> drops below V<sub>BUS\_PRESENT\_F</sub>. In this situation, the swapping procedure from VAC1 to VAC2 is controlled by SGM41604 and does not require intervention from the AP.

**Both VAC1 and VAC2 are valid, the AP controls the swap from VAC1 to VAC2**

1. Both VAC1 and VAC2 are valid, ACDRV1 has been turned on, and ACDRV2 is off.
2. The AP can set REG0x0F[1:0] (ACDRV1\_STAT, ACDRV2\_STAT) from 10b to 01b, the ACDRV1 will be turned off and then ACDRV2 will be turned on until V<sub>VBUS</sub> drops below V<sub>BUS\_PRESENT\_F</sub>.

In this situation, the on/off states of the two sets of back-to-back N-MOSFET are controlled by the AP. The AP can write DIS\_ACDRV\_BOTH = 1 to turn off both two sets of back-to-back N-MOSFET.

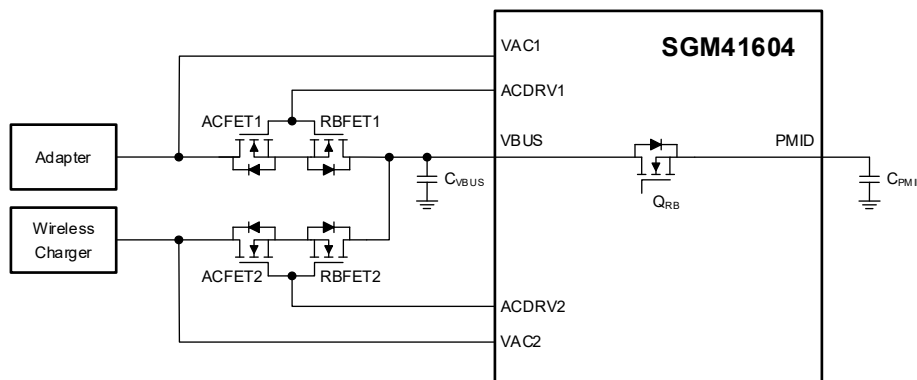
**If VAC1 becomes invalid when ACDRV1 is on, the device will automatically swap to VAC2**

1. Both VAC1 and VAC2 are valid, ACDRV1 has been turned on, and ACDRV2 is off.
2. When VAC1 becomes invalid (V<sub>VAC1</sub> drops below V<sub>VAC\_PRESENT\_F</sub> or rises above V<sub>VAC\_OVP\_R</sub>), the device will turn off ACDRV1, and then turn on ACDRV2 until V<sub>VBUS</sub> drops below V<sub>BUS\_PRESENT\_F</sub>.

In this situation, the on/off state of the two sets of back-to-back N-MOSFET is controlled by SGM41604.

**Table 4. Dual Input with Both ACFET1-RBFET1 and ACFET2-RBFET2**

Input Configuration	Dual Input
External FET Connection	ACFET1-RBFET1, ACFET1-RBFET2
Input Sense Pin Connection	VAC1 tied to input source 1, VAC2 tied to input source 2
ACDRV Pin Connection	ACDRV1 tied to the common gate of ACFET1-RBFET1 ACDRV2 tied to the common gate of ACFET2-RBFET2
ACDRV1_STAT	1 = ACDRV1 ON 0 = ACDRV1 OFF In dual input configuration, the AP can use this bit to swap the input source if both input sources are valid
ACDRV2_STAT	1 = ACDRV2 ON 0 = ACDRV2 OFF In dual input configuration, the AP can use this bit to swap the input source if both input sources are valid
DIS_ACDRV_BOTH	1 = Force both ACDRV to turn off, both ACDRV1_STAT and ACDRV2_STAT become 0 0 = ACDRV1 or ACDRV2 can be turned on when the activation conditions of ACDRV are valid If VAC1 and VAC2 become valid at the same time, ACDRV1 will be turned on with a higher priority, and ACDRV2 will be forcibly turned off
ACRB1_CONFIG_STAT	1 = ACFET1-RBFET1 is placed
ACRB2_CONFIG_STAT	1 = ACFET2-RBFET2 is placed
EN_HIZ	1 = Enter HIZ mode, force both ACDRV1 and ACDRV2 to turn off 0 = Exit HIZ mode, ACDRV1 or ACDRV2 can be turned on when the activation conditions of ACDRV are valid If VAC1 and VAC2 become valid at the same time, ACDRV1 will be turned on with a higher priority, and ACDRV2 will be forcibly turned off



**Figure 12. Dual Input with ACFET1-RBFET1 and ACFET2-RBFET2**



## DETAILED DESCRIPTION (continued)

### OTG Mode Operation

If the switching charger works in OTG mode and the two sets of back-to-back N-MOSFET is controlled by SGM41604, they must be turned on/off manually, depending on which port is desired for OTG output. The corresponding external OVPFETs will be turned off when VAC1\_OVP, VAC2\_OVP, or VBUS\_OVP fault occurs.

To enter OTG mode, the AP needs to follow the steps outlined below:

1. The AP enables OTG mode for switching charger.
2. The AP writes EN\_OTG = 1.
3. SGM41604 sets DIS\_ACDRV\_BOTH = 1 automatically.
4. The AP writes DIS\_ACDRV\_BOTH = 0 to allow ACDRV to be enabled, and then writes ACDRV1\_STAT = 1 or ACDRV2\_STAT = 1 or both, depending on which port is desired for OTG output until VBUSPRESENT\_STAT becomes 1.
5. If VAC1\_OVP or VAC2\_OVP or VBUS\_OVP fault occurs, SGM41604 will turn off the corresponding external OVPFETs but will not reset EN\_OTG. After the fault is cleared, the AP needs to write ACDRV1\_STAT = 1 or ACDRV2\_STAT = 1 or both to enable OTG output again. It is recommended to set VAC1\_OVP and VAC2\_OVP to the same threshold in OTG mode.
6. To disable OTG output, the AP needs to set ACDRV1\_STAT = 0 or ACDRV2\_STAT = 0 or DIS\_ACDRV\_BOTH = 1, and can write 1 to the VAC1/VAC2/VBUS pull-down resistor enable bits (VAC1\_PDN\_EN/VAC2\_PDN\_EN/VBUS\_PDN\_EN) as needed to discharge the residual energy.

To exit OTG mode, the AP needs to follow the steps outlined below:

1. The AP disables OTG mode for switching charger.
2. The AP writes 1 to the VAC1/VAC2/VBUS pull-down resistor enable bits (VAC1\_PDN\_EN/VAC2\_PDN\_EN/VBUS\_PDN\_EN) as needed to discharge the residual energy.
3. After VBUS and VAC are discharged, the AP writes ACDRV1\_STAT = 0 or ACDRV2\_STAT = 0 or DIS\_ACDRV\_BOTH = 1 to turn off ACDRV.
4. The AP writes EN\_OTG = 0 to exit OTG mode.

**Table 5. Selection for I<sup>2</sup>C Address and Operation Mode**

Resistor Value to GND on CDRVL_ADDRMS (kΩ)	I <sup>2</sup> C Address	Configuration
>75.0	0x65	Standalone
6.19	0x67	Standalone
8.02	0x66	Secondary for Parallel Charging
10.2	0x66	Primary for Parallel Charging
13.3	0x66	Standalone
17.8	0x67	Secondary for Parallel Charging
27.4	0x65	Primary for Parallel Charging

### ADC

The SGM41604 integrates a fast 10-channel, 16-bit ADC converter to monitor input/output currents and voltages, as well as the temperature of the device, battery, and cable connector. The ADC is controlled by the ADC\_CONTROL 1 and ADC\_CONTROL 2 registers. Setting the ADC\_EN bit to 1 enables the ADC. This bit can be used to turn off the ADC and save power when it is not needed. The ADC\_RATE bit allows choosing continuous conversion or 1-shot conversion mode. The ADC\_AVG bit is utilized to enable or disable ADC averaging (disabled default), and the ADC\_AVG\_INIT bit can be used to choose the average initial value (use an existing register value or a new value). The ADC operates independently of the faults, unless the AP sets the ADC\_EN bit to 0.

The ADC can operate if  $V_{VAC} > V_{VAC\_PRESENT\_R}$  or  $V_{VBUS} > V_{VBUS\_PRESENT\_R}$  or  $V_{VOUT} > V_{VOUT\_PRESENT\_R}$  condition is valid. Otherwise, the ADC conversion is postponed until one of them is satisfied. The ADC readings are valid only for DC values and not for transients.

By default, all ADC channels are converted in continuous conversion mode except the channels disabled by the ADC\_CONTROL 1 and ADC\_CONTROL 2 registers. If the 1-shot conversion mode is selected, the ADC\_DONE\_FLAG bit is set to 1 when all channels are converted, then the ADC\_EN bit is reset to 0. In the continuous conversion mode, the ADC\_DONE\_FLAG bit is set to 0.

### CDRVH and CDRVL\_ADDRMS Functions

A 0.22μF MLCC capacitor is required between the CDRVH and CDRVL\_ADDRMS pins to provide driver supply. In addition, the CDRVL\_ADDRMS pin is used to set the default I<sup>2</sup>C address and operation mode of the device during the POR procedure. Refer to Table 5 to choose the appropriate resistor from CDRVL\_ADDRMS pin to GND for desired configuration. It is recommended to utilize a surface mount resistor with a tolerance of either ±1% or ±2%. After POR procedure, the AP can read the operation mode of the device from MS[1:0] bits in CHARGER\_CONTROL 5 register.

**DETAILED DESCRIPTION (continued)**

**Parallel Operation**

To achieve higher charging current, it is feasible to use two devices in parallel, with one configured in primary mode and the other in secondary mode. Using two devices in parallel can also enable each device to operate at a lower charging current, resulting in the higher efficiency compared with single device at the same total charging current. During POR procedure, the CDRVL\_ADDRMS pin is used to determine the operation mode of the device. Refer to Table 5 for selecting appropriate resistor from CDRVL\_ADDRMS pin to GND.

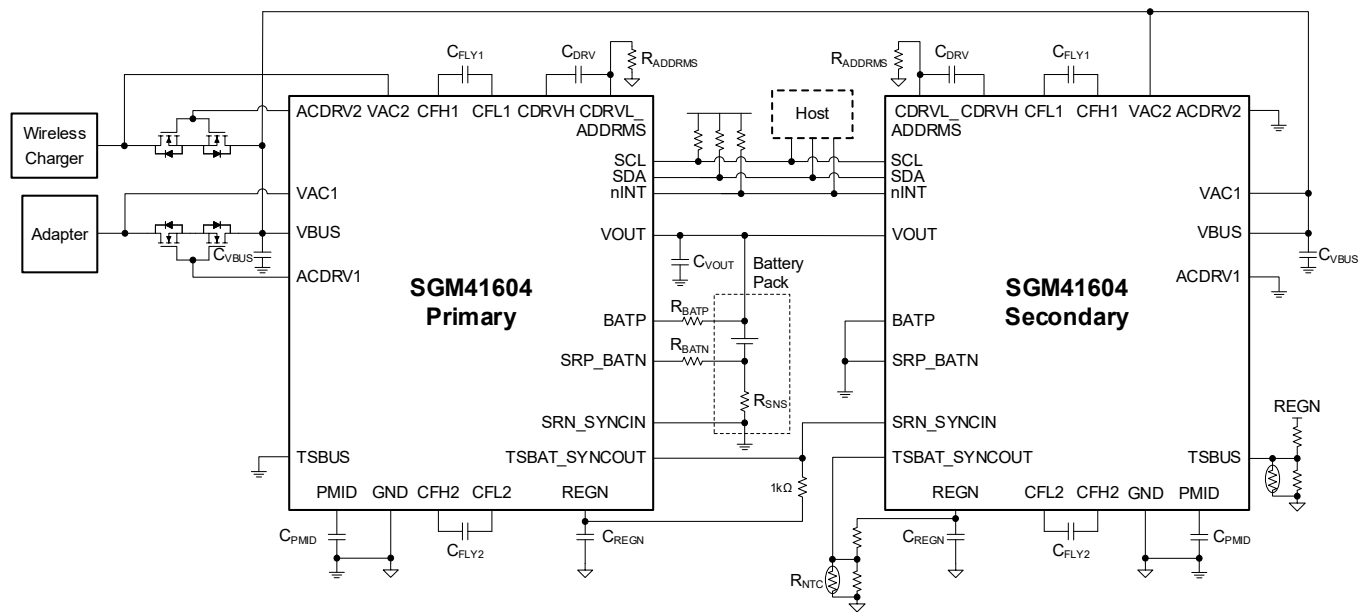
The parallel charging configuration for dual-charger is shown in Figure 13. When set as the primary, the TSBAT\_SYNCOUT pin functions as the synchronization signal output pin, while the SRN\_SYNCIN pin operates as SRN. When set as the secondary, the SRN\_SYNCIN pin functions as the synchronization signal input pin, and the TSBAT\_SYNCOUT pin operates as TSBAT. The TSBAT\_SYNCOUT pin of the primary should be tied to the SRN\_SYNCIN pin of the secondary, and should be pulled up to REGN of the primary through a 1kΩ resistor. The external OVPFETs are controlled by the primary, and the ACDRVx pins of the secondary should short to GND.

The parallel charging configuration can operate in both bypass mode and voltage divider mode. The distribution of current between the primary and secondary is influenced by the loop impedance, and the chargers do not automatically balance it. To achieve current balance, it is essential to design the board layout with maximum symmetry.

**nINT Pin, STAT, Flag and Mask Bits**

The nINT pin is an open-drain output and must be pulled up to a logic high rail. It is pulled low with a duration of  $t_{INT}$  to notify the AP when it is triggered by an event. See the register map for all event flag and control bits.

When an event occurs, a nINT signal is sent to the AP, and the corresponding status and flag bits are set to 1. The flag bit can be read to clear but the status bit remains as 1 if the event is still present. The nINT signal is not sent again if an event is still present after the flag bit is read cleared, unless another kind of event occurs. If an event mask bit is set, that event will not send nINT signal, but the flag bit is still updated independent of the mask bit.



**Figure 13. Parallel Operation of SGM41604**

## DETAILED DESCRIPTION (continued)

### Input Over-Voltage Protection (VAC1\_OVP, VAC2\_OVP)

The SGM41604 monitors the adapter voltage on the VAC1/VAC2 pin to use the ACDRV1/ACDRV2 output to control the external OVPFETs respectively. Taking VAC1\_OVP as an example, the VAC1 over-voltage protection circuit is enabled if  $V_{VAC1}$  rises above  $V_{AC\_PRESENT\_R}$ . If  $V_{VAC1}$  is above  $V_{AC\_PRESENT\_R}$  for at least  $t_{VAC\_IN\_DEG}$  time and  $DIS\_ACDRV\_BOTH = 0$ , the ACDRV1 will output drive signal to turn on the ACFET1-RBFET1. If the  $V_{AC1}$  reaches the  $V_{AC\_OVP\_R}$  threshold, the gate voltage starts to drop and eventually the ACFET1-RBFET1 is fully turned off. Figure 14 shows the VAC\_OVP and ACDRV operation timings. The  $V_{AC\_OVP\_R}$  threshold can be set by I<sup>2</sup>C serial interface. The adapter voltage must never exceed the absolute maximum rating of the VAC1/VAC2 pin and the external OVPFETs.

### Input Short-Circuit Protection (VBUS\_SCP)

The VBUS\_SCP function monitors the VBUS pin for short-circuit. This function is enabled if the external OVPFETs are turned on or if  $V_{VBUS}$  rises above  $V_{BUS\_PRESENT\_R}$ . If the  $V_{VBUS}$  falls below 2V, charging is stopped. CHG\_EN bit is reset to 0 (disable). Also, BUSSCP\_STAT and BUSSCP\_FLAG bits are set to 1, and an INT pulse is asserted. The device will wait for 760ms before automatically re-enabling and initiating startup sequence.

### VBUS Charge Voltage Range (VBUS\_ERRLO & VBUS\_ERRHI)

The VBUS\_ERRLO and VBUS\_ERRHI functions are included to avoid problems due to wrong VBUS setting for forward charging. In bypass mode or in voltage divider charging mode, if  $V_{VBUS}$  is beyond the range between  $V_{BUS\_ERRLO}$  and  $V_{BUS\_ERRHI}$ , CHG\_EN will still be 1. Once  $V_{VBUS}$  is within the charge range, charging will start and VBUS\_ERRLO and VBUS\_ERRHI functions will be disabled.

### Input, Output and Battery Over-Voltage Protection (VBUS\_OVP, VOUT\_OVP and VBAT\_OVP)

The VBUS\_OVP, VOUT\_OVP and VBAT\_OVP functions detect input and output voltage conditions. If either input or output voltage is higher than the protection threshold, the device stops charging and resets CHG\_EN bit to 0 (disable). The VBUS\_OVP function monitors VBUS pin voltage. The VOUT\_OVP function monitors VOUT pin voltage. The VBAT\_OVP uses B ATP and SRP\_BATN remote sense pins to monitor differential voltage between the battery terminals. To minimize the risk of battery terminal short in the manufacturing process, two 100Ω resistors are needed to connect in series to the B ATP and SRP\_BATN pins respectively. The VBUS\_OVP, VOUT\_OVP and VBAT\_OVP thresholds can be set by I<sup>2</sup>C serial interface.

### Input and Battery Over-Current Protection (IBUS\_OCP and IBAT\_OCP)

The IBUS\_OCP function monitors the input current via  $Q_{RB}$ . If CHG\_EN bit are set to enable charge, the  $Q_{RB}$  is turned on and the IBUS\_OCP function starts detecting the input current. If the  $I_{BUS}$  reaches  $I_{BUS\_OCP}$  threshold, the device stops charging and resets CHG\_EN bit to 0 (disable). The battery current is monitored by the voltage across an external series shunt resistor. This differential voltage is measured between SRP\_BATN and SRN\_SYNCIN pins. If  $I_{BAT\_OCP}$  threshold is reached, the device stops charging and resets CHG\_EN bit to 0 (disable). The IBUS\_OCP and IBAT\_OCP thresholds can be set by I<sup>2</sup>C serial interface.

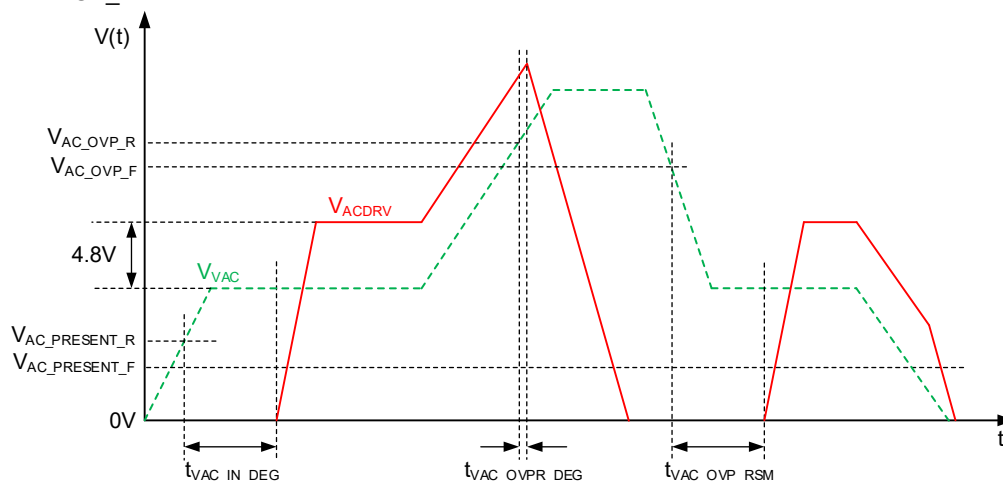


Figure 14. ACDRV Operation Timing

## DETAILED DESCRIPTION (continued)

### Input Under-Current Protection (IBUS\_UCP)

The IBUS\_UCP function detects the input current via Q<sub>RB</sub> during forward charging. After charging is started and soft-start time expired, if I<sub>BUS</sub> is below I<sub>BUS\_UCP</sub> with t<sub>IBUS\_UCP\_DEG</sub> deglitch time, the charging will be stopped and CHG\_EN bit is reset to 0 (disable). The t<sub>IBUS\_UCP\_DEG</sub> timer can be set by I<sup>2</sup>C serial interface.

### CFLY Diagnosis (CFLY\_SHORT)

The CFLY diagnosis function identifies the health of flying capacitors before and during voltage divider switching (charging). The device initialization process is started after CHG\_EN bit is set to 1. When V<sub>VBUS</sub> and V<sub>BAT</sub> are in the charge range, the flying capacitors in both channels are pre-charged. A CFLY short-circuit is detected if they cannot be charged, and the voltage between V<sub>CFHX</sub> and V<sub>CFLX</sub> remains below (V<sub>VOUT</sub> - 0.6V). If so, the initialization process is stopped and CHG\_EN bit is reset to 0 (disable). Even if CFLY capacitors pass the short-circuit test in the initialization process, the CFLY diagnosis function remains active and whenever a V<sub>CFLY</sub> voltage falls below (V<sub>VOUT</sub> - 0.6V), the operation is stopped and CHG\_EN bit is reset to 0 (disable). The CFLY\_SHORT\_FLAG bit is set to 1 and an INT pulse is generated as well. During a CFLY short-circuit event, other protection events such as IBUS\_OCP, VBAT\_OVP or PEAK\_OCP may occur.

### Converter Peak Over-Current Protection (PEAK\_OCP)

The PEAK\_OCP function monitors the converter switch operating currents. If the Q<sub>CLX</sub> or Q<sub>DLX</sub> current reaches switch OCP threshold (I<sub>CONV\_OCP</sub>) during charging, the charging is stopped and CHG\_EN bit is reset to 0.

### TDIE Over-Temperature Protection (TDIE\_OTP)

The TDIE\_OTP function prevents operation in over-temperature condition. The die temperature is monitored and if the T<sub>DIE\_OTP\_R</sub> threshold is reached, the charging is stopped and CHG\_EN bit is reset to 0 (disable). The startup sequence cannot be initiated again until the die temperature falls down with a 30°C hysteresis. The TDIE\_OTP threshold can be set by I<sup>2</sup>C serial interface.

### Battery and Cable Connector Temperature Monitoring (TSBAT\_FLT and TSBUS\_FLT)

The SGM41604 monitors battery and cable connector temperature through the TSBAT\_SYNCOUT and TSBUS pins, which are connected to the external resistor divider that is pulled up to REGN. A negative coefficient thermistor (NTC) is needed in parallel with the low-side resistor. When the

voltage on the TSBUS or TSBAT\_SYNCOUT pin drops below the specific threshold, it indicates a "hot" temperature condition. In response, the device will stop charging and reset CHG\_EN to 0. The startup sequence cannot be initiated again until the battery or cable connector temperature fall down, which resulting a voltage rising on TSBAT\_SYNCOUT or TSBUS pin. The TSBUS\_FLT and TSBAT\_FLT thresholds can be set by I<sup>2</sup>C serial interface.

Take TSBAT\_SYNCOUT pin as an example, the external bias resistors network is shown as Figure 15. The selection of R<sub>T1</sub> and R<sub>T2</sub> resistors depends on the NTC utilized. For a 10kΩ NTC, R<sub>T1</sub> and R<sub>T2</sub> should be 10kΩ resistors. If a 100kΩ NTC is selected, choose 100kΩ resistors as R<sub>T1</sub> and R<sub>T2</sub>.

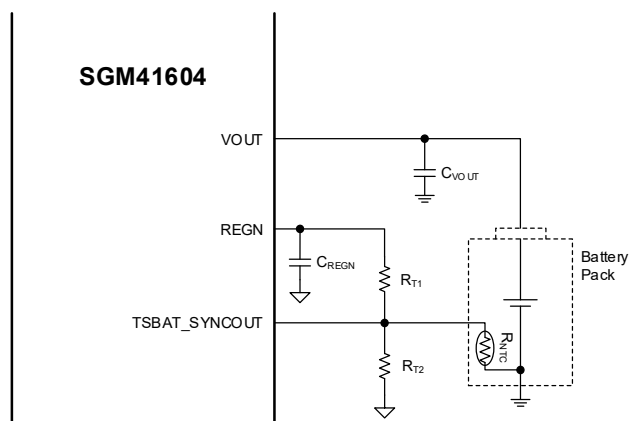


Figure 15. TSBAT\_SYNCOUT Thermistor and Bias Network

The voltage percentage of the TSBUS and TSBAT\_SYNCOUT pin ( $V_{TS}/V_{REGN} \times 100\%$ ) may vary from 0% to 50%, and the voltage on the TSBUS and TSBAT\_SYNCOUT pin is determined by the following equation:

$$V_{TSBUS \text{ or } TSBAT} (V) = \frac{1}{R_{T1} + \frac{1}{\left(\frac{1}{R_{NTC}} + \frac{1}{R_{T2}}\right)}} \times V_{REGN} \quad (8)$$

The voltage percentage of the TSBUS and TSBAT\_SYNCOUT pin is determined by the following equation.

$$TSBUS \text{ or } TSBAT (\%) = \frac{1}{R_{T1} + \frac{1}{\left(\frac{1}{R_{NTC}} + \frac{1}{R_{T2}}\right)}} \quad (9)$$

In addition, a TSBUS\_TSBAT\_ALM warning interrupt will be sent to notify the AP if the voltage percentage of TSBUS falls below TS<sub>BUS\_FLT\_F</sub> plus 5% or the voltage percentage of TSBAT falls below TS<sub>BAT\_FLT\_F</sub> plus 5%.

# I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger with Integrated Protection and Dual-Input Selector

SGM41604

## REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

### I<sup>2</sup>C Register Address Map

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
MS	--	--	--	0x12[1:0]	--	--
DEVICE_REV	--	--	--	0x22[7:4]	--	--
DEVICE_ID	--	--	--	0x22[3:0]	--	--
REG_RST	--	--	--	--	0x0F[7]	--
EN_HIZ	--	--	--	--	0x0F[6]	--
EN_OTG	--	--	--	--	0x0F[5]	--
CHG_EN	0x17[6]	0x1C[6]	0x21[6]	--	0x0F[4]	--
EN_BYPASS	--	--	--	--	0x0F[3]	--
VBUS_ERRLO	0x17[4]	0x1C[4]	0x21[5]	--	0x05[3]	--
VBUS_ERRHI	0x17[5]	0x1C[5]	0x21[4]	--	0x05[2]	--
ACRB1_CONFIG	0x15[1]	0x1A[1]	0x1F[1]	--	0x0F[2]	--
ACRB2_CONFIG	0x15[0]	0x1A[0]	0x1F[0]	--	0x0F[2]	--
ACDRV1_STAT	0x0F[1]	--	--	--	--	--
ACDRV2_STAT	0x0F[0]	--	--	--	--	--
WD_TIMEOUT	0x16[0]	0x1B[0]	0x20[0]	0x10[4:3]	0x10[2]	--
FSW_SET	--	--	--	0x10[7:5]	--	--
FREQ_SHIFT	--	--	--	0x12[4:3]	--	--
RSNS	--	--	--	0x11[7]	--	--
SS_TIMEOUT	0x16[6]	0x1B[6]	0x20[6]	0x11[6:4]	--	--
ADC	0x16[7]	0x1B[7]	0x20[7]	--	0x23[7]	--
AC1_PD_EN	--	--	--	--	0x0E[1]	--
AC2_PD_EN	--	--	--	--	0x0E[0]	--
BUS_PD_EN	--	--	--	--	0x06[7]	--
AC1OVP	0x15[7]	0x1A[7]	0x1F[7]	0x0E[7:5]	--	--
AC2OVP	0x15[6]	0x1A[6]	0x1F[6]	0x0E[4:2]	--	--
BUSOVP_ALM	0x13[0]	0x18[0]	0x1D[0]	0x07[6:0]	0x07[7]	--
BUSOVP	0x13[1]	0x18[1]	0x1D[1]	0x06[6:0]	--	--
BUSUCP	0x14[5]	0x19[5]	0x1E[5]	0x05[6]	0x05[7]	0x11[3:2]
BUSOCP_ALM	0x14[6]	0x19[6]	0x1E[6]	0x09[4:0]	0x09[7]	--
BUSOCP	0x14[7]	0x19[7]	0x1E[7]	0x08[4:0]	--	--
TSBUS_FLT	0x16[4]	0x1B[4]	0x20[4]	0x0C[7:0]	0x0A[3]	--
OUTOVP	0x13[5]	0x18[5]	0x1D[5]	0x12[6:5]	0x12[7]	--
BATOVP_ALM	0x13[6]	0x18[6]	0x1D[6]	0x01[6:0]	0x01[7]	--
BATOVP	0x13[7]	0x18[7]	0x1D[7]	0x00[6:0]	0x00[7]	--
BATUCP_ALM	0x13[2]	0x18[2]	0x1D[2]	0x04[6:0]	0x04[7]	--
CONV_OCP	0x17[1]&0x17[0]	0x1C[1]&0x1C[0]	0x21[1]&0x21[0]	--	0x10[0]	0x10[1]

## REGISTER MAPS (continued)

### I<sup>2</sup>C Register Address Map (continued)

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
PMID2OUT_OVP	0x17[3]	0x1C[2]	0x21[3]	--	--	--
PMID2OUT_UVP	0x17[2]	0x1C[3]	0x21[2]	--	--	--
BUSSCP	0x14[3]	0x19[3]	0x1E[3]	--	--	--
BATOC_P_ALM	0x13[3]	0x18[3]	0x1D[3]	0x03[6:0]	0x03[7]	--
BATOC_P	0x13[4]	0x18[4]	0x1D[4]	0x02[6:0]	0x02[7]	--
CFLY_SHORT	0x14[2]	0x19[2]	0x1E[2]	--	--	--
TSBUS_TSBAT_ALM	0x16[5]	0x1B[5]	0x20[5]	--	--	--
TSBAT_FLT	0x16[3]	0x1B[3]	0x20[3]	0x0D[7:0]	0x0A[2]	--
TDIEOTP_ALM	0x16[1]	0x1B[1]	0x20[1]	0x0B[7:0]	0x0A[4]	--
TDIE_OTP	0x16[2]	0x1B[2]	0x20[2]	0x0A[6:5]	0x0A[7]	--
VOU_PRESENT	0x15[5]	0x1A[5]	0x1F[5]	--	--	--
VAC1_PRESENT	0x15[4]	0x1A[4]	0x1F[4]	--	--	--
VAC2_PRESENT	0x15[3]	0x1A[3]	0x1F[3]	--	--	--
VBUS_PRESENT	0x15[2]	0x1A[2]	0x1F[2]	--	--	--
REGN_GOOD	0x17[7]	0x1C[7]	0x21[7]	--	--	--

**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

**SGM41604**

**REGISTER MAPS (continued)**

Bit Types:

R: Read only

R/W: Read/Write

RC: Read clears the bit

R/WC: Read/Write. Writing a '1' clears the bit. Writing a '0' has no effect.

**REG0x00: BATOVP Register [reset = 0x5A]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BATOVP_DIS	0	R/W	Disable BATOVP 0 = Enable (Default) 1 = Disable	REG_RST
D[6:0]	BATOVP[6:0]	1011010	R/W	VBAT OVP Protection Rising Threshold Setting Bits $V_{BAT\_OVP\_R} = 3.5V + BATOVP[6:0] \times 0.01V$ Default: 4.4V (1011010) Range: 3.5V (0000000) – 4.77V (1111111) Offset: 3.5V	REG_RST

**REG0x01: BATOVP\_ALM Register [reset = 0x46]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BATOVP_ALM_DIS	0	R/W	VBAT OVP Alarm Disable Bit 0 = Enabled (Default) 1 = Disabled	REG_RST
D[6:0]	BATOVP_ALM[6:0]	1000110	R/W	VBAT OVP Alarm Rising Threshold Setting Bits $V_{BATOVP\_ALM\_R} = 3.5V + BATOVP\_ALM[6:0] \times 0.01V$ Default: 4.2V (1000110) Range: 3.5V (0000000) – 4.77V (1111111) Offset: 3.5V	REG_RST

**REG0x02: BATOCP Register [reset = 0x47]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BATOCP_DIS	0	R/W	IBAT OCP Protection Disable Bit 0 = Enabled (Default) 1 = Disabled	REG_RST
D[6:0]	BATOCP[6:0]	1000111	R/W	IBAT OCP Protection Threshold Setting Bits $I_{BAT\_OCP} = BATOCP[6:0] \times 0.1A$ , when $BATOCP[6:0] \leq 1010101b$ ; $I_{BAT\_OCP} = 8.5A + (BATOCP[6:0] - 1010101b) \times 0.3A$ , when $BATOCP[6:0] > 1010101b$ Default: 7.1A (1000111) Range: 2A (0010100) – 11.2A (1011110) Offset: 0A When $BATOCP[6:0] \leq 0010100$ , $I_{BATOCP} = 2A$ . When $BATOCP[6:0] \geq 1011110$ , $I_{BATOCP} = 11.2A$ .	REG_RST

**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

**SGM41604**

**REGISTER MAPS (continued)**

**REG0x03: BATOCP\_ALM Register [reset = 0x46]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BATOCP_ALM_DIS	0	R/W	IBAT OCP Alarm Disable Bit 0 = Enabled (Default) 1 = Disabled	REG_RST
D[6:0]	BATOCP_ALM[6:0]	1000110	R/W	IBAT OCP Alarm Rising Threshold Setting Bits $I_{\text{BATOCP\_ALM\_R}} = \text{BATOCP\_ALM}[6:0] \times 0.1\text{A}$ Default: 7A (1000110) Range: 0A (0000000) – 12.7A (1111111) Offset: 0A The IBAT OCP alarm rising threshold should be set lower than $I_{\text{BUS\_OCP}}$ to ensure proper operation.	REG_RST

**REG0x04: BATUCP\_ALM Register [reset = 0x28]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BATUCP_ALM_DIS	0	R/W	IBAT UCP Alarm Disable Bit 0 = Enable (default) 1 = Disable  Set this bit to '1' before CHG_EN is set to '1'.	REG_RST
D[6:0]	BATUCP_ALM[6:0]	0101000	R/W	Battery Under-Current Alarm Setting Bits $I_{\text{BATUCP\_ALM\_F}} = \text{BATUCP\_ALM}[6:0] \times 0.05\text{A}$ Default: 2A (0101000) Range: 0A (0000000) – 4.5A (1011010) Offset: 0A When $\text{BATUCP\_ALM}[6:0] \geq 1011010$ , $I_{\text{BATUCP\_ALM\_F}} = 4.5\text{A}$ .  When battery current falls below the programmed threshold, an nINT is sent. The host controller should monitor the battery current to determine when to disable the device and hand over charging to the main charger.	REG_RST

**REG0x05: CHARGER\_CONTROL 1 Register [reset = 0x22]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUSUCP_DIS	0	R/W	IBUS UCP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[6]	BUSUCP	0	R/W	BUSUCP Setting Bit 0 = $I_{\text{BUS\_UCP\_R}} = 500\text{mA}$ , $I_{\text{BUS\_UCP\_F}} = 250\text{mA}$ (default) 1 = $I_{\text{BUS\_UCP\_R}} = 250\text{mA}$ , $I_{\text{BUS\_UCP\_F}} = 125\text{mA}$	REG_RST
D[5:4]	Reserved	10	R	Reserved	N/A
D[3]	VBUS_ERRLO_DIS	0	R/W	VBUS_ERRLO Disable Bit 0 = Enable, converter does not switching, but $Q_{\text{RB}}$ is turned on when device is in VBUS_ERRLO (default) 1 = Disable, both converter and $Q_{\text{RB}}$ are turned on when device is in VBUS_ERRLO	REG_RST
D[2]	VBUS_ERRHI_DIS	0	R/W	VBUS_ERRHI Disable Bit 0 = Enable, converter does not switching, but $Q_{\text{RB}}$ is turned on when device is in VBUS_ERRHI (default) 1 = Disable, both converter and $Q_{\text{RB}}$ are turned on when device is in VBUS_ERRHI	REG_RST
D[1:0]	Reserved	10	R	Reserved	N/A



**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

**SGM41604**

**REGISTER MAPS (continued)**

**REG0x06: BUSOVP Register [reset = 0x26]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_PDN_EN	0	R/W	VBUS Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, the VBUS is pulled down by 5.5kΩ R <sub>PDN_VBUS</sub> . This bit will not be automatically reset. The host should write this bit to 0 if there is no need to pull down VBUS.	REG_RST
D[6:0]	VBUS_OVP[6:0]	0100110	R/W	VBUS OVP Protection Rising Threshold Setting Bits.  Voltage Divider Mode: $V_{BUS\_OVP\_R} = 7V + VBUS\_OVP[6:0] \times 0.05V$ Default: 8.9V (0100110) Range: 7V (0000000) – 12.75V (1110011) Offset: 7V If $VBUS\_OVP[6:0] \geq 1110011$ , $V_{BUS\_OVP\_R} = 12.75V$  Bypass Mode: $V_{BUS\_OVP\_R} = 3.5V + VBUS\_OVP[6:0] \times 0.025V$ Default: 4.45V (0100110) Range: 3.5V (0000000) – 6.5V (1111000) Offset: 3.5V If $VBUS\_OVP[6:0] \geq 1111000$ , $V_{BUS\_OVP\_R} = 6.5V$	REG_RST

**REG0x07: BUSOVP\_ALM Register [reset = 0x22]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUSOVP_ALM_DIS	0	R/W	VBUS OVP Alarm Disable Bit 0 = Enabled (Default) 1 = Disabled	REG_RST
D[6:0]	VBUSOVP_ALM[6:0]	0100010	R/W	VBUS OVP Alarm Rising Threshold Setting Bits  Voltage Divider Mode: $V_{BUSOVP\_ALM\_R} = 7V + VBUSOVP\_ALM[6:0] \times 0.05V$ Default: 8.7V (0100010) Range: 7V (0000000) – 13.35V (1111111) Offset: 7V  Bypass Mode: $V_{BUSOVP\_ALM\_R} = 3.5V + VBUSOVP\_ALM[6:0] \times 0.025V$ Default: 4.35V (0100010) Range: 3.5V (0000000) – 6.675V (1111111) Offset: 3.5V The VBUS OVP alarm rising threshold should be set lower than $V_{BUS\_OVP\_R}$ to ensure proper operation.	REG_RST

**REG0x08: BUSOCP Register [reset = 0x0D]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4:0]	BUSOCP[4:0]	01101	R/W	IBUS OCP Protection Threshold Setting Bits  $I_{BUS\_OCP} = 1A + BUSOCP[4:0] \times 0.25A$ Default: 4.25A (01101) Range: 1A (00000) – 6.5A (10110) Offset: 1A When $BUSOCP[4:0] \geq 10110$ , $I_{BUS\_OCP} = 6.5A$ .	REG_RST

**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

**SGM41604**

**REGISTER MAPS (continued)**

**REG0x09: BUSOCP\_ALM Register [reset = 0x0A]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUSOCP_ALM_DIS	0	R/W	BUSOCP_ALM Disable Bit 0 = Enable (default) 1 = Disable	REG_RST
D[6:5]	Reserved	00	R	Reserved	N/A
D[4:0]	BUSOCP_ALM[4:0]	01010	R/W	Bus Over-Voltage Alarm Setting Bits  $I_{BUSOCP\_ALM\_R} = 1A + BUSOCP\_ALM[4:0] \times 0.25A$ Default: 3.5A (01010) Range: 1A (00000) – 8.75A (11111) Offset: 1A The $I_{BUSOCP\_ALM\_R}$ should be set lower than $I_{BUS\_OCP}$ to ensure proper operation.	REG_RST

**REG0x0A: TEMP\_CONTROL Register [reset = 0x60]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TDIE_OTP_DIS	0	R/W	TDIE OTP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[6:5]	TDIE_OTP[1:0]	11	R/W	TDIE OTP Protection Rising Threshold Setting Bits  $T_{DIE\_OTP\_R} = 80^{\circ}C + TDIE\_OTP[1:0] \times 20^{\circ}C$ 00 = +80°C 01 = +100°C 10 = +120°C 11 = +140°C (default)	REG_RST
D[4]	TDIEOTP_ALM_DIS	0	R/W	TDIE OTP Alarm Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[3]	TSBUS_FLT_DIS	0	R/W	TSBUS_FLT Protection Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[2]	TSBAT_FLT_DIS	0	R/W	TSBAT_FLT Protection Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[1:0]	Reserved	00	R	Reserved	N/A

**REG0x0B: TDIEOTP\_ALM Register [reset = 0xC8]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TDIEOTP_ALM[7:0]	11001000	R/W	TDIE OTP Alarm Rising Threshold Setting Bits  $T_{DIEOTP\_ALM\_R} = 25^{\circ}C + TDIEOTP\_ALM[7:0] \times 0.5^{\circ}C$ Default: 125°C (11001000) Range: 25°C (00000000) – 150°C (11111010) Offset: 25°C When $TDIEOTP\_ALM[7:0] \geq 11111010$ , $T_{DIEOTP\_ALM\_R} = 150^{\circ}C$ .  The TDIE OTP alarm rising threshold should be set lower than $T_{DIE\_OTP\_R}$ to ensure proper operation.	REG_RST

## REGISTER MAPS (continued)

### REG0x0C: TSBUS\_FLT Register [reset = 0x15]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBUS_FLT[7:0]	00010101	R/W	TSBUS Percentage Fault Threshold Setting Bits $TS_{BUS\_FLT\_F} = TSBUS\_FLT[7:0] \times 0.19531\%$ Default: 4.10151% (00010101) Range: 0% (00000000) – 49.8041% (11111111) Offset: 0%	REG_RST

### REG0x0D: TSBAT\_FLT Register [reset = 0x15]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBAT_FLT[7:0]	00010101	R/W	TSBAT Percentage Fault Threshold Setting Bits $TS_{BAT\_FLT\_F} = TSBAT\_FLT[7:0] \times 0.19531\%$ Default: 4.10151% (00010101) Range: 0% (00000000) – 49.8041% (11111111) Offset: 0%	REG_RST

### REG0x0E: VAC\_CONTROL Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	VAC1OVP[2:0]	000	R/W	VAC1 OVP Protection Rising Threshold Setting Bits 000 = 6.5V (default) 001 = 10.5V 010 = 12V 011 = 14V 100 = 16V 101 = 18V	REG_RST
D[4:2]	VAC2OVP[2:0]	000	R/W	VAC2 OVP Protection Rising Threshold Setting Bits 000 = 6.5V (default) 001 = 10.5V 010 = 12V 011 = 14V 100 = 16V 101 = 18V	REG_RST
D[1]	VAC1_PDN_EN	0	R/WC	VAC1 Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, the VAC1 is pulled down by 350Ω R <sub>PDN_VAC</sub> . Note that to prevent chip damage, the pull-down current is limited to 35mA. This bit will not be automatically reset. The host should write this bit to 0 if there is no need to pull down VAC1.	REG_RST
D[0]	VAC2_PDN_EN	0	R/WC	VAC2 Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, the VAC2 is pulled down by 350Ω R <sub>PDN_VAC</sub> . Note that to prevent chip damage, the pull-down current is limited to 35mA. This bit will not be automatically reset. The host should write this bit to 0 if there is no need to pull down VAC2.	REG_RST

**REGISTER MAPS (continued)****REG0x0F: CHARGER\_CONTROL 2 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REG_RST	0	R/WC	Register Reset Bit 0 = No register reset (default) 1 = Reset registers to their default values. When enabled, the associated register bits are reset to their default values and then this bit is automatically reset to 0.	REG_RST
D[6]	EN_HIZ	0	R/W	HIZ Mode Enable Bit 0 = Disable HIZ mode (default) 1 = Enable HIZ mode  When device is in HIZ mode, converter stops switching, ADC stops converting, ACDRV is turned off and the REGN LDO is forced off.	REG_RST
D[5]	EN_OTG	0	R/W	Power Path Control Enable Bit During OTG Mode 0 = Don't allow the AP to control ACDRV in OTG mode (default) 1 = Allow the AP to control ACDRV in OTG mode	REG_RST or Watchdog
D[4]	CHG_EN	0	R/W	Charge Enable Bit 0 = Disabled (default) 1 = Enabled. If any fault has occurred, device returns to standby mode and this bit is automatically cleared to 0.	REG_RST or Watchdog
D[3]	EN_BYPASS	0	R/W	Bypass Mode Enable Bit 0 = Disable bypass mode (default) 1 = Enable bypass mode	REG_RST or Watchdog
D[2]	DIS_ACDRV_BOTH	0	R/W	Disable Bit for Both ACDRV When this bit is set, the device forces both ACDRV off. 0 = ACDRV1 and ACDRV2 are allowed to be turned on (default) 1 = ACDRV1 and ACDRV2 are forced off	N/A
D[1]	ACDRV1_STAT	0	R/W	Status and Control Bit of ACDRV1 Driver For dual input configurations with two sets of OVPFETs, this bit can be used for input swapping. 0 = ACDRV1 is turned OFF (default) 1 = ACDRV1 is turned ON	N/A
D[0]	ACDRV2_STAT	0	R/W	Status and Control Bit of ACDRV2 Driver For dual input configurations with two sets of OVPFETs, this bit can be used for input swapping. 0 = ACDRV2 is turned OFF (default) 1 = ACDRV2 is turned ON	N/A

**REG0x10: CHARGER\_CONTROL 3 Register [reset = 0x80]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	FSW_SET[2:0]	100	R/W	Switched-Cap Converter Switching Frequency Setting Bits 000 = 187.5kHz 001 = 250kHz 010 = 300kHz 011 = 375kHz 100 = 500kHz (default) 101 = 750kHz 110 = 1000kHz 111 = 1500kHz	N/A
D[4:3]	WDT_TIMER[1:0]	00	R/W	Watchdog Timer Setting Bits 00 = 0.5s (default) 01 = 1s 10 = 8s 11 = 30s	REG_RST
D[2]	WDT_DIS	0	R/W	Watchdog Timer Disable Bit 0 = Enable (default) 1 = Disable	REG_RST
D[1]	CONV_OCP_TIME_SEL	0	R/W	CONV_OCP Trigger Times Select Bit 0 = CONV_OCP trigger 1 time (default) 1 = CONV_OCP trigger 4 times	REG_RST
D[0]	CONV_OCP_DIS	0	R/W	CONV_OCP Protection Disable bit 0 = Enable (default) 1 = Disable	REG_RST

**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

**SGM41604**

**REGISTER MAPS (continued)**

**REG0x11: CHARGER\_CONTROL 4 Register [reset = 0x71]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBAT_RSNS	0	R/W	External IBAT Current Sense Resistor Setting Bit 0 = 2mΩ (default) 1 = 5mΩ	REG_RST
D[6:4]	SS_TIMEOUT[2:0]	111	R/W	Soft-Start Timeout Setting Bits After soft-start timeout, the device checks if I <sub>BUS</sub> is above IBUS UCP threshold. 000 = 6.25ms 001 = 12.5ms 010 = 25ms 011 = 50ms 100 = 100ms 101 = 400ms 110 = 1.5s 111 = 12s (default)	N/A
D[3:2]	IBUSUCP_FALL_DEG[1:0]	00	R/W	IBUS UCP Protection Deglitch Time Setting Bits 00 = 0.01ms (default) 01 = 5ms 10 = 40ms 11 = 150ms	REG_RST
D[1:0]	Reserved	01	R/W	Reserved	N/A

**REG0x12: CHARGER\_CONTROL 5 Register [reset = 0x60]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VOUT_OVP_DIS	0	R/W	VOUT OVP Protection Disable Bit 0 = Enable (default) 1 = Disable	REG_RST
D[6:5]	VOUT_OVP[1:0]	11	R/W	VOUT OVP Protection Rising Threshold Setting Bits $V_{OUT\_OVP\_R} = 4.7V + V_{OUT\_OVP}[1:0] \times 0.1V$ 00 = 4.7V 01 = 4.8V 10 = 4.9V 11 = 5.0V (default)	REG_RST
D[4:3]	FREQ_SHIFT[1:0]	00	R/W	Bits of Adjusting Switching Frequency 00 = Nominal switching frequency set in REG0x10[7:5] 01 = Set switching frequency 10% higher than normal 10 = Set switching frequency 10% lower than normal	REG_RST
D[2]	Reserved	0	R/W	Reserved	N/A
D[1:0]	MS[1:0]	00	R	Primary, Secondary, Standalone Operation 00 = Standalone (default) 01 = Secondary 10 = Primary	N/A

**REGISTER MAPS (continued)**

**REG0x13: STAT 1 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BATOVP_STAT	0	R	VBAT OVP Fault Status Bit 0 = Not in BATOVP (default) 1 = In BATOVP	N/A
D[6]	BATOVP_ALM_STAT	0	R	BATOVP_ALM Status Bit 0 = Not in BATOVP_ALM (default) 1 = In BATOVP_ALM	N/A
D[5]	VOUTOVP_STAT	0	R	VOUTOVP Status Bit 0 = Not in VOUTOVP (default) 1 = in VOUTOVP	N/A
D[4]	BATOCP_STAT	0	R	BATOCP Status Bit 0 = Not in BATOCP (default) 1 = In BATOCP	N/A
D[3]	BATOCP_ALM_STAT	0	R	BATOCP_ALM Status Bit 0 = Not in BATOCP_ALM (default) 1 = In BATOCP_ALM	N/A
D[2]	BATUCP_ALM_STAT	0	R	BATUCP_ALM Status Bit 0 = Not in BATUCP_ALM (default) 1 = In BATUCP_ALM	N/A
D[1]	BUSOVP_STAT	0	R	VBUSOVP Status Bit 0 = Not in VBUS OVP (default) 1 = In VBUS OVP	N/A
D[0]	BUSOVP_ALM_STAT	0	R	BUSOVP_ALM Status Bit 0 = Not in BUSOVP_ALM (default) 1 = In BUSOVP_ALM	N/A

**REG0x14: STAT 2 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUSOCP_STAT	0	R	BUSOCP Status Bit 0 = Not in BUSOCP (default) 1 = In BUSOCP	N/A
D[6]	BUSOCP_ALM_STAT	0	R	BUSOCP_ALM Status Bit 0 = Not in BUSOCP_ALM (default) 1 = In BUSOCP_ALM	N/A
D[5]	BUSUCP_STAT	0	R	BUSUCP Status Bit 0 = Not in BUSUCP (default) 1 = In BUSUCP	N/A
D[4]	Reserved	0	R	Reserved	N/A
D[3]	BUSSCP_STAT	0	R	BUSSCP Status Bit 0 = Not in BUSSCP (default) 1 = In BUSSCP	N/A
D[2]	CFLY_SHORT_STAT	0	R	CFLY Short Detection Status Bit 0 = CFLY not shorted (default) 1 = CFLY shorted	N/A
D[1:0]	Reserved	00	R	Reserved	N/A

**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

**SGM41604**

**REGISTER MAPS (continued)**

**REG0x15: STAT 3 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VAC1OVP_STAT	0	R	VAC1 OVP Status Bit 0 = Not in VAC1 OVP (default) 1 = In VAC1 OVP	N/A
D[6]	VAC2OVP_STAT	0	R	VAC2 OVP Status Bit 0 = Not in VAC2 OVP (default) 1 = In VAC2 OVP	N/A
D[5]	VOUTPRESENT_STAT	0	R	VOUT Present Status Bit 0 = VOOUT not present (default) 1 = VOOUT present	N/A
D[4]	VAC1PRESENT_STAT	0	R	VAC1 Present Status Bit 0 = VAC1 not present (default) 1 = VAC1 present	N/A
D[3]	VAC2PRESENT_STAT	0	R	VAC2 Present Status Bit 0 = VAC2 not present (default) 1 = VAC2 present	N/A
D[2]	VBUSPRESENT_STAT	0	R	VBUS Present Status Bit 0 = VBUS not present (default) 1 = VBUS present	N/A
D[1]	ACRB1_CONFIG_STAT	0	R	ACFET1-RBFET1 Status Bit 0 = ACFET1-RBFET1 is not placed (default) 1 = ACFET1-RBFET1 is placed	N/A
D[0]	ACRB2_CONFIG_STAT	0	R	ACFET2-RBFET1 Status Bit 0 = ACFET2-RBFET2 is not placed (default) 1 = ACFET2-RBFET2 is placed	N/A

**REG0x16: STAT 4 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_DONE_STAT	0	R	ADC Conversion Status Bit (in 1-Shot Mode Only) 0 = Conversion not completed (default) 1 = Conversion completed  Note: Always reads 0 in continuous mode	N/A
D[6]	SS_TIMEOUT_STAT	0	R	Soft-Start Timeout Status Bit 0 = Device not in soft timeout (default) 1 = Device in soft timeout	N/A
D[5]	TSBUS_TSBAT_ALM_STAT	0	R	TSBUS and TSBAT Alarm Status Bit 0 = TSBUS or TSBAT threshold is not within 5% of the TSBUS_FLT or TSBAT_FLT set threshold (default) 1 = TSBUS or TSBAT threshold is within 5% of the TSBUS_FLT or TSBAT_FLT set threshold	N/A
D[4]	TSBUS_FLT_STAT	0	R	TSBUS_FLT Status Bit 0 = Not in TSBUS_FLT (default) 1 = In TSBUS_FLT	N/A
D[3]	TSBAT_FLT_STAT	0	R	TSBAT_FLT Status Bit 0 = Not in TSBAT_FLT (default) 1 = In TSBAT_FLT	N/A
D[2]	TDIE_OTP_STAT	0	R	TDIE Over-Temperature Fault Status Bit 0 = Not in TDIE fault (default) 1 = In TDIE fault	N/A
D[1]	TDIEOTP_ALM_STAT	0	R	TDIE Over-Temperature Alarm Status Bit 0 = Not in TDIEOTP_ALM (default) 1 = In TDIEOTP_ALM	N/A
D[0]	WDT_STAT	0	R	Watchdog Timer Status Bit 0 = Normal (default) 1 = Watchdog timer expired	N/A

**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

**SGM41604**

**REGISTER MAPS (continued)**

**REG0x17: STAT 5 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REGN_GOOD_STAT	0	R	REGN_GOOD Status Bit 0 = REGN not good (default) 1 = REGN good	N/A
D[6]	CONV_ACTIVE_STAT	0	R	Converter active Status Bit 0 = Converter not running (default) 1 = Converter running	N/A
D[5]	VBUS_ERRHI_STAT	0	R	VBUS_ERRHI Status Bit 0 = Not in VBUS_ERRHI status (default) 1 = In VBUS_ERRHI status	N/A
D[4]	VBUS_ERRLO_STAT	0	R	VBUS_ERRLO Status Bit 0 = Not in VBUS_ERRLO status (default) 1 = In VBUS_ERRLO status	N/A
D[3]	PMID2VOUT_OVP_STAT	0	R	PMID2VOUT_OVP_STAT Bit 0 = Not in PMID2VOUT_OVP_STAT (default) 1 = PMID2VOUT_OVP_STAT	N/A
D[2]	PMID2VOUT_UVP_STAT	0	R	PMID2VOUT_UVP_STAT Bit 0 = Not in PMID2VOUT_UVP_STAT (default) 1 = In PMID2VOUT_UVP_STAT	N/A
D[1]	CONV_OCP_STAT	0	R	CONV_OCP_STAT Bit 0 = Not in CONV_OCP_STAT (default) 1 = In CONV_OCP_STAT	N/A
D[0]	CFL_RVS_OCP_STAT	0	R	CFL_RVS_OCP_STAT Bit 0 = Not in CFL_RVS_OCP_STAT (default) 1 = In CFL_RVS_OCP_STAT	N/A

**REG0x18: FLAG 1 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BATOVP_FLAG	0	RC	VBAT OVP Fault Flag Bit 0 = No VBAT OVP fault (default) 1 = VBAT OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	BATOVP_ALM_FLAG	0	RC	VBAT OVP Alarm Flag Bit 0 = No VBAT OVP alarm (default) 1 = VBAT OVP alarm has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[5]	VOUTOVP_FLAG	0	RC	VOUT OVP Fault Flag Bit 0 = No VOUT OVP fault (default) 1 = VOUT OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	BATOCP_FLAG	0	RC	IBAT OCP Fault Flag Bit 0 = No IBAT OCP fault (default) 1 = IBAT OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	BATOCP_ALM_FLAG	0	RC	IBAT OCP Alarm Flag Bit 0 = No IBAT OCP alarm (default) 1 = IBAT OCP alarm has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	BATUCP_ALM_FLAG	0	RC	IBAT UCP Alarm Flag Bit 0 = No IBAT UCP alarm (default) 1 = IBAT UCP alarm has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[1]	BUSOVP_FLAG	0	RC	VBUS OVP Fault Flag Bit 0 = No VBUS OVP fault (default) 1 = VBUS OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	BUSOVP_ALM_FLAG	0	RC	VBUS OVP Alarm Flag Bit 0 = No VBUS OVP alarm (default) 1 = VBUS OVP alarm has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A



**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

**SGM41604**

**REGISTER MAPS (continued)**

**REG0x19: FLAG 2 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUSOCP_FLAG	0	RC	IBUS OCP Fault Flag Bit 0 = No IBUS OCP fault (default) 1 = IBUS OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	BUSOCP_ALM_FLAG	0	RC	BUSOCP_ALM Fault Flag Bit 0 = No IBUS OCP ALM fault (default) 1 = IBUS OCP ALM fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[5]	BUSUCP_FLAG	0	RC	IBUS UCP Fault Flag Bit 0 = No IBUS UCP fault (default) 1 = IBUS UCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	Reserved	0	R	Reserved	N/A
D[3]	BUSSCP_FLAG	0	RC	VBUS SCP Fault Flag Bit 0 = No VBUS SCP fault (default) 1 = VBUS SCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	CFLY_SHORT_FLAG	0	RC	CFLY Short Detection Fault Flag Bit 0 = No CFLY short fault (default) 1 = CFLY short fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[1:0]	Reserved	00	R	Reserved	N/A

**REG0x1A: FLAG 3 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VAC1OVP_FLAG	0	RC	VAC1 OVP Fault Flag Bit 0 = No VAC1 OVP fault (default) 1 = VAC1 OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	VAC2OVP_FLAG	0	RC	VAC2 OVP Fault Flag Bit 0 = No VAC2 OVP fault (default) 1 = VAC2 OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[5]	VOUTPRESENT_FLAG	0	RC	VOUT Present Flag Bit 0 = No VOUT present event (default) 1 = VOUT present event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	VAC1PRESENT_FLAG	0	RC	VAC1 Present Flag Bit 0 = No VAC1 present event (default) 1 = VAC1 present event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	VAC2PRESENT_FLAG	0	RC	VAC2 Present Flag Bit 0 = No VAC2 present event (default) 1 = VAC2 present event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	VBUSPRESENT_FLAG	0	RC	VBUS Present Flag Bit 0 = No VBUS present event (default) 1 = VBUS present event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[1]	ACRB1_CONFIG_FLAG	0	RC	ACFET1-RBFET1 Configuration Detection Flag Bit 0 = Normal (default) 1 = ACFET1-RBFET1 configuration status changed. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	ACRB2_CONFIG_FLAG	0	RC	ACFET2-RBFET2 Configuration Detection Flag Bit 0 = Normal (default) 1 = ACFET2-RBFET2 configuration status changed. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A

**REGISTER MAPS (continued)****REG0x1B: FLAG 4 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_DONE_FLAG	0	RC	ADC Conversion Complete Event Flag Bit In 1-shot conversion mode, this bit is set to 1 after ADC conversion of all enabled channels is completed. 0 = Normal (default) 1 = ADC conversion has completed.	N/A
D[6]	SS_TIMEOUT_FLAG	0	RC	Soft-Start Timeout Flag Bit 0 = No soft-start timeout event (default) 1 = Soft-start timeout event has occurred.	N/A
D[5]	TSBUS_TSBAT_ALM_FLAG	0	RC	TSBUS_TSBAT Alarm Flag Bit 0 = No TSBUS_TSBAT alarm (default) 1 = TSBUS_TSBAT alarm has occurred.	N/A
D[4]	TSBUS_FLT_FLAG	0	RC	TSBUS_FLT Flag Bit 0 = No TSBUS Fault (default) 1 = TSBUS fault has occurred.	N/A
D[3]	TSBAT_FLT_FLAG	0	RC	TSBAT_FLT Flag Bit 0 = No TSBAT Fault (default) 1 = TSBAT fault has occurred.	N/A
D[2]	TDIE_OTP_FLAG	0	RC	TDIE Over-Temperature Fault Flag Bit 0 = No TDIE over-temperature fault (default) 1 = TDIE over-temperature fault has occurred.	N/A
D[1]	TDIEOTP_ALM_FLAG	0	RC	TDIE Over-Temperature Alarm Flag Bit 0 = No TDIE over-temperature alarm (default) 1 = TDIE over-temperature alarm has occurred.	N/A
D[0]	WDT_FLAG	0	RC	Watchdog Timeout Fault Flag Bit 0 = No watchdog timeout fault (default) 1 = Watchdog timeout fault has occurred.	N/A

**REG0x1C: FLAG 5 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REGN_GOOD_FLAG	0	RC	REGN_GOOD Event Flag Bit 0 = No REGN_GOOD event (default) 1 = REGN_GOOD event has occurred.	N/A
D[6]	CONV_ACTIVE_FLAG	0	RC	Converter Active Event Flag Bit 0 = No converter active event (default) 1 = Converter active event has occurred.	N/A
D[5]	VBUS_ERRHI_FLAG	0	RC	VBUS High Voltage Fault Flag Bit 0 = No VBUS high voltage fault (default) 1 = Device in VBUS high voltage fault has occurred.	N/A
D[4]	VBUS_ERRLO_FLAG	0	RC	VBUS Low Voltage Fault Flag Bit 0 = No VBUS low voltage fault (default) 1 = Device in VBUS low voltage fault has occurred.	N/A
D[3]	PMID2VOUT_UVP_FLAG	0	RC	PMID2VOUT_UVP_FLAG Bit 0 = Normal (default) 1 = PMID2VOUT_UVP status changed	N/A
D[2]	PMID2VOUT_OVP_FLAG	0	RC	PMID2VOUT_OVP_FLAG Bit 0 = Normal (default) 1 = PMID2VOUT_OVP status changed	N/A
D[1]	CONV_OCP_FLAG	0	RC	CONV_OCP_FLAG Bit 0 = Normal (default) 1 = CONV_OCP_STAT changed	N/A
D[0]	CFL_RVS_OCP_FLAG	0	RC	CFL_RVS_OCP_FLAG Bit 0 = Normal (default) 1 = CFL_RVS_OCP_STAT changed	N/A

**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

**SGM41604**

**REGISTER MAPS (continued)**

**REG0x1D: MASK 1 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BATOVP_MASK	0	R/W	Mask VBAT OVP Fault Interrupt 0 = VBAT OVP fault interrupt can work (default) 1 = Mask VBAT OVP fault interrupt. VBAT_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[6]	BATOVP_ALM_MASK	0	R/W	Mask VBAT OVP Alarm Interrupt 0 = VBAT OVP alarm interrupt can work (default) 1 = Mask VBAT OVP alarm interrupt. VBAT_OVP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[5]	VOUOVP_MASK	0	R/W	Mask VOUT OVP Fault Interrupt 0 = VOUT OVP fault interrupt can work (default) 1 = Mask VOUT OVP fault interrupt. VOUT_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[4]	BATOCP_MASK	0	R/W	Mask IBAT OCP Fault Interrupt 0 = IBAT OCP fault interrupt can work (default) 1 = Mask IBAT OCP fault interrupt. IBAT_OCP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[3]	BATOCP_ALM_MASK	0	R/W	Mask IBAT OCP Alarm Interrupt 0 = IBAT OCP alarm interrupt can work (default) 1 = Mask IBAT OCP alarm interrupt. IBATOCP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	BATUCP_ALM_MASK	0	R/W	Mask BATUCP Alarm Interrupt 0 = IBAT UCP alarm interrupt can work (default) 1 = Mask IBAT UCP alarm interrupt. IBATUCP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	BUSOVP_MASK	0	R/W	Mask VBUS OVP Fault Interrupt 0 = VBUS OVP fault interrupt can work (default) 1 = Mask VBUS OVP fault interrupt. VBUS_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[0]	BUSOVP_ALM_MASK	0	R/W	Mask VBUS OVP Alarm Interrupt 0 = VBUS OVP alarm interrupt can work (default) 1 = Mask VBUS OVP alarm interrupt. VBUSOVP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

**REG0x1E: MASK 2 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUSOCP_MASK	0	R/W	Mask IBUS OCP Fault Interrupt 0 = IBUS OCP fault interrupt can work (default) 1 = Mask IBUS OCP fault interrupt. IBUS_OCP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[6]	BUSOCP_ALM_MASK	0	R/W	Mask IBUS OCP Alarm Interrupt 0 = IBUS OCP alarm interrupt can work (default) 1 = Mask IBUS OCP alarm interrupt. IBUS_OCP_ALM_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[5]	BUSUCP_MASK	0	R/W	Mask IBUS UCP Fault Interrupt 0 = IBUS UCP fault interrupt can work (default) 1 = Mask IBUS UCP fault interrupt. IBUS_UCP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[4]	Reserved	0	R	Reserved	N/A
D[3]	BUSSCP_MASK	0	R/W	Mask VBUS SCP Fault Interrupt 0 = VBUS SCP fault interrupt can work (default) 1 = Mask VBUS SCP fault interrupt. VBUS_SCP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[2]	CFLY_SHORT_MASK	0	R/W	Mask CFLY Short Fault Interrupt 0 = CFLY short fault interrupt can work (default) 1 = Mask CFLY short fault interrupt. CFLY_SHORT_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[1:0]	Reserved	00	R/W	Reserved	N/A

**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

**SGM41604**

**REGISTER MAPS (continued)**

**REG0x1F: MASK 3 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VAC1OVP_MASK	0	R/W	Mask VAC1 OVP Fault Interrupt 0 = VAC1 OVP fault interrupt can work (default) 1 = Mask VAC1 OVP fault interrupt.	REG_RST
D[6]	VAC2OVP_MASK	0	R/W	Mask VAC2 OVP Fault Interrupt 0 = VAC2 OVP fault interrupt can work (default) 1 = Mask VAC2 OVP fault interrupt.	REG_RST
D[5]	VOUTPRESENT_MASK	0	R/W	Mask VOUT Present Event Interrupt 0 = VOUT present event interrupt can work (default) 1 = Mask VOUT present event interrupt.	REG_RST
D[4]	VAC1PRESENT_MASK	0	R/W	Mask VAC1 Present Event Interrupt 0 = VAC1 present event interrupt can work (default) 1 = Mask VAC1 present event interrupt.	REG_RST
D[3]	VAC2PRESENT_MASK	0	R/W	Mask VAC2 Present Event Interrupt 0 = VAC2 present event interrupt can work (default) 1 = Mask VAC2 present event interrupt.	REG_RST
D[2]	VBUSPRESENT_MASK	0	R/W	Mask VBUS Present Event Interrupt 0 = VBUS present event interrupt can work (default) 1 = Mask VBUS present event interrupt.	REG_RST
D[1]	ACRB1_CONFIG_MASK	0	R/W	Mask ACFET1-RBFET1 Configuration Status Change Event Interrupt 0 = ACRB1_CONFIG status bit change event interrupt can work (default) 1 = Mask ACRB1_CONFIG status bit change event interrupt. ACRB1_CONFIG_FLAG is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	ACRB2_CONFIG_MASK	0	R/W	Mask ACFET2-RBFET2 Configuration Status Change Event Interrupt 0 = ACRB2_CONFIG status bit change event interrupt can work (default) 1 = Mask ACRB2_CONFIG status bit change event interrupt. ACRB2_CONFIG_FLAG is set after the event, but the interrupt signal is not generated.	REG_RST

**REG0x20: MASK 4 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_DONE_MASK	0	R/W	ADC_DONE Mask 0 = ADC_DONE flag produce nINT (default) 1 = ADC_DONE flag does not produce nINT	REG_RST
D[6]	SS_TIMEOUT_MASK	0	R/W	SS_TIMEOUT Mask 0 = SS_TIMEOUT flag produce nINT (default) 1 = SS_TIMEOUT flag does not produce nINT	REG_RST
D[5]	TSBUS_TSBAT_ALM_MASK	0	R/W	TSBUS_TSBAT_ALM Mask 0 = TSBUS_TSBAT_ALM flag produce nINT (default) 1 = TSBUS_TSBAT_ALM flag does not produce nINT	REG_RST
D[4]	TSBUS_FLT_MASK	0	R/W	TSBUS_FLT Mask 0 = TSBUS_FLT flag produce nINT (default) 1 = TSBUS_FLT flag does not produce nINT	REG_RST
D[3]	TSBAT_FLT_MASK	0	R/W	TSBAT_FLT Mask 0 = TSBAT_FLT flag produce nINT (default) 1 = TSBAT_FLT flag does not produce nINT	REG_RST
D[2]	TDIE_OTP_MASK	0	R/W	TDIE_OTP Mask 0 = TDIE_OTP flag produce nINT (default) 1 = TDIE_OTP flag does not produce nINT	REG_RST
D[1]	TDIEOTP_ALM_MASK	0	R/W	TDIEOTP_ALM Mask 0 = TDIEOTP_ALM flag produce nINT (default) 1 = TDIEOTP_ALM flag does not produce nINT	REG_RST
D[0]	WDT_MASK	0	R/W	Watchdog Mask 0 = Watchdog timeout flag produce nINT (default) 1 = Watchdog timeout flag does not produce nINT	REG_RST

**REGISTER MAPS (continued)****REG0x21: MASK 5 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REGN_GOOD_MASK	0	R/W	REGN_GOOD Mask 0 = REGN_GOOD flag produce nINT (default) 1 = REGN_GOOD flag does not produce nINT	REG_RST
D[6]	CONV_ACTIVE_MASK	0	R/W	CONV_ACTIVE Mask 0 = CONV_ACTIVE flag produce nINT (default) 1 = CONV_ACTIVE flag does not produce nINT	REG_RST
D[5]	VBUS_ERRLO_MASK	0	R/W	VBUS_ERRLO Mask 0 = VBUS_ERRLO flag produce nINT (default) 1 = VBUS_ERRLO flag does not produce nINT	REG_RST
D[4]	VBUS_ERRHI_MASK	0	R/W	VBUS_ERRHI mMask 0 = VBUS_ERRHI flag produce nINT (default) 1 = VBUS_ERRHI flag does not produce nINT	REG_RST
D[3]	PMID2VOUTOVP_MASK	0	R/W	PMID2VOUTOVP_MASK 0 = PMID2VOUTOVP flag produce nINT (default) 1 = PMID2VOUTOVP flag does not produce nINT	REG_RST
D[2]	PMID2VOUTUVP_MASK	0	R/W	PMID2VOUTUVP_MASK 0 = PMID2VOUTUVP flag produce nINT (default) 1 = PMID2VOUTUVP flag does not produce nINT	REG_RST
D[1]	CONV_OCP_MASK	0	R/W	CONV_OCP_MASK 0 = CONV_OCP flag produce nINT (default) 1 = CONV_OCP flag does not produce nINT	REG_RST
D[0]	CFL_RVS_OCP_MASK	0	R/W	CFL_RVS_OCP_MASK 0 = CFL_RVS_OCP flag produce nINT (default) 1 = CFL_RVS_OCP flag does not produce nINT	REG_RST

**REG0x22: DEVICE\_INFO Register [reset = 0x11]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	DEVICE_REV[3:0]	0001	R	Device Revision Default: 0001	N/A
D[3:0]	DEVICE_ID[3:0]	0001	R	Device ID Default: 0001	N/A

**REG0x23: ADC\_CONTROL 1 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_EN	0	R/W	ADC Conversion Enable 0 = Disabled (default) 1 = Enabled  Note: In 1-shot mode when the selected channel conversions are completed, the ADC_EN bit is automatically reset to 0.	REG_RST or Watchdog
D[6]	ADC_RATE	0	R/W	ADC Conversion Mode Control 0 = Continuous conversion (default) 1 = 1-shot	REG_RST
D[5]	ADC_AVG	0	R/W	ADC Average Enable Bit 0 = Single value (default) 1 = Running average	REG_RST
D[4]	ADC_AVG_INIT	0	R/W	ADC Average Initial Value Setting Bit 0 = Start average using the existing register value (default) 1 = Start average using a new conversion	REG_RST
D[3:2]	ADC_SAMPLE[1:0]	00	R/W	Sample Speed 00 = 15 bit (default) 01 = 14 bit 10 = 13 bit 11 = 11 bit	REG_RST
D[1]	IBUS_ADC_DIS	0	R/W	IBUS ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[0]	VBUS_ADC_DIS	0	R/W	VBUS ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST

**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

**SGM41604**

**REGISTER MAPS (continued)**

**REG0x24: ADC\_CONTROL 2 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VAC1_ADC_DIS	0	R/W	VAC1 ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[6]	VAC2_ADC_DIS	0	R/W	VAC2 ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[5]	VOUT_ADC_DIS	0	R/W	VOUT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[4]	VBAT_ADC_DIS	0	R/W	VBAT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[3]	IBAT_ADC_DIS	0	R/W	IBAT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[2]	TSBUS_ADC_DIS	0	R/W	TSBUS ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[1]	TSBAT_ADC_DIS	0	R/W	TSBAT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[0]	TDIE_ADC_DIS	0	R/W	TDIE ADC Control 0 = Enable (default) 1 = Disable	REG_RST

**REG0x25: IBUS\_ADC1 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBUS_ADC[15:8]	00000000	R	High Byte of the 16-bit ADC IBUS Data (resolution: 1mA, range: 0mA – 7000mA) MSB<7:0>: 32768mA, 16384mA, 8192mA, 4096mA, 2048mA, 1024mA, 512mA, 256mA	N/A

**REG0x26: IBUS\_ADC0 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBUS_ADC[7:0]	00000000	R	Low Byte of the 16-bit ADC IBUS Data (resolution: 1mA, range: 0mA – 7000mA) LSB<7:0>: 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA, 1mA	N/A

**REG0x27: VBUS\_ADC1 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBUS_ADC[15:8]	00000000	R	High Byte of the 16-bit ADC VBUS Data (resolution: 1mV, range: 0V – 16.39V) MSB<7:0>: 32768mV, 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV	N/A

**REG0x28: VBUS\_ADC0 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBUS_ADC[7:0]	00000000	R	Low Byte of the 16-bit ADC VBUS Data (resolution: 1mV, range: 0V – 16.39V) LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

## REGISTER MAPS (continued)

### REG0x29: VAC1\_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VAC1_ADC[15:8]	00000000	R	High Byte of the 16-bit ADC VAC1 Data (resolution: 1mV, range: 0V – 14V) MSB<7:0>: 32768mV, 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV	N/A

### REG0x2A: VAC1\_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VAC1_ADC[7:0]	00000000	R	Low Byte of the 16-bit ADC VAC1 Data (resolution: 1mV, range: 0V – 14V) LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

### REG0x2B: VAC2\_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VAC2_ADC[15:8]	00000000	R	High Byte of the 16-bit ADC VAC2 Data (resolution: 1mV, range: 0V – 14V) MSB<7:0>: 32768mV, 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV	N/A

### REG0x2C: VAC2\_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VAC2_ADC[7:0]	00000000	R	Low Byte of the 16-bit ADC VAC2 Data (resolution: 1mV, range: 0V – 14V) LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

### REG0x2D: VOUT\_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VOUT_ADC[15:8]	00000000	R	High Byte of the 16-bit ADC VOUT Data (resolution: 1mV, range: 0V – 6V) MSB<7:0>: 32768mV, 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV	N/A

### REG0x2E: VOUT\_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VOUT_ADC[7:0]	00000000	R	Low Byte of the 16-bit ADC VOUT Data (resolution: 1mV, range: 0V – 6V) LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

### REG0x2F: VBAT\_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBAT_ADC[15:8]	00000000	R	High Byte of the 16-bit ADC VBAT Data (resolution: 1mV, range: 0V – 6V) MSB<7:0>: 32768mV, 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV	N/A

**REGISTER MAPS (continued)****REG0x30: VBAT\_ADC0 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBAT_ADC[7:0]	00000000	R	Low Byte of the 16-bit ADC VBAT Data (resolution: 1mV, range: 0V – 6V) LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

**REG0x31: IBAT\_ADC1 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBAT_ADC[15:8]	00000000	R	High Byte of the 16-bit ADC IBAT Data (resolution: 1mA, range: 0A – 12A) MSB<7:0>: 32768mA, 16384mA, 8192mA, 4096mA, 2048mA, 1024mA, 512mA, 256mA	N/A

**REG0x32: IBAT\_ADC0 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBAT_ADC[7:0]	00000000	R	Low Byte of the 16-bit ADC IBAT Data (resolution: 1mA, range: 0A – 12A) LSB<7:0>: 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA, 1mA	N/A

**REG0x33: TSBUS\_ADC1 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:2]	Reserved	000000	R	Reserved	N/A
D[1:0]	TSBUS_ADC[9:8]	00	R	Higher 2 bits of the 10-bit ADC TSBUS Data (resolution: 0.09766%, range: 0% – 50%) MSB<2:0>: 50.00192%, 25.00096% Range: 0% – 50%	N/A

**REG0x34: TSBUS\_ADC0 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBUS_ADC[7:0]	00000000	R	Low Byte of the 10-bit ADC TSBUS Data (resolution: 0.09766%, range: 0% – 50%) LSB<2:0>: 12.50048%, 6.25024%, 3.12512%, 1.56256%, 0.78128%, 0.39064%, 0.19532%, 0.09766%	N/A

**REG0x35: TSBAT\_ADC1 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:2]	Reserved	000000	R	Reserved	N/A
D[1:0]	TSBAT_ADC[9:8]	00	R	Higher 2 bits of the 10-bit ADC TSBAT Data (resolution: 0.09766%, range: 0% – 50%) MSB<2:0>: 50.00192%, 25.00096% Range: 0% – 50%	N/A

**REG0x36: TSBAT\_ADC0 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBAT_ADC[7:0]	00000000	R	Low Byte of the 10-bit ADC TSBAT Data (resolution: 0.09766%, range: 0% – 50%) LSB<2:0>: 12.50048%, 6.25024%, 3.12512%, 1.56256%, 0.78128%, 0.39064%, 0.19532%, 0.09766%	N/A



**I<sup>2</sup>C Controlled, Single-Cell, 8A Switched Cap Parallel Battery Charger  
with Integrated Protection and Dual-Input Selector**

**SGM41604**

**REGISTER MAPS (continued)**

**REG0x37: TDIE\_ADC1 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TDIE_ADC_POL	0	R	Polarity of the 16-bit ADC TDIE Data 0 = Positive 1 = Negative	N/A
D[6:0]	TDIE_ADC[14:8]	0000000	R	Higher 7 bits of the 16-bit ADC TDIE Data (resolution: 0.5°C, range: -40°C – 150°C) MSB<7:0>: 8192°C, 4096°C, 2048°C, 1024°C, 512°C, 256°C, 128°C	N/A

**REG0x38: TDIE\_ADC0 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TDIE_ADC[7:0]	00000000	R	Low Byte of the 16-bit ADC TDIE Data (resolution: 0.5°C, range: -40°C – 150°C) LSB<7:0>: 64°C, 32°C, 16°C, 8°C, 4°C, 2°C, 1°C, 0.5°C	N/A

## APPLICATION INFORMATION

### Input Capacitors (C<sub>VAC1</sub>, C<sub>VAC2</sub>, C<sub>VBUS</sub> and C<sub>PMID</sub>)

Input capacitors are selected by considering two main factors:

1. Adequate voltage margin above maximum surge voltage.
2. Not too large voltage margin in order to limit the peak currents drawn from the source and reduce the input noise.

For C<sub>VAC1</sub>, C<sub>VAC2</sub> and C<sub>VBUS</sub>, use low ESR bypass ceramic capacitors to place close to the VAC1/VAC2/VBUS and GND pins respectively. The C<sub>PMID</sub> are determined by the minimum capacitance needed for stable operation and the required ESR to minimize the voltage ripple and load step transients. Typically, 10µF or larger X5R ceramic capacitors are sufficient to meet the C<sub>PMID</sub> requirements of two channels. Consider the DC bias derating of the ceramic capacitors. The X5R and X7R capacitors are relatively stable against DC bias and high temperature. Note that the bias effect is more severe with smaller package sizes, so choose the largest affordable package size. Also consider a large margin for the voltage rating for the worst-case transient input voltages.

### External OVPFETs (ACFET1-RBFET1 and ACFET2-RBFET2)

The maximum recommended input range is 12V. If the supplied VAC1 or VAC2 voltage is above 12V, two sets of back-to-back N-channel OVPFETs are recommended between the adapter inputs and the SGM41604. Choose a low R<sub>DS(on)</sub> MOSFET for the OVPFET to minimize power losses.

### Flying Capacitors (C<sub>FLY</sub>)

For selection of the C<sub>FLY</sub> capacitors, the current rating, ESR and the bias voltage derating are critical parameters. The C<sub>FLY</sub> capacitors are biased to different DC voltages according to the operation mode. To trade-off between efficiency and power density, set the C<sub>FLY</sub> voltage ripple to the 2% of the V<sub>VOUT</sub> as a good starting point. The C<sub>FLY</sub> for each channel can be calculated by Equation 10:

$$C_{FLY} = \frac{I_{BAT}}{4f_{SW}V_{CFLY\_RPP}} = \frac{I_{BAT}}{8\%f_{SW}V_{DC\_CFLY}} \quad (10)$$

where I<sub>BAT</sub> is the charging current and V<sub>CFLY\_RPP</sub> is the peak-to-peak voltage ripple of the C<sub>FLY</sub>.

Choosing a too small capacitor for C<sub>FLY</sub> results in lower efficiency and high output voltage/current ripples. However choosing a too large C<sub>FLY</sub> only provides minor efficiency and output ripple improvements.

The default switching frequency is f<sub>SW</sub> = 500kHz. It can be adjusted by FSW\_SET[2:0] bits in REG0x10. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance (R<sub>EFF</sub>). An optimum switching frequency can be found for any selected C<sub>FLY</sub> capacitor to minimize losses.

### Output Capacitor (C<sub>VOUT</sub>)

C<sub>VOUT</sub> selection criteria are similar to the C<sub>FLY</sub> capacitor. Larger C<sub>VOUT</sub> value results in less output voltage ripple, but due to the dual-channel operation, the C<sub>VOUT</sub> RMS current is much smaller than C<sub>FLY</sub>, so smaller capacitance value can be chosen for C<sub>VOUT</sub> as given in Equation 11:

$$C_{VOUT} = \frac{I_{BAT} \times t_{DEAD}}{0.5 \times V_{VOUT\_RPP}} \quad (11)$$

where t<sub>DEAD</sub> is the dead time between the two channels and V<sub>VOUT\_RPP</sub> is the peak-to-peak output voltage ripple and is typically set to the 2% of V<sub>VOUT</sub>.

C<sub>VOUT</sub> is biased to the battery voltage and its nominal value should be derated for battery voltage DC bias. Typically a 22µF, X5R or better grade ceramic capacitors placed close to the VOUT and GND pins provide stable performance of two channels.

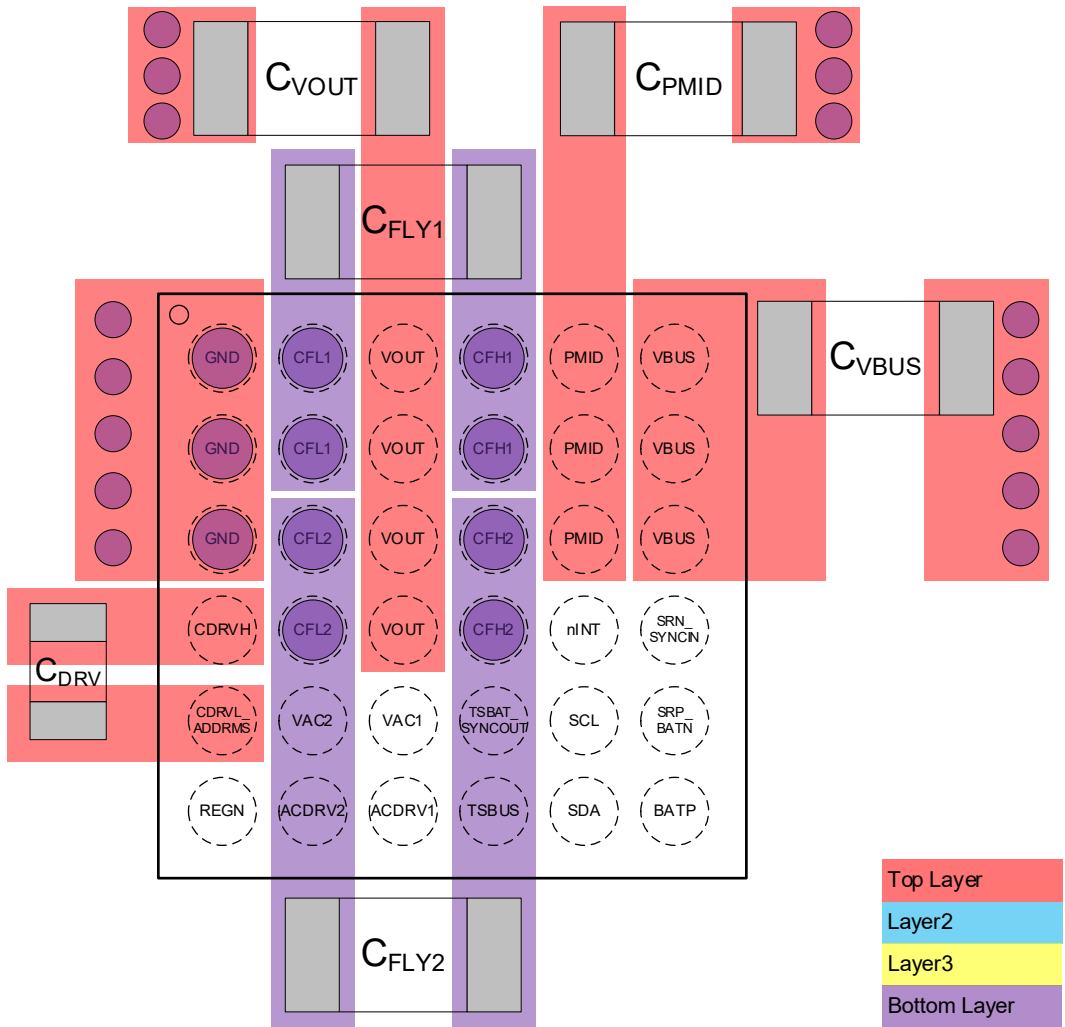
### PCB Layout Guidelines

A good PCB layout is critical for stable operation of the SGM41604. Follow these guidelines for the best results:

1. Use short and wide traces for VBUS as it carries high current.
2. Minimize connectors wherever possible. Connector losses are significant especially at high currents.
3. Use solid thermal vias for better thermal relief.
4. Bypass VBUS, PMID and VOUT pins to GND with ceramic capacitors as close to the device pins as possible.
5. Place C<sub>FLY</sub> capacitors as close as possible to the device with small pad areas to reduce switching noise and EMI.
6. CLFY pours of the two channels should be as symmetrical as possible.
7. Connect and reference all power signals to the GND pins (preferably the nearest ones).
8. Try not to interrupt or break the power planes by signal traces.

The reference layout is shown in Figure 16.

**APPLICATION INFORMATION (continued)**



**Figure 16. Reference Layout**

**TYPICAL APPLICATION CIRCUIT**

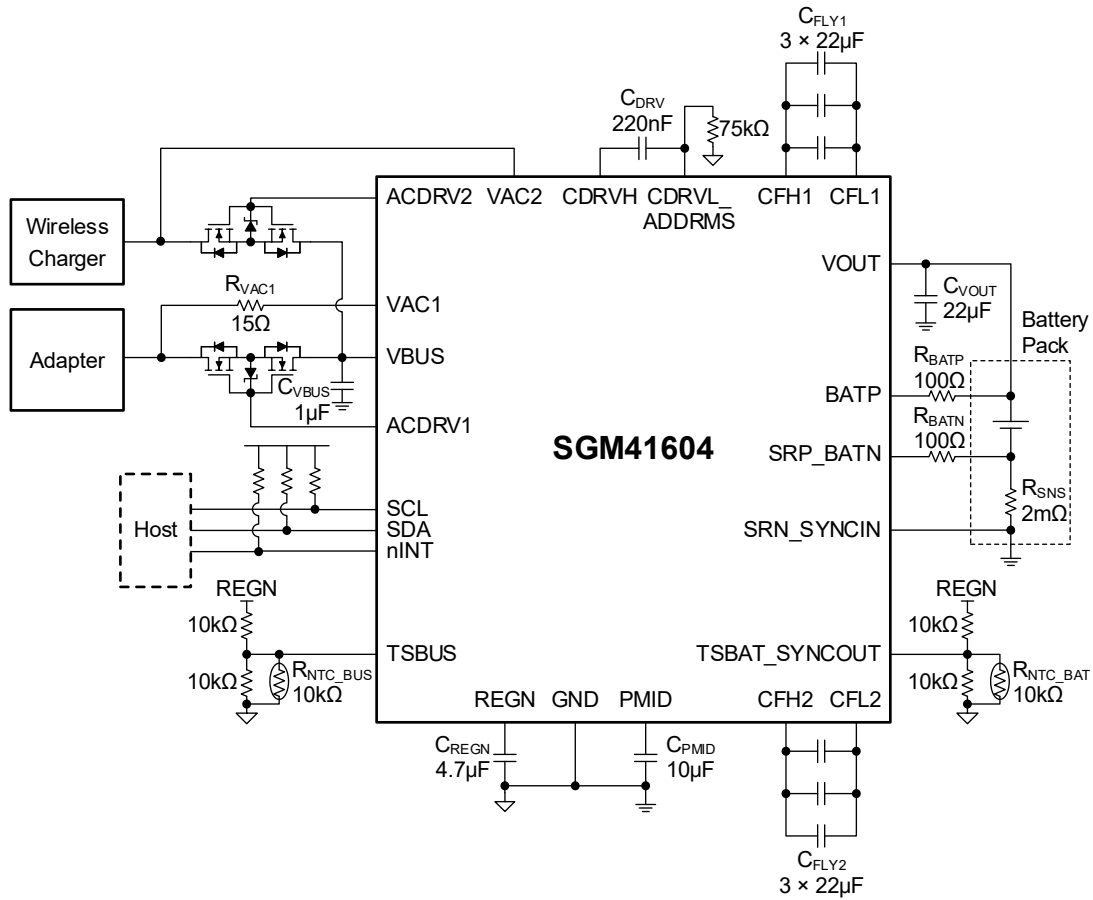


Figure 17. Typical Application Circuit of SGM41604

**REVISION HISTORY**

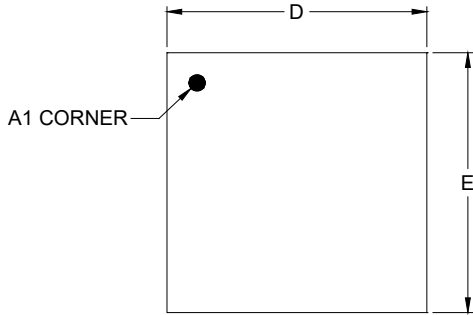
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (OCTOBER 2025)	Page
Changed from product preview to production data.....	All

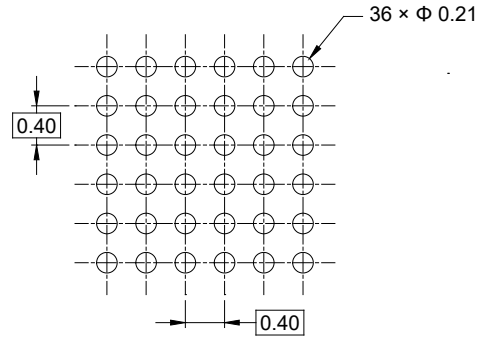
# PACKAGE INFORMATION

## PACKAGE OUTLINE DIMENSIONS

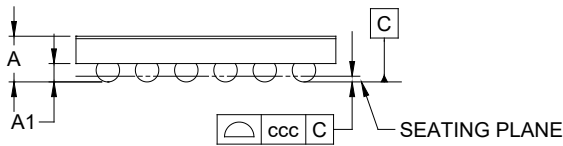
### WLCSP-2.65×2.65-36B-A



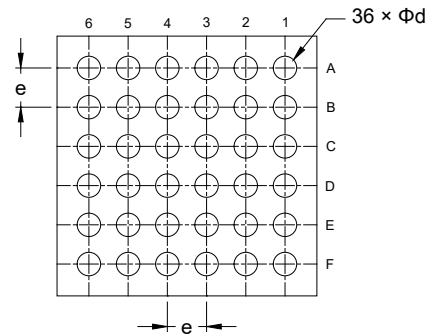
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



BOTTOM VIEW

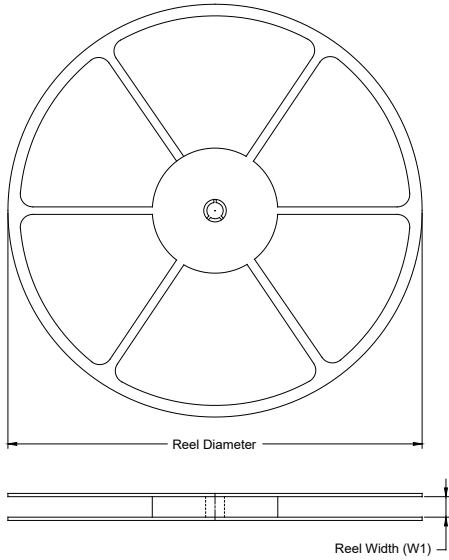
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.500
A1	0.159	-	0.215
D	2.620	-	2.680
E	2.620	-	2.680
d	0.209	-	0.269
e	0.400 BSC		
ccc	0.050		

NOTE: This drawing is subject to change without notice.

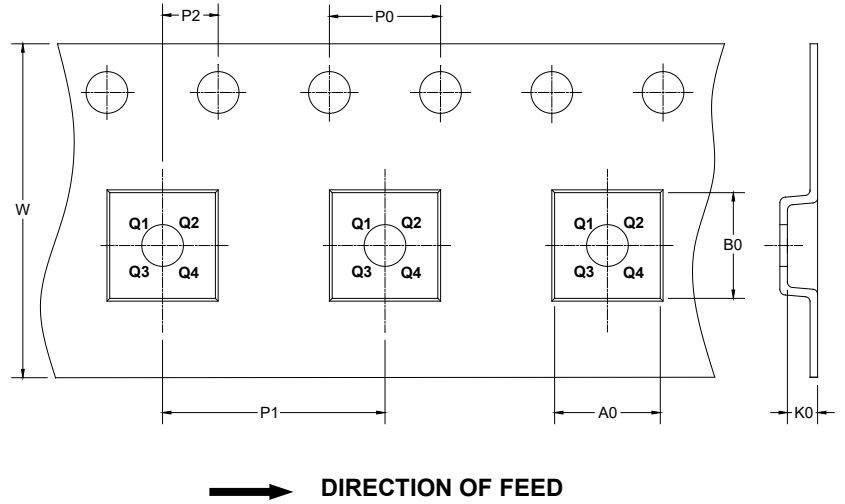
# PACKAGE INFORMATION

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

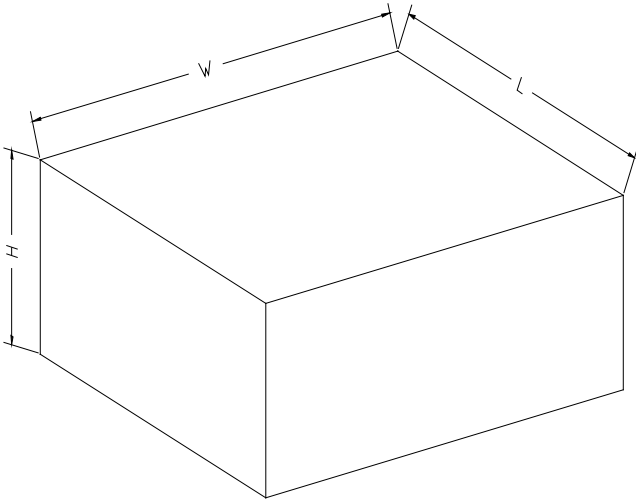
### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.65×2.65-36B-A	7"	9.5	2.75	2.75	0.81	4.0	4.0	2.0	8.0	Q1

DD0001

# PACKAGE INFORMATION

## CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

DD0002