# SGM3810
# Boost WLED Driver with Dual Output Power Supply for TFT LCD Bias

## GENERAL DESCRIPTION

The SGM3810 is an integrated Boost mode WLED driver with single inductor dual output (SIDO) topological LCD Bias supply.

The SGM3810 integrates an asynchronous Boost WLED driver with high efficiency, low EMI and high output voltage. The Boost converter has a 32V, 1.6A internal FET and can work at 1.25MHz switching frequency. Its strong driving ability can drive single or multiple parallel LED strings, which can be well applied to LED drivers such as smart phone backlight and tablet backlight.

The maximum LED current can be programmed by the external current-sense resistor ($R_{SET}$), and the LED current is programmed through an $I^2C$ interface by regulating the LED_FB pin voltage ($V_{FB}$) as percentage of 200mV.

The SGM3810 generates both positive and negative precision regulated voltage power sources, with a single inductor dual output converter. Outputs are programmable in 100mV steps in 4.0V to 6.4V range and -4.0V to -6.4V range, which are commonly used in drivers for LCD displays, as well as in any other circuits requiring both rails with different loading on each rail. With input in the range of 2.5V to 5.5V, the device is optimized for loading 100mA in boost-inverter mode and also works in buck-inverter mode.

It also has complete protection functions, including open LED protection, OCP/OVP protection and thermal shutdown protection.

The SGM3810 is available in a Green WLCSP-1.1×1.75 -15B package. It operates over an ambient temperature range of -40℃ to +85℃.

## FEATURES

- **WLED Driver**
  - **Asynchronous Boost Topologic**
  - **12-Bit Resolution for Dimming Control**
  - **Integrated 32V, 1.6A Current Limit MOSFET**
  - **32V Open LED Protection for 10 LEDs in Series**
  - **Maximum 200mV Reference Voltage**
  - **Up to 90% Efficiency**
  - **1.25MHz Switching Frequency**
- **LCD Bias**
  - **Single Inductor for Positive & Negative Outputs**
  - **4.0V to 6.4V Programmable for Positive Output**
  - **-4.0V to -6.4V Programmable for Negative Output**
  - **120mA Output Current for $V_{VPO}$ and $V_{VNO}$ at $V_{IN}$ > 3.0V**
  - **1% Output Voltage Accuracy**
  - **1.2MHz Switching Frequency**
  - **Configurable Active Discharge**
- **$I^2C$ Interface with 1.2V Logic**
- **Under-Voltage Lockout (UVLO)**
- **Over-Temperature Protection (OTP)**
- **Short-Circuit Protection (SCP)**
- **Available in a Green WLCSP-1.1×1.75-15B Package**

## APPLICATIONS

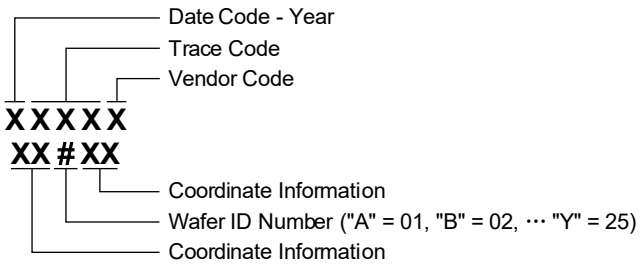
Smart Phones
Tablets
PADs

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM3810 | WLCSP-1.1×1.75-15B | -40℃ to +85℃ | SGM3810YG/TR | 3810<br>XXXXX<br>XX#XX | Tape and Reel, 3000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

VIN, LED_FB Voltages ..... -0.3V to 6V
LED_SW Voltages ..... -0.3V to 33V
HWEN, SCL, SDA Voltage ..... -0.3V to $V_{IN}$ + 0.3V
SWP, PO, VPO Voltages ..... -0.3V to 7.5V
SWP Voltage (Transient: 10ns) ..... -2V to 8V
VNO Voltages ..... -7.5V to 0.3V
SWN Voltage ..... -7.5V to 6V
SWN Voltage (Transient: 10ns) ..... -8V to 8V
Package Thermal Resistance
WLCSP-1.1×1.75-15B, $\theta_{JA}$ ..... 66.9℃/W
WLCSP-1.1×1.75-15B, $\theta_{JB}$ ..... 9.7℃/W
WLCSP-1.1×1.75-15B, $\theta_{JC}$ ..... 32℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±1000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.5V to 5.5V
Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

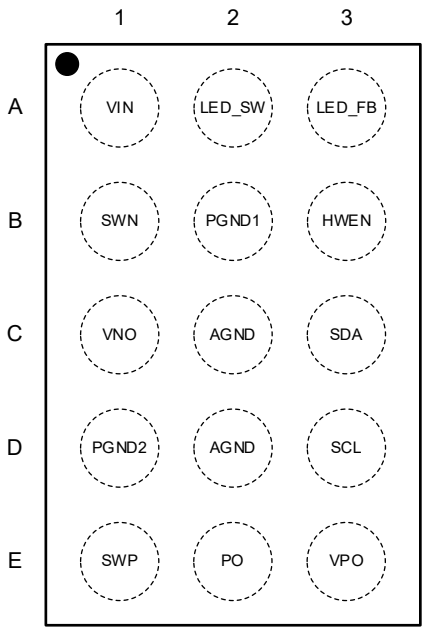
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




WLCSP-1.1×1.75-15B

## PIN DESCRIPTION

| PIN | NAME | I/O | FUNCTION |
|---|---|---|---|
| A1 | VIN | P | Power Supply Input. |
| A2 | LED_SW | P | WLED Boost Switch Node. |
| A3 | LED_FB | I | WLED LED Current Feedback Pin. Connect a Sense Resistor $R_{SET}$ from LED_FB to GND. |
| B1 | SWN | P | Switch Node N. Connect this pin to one end of power inductor. |
| B2 | PGND1 | G | WLED Boost Power Ground Pin. |
| B3 | HWEN | I | Hardware Enable Input Pin. Drive HWEN high to enable the device and allow $I^2C$ write commands. |
| C1 | VNO | P | Negative-Rail Output. |
| C2, D2 | AGND | G | Analog Ground. |
| C3 | SDA | I/O | Data Signal of $I^2C$ Interface. |
| D1 | PGND2 | G | LCD Bias Power Ground. |
| D3 | SCL | I | Clock Signal of $I^2C$ Interface. |
| E1 | SWP | P | Switch Node P. Connect this pin to the other end of power inductor. |
| E2 | PO | P | Positive Output Middle Node. |
| E3 | VPO | P | Positive-Rail Output. |

NOTE: I = input, I/O = input or output, P = power, G = ground.

## TYPICAL APPLICATION

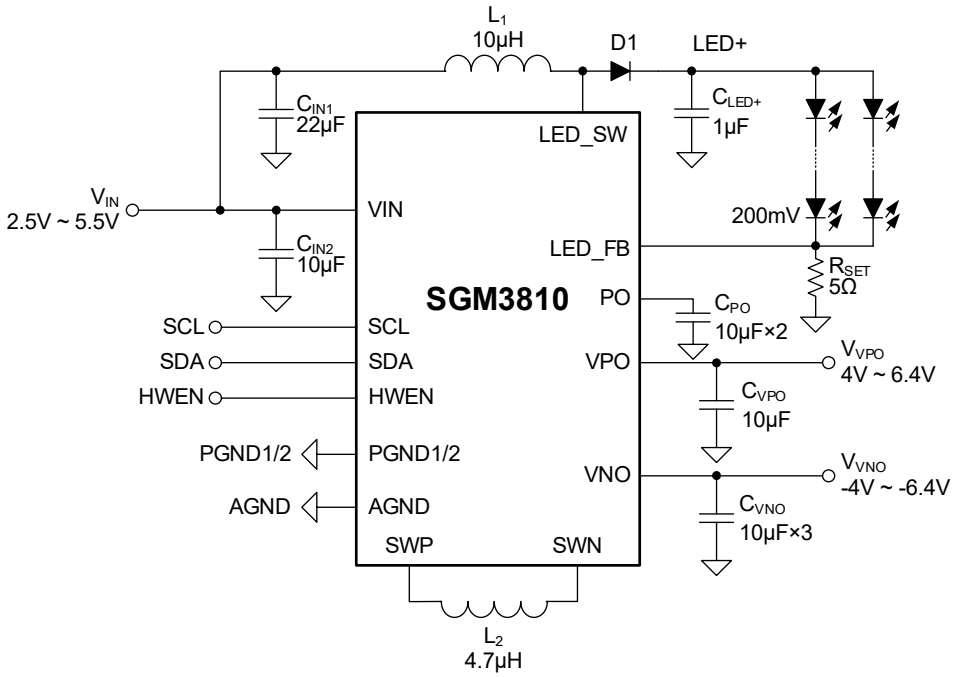



**Figure 1. Typical Application Circuit**

## RECOMMENDED COMPONENT SELECTION

**Table 1. Recommended Component Selection**

| Component | Value | Number | Electrical Spec | Part Number | Manufacturer |
|---|---|---|---|---|---|
| $C_{IN1}$ | 22μF | 1 | X5R, 16V, 0603 | GRM188R61A226ME15D | Murata |
| $C_{IN2}$, $C_{PO}$, $C_{VPO}$ | 10μF | 4 | X5R, 16V, 0603 | GRM188R61C106KAAL | Murata |
| $C_{VNO}$ | 10μF | 3 | X5R, 16V, 0603 | GRM188R61C106KAAL | Murata |
| $C_{LED+}$ | 1μF | 1 | X5R, 50V, 0402 | GRM155R61H105KE05D | Murata |
| $L_1$ | 10μH | 1 | 2A, 190mΩ, 404012 | CKSTTH0412N-10uH/M | Cenker |
| | | | 1.3A, 390mΩ, 252012 | SDEM25201B-100MS | Cyntec |
| $L_2$ | 4.7μH | 1 | 2.2A, 130mΩ, 252010 | CIGW252010EH4R7 | Samsung |
| $R_{SET}$ | 5Ω | 1 | 5Ω for 40mA ILED | - | - |
| D1 | Diode | 1 | 40V, 1A, Schottky diode | PMEG4010EH | NXP |

# ELECTRICAL CHARACTERISTICS

($V_{IN}$ = 3.7V, $T_J$ = -40℃ to +85℃, typical values are at $T_J$ = +25℃, unless otherwise specified noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **General Features** | | | | | | |
| Input Voltage Range | $V_{IN}$ | | 2.5 | | 5.5 | V |
| Under-Voltage Lockout Threshold | $V_{UVLO}$ | $V_{IN}$ falling | 1.9 | 2.0 | 2.1 | V |
| | | $V_{IN}$ rising | 2.0 | 2.1 | 2.2 | V |
| Supply Current with No Load | $I_Q$ | $V_{IN}$ = 3.7V, no switching | | 0.3 | 0.5 | mA |
| | | $V_{IN}$ = 3.7V, only SIDO switching with no load | | 0.45 | | |
| Shutdown Current | $I_{SD}$ | $V_{IN}$ = 3.7V, HWEN = Low | | 0.3 | 1.0 | μA |
| **WLED Driver** | | | | | | |
| Switching Frequency | $f_{LED\_SW}$ | $V_{IN}$ = 3.7V, $T_J$ = +25℃ | 1.1 | 1.25 | 1.4 | MHz |
| Maximum Boost Duty Cycle | $D_{MAX}$ | | 93.2 (1) | 94.5 | | % |
| Switching MOSFET Current Limit | $I_{PEAK\_LED}$ | $V_{IN}$ = 3.7V | 1.05 | 1.6 | 2.2 | A |
| N-Channel MOSFET On-Resistance | $R_{DS(ON)}$ | I = 0.2A | | 0.35 | | Ω |
| Output Over-Voltage Threshold | $V_{OVP\_SW}$ | | 31.5 | 32.2 | 33 | V |
| LED_FB Pin Bias Current | $I_{FB}$ | $V_{FB}$ = 200mV | | 0.01 | 0.05 | μA |
| Voltage Feedback Regulation Voltage | $V_{REF}$ | $V_{REF}$ = 200mV × Code/4095 | | | | |
| | | 100%, Code = 4095, $T_J$ = +25℃ | 194 | 200 | 206 | mV |
| | | 10%, Code = 410, $T_J$ = +25℃ | 19 | 20 | 21 | mV |
| | | 1%, Code = 41, $T_J$ = +25℃ | 1.9 | 2.1 | 2.3 | mV |
| | | 0.2%, Code = 8, $T_J$ = +25℃ | 0.4 | 0.5 | 0.6 | mV |
| **SIDO Bias Converter** | | | | | | |
| Switching Frequency | $f_{SW\_BIAS}$ | $V_{IN}$ = 3.7V | 1.05 | 1.2 | 1.35 | MHz |
| Inductor Peak Current | $I_{PEAK\_BIAS}$ | $V_{IN}$ = 3.7V | 1.3 | 1.6 | 1.9 | A |
| Positive Output Voltage Range | $V_{VPO}$ | | 4.0 | | 6.4 | V |
| Positive Output Current Capability | $I_{VPO\_MAX}$ | $V_{IN}$ = 3.0V, $V_{VPO}$ = +6.4V | 120 | | | mA |
| Positive Output Voltage Accuracy | $V_{VPO\_ACC\_54}$ | $V_{IN}$ = 3.7V, $V_{VPO}$ = +5.4V | -45 | | 45 | mV |
| | $V_{VPO\_ACC\_60}$ | $V_{IN}$ = 3.7V, $V_{VPO}$ = +6.0V | -50 | | 50 | mV |
| Positive Output Ripple | $V_{VPO\_RIPPLE}$ | $V_{IN}$ = 2.5V to 5.5V, $I_{OUTP}$ = 40mA | | 30 | | mV |
| Positive Output Line Regulation | $V_{VPO\_LINEREG}$ | $V_{IN}$ = 2.5V to 5.5V, $I_{OUTP}$ = 40mA | | 3 | | mV |
| Positive Output Line Transient | $V_{VPO\_LINETRAN}$ | $\Delta V_{IN}$ = 0.5V, $t_R/t_F$ = 10μs, $I_{OUTP}$ = 0mA to 100mA | | 30 | | mV |
| Positive Output Load Regulation | $V_{VPO\_LOADREG}$ | $V_{IN}$ = 2.5V to 5.5V, $I_{OUTP}$ = 0mA to 100mA | | 3 | | mV |
| Discharge Resistor of Positive Output | $R_{DP}$ | | | 330 | | Ω |
| Discharge Time of Positive Output | $t_{DISP}$ | | | 5 | | ms |
| Negative Output Voltage Range | $V_{VNO}$ | | -6.4 | | -4.0 | V |
| Negative Output Current Capability | $I_{VNO\_MAX}$ | $V_{IN}$ = 3.0V, $V_{VNO}$ = -6.4V | 120 | | | mA |
| Negative Output Voltage Accuracy | $V_{VNO\_ACC\_54}$ | $V_{IN}$ = 3.7V, $V_{VNO}$ = -5.4V | -45 | | 45 | mV |
| | $V_{VNO\_ACC\_60}$ | $V_{IN}$ = 3.7V, $V_{VNO}$ = -6.0V | -50 | | 50 | mV |
| Negative Output Ripple | $V_{VNO\_RIPPLE}$ | $V_{IN}$ = 2.5V to 5.5V, $I_{OUTN}$ = 40mA | | 30 | | mV |
| Negative Output Line Regulation | $V_{VNO\_LINEREG}$ | $V_{IN}$ = 2.5V to 5.5V, $I_{OUTN}$ = 40mA | | 3 | | mV |
| Negative Output Line Transient | $V_{VNO\_LINETRAN}$ | $\Delta V_{IN}$ = 0.5V, $t_R/t_F$ = 10μs, $I_{OUTN}$ = 0mA to 100mA | | 60 | | mV |
| Negative Output Load Regulation | $V_{VNO\_LOADREG}$ | $V_{IN}$ = 2.5V to 5.5V, $I_{OUTN}$ = 0mA to 100mA | | 3 | | mV |
| Discharge Resistor of Negative Output | $R_{DN}$ | | | 160 | | Ω |
| Discharge Time of Negative Output | $t_{DISN}$ | | | 5 | | ms |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{IN}$ = 3.7V, $T_J$ = -40℃ to +85℃, typical values are at $T_J$ = +25℃, unless otherwise specified noted.)

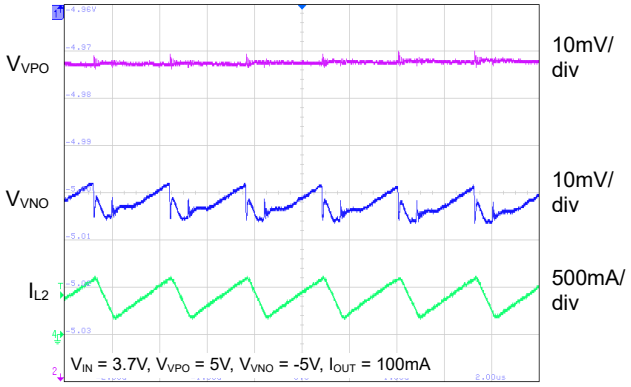
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Digital Interface ($I^2C$, HWEN)** | | | | | | |
| $I^2C$ Clock Frequency | $f_{SCL}$ | $V_{IN}$ = 2.5V to 5.5V | 10 | 400 | 1000 | kHz |
| Low Level Input Voltage | $V_{IL}$ | $V_{IN}$ = 2.5V to 5.5V, $T_J$ = +25℃ | | | 0.36 | V |
| High Level Input Voltage | $V_{IH}$ | $V_{IN}$ = 2.5V to 5.5V, $T_J$ = +25℃ | 0.8 | | | V |
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown Threshold | $T_{SHUTDOWN}$ | | | 150 | | ℃ |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | | 20 | | ℃ |

NOTE: 1. Guaranteed by design.

## TYPICAL PERFORMANCE CHARACTERISTICS

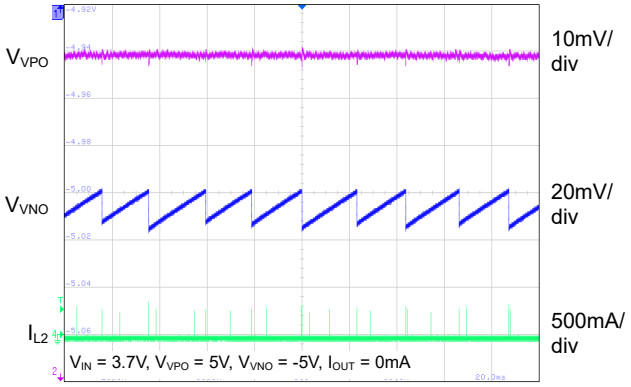
$T_A$ = +25℃, $V_{IN}$ = 3.7V, $V_{VPO}$ = 5V, $V_{VNO}$ = -5V, 8S2P LEDs, unless otherwise noted.

Ripple at Heavy Load - LCD Bias



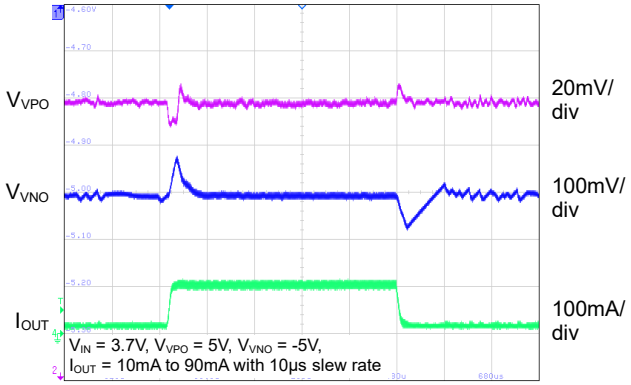

Time (500ns/div)

Ripple at Light Load - LCD Bias



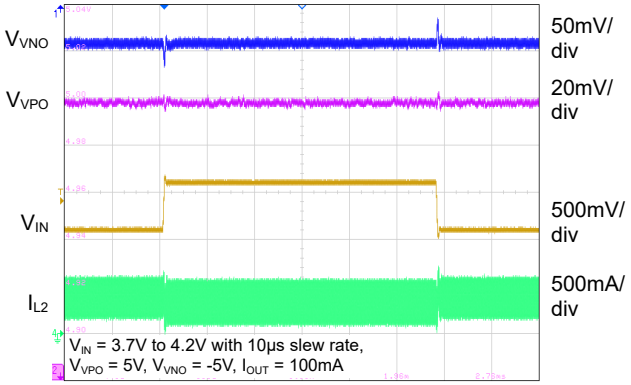

Time (5ms/div)

Load Transient - LCD Bias



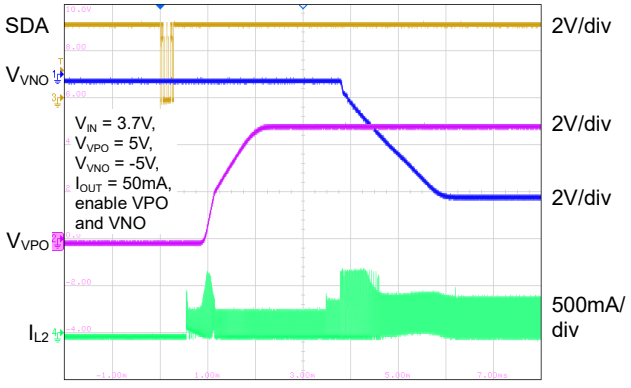

Time (100μs/div)

Line Transient - LCD Bias



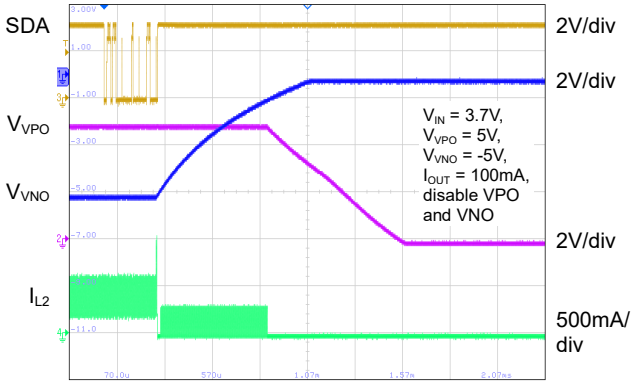

Time (400μs/div)

Startup - LCD Bias




Time (1ms/div)

Shutdown - LCD Bias

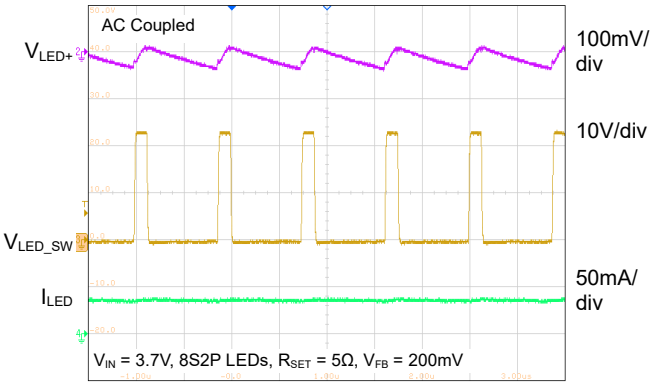



Time (250μs/div)

## TYPICAL PERFORMANCE CHARACTERISTICS

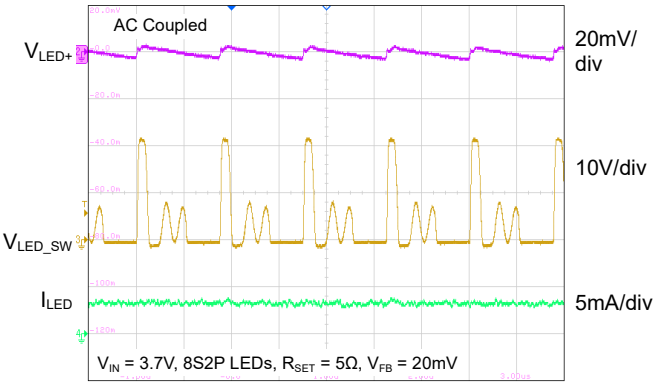
$T_A$ = +25℃, $V_{IN}$ = 3.7V, $V_{VPO}$ = 5V, $V_{VNO}$ = -5V, 8S2P LEDs, unless otherwise noted.

Ripple at Heavy Load - LED Diver



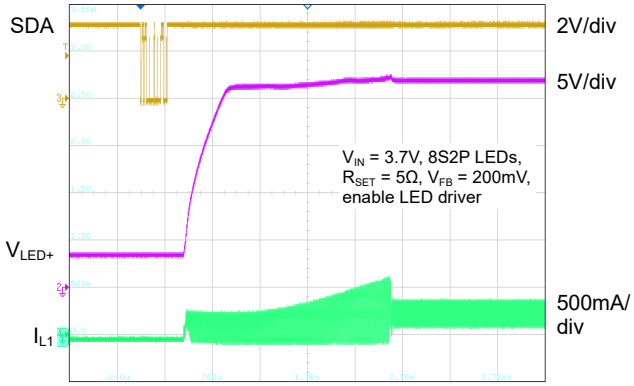

Time (500ns/div)

Ripple at Light Load - LED Diver



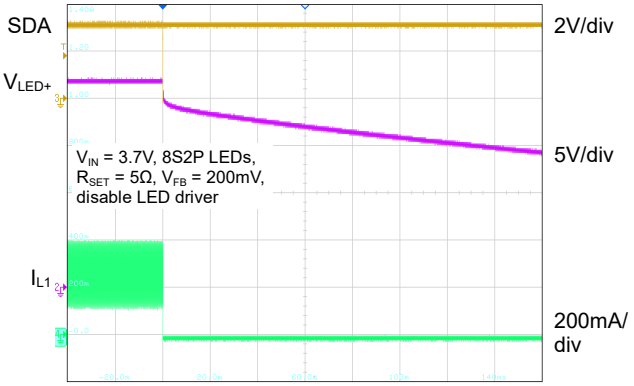

Time (500ns/div)

Startup - LED Diver



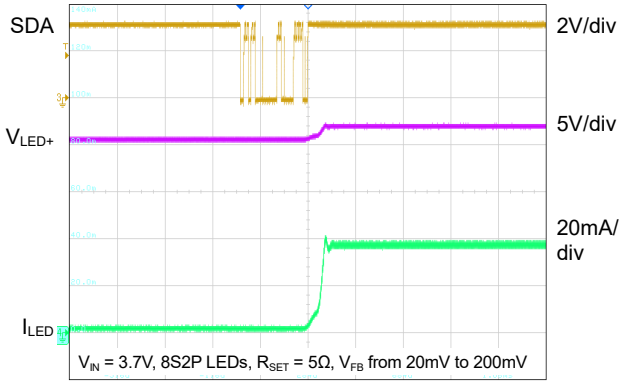

Time (500μs/div)

Shutdown - LED Diver



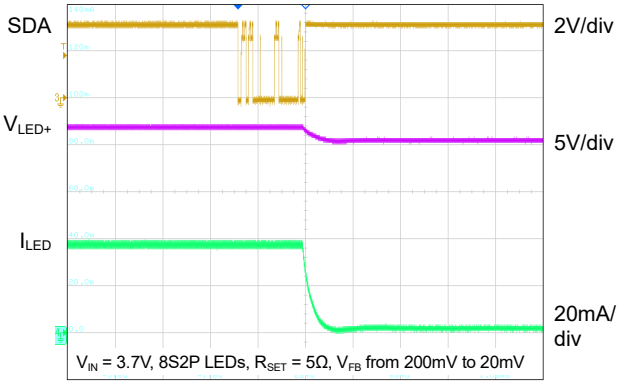

Time (20ms/div)

Brightness Dimming - LED Diver




Time (200μs/div)

Brightness Dimming - LED Diver

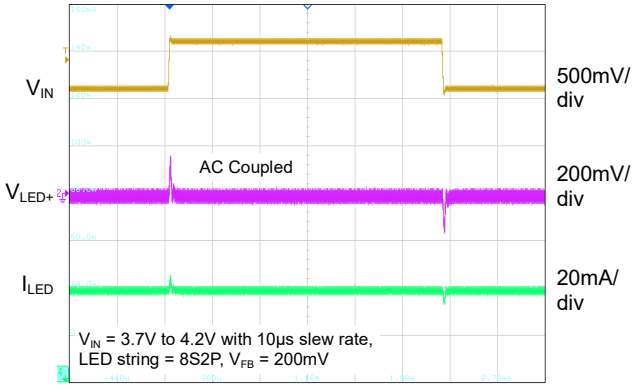



Time (200μs/div)

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

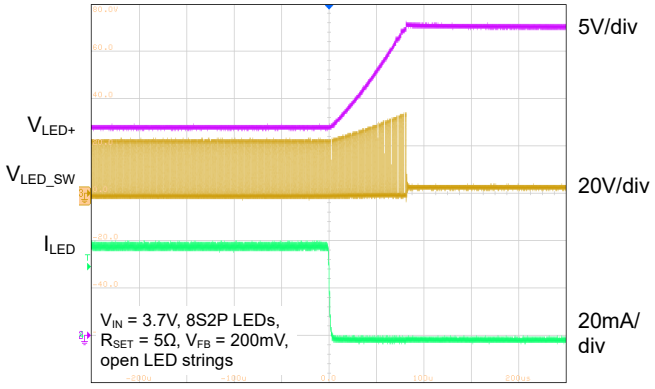
$T_A$ = +25℃, $V_{IN}$ = 3.7V, $V_{VPO}$ = 5V, $V_{VNO}$ = -5V, 8S2P LEDs, unless otherwise noted.

Line Transient - LED Diver



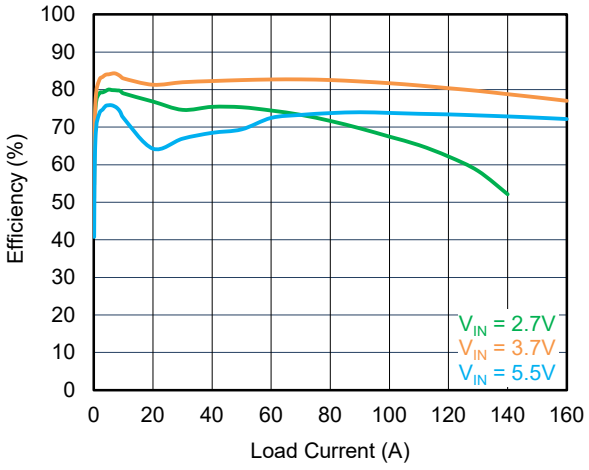

Time (400μs/div)

LED Open Protection - LED Diver

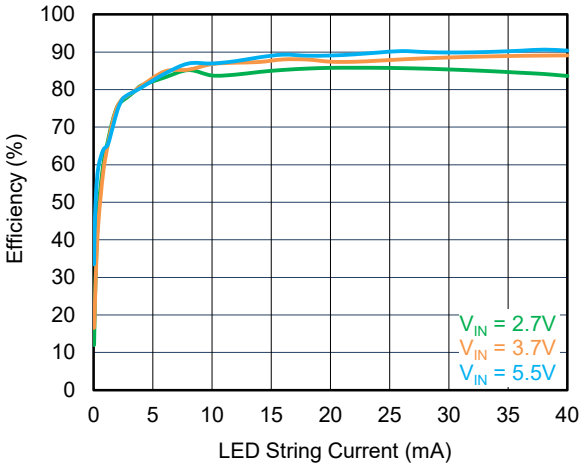



Time (50μs/div)

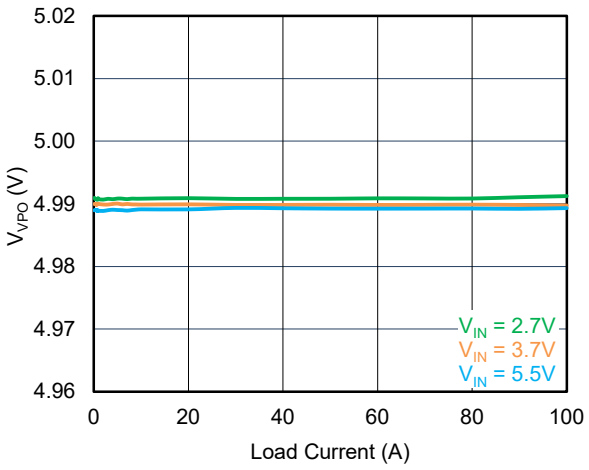
SIDO Efficiency vs. Load Current



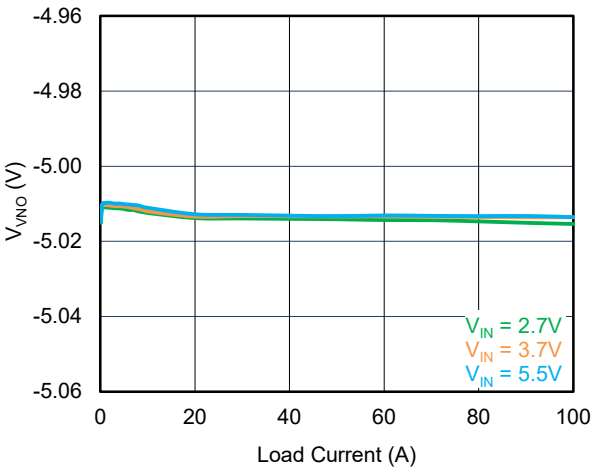

Efficiency vs. LED String Current




Load Regulation



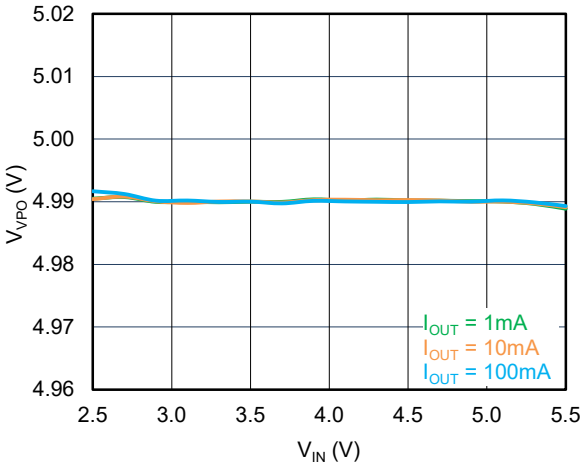

Load Regulation



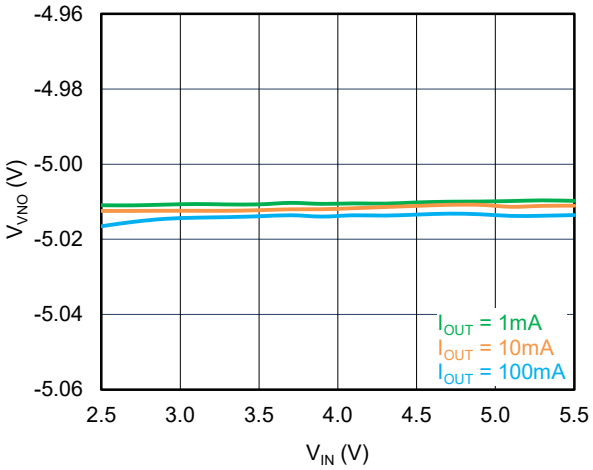
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{IN}$ = 3.7V, $V_{VPO}$ = 5V, $V_{VNO}$ = -5V, 8S2P LEDs, unless otherwise noted.

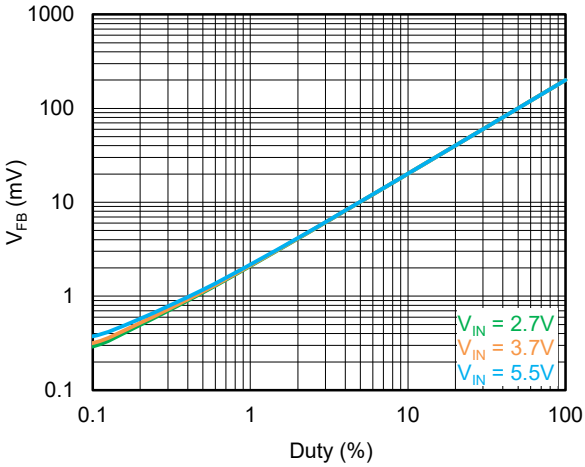
Line Regulation




Line Regulation




$V_{FB}$ Regulation



## FUNCTIONAL BLOCK DIAGRAM

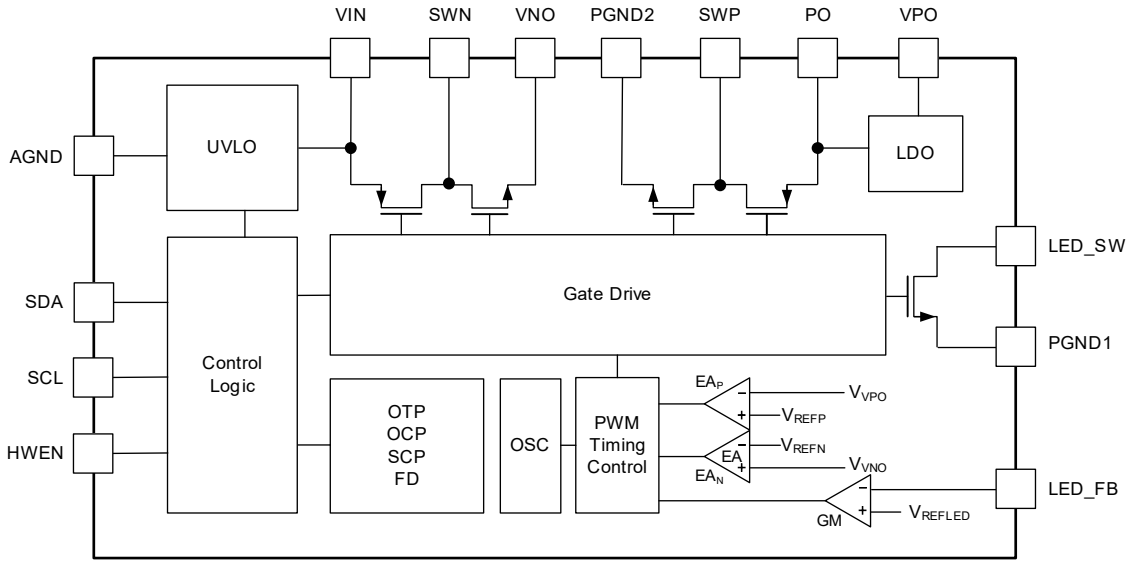



**Figure 2. SGM3810 Functional Block Diagram**

## DETAILED DESCRIPTION

The SGM3810 is an integrated Boost mode WLED driver with single inductor dual output (SIDO) topological LCD Bias supply.

The SGM3810 integrates an asynchronous Boost WLED driver with high efficiency, low EMI and high output voltage. The Boost converter has a 32V, 1.6A internal FET and can work at 1.25MHz switching frequency. Its strong driving ability can drive single or multiple parallel LED strings, which can be well applied to LED drivers such as smart phone backlight and tablet backlight.

The maximum LED current can be programmed by the external current-sense resistor $R_{SET}$, and the LED current is programmed through an $I^2C$ interface by regulating the LED_FB pin voltage $V_{FB}$ as percentage of 200mV.

The SGM3810 generates both positive and negative precision regulated voltage power sources, with a single inductor dual output converter. Outputs are programmable with 100mV steps in 4.0V to 6.4V range and -4.0V to -6.4V range, which are commonly used in drivers for LCD displays, as well as in any other circuits requiring both rails with different loading on each rail. With input in the range of 2.5V to 5.5V, the device is optimized for loading 100mA in boost-inverter mode and also works in buck-inverter mode.

It also has complete protection functions, including open LED protection, OCP/SCP/OVP protection and thermal shutdown protection.

### Enabling the SGM3810

The SGM3810 has a logic level input HWEN which serves as the master enable/disable for the device. When HWEN is low and the input voltage is above UVLO rising threshold, the device is disabled, and the registers except the flag register are reset to their default states, the $I^2C$ bus is inactive, and the device is in a low-power shutdown mode. When HWEN is forced high, the device is enabled, and $I^2C$ writes are allowed to the device.

### Soft Start-Up

SGM3810 integrates the soft start-up function. It can ensure that the output voltage of Boost converter and the SIDO converter rise slowly by limiting the output voltage of GM/EA amplifiers during start-up. This means that the device can effectively avoid the surge current. After the start-up is completed, the device transforms to the internal reference voltage for closed-loop control.

## DETAILED DESCRIPTION (continued)

### Open LED Protection

Open LED protection can close the WLED driver in case of LED or $R_{SET}$ disconnection, and prevent damage to the device. The SGM3810 will monitor the voltage of LED_SW pin in each switching cycle. When the voltage of LED_SW pin exceeds $V_{OVP}$ threshold for 8 consecutive cycles, the device turns off the switch FET and closes the WLED driver. When the output of the Boost converter is open, the LED_FB pin voltage becomes 0V. This can lead to the switch FET continues to turn on and the output voltage raises, which triggers the open LED protection. The device remains in shutdown mode until it is enabled by setting the WLED_EN bit. This function can effectively prevent the device from damaging when the output voltage exceeds $V_{OVP}$ threshold.

### WLED Driver Shutdown

The WLED driver enters shutdown mode when setting WLED_EN bit to 0. In shutdown mode, the internal switch FET does not work, and the device maintains in a low loss condition. At the same time, the minimum forward voltage of the LED array should be kept higher than the maximum input voltage. Otherwise, the DC current path will make the LED array work through the inductor and Schottky diode, which often does not meet design requirement.

### WLED Current Program

The LED_FB pin voltage $V_{FB}$ of SGM3810 depends on the internal reference voltage $V_{REF\_LED}$. The maximum value of $V_{REF}$ is 200mV. The external programming of LED current can be realized by using the current-sense resistance connected in series with the LED. The value of the $R_{SET}$ is calculated using Equation 1:

$$I_{LED} = \frac{V_{FB}}{R_{SET}} \quad (1)$$

where

$I_{LED}$ = total output current of LED string(s)

$V_{FB}$ = regulated voltage of LED_FB pin

$R_{SET}$ = current-sense resistor

The SGM3810 controls LED current by receiving $I^2C$ WLED dimming bits VREF[11:0] as the internal DAC of $V_{REF}$.

$$V_{FB} = V_{REF} = VREF[11:0]/4095 \times 200mV \quad (2)$$

The output current tolerance depends on the LED_FB accuracy and the current sensor resistor accuracy.

### LCD Bias VPO and VNO

This device provides two independent power rails, one positive and one negative for powering TFT LCD displays, in a small overall board area with just a few external components, which are one inductor and several capacitors. A unique SIDO (single inductor dual output) control scheme is developed for suppressing the loading cross interference between two rails, which is considered as a common drawback when using single inductor to generate two rails. The circuit maintains regulation on both rails without compromising performance in either boost-inverter operation with any loading condition or buck-inverter operation with almost any loading condition.

The LCD bias supply positive voltage VPO and negative voltage VNO are generated by the SIDO converter that controlled by VPO_EN and VNO_EN, and the output voltages can be easily programmed through the VPO_SET[4:0] and VNO_SET[4:0] bits.

The VPO and VNO can be discharged when shutdown, and the discharge function can be disabled by writing DISP and DISN bits to 0.

### Fault Flag

SGM3810 monitors fault events and indicates them in the fault flag register, such as:

- WLED over-voltage – LED_OVP
- VPO short-circuit – VPO_SC
- VNO short-circuit – VNO_SC
- VPO over-voltage – VPO_OVP
- VNO over-voltage – VNO_OVP
- Thermal shutdown – TSD

### Under-Voltage Lockout

The SGM3810 integrates an under-voltage lockout block (or UVLO) that enables the device once the voltage on VIN pin exceeds the UVLO rising threshold. The device will be disabled as soon as the VIN voltage falls below the UVLO falling threshold.

### Over-Current Protection (OCP)

The SGM3810 includes a current sensing circuitry which monitors the inductor current during each ON period. If the current value becomes greater than the current limit, the switch that is charging the inductor turns off, and it forces the inductor to discharge.

## DETAILED DESCRIPTION (continued)

### LCD Bias Short-Circuit Protection (SCP)

The SGM3810 has an advanced short-circuit protection mechanism which prevents damage to these devices from unexpected applications. When the VPO or VNO output becomes shorted to ground, the SIDO converter current limit will decrease to 750mA.

An SCP or overload occurs if any of the following events happens:

- VPO is not in regulation 2ms after VPO is enabled then VPO (and VNO) converter/s shut down.
- VNO is not in regulation 2ms after VNO is enabled (after $t_{DELAY}$) then VNO (and VPO) converter/s shut down.
- VPO falls below 85% of the programmed output voltage longer than 100μs then all converters shut down.
- VNO rises above 85% of the programmed output voltage longer than 100μs then all converters shut down.

### EMI and Acoustic Interference

Switching noise propagating along wire connections commonly dominates the EMI from the device operation, which may degrade receiver sensitivities by injecting interference into its carrier band or interim band through inter-modulation in its down converters. Inserting a ferrite bead into input power path and making short and straightforward path always work well in practice.

### Component and Parameter Selection

$C_{IN1}$, $C_{IN2}$, $C_{PO,}$ $C_{VPO}$ and $C_{VNO}$ can be any capacitance in the range of 10μF ~ 47μF, and low loss Z5U, X7R and X5R dielectric capacitors are recommended for better performance. A 10μH ~ 33μH inductor is recommended for $L_1$. A 2.2μH ~ 10μH inductor is recommended for $L_2$.

### Schottky Diode Selection

In order to ensure the best efficiency of SGM3810, the selected Schottky diode should have low forward voltage, fast reverse recovery speed, and low junction capacitance. At the same time, the average and peak current ratings of the selected diode should exceed the average output current and peak inductor current. It is recommended to have a 20% current margin. Additionally, the Schottky diode reverse breakdown voltage should be higher than the open LED protection voltage threshold to avoid damage. It is recommended to use NXP PMEG4010EH for the SGM3810.

### Thermal Shutdown

The SGM3810 includes an OTP feature to prevent excessive power dissipation from overheating these devices. When the junction temperature of the IC exceeds the typical value of +150℃, the internal thermal shutdown is triggered and the device enters the shutdown state and latches. When the junction temperature decreases by 20℃, the device can be restarted by toggling HWEN and rewriting the ENABLE bit.

### Device Reset

In order to reset the whole device, VIN has to decrease below UVLO falling threshold.

- All voltage settings can only be reset by input power restart or toggling HWEN to Low.
- The flag registers can only be reset by read or input power restart.

# DETAILED DESCRIPTION (continued)

## I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM3810 parameters and get status reports. I²C is well-known 2 wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master and generates the SCL clock as long as it is master. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM3810 operates as a slave device with address 0x36 (36H). It has six 8-bit registers.

### Physical Layer

Bus lines are pulled high by pull-up resistors and in logic high state with no clocking when the bus is free. The pull-up resistors that are tied to SDA and SCL lines should meet I²C specification. The SGM3810 does not support the general call. The SDA pin is open-drain.

## I²C Data Communication

### START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 3. All transactions are started by the master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.

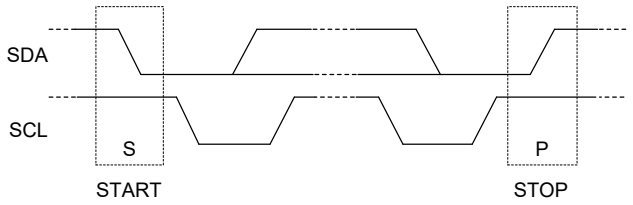



**Figure 3. I²C Bus in START and STOP Conditions**

### Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the high period of the clock. The state of the SDA can only change when the clock (SCL) is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 4.

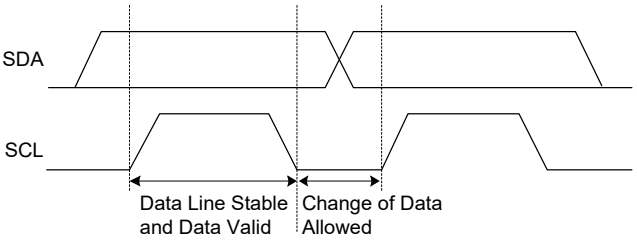



**Figure 4. I²C Bus Bit Transfer**

### Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 5 shows the byte transfer process with I²C interface.

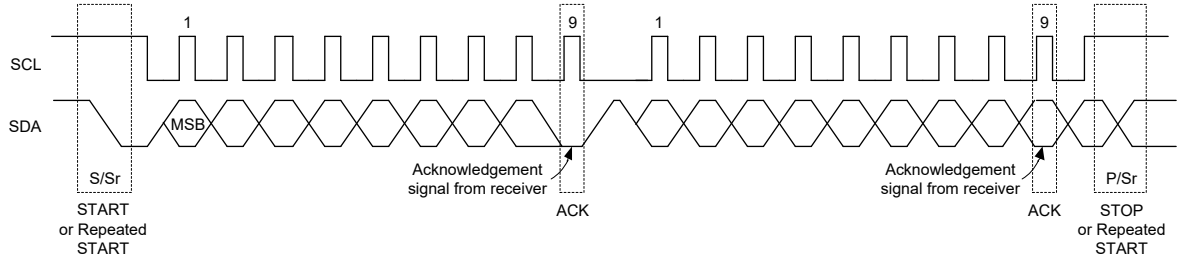



**Figure 5. Byte Transfer Process**

## DETAILED DESCRIPTION (continued)

### Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

### Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 6.

**WRITE:** If the master wants to write in the register, the third byte can be written directly as shown in Figure 7 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

**READ:** If the master wants to read a single register (Figure 8), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

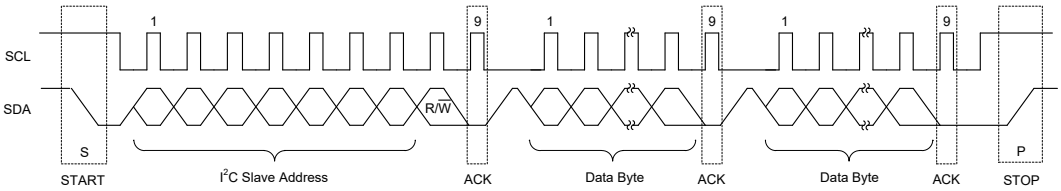



**Figure 6. Data Transfer Transaction**

## DETAILED DESCRIPTION (continued)

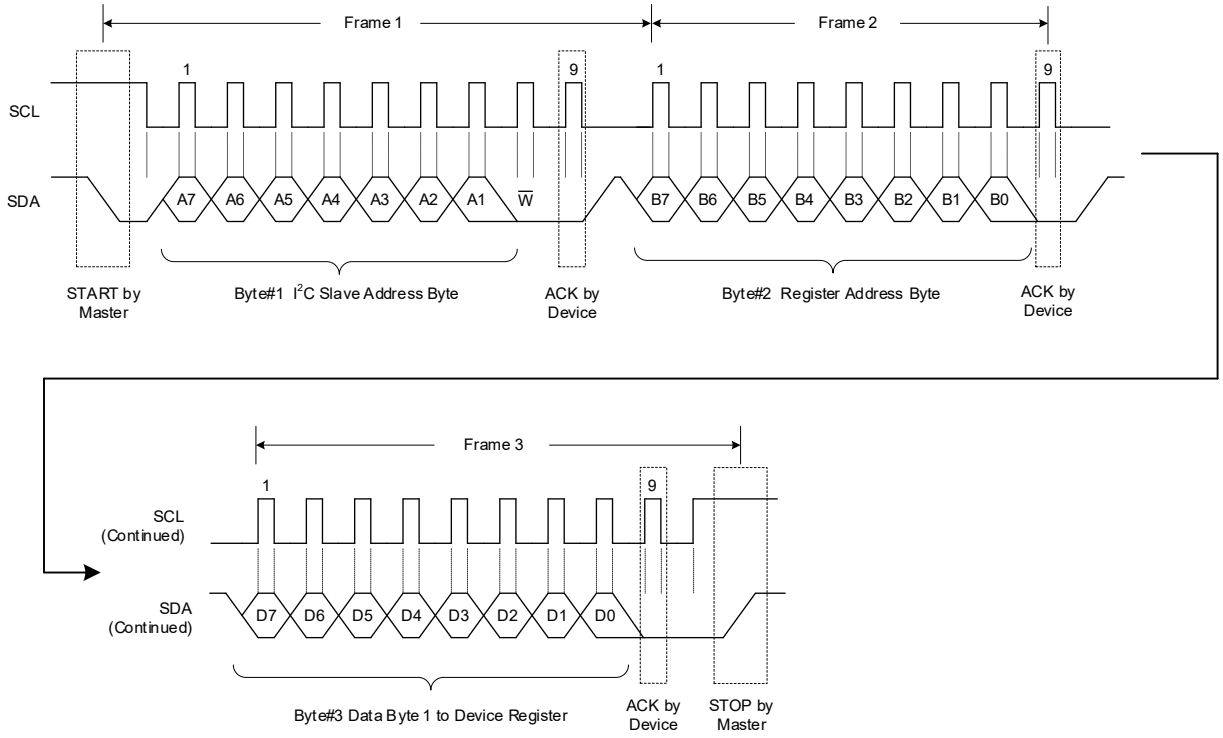



**Figure 7. A Single Write Transaction**

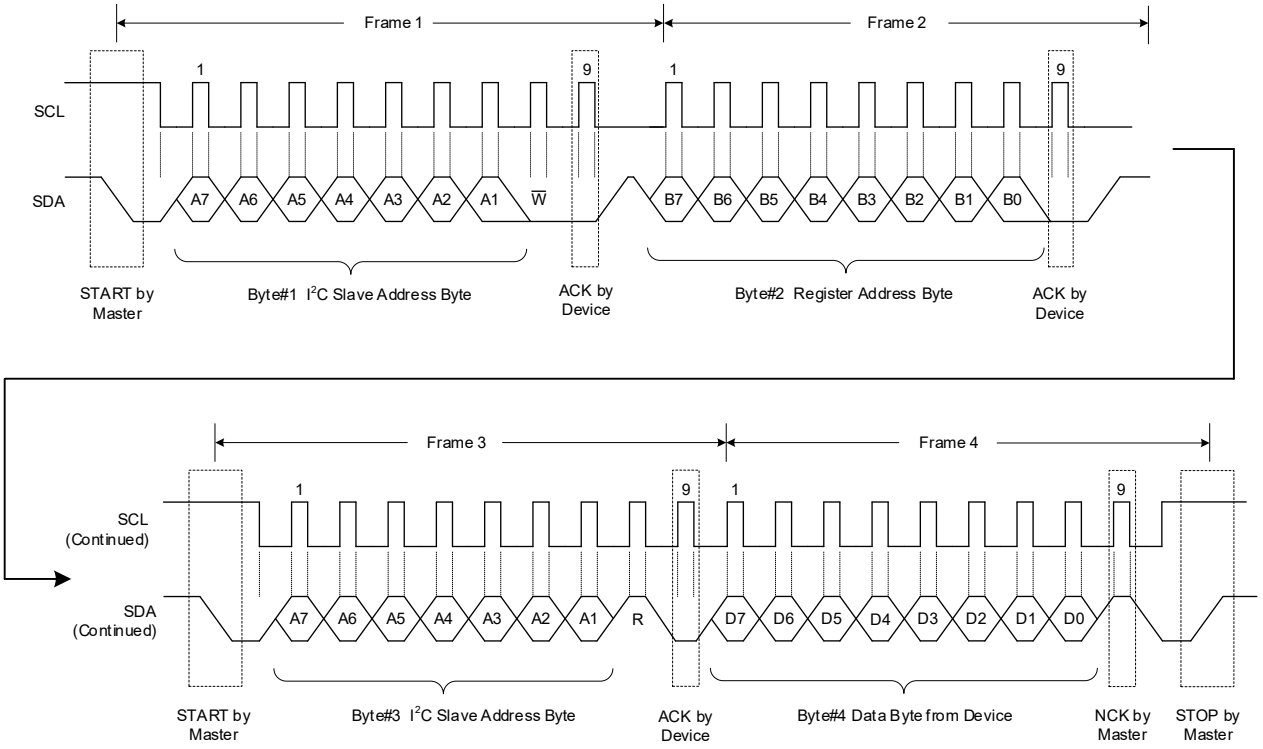



**Figure 8. A Single Read Transaction**

## DETAILED DESCRIPTION (continued)

### Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM3810 as explained in Figure 9 and Figure 10. In a multi-write transaction, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (whose address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

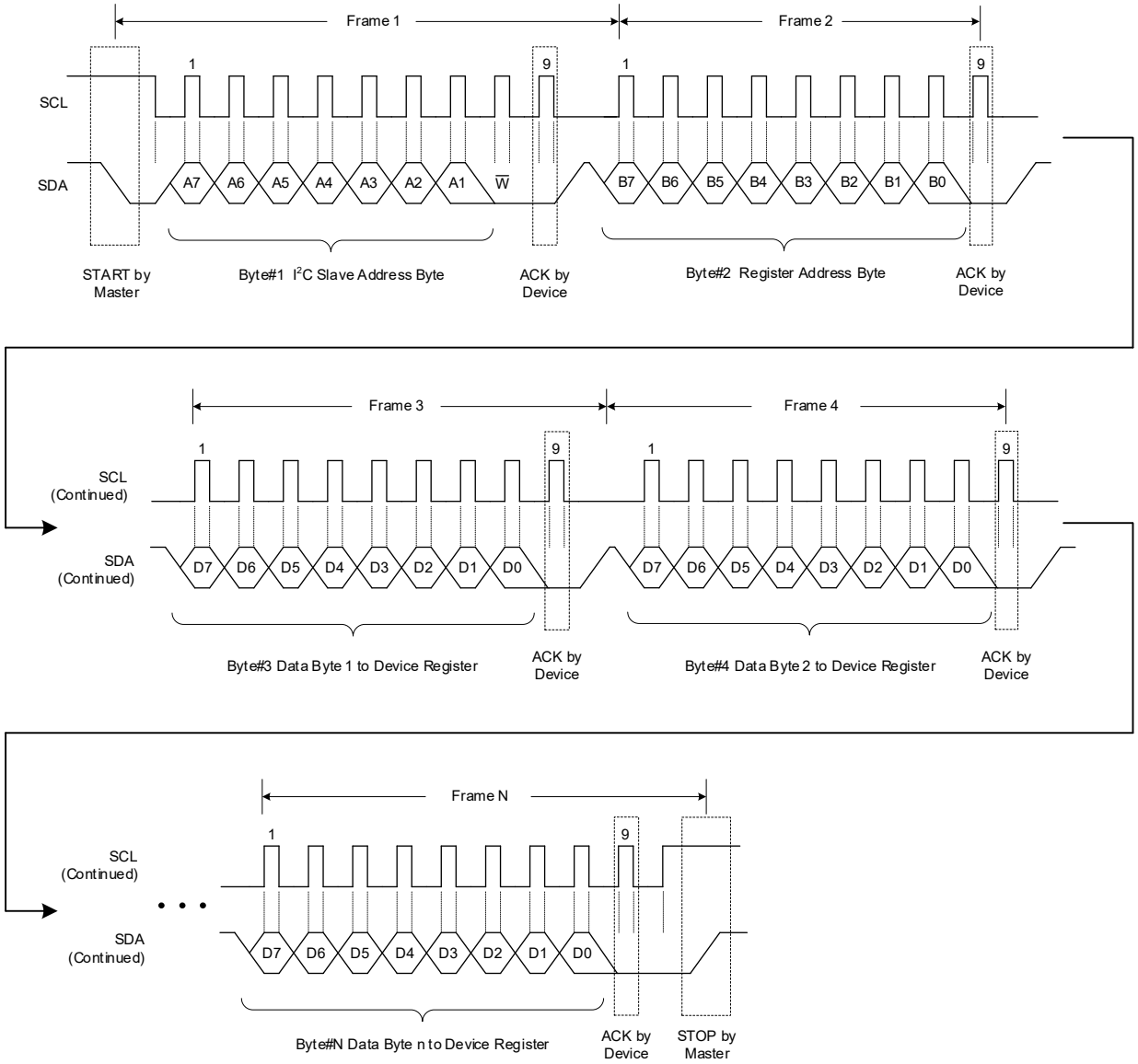



**Figure 9. A Multi-Write Transaction**

## DETAILED DESCRIPTION (continued)

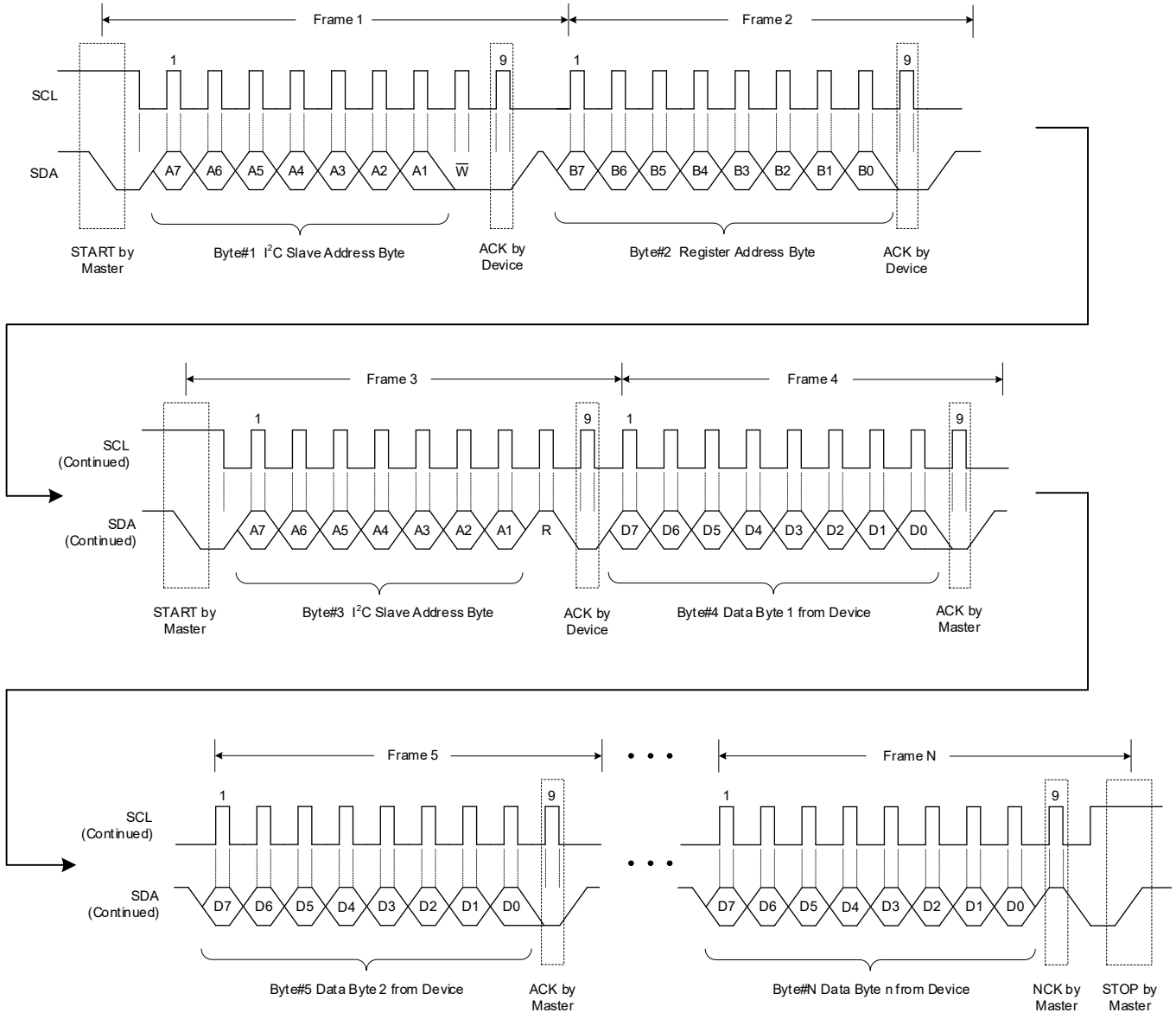



**Figure 10. A Multi-Read Transaction**

# REGISTER MAP

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

## $I^2C$ Slave Address of SGM3810 is: 0x36 (0b0110110 + R/W)

Bit Types:
R: Read only
R/W: Read/Write

**Table 2. Register Map**

| ADDRESS | REGISTER NAME | DEFAULT VALUE (Hex) | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | VPO_SET | 0x0A | Reserved | | | VPO_SET[4:0] | | | | |
| 0x01 | VNO_SET | 0x2A | Reserved | | | VNO_SET[4:0] | | | | |
| 0x02 | VREF_LB | 0xFF | VREF[7:0] | | | | | | | |
| 0x03 | VREF_HB | 0x07 | Reserved | | | | VREF[11:8] | | | |
| 0x04 | ENABLE | 0x0C | P2N_SEQ | TDELAY[1:0] | | WLED_EN | DISN | DISP | VPO_VNO_EN[1:0] | |
| 0x05 | FLAG | 0x00 | Reserved | | VNO_OVP | VPO_OVP | TSD_FLAG | LED_OVP | VNO_SC | VPO_SC |

## REG0x00: VPO_SET Register [reset = 0x0A]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:5] | Reserved | 000 | R/W | Reserved |
| D[4:0] | VPO_SET[4:0] | 01010 | R/W | VPO Output Voltage Setting<br>$V_{VPO}$ = VPO_SET[4:0] × 100mV + 4.0V<br>Offset: 4.0V<br>Range: 4.0V (00000) ~ 6.4V (11000)<br>Default: 5.0V (01010) |

**Table 3. VPO_SET[4:0] Description, VPO Output Voltage Setting**

| Data (Hex) | VPO (V) | Data (Hex) | VPO (V) |
|---|---|---|---|
| 0x00 | 4.0 | 0x0D | 5.3 |
| 0x01 | 4.1 | 0x0E | 5.4 |
| 0x02 | 4.2 | 0x0F | 5.5 |
| 0x03 | 4.3 | 0x10 | 5.6 |
| 0x04 | 4.4 | 0x11 | 5.7 |
| 0x05 | 4.5 | 0x12 | 5.8 |
| 0x06 | 4.6 | 0x13 | 5.9 |
| 0x07 | 4.7 | 0x14 | 6.0 |
| 0x08 | 4.8 | 0x15 | 6.1 |
| 0x09 | 4.9 | 0x16 | 6.2 |
| 0x0A | 5.0 | 0x17 | 6.3 |
| 0x0B | 5.1 | 0x18 | 6.4 |
| 0x0C | 5.2 | 0x19 ~ 0xFF | Null |

# REGISTER MAPS (continued)

## REG0x01: VNO_SET Register [reset = 0x2A]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:5] | Reserved | 001 | R/W | Reserved |
| D[4:0] | VNO_SET[4:0] | 01010 | R/W | VNO Output Voltage Setting<br>$V_{VNO}$ = VNO_SET[4:0] × (-100mV) - 4.0V<br>Offset: -4.0V<br>Range: -4.0V (00000) ~ -6.4V (11000)<br>Default: -5.0V (01010) |

**Table 4. VNO_SET[4:0] Description, VNO Output Voltage Setting**

| Data (Hex) | VNO (V) | Data (Hex) | VNO (V) |
|---|---|---|---|
| 0x00 | -4.0 | 0x0D | -5.3 |
| 0x01 | -4.1 | 0x0E | -5.4 |
| 0x02 | -4.2 | 0x0F | -5.5 |
| 0x03 | -4.3 | 0x10 | -5.6 |
| 0x04 | -4.4 | 0x11 | -5.7 |
| 0x05 | -4.5 | 0x12 | -5.8 |
| 0x06 | -4.6 | 0x13 | -5.9 |
| 0x07 | -4.7 | 0x14 | -6.0 |
| 0x08 | -4.8 | 0x15 | -6.1 |
| 0x09 | -4.9 | 0x16 | -6.2 |
| 0x0A | -5.0 | 0x17 | -6.3 |
| 0x0B | -5.1 | 0x18 | -6.4 |
| 0x0C | -5.2 | 0x19 ~ 0xFF | Null |

## REG0x02: VREF_LB Register [reset = 0xFF]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | VREF[7:0] | 11111111 | R/W | Low Byte of the 12-Bit Brightness Dimming Factor<br>LSB<7:0>: 128, 64, 32, 16, 8, 4, 2, 1<br><br>WLED Feedback Voltage Setting:<br>$V_{REF}$ = 200mV × VREF[11:0]/4095 (VREF[11:0] ≥ 4) |

## REG0x03: VREF_HB Register [reset = 0x07]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:4] | Reserved | 0000 | R/W | Reserved |
| D[3:0] | VREF[11:8] | 0111 | R/W | Higher Bits of the 12-Bit Brightness Dimming Factor<br>MSB<3:0>: 2048, 1024, 512, 256 |

# REGISTER MAPS (continued)

## REG0x04: ENABLE Register [reset = 0x0C]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7] | P2N_SEQ | 0 | R/W | VPO and VNO Output Sequence<br>0 = VNO starts $t_{DELAY}$ after VPO and shuts down $t_{DELAY}$ before VPO (default)<br>1 = VPO starts $t_{DELAY}$ after VNO and shuts down $t_{DELAY}$ before VNO<br>Note: This bit only actives when VPO_VNO_EN[1:0] = 11. |
| D[6:5] | TDELAY[1:0] | 00 | R/W | VPO and VNO Delay Timer $t_{DELAY}$<br>00 = 1.5ms (default)<br>01 = 3ms<br>10 = 6ms<br>11 = 12ms<br>Note: These bits only active when VPO_VNO_EN[1:0] = 11. |
| D[4] | WLED_EN | 0 | R/W | WLED Driver Boost Enable Control<br>0 = Shutdown (default)<br>1 = Enable |
| D[3] | DISN | 1 | R/W | VNO Active Discharge Control when Shutdown<br>0 = No Discharge<br>1 = Discharge (default) |
| D[2] | DISP | 1 | R/W | VPO Active Discharge Control when Shutdown<br>0 = No Discharge<br>1 = Discharge (default) |
| D[1:0] | VPO_VNO_EN[1:0] | 00 | R/W | VPO & VNO Enable Control<br>00 = Disable Both VPO and VNO (default)<br>01 = Enable VPO and Disable VNO<br>10 = Enable VNO and Disable VPO<br>11 = Enable Both VPO and VNO with $t_{DELAY}$ |

## REG0x05: FLAG Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:6] | Reserved | 00 | R | Reserved |
| D[5] | VNO_OVP | 0 | R | VNO Output Over-Voltage Fault Flag<br>0 = No over-voltage fault (default)<br>1 = Over-voltage fault |
| D[4] | VPO_OVP | 0 | R | VPO Output Over-Voltage Fault Flag<br>0 = No over-voltage fault (default)<br>1 = Over-voltage fault |
| D[3] | TSD_FLAG | 0 | R | Thermal Shutdown Fault Flag<br>0 = No thermal shutdown fault (default)<br>1 = Thermal shutdown fault |
| D[2] | LED_OVP | 0 | R | WLED Output Over-Voltage Fault Flag<br>0 = No over-voltage fault (default)<br>1 = Over-voltage fault |
| D[1] | VNO_SC | 0 | R | VNO Short-Circuit Fault Flag<br>0 = No VNO short fault (default)<br>1 = VNO short fault |
| D[0] | VPO_SC | 0 | R | VPO Short-Circuit Fault Flag<br>0 = No VPO short fault (default)<br>1 = VPO short fault |

NOTE: The FLAG Register can only be reset by READ or POR.

# APPLICATION INFORMATION

## Layout Considerations

Layout design is an important step in all switching power supplies design, especially in switching power supplies with high frequency and high current. Good layout plays a positive role in loop stability, signal integrity and low EMI. Since the switch FETs of SGM3810 works at a typical switching frequency of 1.25MHz, its power circuit layout needs to be designed more carefully. The switching pins (LED_SW, SWP and SWN) carry high current with fast rising and falling edge, so the EMI problem of the switching nodes should be avoided as far as possible. The area of switching nodes should be as small as possible, and the input loop and output loop need to maintain the minimum loop path, which can effectively suppress the generation of ringing. For the high current path, it should be as wide and short as possible, which is conducive to reducing the voltage drop and heat loss on the line. The input capacitance $C_{IN1}$ and $C_{IN2}$ should be close to VIN pin and PGND pin to reduce the influence of parasitic parameters on the line, which is conducive to ensuring the relative stability of the input voltage. The inductor and the Schottky diode D1 should close to the LED_SW pin as possible to reduce the area of the switching node, so it can reduce EMI. The output capacitance $C_{VPO}$ and $C_{VNO}$ should be as close to VPO and VNO as possible, and the grounding should be close to PGND pin to reduce grounding return. FB resistor $R_{SET}$ should be close to LED_FB pin, and Kelvin connection can be used if necessary. When arranging signal grounding, it is recommended to use short traces separated from the power grounding trace and connect them together at a single point close to the PGND pins.

## Layout Example

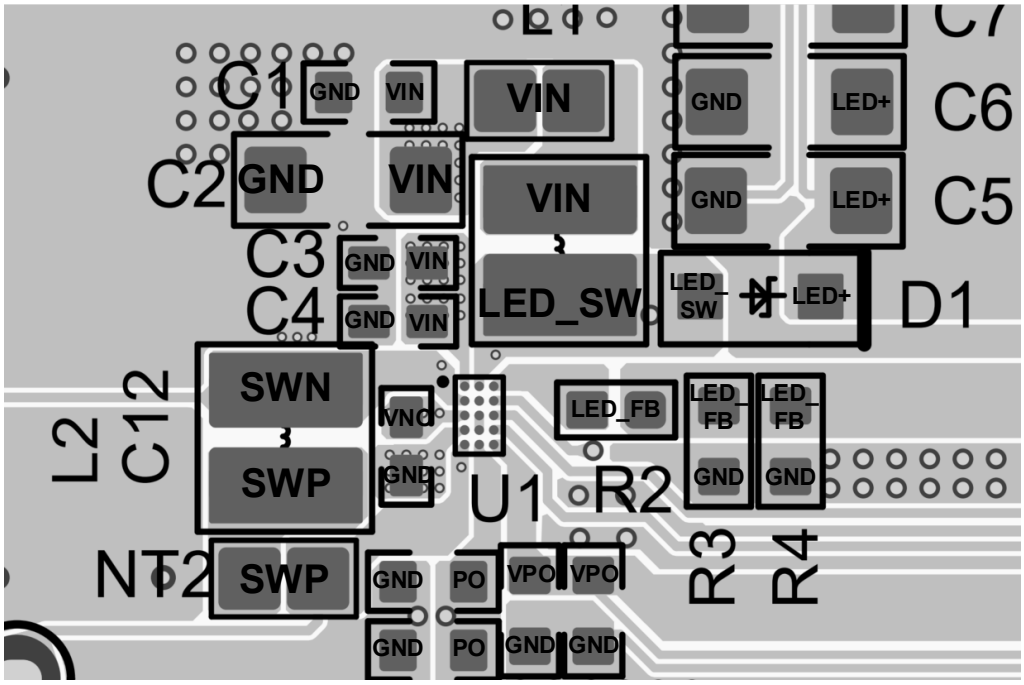



**Figure 11. SGM3810 PCB Layout (Top Layer)**

## APPLICATION INFORMATION (continued)

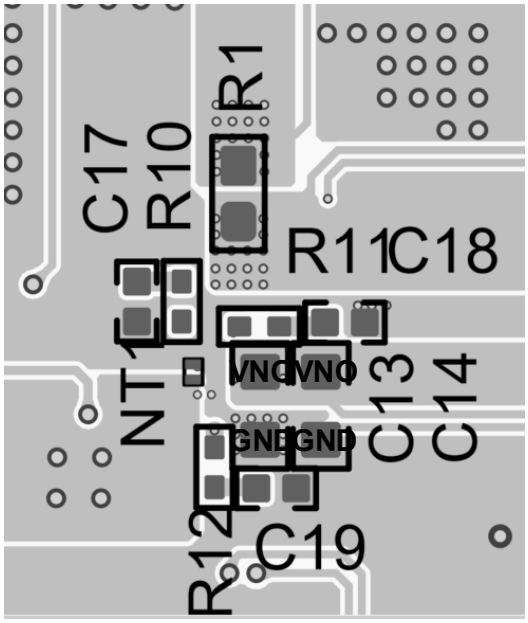



**Figure 12. SGM3810 PCB Layout (Bottom Layer)**

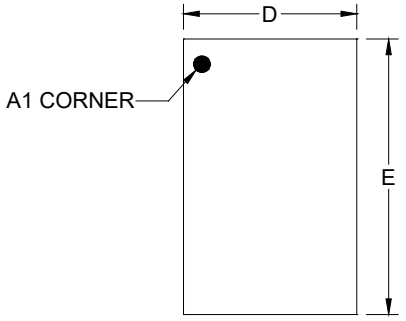
## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

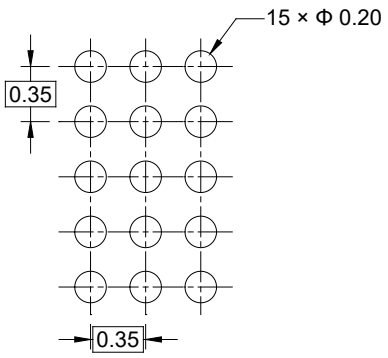
| Changes from Original to REV.A (DECEMBER 2025) | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

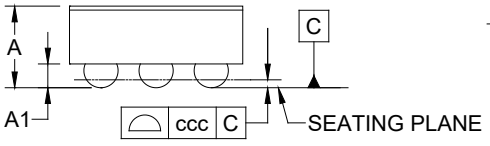
## WLCSP-1.1×1.75-15B



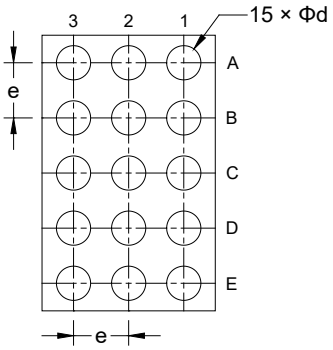

TOP VIEW




**RECOMMENDED LAND PATTERN** (Unit: mm)




SIDE VIEW



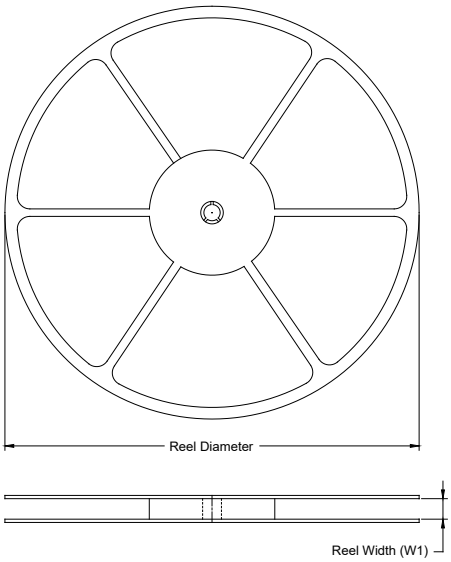

BOTTOM VIEW

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 0.548 |
| A1 | 0.131 | - | 0.171 |
| D | 1.070 | - | 1.130 |
| E | 1.720 | - | 1.780 |
| d | 0.187 | - | 0.247 |
| e | 0.350 BSC | | |
| ccc | 0.050 | | |

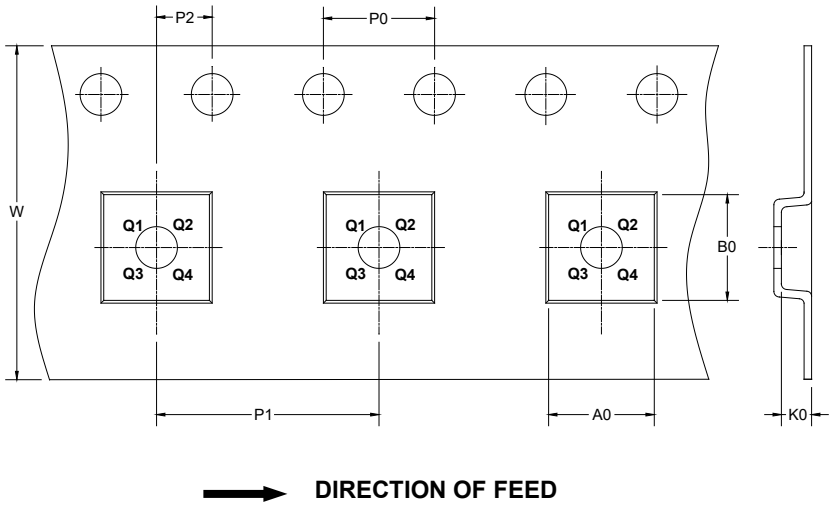
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

## REEL DIMENSIONS




## TAPE DIMENSIONS



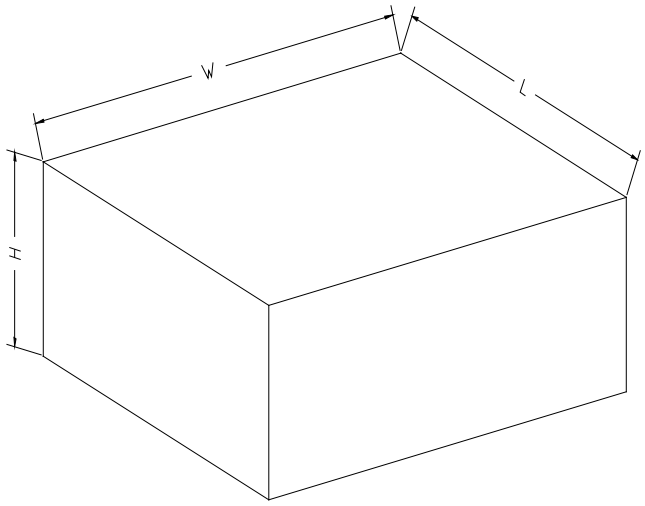

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP-1.1×1.75-15B | 7" | 9.5 | 1.25 | 1.95 | 0.75 | 4.0 | 4.0 | 2.0 | 8.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 7″ (Option) | 368 | 227 | 224 | 8 |
| 7″ | 442 | 410 | 224 | 18 |

DD0002