SGM42636
45V, 1.5A Stepper Driver with Integrated Current Sense, 1/256 Microstepping and Advance Decay Mode

GENERAL DESCRIPTION

The SGM42636 is a highly integrated bipolar stepper motor driver with 7V to 45V voltage range and full-scale current of 1.5A per winding respectively. It can be used in a verity of applications including consumer, industrial, and medical equipment. The integration of power MOSFETs, current sensing, microstepping indexer, and current regulators in these devices, allows compact system design with minimal number of peripheral components.

The integrated current sensing architecture ensures high current accuracy with no need for external lossy current sense resistors.

The popular STEP/DIR/ENABLE interface is used with an indexer that is capable of up to 256 micro-steps allowing smooth and low stepping noise operation.

The current regulators can be configured in several decay modes including the conventional slow and mixed decay, and the advanced dynamic decay and ripple control modes to minimize current ripple.

Sleep mode can be used to reduce the device current to the 1μA level by pulling the nSLEEP pin to the low state.

A comprehensive set of protection features including under-voltage, short-circuit, over-current and over-temperature is supported. The nFAULT indicator output reports occurrences of the faults.

The SGM42636 is available in Green TQFN-4×4-24L, TSSOP-24 (Exposed Pad) and TSSOP-28 (Exposed Pad) packages.

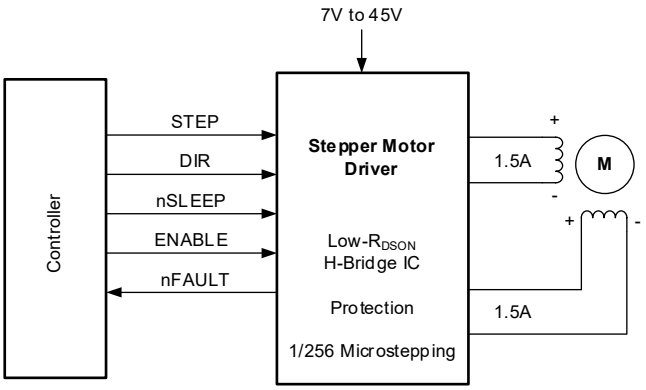
APPLICATIONS

ATMs
3D/Laser Beam Printers
Stage Lighting Equipment
Multi-Function Printers/Scanners
Textile and Sewing Machines

FEATURES

- **Fully Integrated Stepper Motor Driver**
  - **Two H-Bridge Drivers with Power MOSFETs**
  - **Internal Current Sensing and Regulation**
- **Operating Supply Voltage Range: 7V to 45V**
- **Low On-Resistance: 900mΩ HS + LS at 24V, +25℃**
- **High Current Capacity for each Winding**
  - **1.5A Full-Scale, 1.1A RMS Output**
- **Up to 1/256 Microstepping Indexer**
- **Conventional Slow, Mixed, and Fast Decay Modes**
- **Smart Tune Dynamic Decay Mode**
- **Smart Tune Ripple Control Mode**
- **PWM Chopping with Configurable Off-Time**
  - **7μs, 16μs, 24μs, or 32μs**
- **Supports 1.8V, 3.3V, 5.0V Logic Input**
- **Low Current Sleep Mode: 1μA (TYP)**
- **Protection Features**
  - **VM Under-Voltage Lockout (UVLO)**
  - **Charge Pump Under-Voltage (CPUV)**
  - **Over-Current Protection (OCP)**
  - **Thermal Shutdown (TSD)**
  - **Fault Condition Output (nFAULT)**
- **Latching/Auto-Retry Options for OCP**

SIMPLIFIED SCHEMATIC

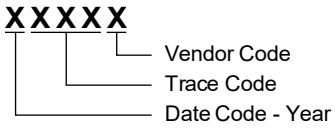


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42636	TSSOP-24 (Exposed Pad)	-40℃ to +125℃	SGM42636XPTS24G/TR	SGM42636 XPTS24 XXXXX	Tape and Reel, 4000
	TSSOP-28 (Exposed Pad)	-40℃ to +125℃	SGM42636XPTS28G/TR	SGM42636 XPTS28 XXXXX	Tape and Reel, 4000
	TQFN-4×4-24L	-40℃ to +125℃	SGM42636XTQF24G/TR	SGM42636 XTQF24 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, V_M ..... -0.3V to 50V
Charge Pump Voltage, VCP, CPH..... -0.3V to V_M + 5.5V
Charge Pump Negative Switching Pin, CPL ..... -0.3V to 5.5V
Internal Regulator Voltage, DVDD ..... -0.3V to 5.5V
Control Pin Voltage, ENABLE, STEP, DIR, nFAULT, DECAY0, DECAY1, TOFF, M0, M1, nSLEEP .. -0.3V to 5.5V
nFAULT Open-Drain Output Sink Current .....0mA to 10mA
Reference Input Pin Voltage, VREF ..... -0.3V to 5.5V
Phase Nodes Voltage (Continuous), AOUT1, AOUT2, BOUT1, BOUT2.....-0.7V to V_M + 0.7V
Package Thermal Resistance
TSSOP-24 (Exposed Pad), θ_{JA} ..... 28.4℃/W
TSSOP-24 (Exposed Pad), θ_{JB} ..... 9.1℃/W
TSSOP-24 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 22℃/W
TSSOP-24 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 1.8℃/W
TSSOP-28 (Exposed Pad), θ_{JA} ..... 31.5℃/W
TSSOP-28 (Exposed Pad), θ_{JB} .....11.9℃/W
TSSOP-28 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 19.8℃/W
TSSOP-28 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 1.8℃/W
TQFN-4×4-24L, θ_{JA} ..... 28.5℃/W
TQFN-4×4-24L, θ_{JB} ..... 7.9℃/W
TQFN-4×4-24L, $\theta_{JC\ (TOP)}$ ..... 25.3℃/W
TQFN-4×4-24L, $\theta_{JC\ (BOT)}$ ..... 1.6℃/W
Junction Temperature .....+150℃
Storage Temperature Range.....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility (1) (2)
HBM.....±2000V
CDM .....±2000V

NOTES:
1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage for Normal (DC) Operation, V_M ..... 7V to 45V
Logic-Level Input Voltage, V_I ..... 0V to 5.3V
VREF Voltage V_{REF} ..... 0.05V to 3.3V
Applied STEP Signal (STEP), f_{PWM}.....0kHz to 400kHz
Motor Full-Scale Current, I_{MAX} ..... 0A to 1.5A
Motor RMS Current, I_{RMS} ..... 0A to 1.1A
Operating Ambient Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

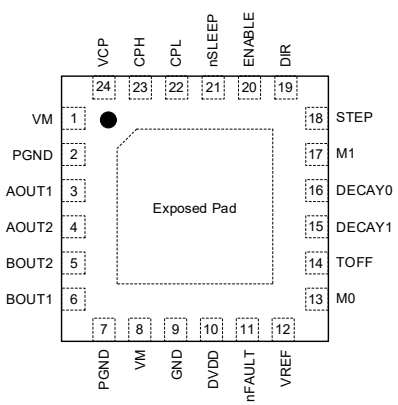
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

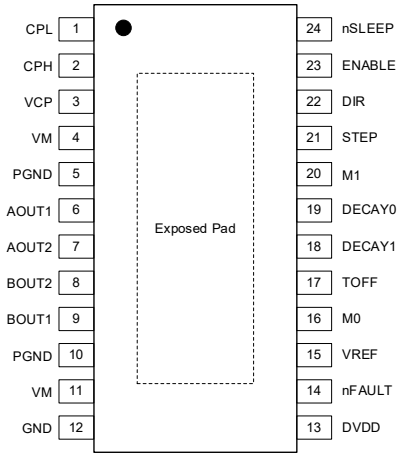
PIN CONFIGURATIONS

(TOP VIEW)



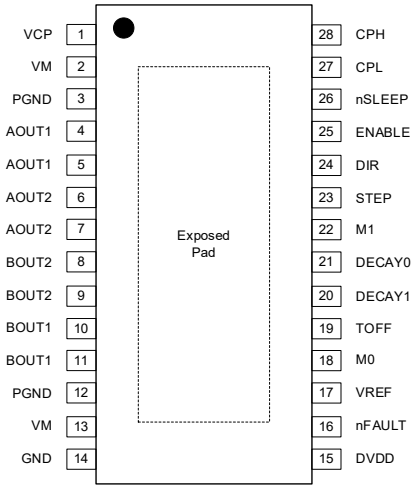
TQFN-4×4-24L

(TOP VIEW)



TSSOP-24 (Exposed Pad)

(TOP VIEW)



TSSOP-28 (Exposed Pad)

PIN DESCRIPTION

NAME	FUNCTION
AOUT1	Bridge A Output 1.
AOUT2	Bridge A Output 2.
PGND	Power Ground Return.
BOUT2	Bridge B Output 2.
BOUT1	Bridge B Output 1.
CPH	Charge Pump Pins for the External Flying Capacitor. Place a 0.022μF, X7R, ceramic capacitor with sufficient voltage rating between these two pins.
CPL	
DIR	Direction Logic Input Pin. Control the direction of stepping (rotation). DIR is weakly pulled down internally.
ENABLE	Active-High Logic Enable Input Pin. ENABLE is a tri-level digital input and is internally pulled up to DVDD. It should be pulled low to disable the device. It also determines the OCP response type. If it is left open (Hi-Z), latching mode is selected. To choose the auto-retry option for OCP, tie this pin to a logic-high voltage like DVDD.
DVDD	Internal 5V Regulator and Reference Output. Decouple this pin with a 0.47μF ~ 1μF, X7R, 6.3V (or 10V) ceramic capacitor to GND. The maximum load current is 2mA. It can be used for digital logic or setting the voltages of configuration inputs.
GND	Ground Reference (Logic/Signal).
VREF	Input Voltage for Current Reference. The full-scale output current is proportional to this voltage (within the device range): I_{FS} (A) = V_{REF} (V)/K_V. It should be set below 3.3V. DVDD and a resistor divider can be used to set VREF to a fix voltage.
M0	Micro-Step Mode Selection Inputs. These multi-level logic inputs set the motor stepping size with each STEP pulse. Stepping can be set to full step with 71% current, full step with 100% current, 1/2, 1/2 non-circular, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128 and 1/256. M0 is a tri-level and M1 is a quad-level input.
M1	
DECAY0	Decay Mode Selection Input Pins.
DECAY1	
STEP	Step Logic Input. A rising clock edge increments the microstepping indexer for one step. It is weakly pulled down internally.
VCP	Charge Pump Gate Driving Voltage Output for the High-side MOSFETs. Decouple it with a 0.22μF ceramic capacitor to VM pin.
VM	Power Supply Pin. Connect to the stepper motor power source (7V to 45V). Decouple them to their adjacent PGND pins with high frequency 0.01μF ceramic capacitors. Use a decoupling bulk capacitor (e.g. 100μF) to PGND near the device.
TOFF	PWM Off-Time Setting Pin. TOFF is a quad-level input to select one of the four t_{OFF} times options (7μs, 16μs, 24μs, 32μs). TOFF level can be dynamically changed on the fly, while the motor is running.
nFAULT	Open-Darin Fault Indicator Output. If a fault occurs, this output will be pulled down. The pull-up voltage should be 5V or less.
nSLEEP	Active-Low Sleep Mode and Fault Reset Input. This logic input is weakly pulled down internally. When nSLEEP is logic low, the chip will enter low-power sleep mode whatever the input of EN is high, Hi-Z or low. A negative pulse (10μs to 20μs width) resets latched shutdown.
Exposed Pad	Thermal Pad. Connect this pad to the system ground. A large copper area improves cooling of the device.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, V_M = 24V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supplies (VM, DVDD)						
VM Power Supply Voltage	V_M	Normal (DC) operation	7		45	V
VM Operating Supply Current	I_{VM}	ENABLE = high, nSLEEP = high, no motor load		6.5	10	mA
VM Sleep Mode Supply Current	I_{VMQ}	nSLEEP = low		1	10	μA
Time to Enter Sleep Mode	t_{SLEEP}	nSLEEP = low to sleep mode	130			μs
nSLEEP Reset Pulse	t_{RESET}	nSLEEP = low to clear fault	10		20	μs
Wake-Up Time	t_{WAKE}	nSLEEP = high to output transition		1	1.3	ms
Turn-On Time	t_{ON}	V_M > V_{UVLO} to output transition		1	1.3	ms
Internal Regulator Voltage	V_{DVDD}	No external load	4.7	5	5.2	V
Charge Pump (VCP, CPH, CPL)						
CP Operating Voltage	V_{CP}			V_M + 4.5		V
Charge Pump Switching Frequency	f_{CP}	V_M > V_{UVLO}, nSLEEP = high		155		kHz
Logic-Level Inputs (DIR, STEP, nSLEEP, DECAY0)						
Input Logic-Low Voltage	V_{IL}		0		0.4	V
Input Logic-High Voltage	V_{IH}		1.6		5.3	V
Input Hysteresis	V_{HYS}			150		mV
Input Logic-Low Current	I_{IL}	V_{IN} = 0V	-1		1	μA
Input Logic-High Current	I_{IH}	V_{IN} = 5V			100	μA
Tri-Level Inputs (M0, DECAY1, ENABLE)						
Input Logic-Low Voltage	V_{I1}		0		0.5	V
Input Hi-Z Voltage	V_{I2}	Hi-Z		1		V
Input Logic-High Voltage	V_{I3}		1.8		5.3	V
Output Pull-Up Current	I_O			10		μA
Quad-Level Inputs (M1, TOFF)						
Input Logic-Low Voltage	V_{I1}		0		0.5	V
	V_{I2}	330kΩ ± 5% to GND		1.1		V
Input Hi-Z Voltage	V_{I3}	Hi-Z		1.8		V
Input Logic-High Voltage	V_{I4}		2.9		5.3	V
Output Pull-Up Current	I_{IL}			10		μA
Control Outputs (nFAULT)						
Output Logic-Low Voltage	V_{OL}	I_O = 5mA			0.5	V
Output Logic-High Leakage	I_{OH}	V_{PULL_UP} = 5V	-1		1	μA
Motor Driver Outputs (xOUTx)						
High-side FET On-Resistance	R_{DSON_H}	V_M = 24V, I_O = 0.5A		450	800	mΩ
Low-side FET On-Resistance	R_{DSON_L}	V_M = 24V, I_O = 0.5A		450	800	mΩ
Output Slew Rate	t_{SR}	V_M = 24V, I_O = 0.5A, 10% to 90%		640		V/μs

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, V_M = 24V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM Current Control (VREF)						
Trans-Impedance Gain (V_{REF}/I_{FS})	K_V			2.2		V/A
PWM Off-Time	t_{OFF}	TOFF pin Grounded		7		μs
		TOFF pin connected with a 330kΩ to GND		16		
		TOFF pin left open (Hi-Z)		24		
		TOFF pin set to logic high		32		
Current Trip Level Accuracy	ΔI_{TRIP}	I_O = 1.5A, current setting: 10% to 63%	-12.5		12.5	%
		I_O = 1.5A, current setting: 71% to 100%	-7.5		7.5	
AOUT and BOUT Current Matching	$I_{O,CH}$	I_O = 1.5A, initial accuracy, T_J = +25℃	-2.5		2.5	%
Protection Circuits						
VM Supply Under-Voltage Lockout	V_{UVLO}	Falling	5.6	5.9	6.1	V
		Rising	6.2	6.5	6.7	
VM Under-Voltage Hysteresis	V_{UVLO_HYS}	Rising to falling hysteresis band		600		mV
Charge Pump Under-Voltage	V_{CPUV}	VCP falling, CPUV report		V_M + 2		V
Over-Current Protection	I_{OCP}	Current through any FET		2		A
Over-Current Deglitch Time	t_{OCP}			2		μs
Over-Current Retry Time	t_{RETRY}			4		ms
Thermal Shutdown Threshold	T_{SD}	Die temperature T_J		165		℃
Thermal Shutdown Hysteresis	T_{HYS}	Die temperature T_J		40		℃

INDEXER TIMING REQUIREMENTS

(T_J = +25℃, V_M = 24V, unless otherwise noted.)

SYMBOL	FUNCTION	MIN	MAX	UNITS
f_{STEP}	Step frequency.		400	kHz
t_{WH_STEP}	Pulse duration, STEP high.	1.25		μs
t_{WL_STEP}	Pulse duration, STEP low.	1.25		μs
$t_{SU\_DIR, Mx}$	Set-up time (DIR or M0 or M1 level change until STEP rising).	250		ns
$t_{H\_DIR, Mx}$	Hold time (DIR or M0 or M1 must remain stable after STEP rising).	250		ns

NOTE: STEP clocking can be as high as 400kHz, but the system bandwidth is effectively limited by the motor and its load.

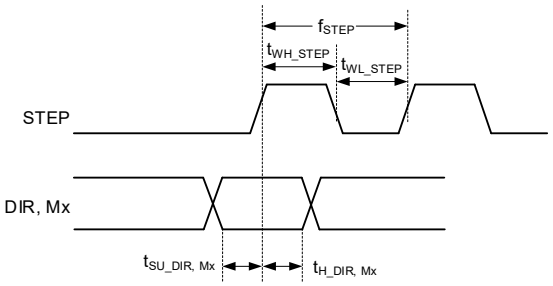
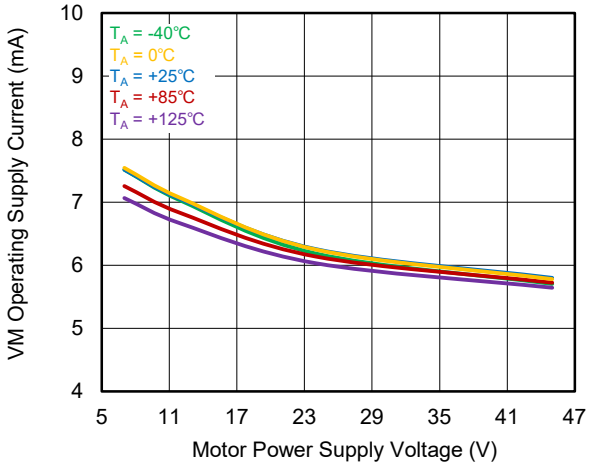


Figure 1. Indexer Timing Diagram

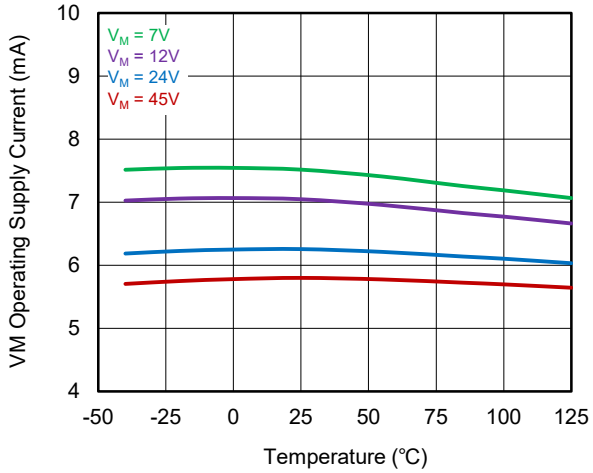
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, unless otherwise noted.

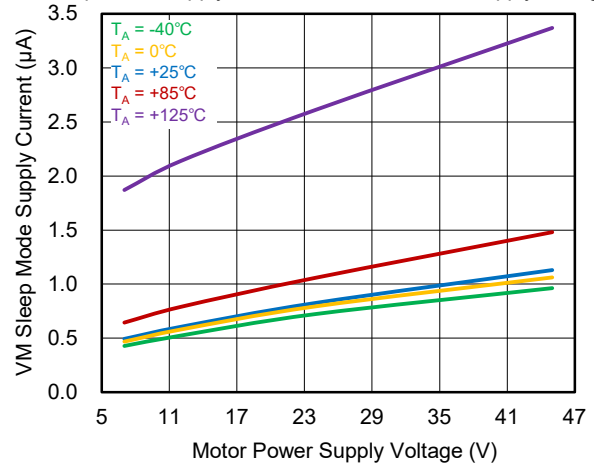
VM Operating Supply Current vs. Motor Power Supply Voltage



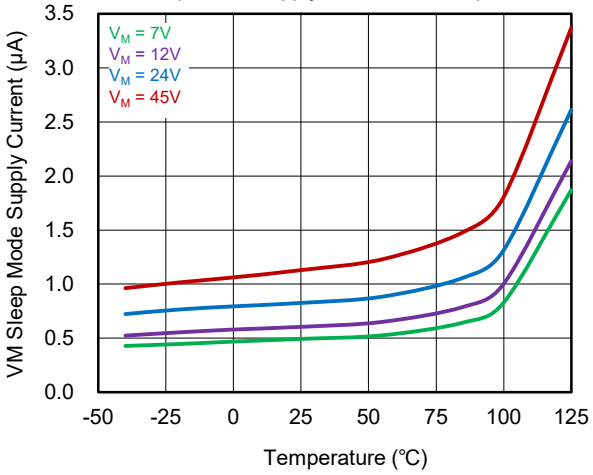
VM Operating Supply Current vs. Temperature



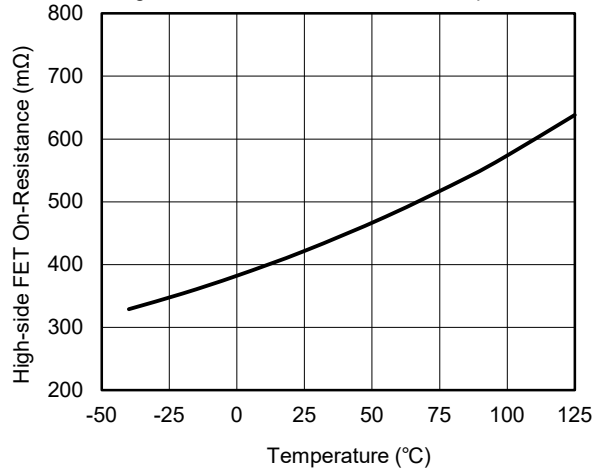
VM Sleep Mode Supply Current vs. Motor Power Supply Voltage



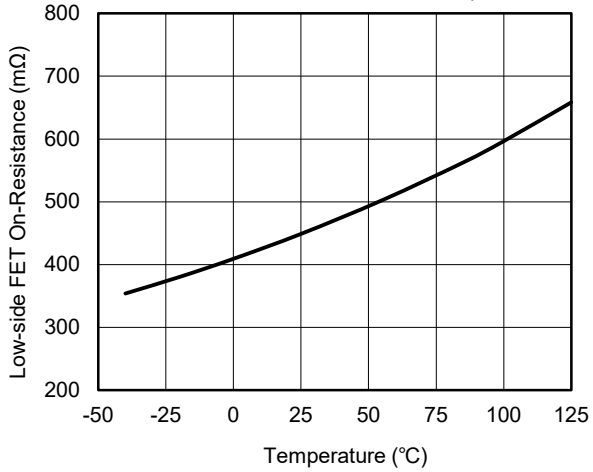
VM Sleep Mode Supply Current vs. Temperature



High-side FET On-Resistance vs. Temperature



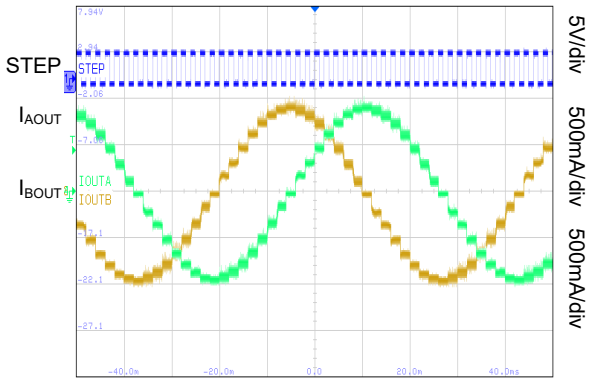
Low-side FET On-Resistance vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

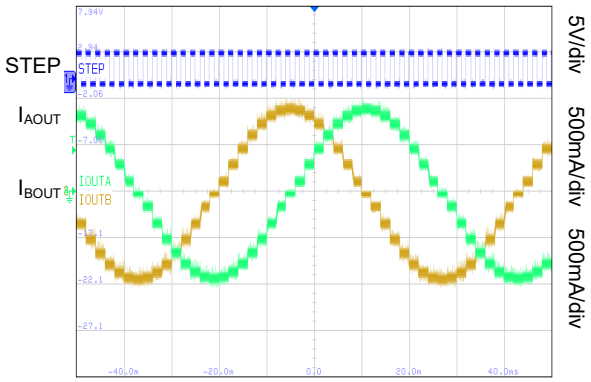
T_J = +25℃, unless otherwise noted.

1/8 Microstepping with Slow-Mixed Decay



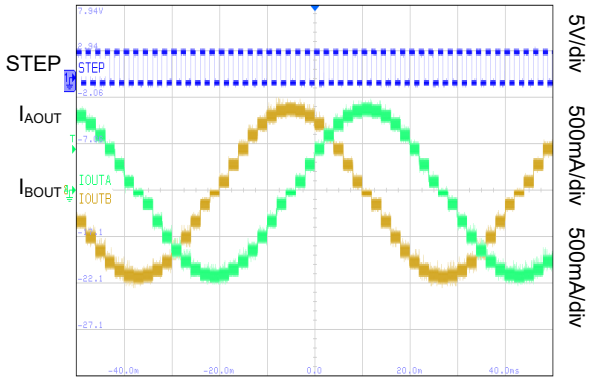
Time (10ms/div)

1/8 Microstepping with Mixed-Mixed Decay (30% Fast)



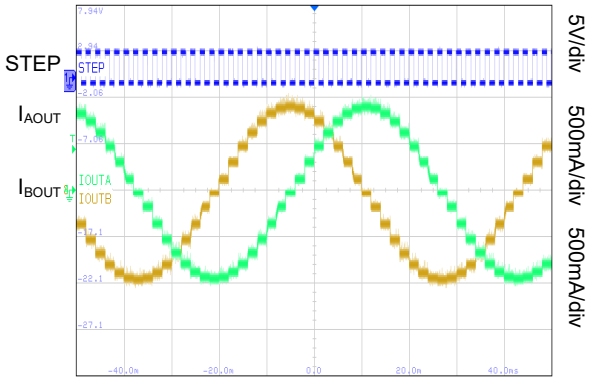
Time (10ms/div)

1/8 Microstepping with Mixed-Mixed Decay (60% Fast)



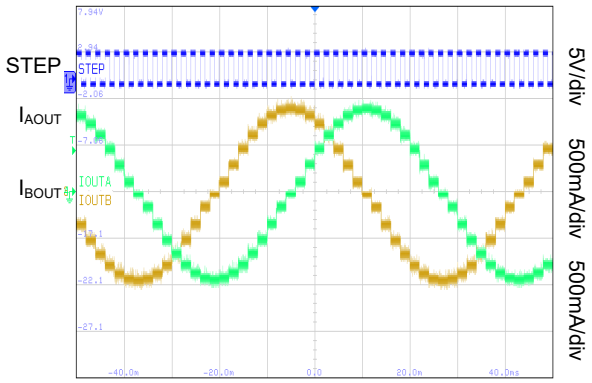
Time (10ms/div)

1/8 Microstepping with Auto Tune Ripple Control



Time (10ms/div)

1/8 Microstepping with Dynamic Decay



Time (10ms/div)

FUNCTIONAL BLOCK DIAGRAM

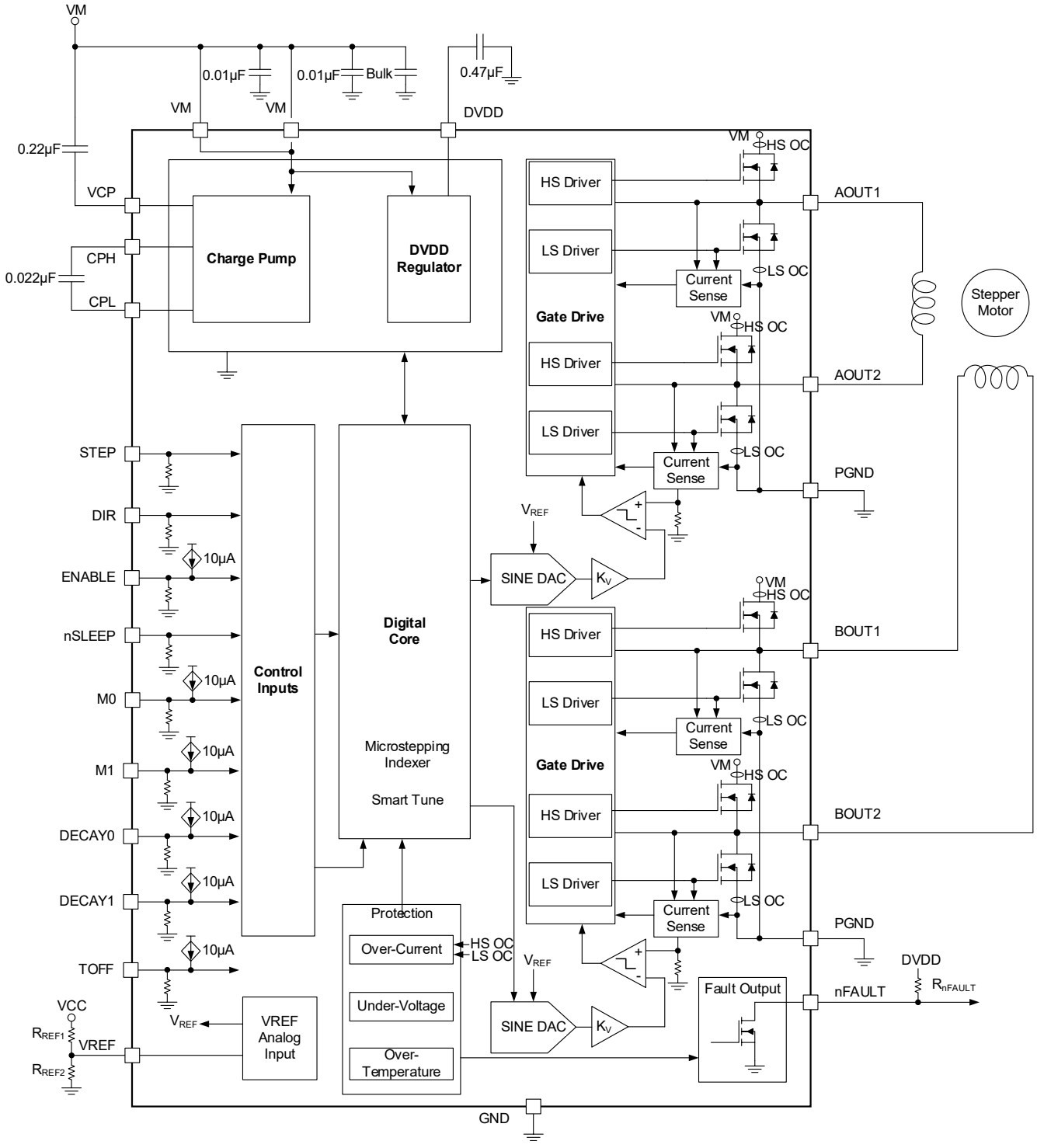


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Overview

The SGM42636 is a highly integrated bipolar stepper motor driver offering compact solution size with high efficiency and minimal number of external components. It includes two N-MOSFET H-bridges for driving the motor windings with current sense and current regulation circuitry and a microstepping indexer. It can be powered with a supply voltage in the 7V to 45V range. The SGM42636 can provide up to 1.5A continuous current (full-scale current) and 1.1A RMS current for each winding. The actual full-scale and safe RMS currents are de-rated based on the device temperature that is affected by the ambient temperature, device cooling, running frequency and supply voltage. The sleep mode (low-power) can be used to save power when the system does not actively drive the motor.

There is no need for external power sense resistors due to the integrated current sensing architecture used in the SGM42636. This feature eliminates the need for external resistors and removes their losses from the system. The set point for regulating the output current is controlled by the VREF input pin voltage.

The simple and conventional STEP/DIR interface is used for control of the motor direction and step rate. The integrated indexer can provide accurate microstepping with no need for external current controller. Full step, 1/2 step, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping are available. Moreover, in addition to the standard half stepping, a non-circular half stepping mode is included that can be used to boost the torque at higher RPM.

Several decay modes are available and can be chosen for current regulation by configuring the DECAY0 and DECAY1 pin voltages. During a slow decay, the winding current is circulated through the lower bridge MOSFETs to decay, while in fast decay, the bridge applies a reverse voltage to accelerate the current decay. Combinations of slow and fast decays are used to define several decay mode current regulation schemes, including slow-mixed, mixed-decay (30% or 60% fast), smart tune ripple control, and smart tune dynamic decay. The slow-mixed decay mode uses slow decay on increasing steps and mixed decay on decreasing steps. The smart tune decay modes automatically adjust the decay segments for optimal current regulation performance and compensate for motor parameter variations and aging effects. Smart tune ripple control uses a variable off-time ripple control scheme like hysteretic control to minimize winding current ripple at the cost of variable frequency operation. Smart tune dynamic decay uses a fixed off-time and dynamically adjusts decay percentages to minimize current ripple without changing frequency.

A list of recommended external components for use with the SGM42636 is provided in Table 1.

Table 1. SGM42636 Suggested External Component Values

Peripheral	PIN 1	PIN 2	Recommended Values
C_{VM1}	VM	GND	Two parallel X7R, 0.01μF ceramic capacitors rated for operating at VM voltage
C_{VM2}	VM	GND	A bulk capacitor rated for operating at VM voltage
C_{CP}	VCP	VM	X7R, 0.22μF, 16V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.022μF ceramic capacitor rated for operating at VM voltage
C_{DVDD}	DVDD	GND	X7R, 0.47μF to 1μF, 6.3V ceramic capacitor
R_{nFAULT}	VCC (1)	nFAULT	> 4.7kΩ resistor (10kΩ typical)
R_{REF1}	VREF	VCC	Resistors to set I_{TRIP} current. It is recommended to select resistors such that R_{REF1}||R_{REF2} ≤ 50kΩ.
R_{REF2} (Optional)	VREF	GND	

NOTE: 1. VCC is the pull-up voltage for nFAULT open-drain output. DVDD may be used as VCC.

DETAILED DESCRIPTION (continued)

Stepper Motor Driver Current Ratings

For a stepper motor driver, the output current peak, RMS and full-scale ratings are usually specified. For the SGM42636, these ratings are described as follows.

Peak Current Rating

The driver peak current is usually limited by the over-current protection trip threshold (I_{OCP}). Such peaks usually occur during current transients with very low duty cycle in a current pulse, for example, due to charging of a capacitance. The minimum I_{OCP} threshold usually specifies the rated peak current of the stepper motor driver.

RMS Current Rating

The RMS current is limited by the maximum operation temperature of the device junction. Thermal performance of the system may increase or decrease the effective maximum RMS current. The junction temperature depends on the MOSFETs R_{DSON}, rise and fall times of the output pulses, PWM frequency, device quiescent current, heat removal performance of the system and ambient temperature. The specified RMS values are given for a typical system operating at +25℃. The rated RMS current is 1.1A for the SGM42636 per bridge.

Full-Scale Current Rating

The full-scale current is the peak of the quasi-sinusoid current waveform during microstepping and rotation. Like a sinusoid current, the peak and RMS values are not independent and the full-scale current is almost $\sqrt{2}$ times the rated RMS value ($I_{FS} \approx 1.41 \times I_{RMS}$). Therefore, the peak current is effectively limited by the thermal performance as well. The rated full-scale current is 1.5A for the SGM42636 per bridge.

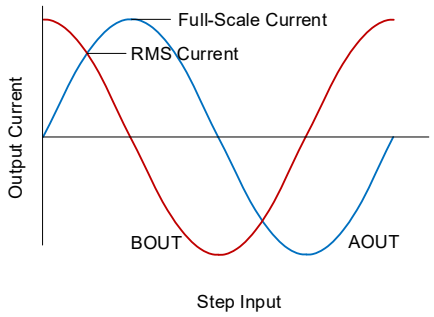


Figure 3. Full-Scale and RMS Current

Full-Bridge Drivers

Each driver has two N-channel full H-bridges (A and B) that drive the two windings (A and B) of the bipolar stepper motor respectively. The structure of each full bridge is shown in Figure 4 for winding A as example.

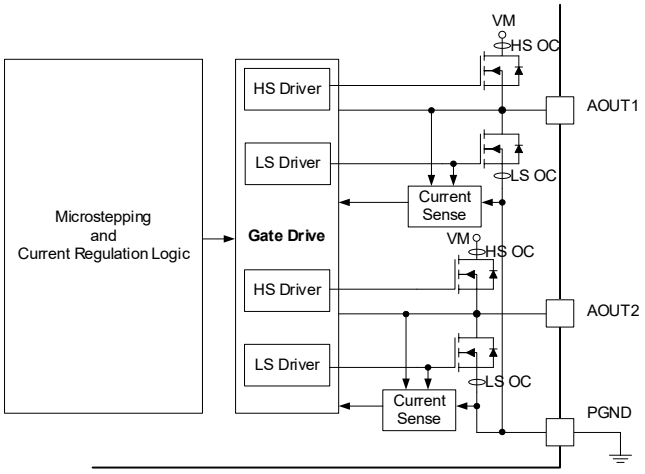


Figure 4. Full-Bridge Driver Block Diagram

DETAILED DESCRIPTION (continued)

Microstepping Indexer

Several stepping modes can be applied with the indexer integrated in the SGM42636. The mode pins (M0 and M1) are biased to select the stepping mode as given in Table 2. Stepping modes can be changed on the fly.

Table 2. Using Mode Pins (M0 and M1) to Configure Microstepping

M0	M1	STEP MODE
0	0	Full step (2-phase excitation) with 100% current (high torque full step)
0	330kΩ to GND	Full step (2-phase excitation) with 71% current
1	0	Non-circular 1/2 step (high torque 1/2 step)
Hi-Z	0	1/2 step
0	1	1/4 step
1	1	1/8 step
Hi-Z	1	1/16 step
0	Hi-Z	1/32 step
Hi-Z	330kΩ to GND	1/64 step
Hi-Z	Hi-Z	1/128 step
1	Hi-Z	1/256 step

In Table 3, the winding currents (as percentage of the full-scale) and the electrical angles in each indexer state are listed for full step (71% current), 1/2 step, 1/4 step and 1/8 step operation modes. Table 4 and Table 5 list the same parameters for 100% full step and non-circular half-step modes. The currents and electrical angles for higher stepping resolutions (1/16, 1/32, 1/64, 1/128 and 1/256) can be extended similarly from Table 3. The AOUT and BOUT currents in this table are approximate sine and cosine functions of the electrical angle respectively. Winding current is positive when flowing from terminal 1 to terminal 2 (xOUT1 to xOUT2).

With every rising edge of the STEP input, the indexer advances to its next state shown in the table when the DIR input is high. If the DIR is set to logic low, the sequence is reversed. The step size is set by M0 and M1 inputs and may be changed on the fly during stepping. If the mode is changed on the fly, the next rising edge of STEP input transfers the indexer state to the next valid state of the new stepping mode.

The indexer resets to home state at 45° electrical angle after power-up, under-voltage lockout, or exit from sleep mode.

Table 3. Output Currents and Electrical Rotor Angle for Each Indexer Stepping State (for DIR = High)

Indexer State				AOUT Current (% Full-Scale)	BOUT Current (% Full-Scale)	Electrical Angle (Degrees)
1/8 Step	1/4 Step	1/2 Step	Full Step 71%			
1	1	1		0%	100%	0.00
2				20%	98%	11.25
3	2			38%	92%	22.50
4				56%	83%	33.75
5	3	2	1	71%	71%	45.00
6				83%	56%	56.25
7	4			92%	38%	67.50
8				98%	20%	78.75
9	5	3		100%	0%	90.00
10				98%	-20%	101.25
11	6			92%	-38%	112.50
12				83%	-56%	123.75
13	7	4	2	71%	-71%	135.00

DETAILED DESCRIPTION (continued)

Indexer State				AOUT Current (% Full-Scale)	BOUT Current (% Full-Scale)	Electrical Angle (Degrees)
1/8 Step	1/4 Step	1/2 Step	Full Step 71%			
14				56%	-83%	146.25
15	8			38%	-92%	157.50
16				20%	-98%	168.75
17	9	5		0%	-100%	180.00
18				-20%	-98%	191.25
19	10			-38%	-92%	202.50
20				-56%	-83%	213.75
21	11	6	3	-71%	-71%	225.00
22				-83%	-56%	236.25
23	12			-92%	-38%	247.50
24				-98%	-20%	258.75
25	13	7		-100%	0%	270.00
26				-98%	20%	281.25
27	14			-92%	38%	292.50
28				-83%	56%	303.75
29	15	8	4	-71%	71%	315.00
30				-56%	83%	326.25
31	16			-38%	92%	337.50
32				-20%	98%	348.75

Table 4 lists the same parameters as Table 3 but for the full step operation with 100% full-scale current. This mode uses more power compared to the 71% full step but provides higher torque (usually needed at higher speeds).

Table 4. Output Currents and Electrical Angle for Indexer Steps in 100% Full Step Mode (for DIR = High)

Indexer State (Full Step 100%)	AOUT Current (% Full-Scale)	BOUT Current (% Full-Scale)	Electrical Angle (Degrees)
1	100	100	45
2	-100	100	135
3	-100	-100	225
4	100	-100	315

Similarly, Table 5 lists the parameters for the non-circular 1/2 step mode. This mode uses more power compared to the normal (circular) 1/2 step, but produces higher torque (usually needed for higher motor speeds).

Table 5. Output Currents and Electrical Angle for Indexer Steps in Non-Circular 1/2 Step Mode (for DIR = High)

Indexer State Non-Circular 1/2 Step Mode	AOUT Current (% Full-Scale)	BOUT Current (% Full-Scale)	Electrical Angle (Degrees)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	-100	135
5	0	-100	180
6	-100	-100	225
7	-100	0	270
8	-100	100	315

DETAILED DESCRIPTION (continued)

V_{REF} Control for Full-Scale Current Adjustment

VREF pin voltage controls the magnitude of the deliverable full-scale current by scaling the current regulation set point. It can be fixed by a voltage divider or can be used as a current adjustment input for applications that need to set motor current based on the motor loading and speed. A DAC output from MCU may be used to set the VREF voltage for adjusting the full-scale current as shown in Figure 5. VREF voltage should not exceed 3.3V. A PWM output signal along with a low-pass filter may also be used to set the VREF voltage as shown in Figure 6.

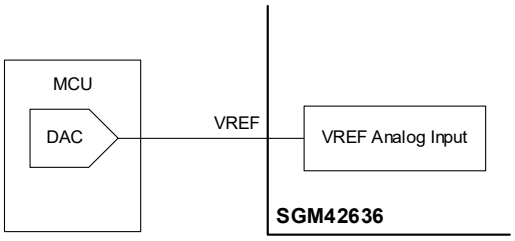


Figure 5. Control of the VREF Voltage with a DAC

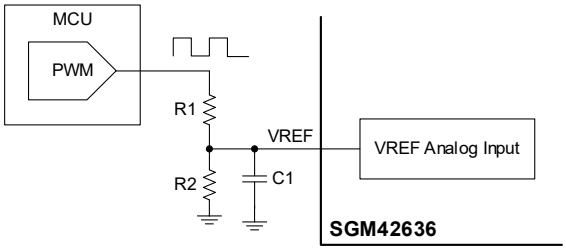


Figure 6. Control of the VREF with a PWM Output and an LPF

Current Regulation

An adjustable, off-time control PWM current regulation scheme is used to control the motor winding currents as shown in Figure 7. With activation of the H-bridge, the current rises with a rate determined by the VM voltage, winding inductance, and the back-EMF induced by rotor rotation. In each PWM cycle, the bridge is active for at least t_{BLANK} time. The PWM pulse is on until t_{DRIVE} where the current exceeds the I_{TRIP} regulation threshold and then the decay (current drop) begins and continuous during the t_{OFF} time. This time is set by the TOFF pin. In some cases, the off-time is extended for one or more t_{OFF} periods to let the current fall below the I_{TRIP} level. The I_{TRIP} comparator monitors the voltage of the current sense MOSFETs that are in parallel with the low-side power MOSFETs. The current sense MOSFETs are biased with a current mode sine-weighted DAC output to generate the reference current. So, in each PWM cycle, the I_{TRIP} level is updated with a quantized sine (or cosine) waveform. The full-scale value of this reference current is set by the VREF voltage. The ratio of the full-scale regulation current (I_{FS}) to the VREF voltage is 1A per 2.2V for SGM42636, that is:

$$I_{FS}(A) = \frac{V_{REF}(V)}{K_V}$$

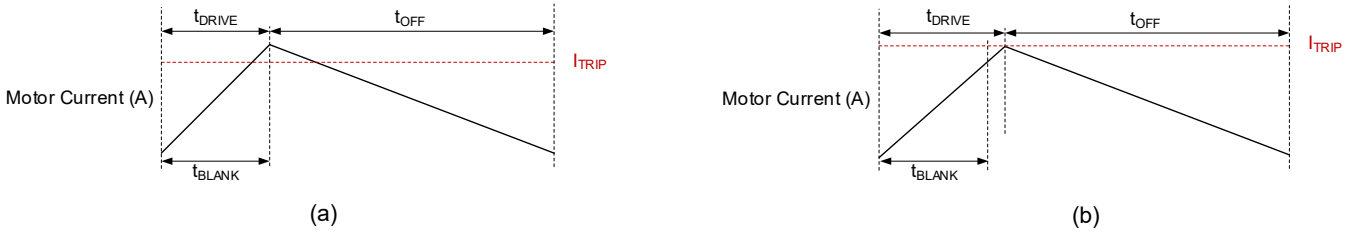


Figure 7. Bridge Output PWM Current Chopping Waveform (Simplified Decay Current is Shown)

DETAILED DESCRIPTION (continued)

PWM Off-Time

The TOFF pin is used to configure the PWM off-time (t_{OFF}), as shown in Table 6. The off-time can be changed on the fly (while stepping).

Table 6. Off-Time Settings by TOFF Pin

TOFF Pin State	Off-Time (t_{OFF})
0	7μs
330kΩ to GND	16μs
Hi-Z	24μs
1	32μs

Blanking Time

At the beginning of each PWM cycle, the H-bridge begins driving current into the motor winding. In order to obtain a stable and reliable trigger signal, t_{BLANK} is usually set as the blanking time. After the t_{BLANK} has passed, the driver will perform the corresponding action based on the output state of the internal comparator. For small inductance or large supply voltage, the current in the motor coil will rise rapidly, even if the I_{TRIP} and current comparator have been triggered, the driver will not immediately enter the decay state, but at least continue to t_{BLANK} the on-time. For SGM42636, t_{BLANK} is a fixed value of about 2μs. After t_{BLANK}, the drive switches to either fast decay or slow decay according to the current decay mode.

PWM Decay Modes

During PWM off-time, the H-bridge current begins to decay either in fast rate or slow as shown in Figure 8. In the fast decay, when the current exceeds the I_{TRIP} threshold, the bridge applies a reverse voltage by turning the opposite switches and forcing the current to reverse its direction. Bridge is deactivated before the current reversal. In the slow decay mode, the lower switches are both turned on to freewheel the winding current. In this mode, a near zero voltage is applied to the winding to decay the current. In a mixed decay, the off-time initially begins with fast decay that lasts for a fixed time (t_{FAST}) and then a slow decay phase for the remainder of t_{OFF} time.

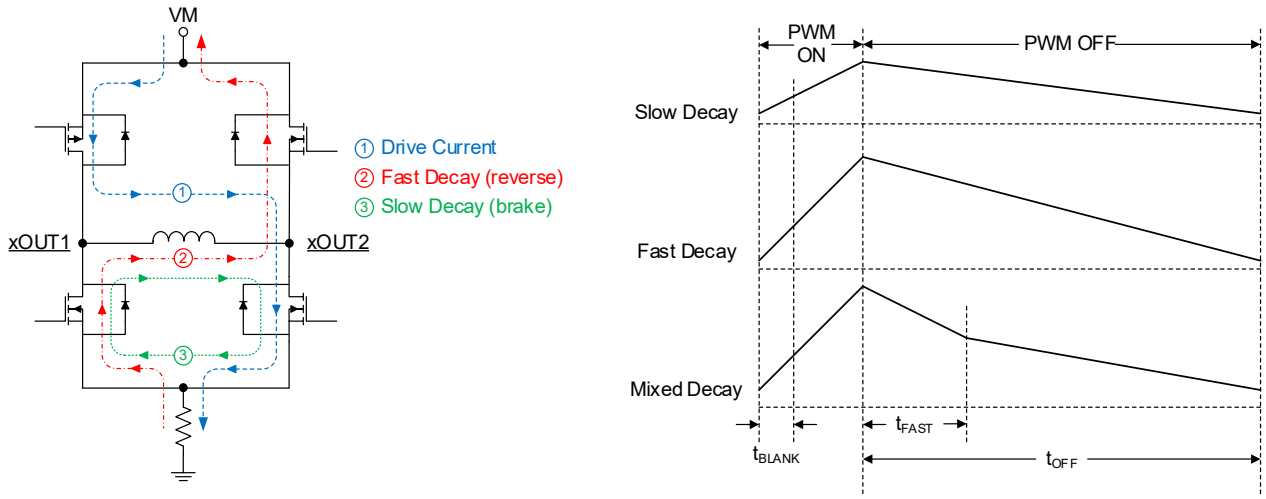


Figure 8. Slow, Fast and Mixed Decay Current Chopping Modes

By combining the slow and fast decays based on different criteria, 6 decay mode options are available in the SGM42636 as listed in Table 7. Decay mode is set by the DECAY0 and DECAY1 inputs and can be changed on the fly. As shown in Figure 9 with red and blue phases, based on the increasing or decreasing of the current reference (I_{TRIP}) in the next step, the bridge can be in increasing steps (INC) or decreasing steps (DEC) state.

DETAILED DESCRIPTION (continued)

Table 7. Decay Mode Settings

DECAY0	DECAY1	Increasing Steps (INC)	Decreasing Steps (DEC)
0	0	Smart Tune Dynamic Decay	Smart Tune Dynamic Decay
1	0	Smart Tune Ripple Control	Smart Tune Ripple Control
0	1	Mixed Decay: t_{FAST} = 0.3 × t_{OFF}	Mixed Decay: t_{FAST} = 0.3 × t_{OFF}
1	1	Slow Decay	Mixed Decay: t_{FAST} = 0.3 × t_{OFF}
0	Hi-Z	Mixed Decay: t_{FAST} = 0.6 × t_{OFF}	Mixed Decay: t_{FAST} = 0.6 × t_{OFF}
1	Hi-Z	Slow Decay	Slow Decay

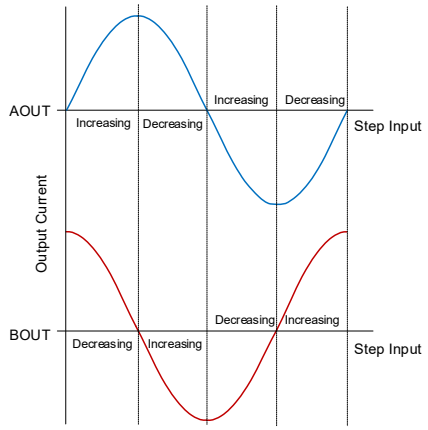


Figure 9. Definition of Bridge Increasing (INC) and Decreasing (DEC) Step Phases

The slow decay has the lowest current ripple for a given t_{OFF} time. However, during the current decreasing phases, it may take a long time to reach the new I_{TRIP} level due to the slow current drop rate. If the current is still above the I_{TRIP} at the end of the off-time, it will be extended for one or more t_{OFF} periods until the current drops below I_{TRIP} level.

An important case occurs when the speed is very low (slow stepping) and the back-EMF is almost zero. The current rises sharply during the blank time in such condition. The high peak current may require several off-time extensions to bring the current below I_{TRIP} or it may even result in loss of regulation. Therefore, slow decay may not be an appropriate choice to regulate the current at low speeds and more intense decay modes are needed.

Slow-Slow (DECAY0 = 1, DECAY1 = Hi-Z)

In the slow-slow decay mode, slow decay is used for both increase or decrease phases. The current regulation during INC and DEC phases are shown in Figure 10.

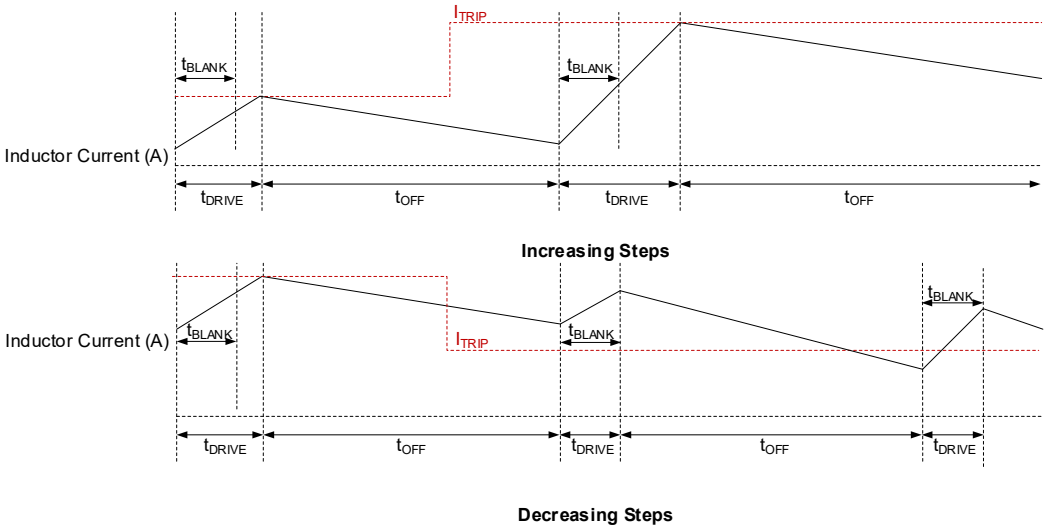


Figure 10. Current Regulation with Slow/Slow Decay Mode (Slow for both INC and DEC Phases)

DETAILED DESCRIPTION (continued)

Slow-Mixed (DECAY0 = 1, DECAY1 = 1)

In this mode, mixed decay is only used in the decreasing current phase and slow decay is used for increasing phase. The current ripple in the INC phases is small (slow decay), but in the DEC phases, the ripple is larger (but still less than pure fast decay ripple). With mixed decay, the current settling to the new I_{TRIP} level during DEC phase is faster than slow decay. See Figure 11 for the current regulation waveforms during INC and DEC phases for this decay mode.

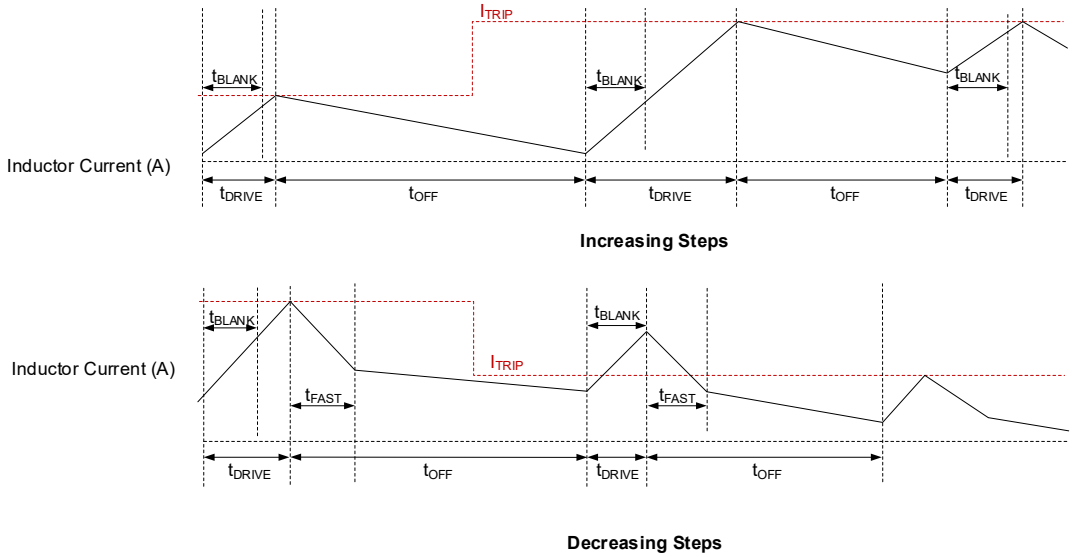


Figure 11. Current Regulation with Slow-Mixed Decay Mode: Slow for INC Phase and Mixed for DEC Phase

Mixed-Mixed Modes (DECAY0 = 0, DECAY1 = 1 or Hi-Z)

In these two modes, mixed decay is used for both increasing and decreasing current steps. If DECAY1 is set to 1, then t_{FAST} is set to 30% of the t_{OFF} period and if DECAY1 input is left open (Hi-Z state), t_{FAST} is set to 60% of the t_{OFF}. The current ripple is larger compared to slow decay, but still less than pure fast decay in both INC and DEC phases.

Figure 12 shows the current regulation waveforms during INC and DEC phases for the mixed-mixed decay modes.

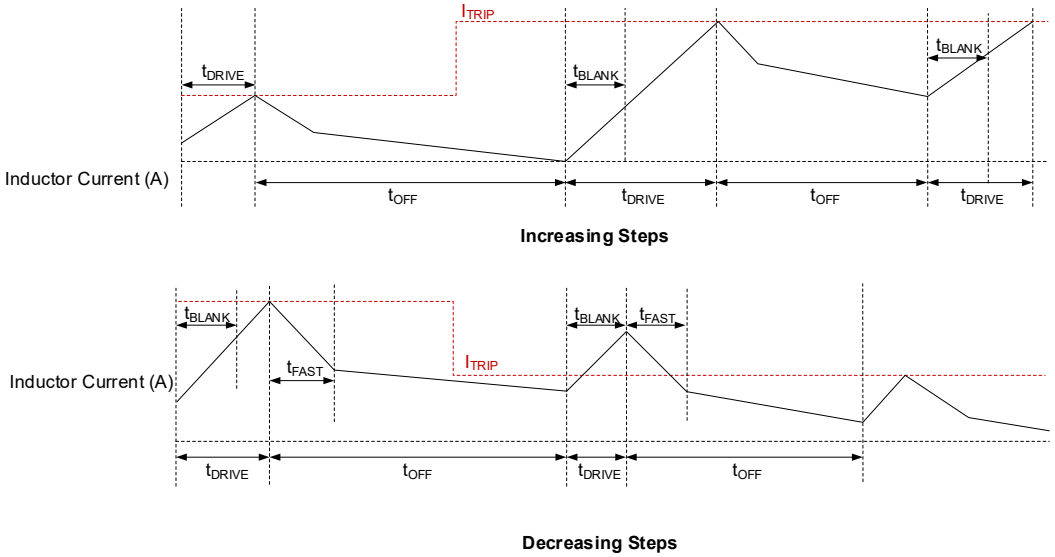


Figure 12. Current Regulation with Mixed-Mixed Decay Mode: Mixed for both INC and DEC Phases

DETAILED DESCRIPTION (continued)

Smart Tune Decay Modes

The smart tune decay modes are advanced current regulation schemes that use more complex current regulation control compared to the conventional fixed off-time methods. In the smart tune modes the decay schemes and current regulation is adapted with the motor and system operational parameters such as:

- Motor winding resistance and inductance
- Motor aging factors
- Motor speed and load dynamics
- Motor back-EMF variations between rising and falling steps
- Supply voltage variation
- Step transition dynamics
- di/dt consideration in the low-current and high-current operation

Smart tune dynamic decay mode and smart tune ripple control mode are the two smart tune current regulation options in the SGM42636.

Smart Tune Dynamic Decay Mode (DECAY0 = 0, DECAY1 = 0)

In this mode, the slow, mixed and fast decay modes are automatically selected by the device. This will save a lot of design time and simplifies the initial tuning of the system. With smart tune, the percentage of the fast decay time in the mixed mode is also dynamically adjusted. With this feature, the best decay setting for minimal ripple is automatically obtained and initial system tuning is not needed.

The optimal decay mode is found by iterative updating of the decay parameters in each PWM cycle and adjusting them towards better performance. For example, if the current overshoots above the desired I_{TRIP} level, the decay mode will be updated to be more aggressive in the next cycle (like increasing the fast decay percentage) to reduce the peak current and prevent the loss of regulation. On the other hand, if the t_{DRIVE} becomes too long for the current to reach the I_{TRIP} level, the decay mode will be updated with a less aggressive one in the next cycle (like reduction or removal of the fast decay percentage). This will decrease ripple and improves efficiently. In the smart tune dynamic decay mode, after each falling step, fast decay mode is automatically applied to avoid off-time extension and quick transition to the next step.

The smart tune dynamic decay is an optimal choice for applications that require fixed frequency operation for current regulation with minimum current ripple. Typical current regulation waveforms during INC and DEC phases for this mode are shown in Figure 13.

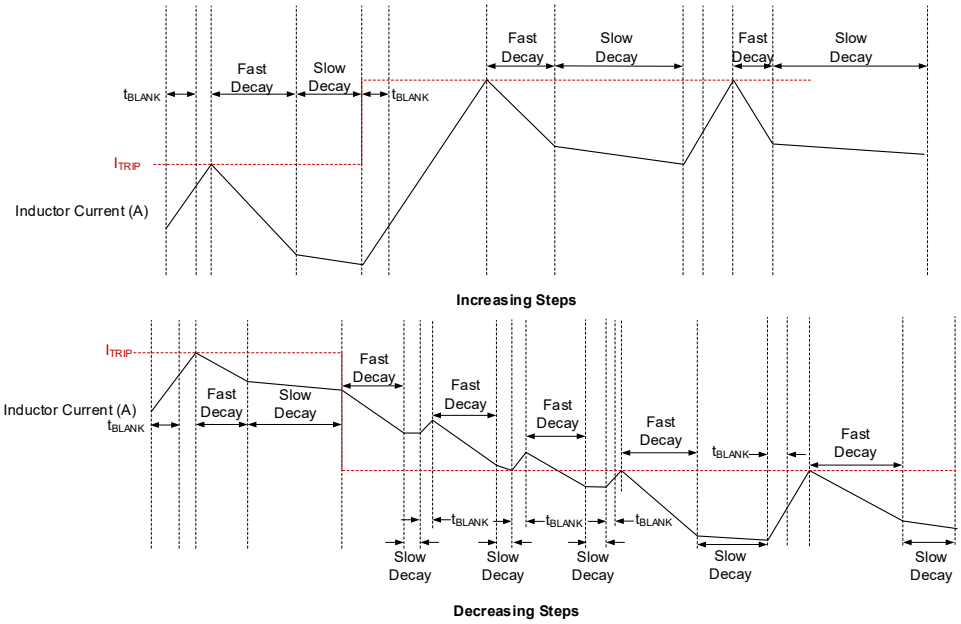


Figure 13. Smart Tune Dynamic Decay Mode Current Waveforms during INC and DEC Phases

DETAILED DESCRIPTION (continued)

Smart Tune Ripple Control Mode (DECAY0 = 1, DECAY1 = 0)

In the smart tune ripple control mode, besides the I_{TRIP} upper-level comparator for the current rising, a I_{TRIP} lower-level comparator is also used for current falling. In this smart mode, the decay switches between slow and mixed decay. When t_{DRIVE} is larger than t_{BLANK}, the chopper maintains a slow decay time of t_{OFF} after t_{DRIVE}. When the t_{BLANK} is equal to t_{DRIVE} or step changes during DEC phase, the chopper will insert a fast decay period until the current drops to I_{TRIP} again.

The smart tune ripple control makes it possible to quickly adjust the current to the target value and reduces power consumption.

See Figure 14 for an illustration of smart tune ripple control decay mode and the current regulation waveforms.

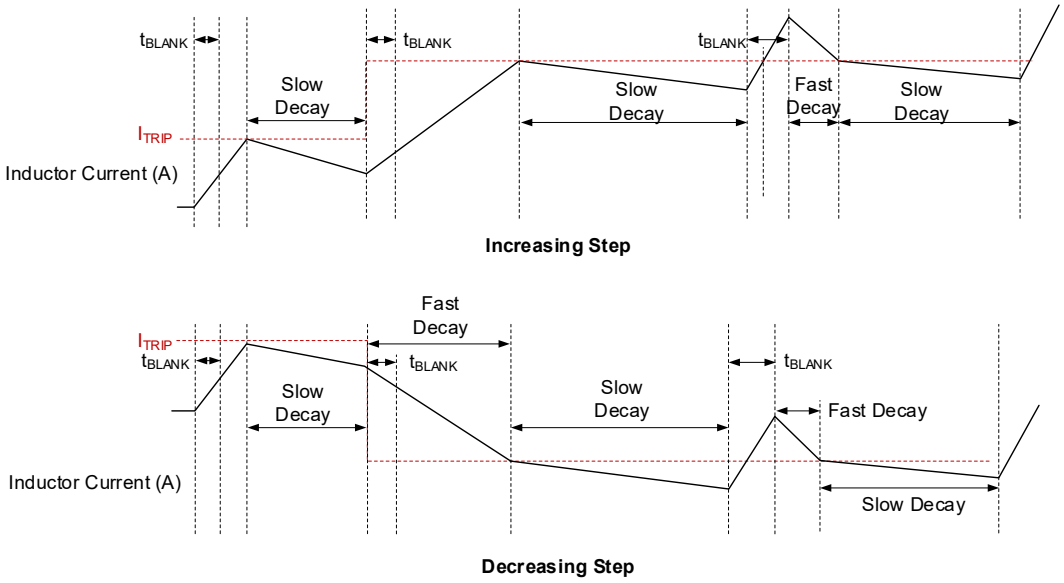


Figure 14. Smart Tune Ripple Control Decay Mode Current Waveforms during INC and DEC Phases

Charge Pump

The high-side N-channel power MOSFETs require a gate-drive voltage higher than the VM supply voltage. A charge pump is integrated to generate this supply voltage and its output is available on the VCP pin. A filter capacitor should be connected externally between VM and VCP pins and another ceramic capacitor is needed between CPL and CPH pins for pump operation. The structure of the charge pump is shown in Figure 15.

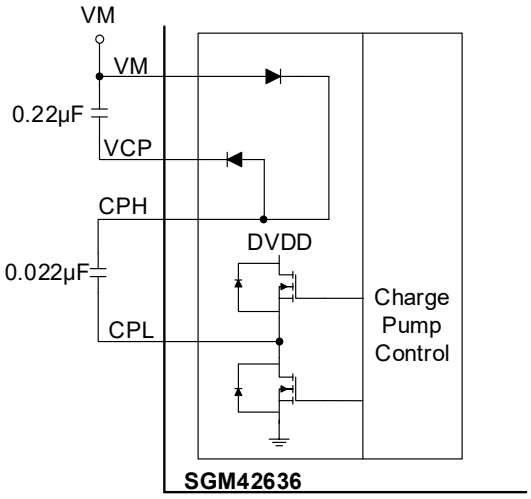


Figure 15. Integrated Charge Pump Block Diagram

DETAILED DESCRIPTION (continued)

Integrated DVDD Regulator

The SGM42636 includes a linear voltage regulator that provides a 5V (nominal) reference voltage on the DVDD output as shown in Figure 16. The maximum load on this pin is limited to 2mA and if this limit is exceeded, the output will drop significantly. Bypass the DVDD to GND with a ceramic capacitor.

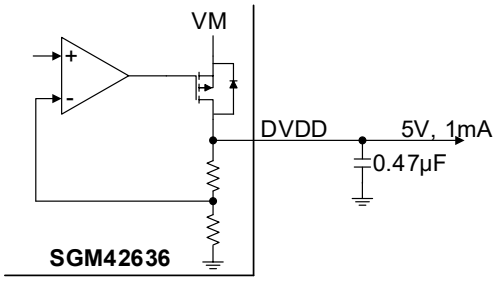


Figure 16. DVDD Linear Voltage Regulator Block Diagram

If a digital input (like, M0, M1, DECAY0, DECAY1, or TOFF) needs a permanent pull up, it is preferred to use DVDD output for better power saving in sleep mode. When VM voltage is removed, the regulator is disabled and no current flows in the internal pull-down resistors.

Note that the nSLEEP pin must not be pulled up to DVDD, otherwise the device cannot exit the sleep mode.

Logic and Multi-Level Input Pins

The SGM42636 uses multi-level inputs for configuring its operation. The block diagram of the tri-level inputs (M0, DECAY1 and ENABLE) are shown in Figure 17.

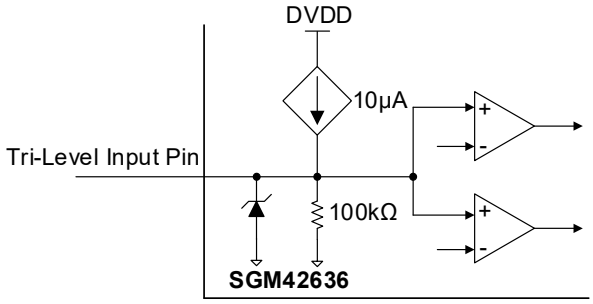


Figure 17. Internal Structure of the Tri-Level Input Pins (M0, DECAY1 and ENABLE)

The quad-level input structure of the M1 and TOFF pins is shown in Figure 18.

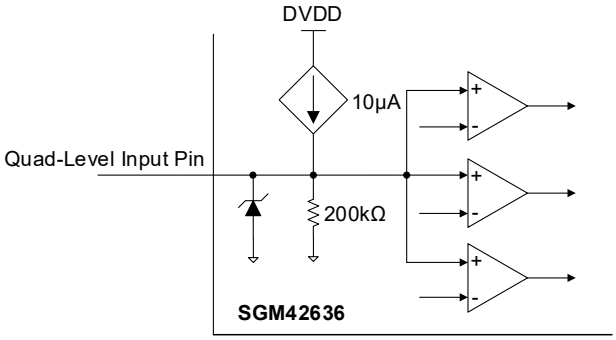


Figure 18. Internal Structure of the Quad-Level Input Pins (M1 and TOFF)

DETAILED DESCRIPTION (continued)

The block diagram of the two-level logic inputs (DECAY0, STEP, DIR and nSLEEP) is also shown in Figure 19.

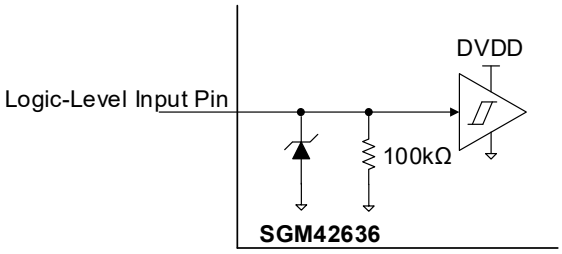


Figure 19. Internal Structure of the Two-Level (Logic) Input Pins (STEP, DIR, DECAY0 and nSLEEP)

nFAULT Output

The nFAULT is an open-drain output that is pulled low when a fault is detected. It should be pulled up to a 5V (like DVDD) or 3.3V supply voltage as shown in Figure 20. After power-up, nFAULT is released to go high.

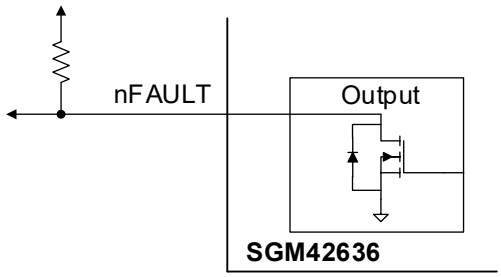


Figure 20. The nFAULT Output

Faults and Protections

The SGM42636 has a complete set of protection features to protect it against faults including VM supply under-voltage, VCP under-voltage, output over-current, and junction over-temperature. A summary of the fault conditions and the resulting protection functions is provided in Table 8. Each item is explained in the following sections.

Table 8. SGM42636 Faults and Protections Summary

Fault	Condition	Configuration	Report	H-Bridge	Charge Pump	Indexer	Logic Circuitry	Recovery
VM under-voltage (UVLO)	$V_M < V_{UVLO}$	-	nFAULT	Disabled	Disabled	Disabled	Resets and V_{DVDD} falls below 3.9V	Automatic when $V_M > V_{UVLO}$
VCP under-voltage (CPUV)	$V_{CP} < V_{CPUV}$	-	nFAULT	Disabled	Operating	Operating	Operating	Automatic when $V_{CP} > V_{CPUV}$
Over-Current (OCP)	$I_{OUT1} > I_{OCP}$ or $I_{OUT2} > I_{OCP}$	ENABLE = Hi-Z	nFAULT	Disabled	Operating	Operating	Operating	Latched Needs nSLEEP or power cycling
		ENABLE = 1	nFAULT	Disabled	Operating	Operating	Operating	Auto-retry after t_{RETRY}
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	-	nFAULT	Disabled	Disabled	Operating	Operating	Normal operation resumes and the nFAULT is released when the TSD condition is removed.

VM Under-Voltage Lockout (UVLO)

If the V_M supply voltage drops below the V_{UVLO} falling threshold, all outputs, charge pump and logic circuit will be disabled, and nFAULT goes low. Device will recover and nFAULT is released like a new power-up when the V_M voltage exceeds the V_{UVLO} rising threshold.

DETAILED DESCRIPTION (continued)

Charge Pump Under-Voltage Lockout (CPUV)

If the VCP voltage drops below the CPUV falling threshold, all outputs are disabled and nFAULT is pulled low. The charge pump and logic circuits continue operation. The outputs will resume operation and nFAULT is released when VCP exceeds the CPUV rising threshold and returns to its normal range.

Over-Current Protection (OCP)

Over-current protection is implemented by an analog circuit that senses the MOSFET currents and stops the gate pulses if the current limit is exceeded. If after t_{OCP} time the current is still high, all MOSFETs in that bridge will be disabled and nFAULT is asserted. The charge pump continues to operate. Two options are available for OCP recovery that can be selected through ENABLE input: latched protection (ENABLE = Hi-Z) and Auto-Retry after t_{RETRY} time (ENABLE = 1).

Latched OCP Shutdown

To select the latching OC protection, the ENABLE input should be left open (Hi-Z). In this mode, the bridge that is in OCP condition will remain disabled and nFAULT is kept low until an nSLEEP cycling or a power cycling occurs.

OCP with Auto-Retry

To select the auto-retry OCP protection, set the ENABLE pin to high state (connect to DVDD). In this mode, after a t_{RETRY} wait time, the bridge in the OCP condition is re-enabled for normal operation and nFAULT is released. If the OC condition persists, the bridge output is disabled and nFAULT is asserted until another retry.

Thermal Protection and Shutdown (TSD)

To prevent overheating damage to the device, an over-temperature shutdown protection is implemented in the device. If the die temperature (T_J) exceeds the T_{SD} limit, all H-bridge MOSFETs are turned off and nFAULT is asserted. The charge pump and logic circuits continue operation. Normal operation resumes and the nFAULT is released when the TSD condition is removed.

Functional Modes

The SGM42636 can be in different functional conditions as summarized in Table 9 and explained below.

Sleep Mode (nSLEEP = 0)

This state is controlled by the nSLEEP input. When the nSLEEP input is pulled low for at least t_{SLEEP} time, the SGM42636 enters low-power mode (sleep) in which both bridges and the charge pump are disabled. By pulling the nSLEEP high and after t_{WAKE} time, the device exits sleep mode. During the t_{WAKE} time, the inputs are ignored.

Disable Mode (nSLEEP = 1, ENABLE = 0)

The ENABLE input is used to enable or disable the bridges. If ENABLE = 0, the outputs go to Hi-Z state.

Run Mode (nSLEEP = 1, ENABLE = Hi-Z or 1)

With $V_M \geq V_{UVLO}$, if nSLEEP = 1 and ENABLE is set to Hi-Z or 1 state, the device will be activated and enters the run mode. The inputs are ignored for the t_{WAKE} time after the two conditions are both valid.

DETAILED DESCRIPTION (continued)

nSLEEP Reset Pulse

To clear a latched fault, a quick negative nSLEEP pulse can be applied to the device. The pulse width must be shorter than 20μs and longer than the 10μs (nSLEEP deglitch time) to reset the fault. A reset pulse has no effect on the state of charge pump or other functional blocks. If the nSLEEP remains low for longer than 20μs, but less than 130μs, the faults are cleared but entry to the shutdown mode is not assured. To ensure device sleep mode, the nSLEEP must remain low for at least 130μs. Figure 21 illustrates all nSLEEP timings.

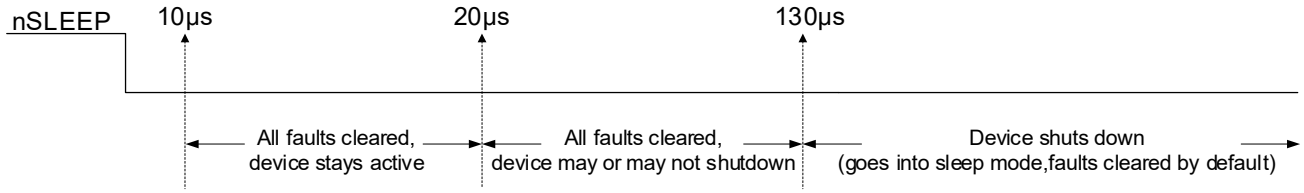


Figure 21. nSLEEP Timing Conditions for Reset Pulse (to Exit a Latched Fault), and Entry to Sleep Mode.

Table 9. Summary of the Device Functional Modes

Condition		Configuration	H-Bridges	DVDD Regulator	Charge Pump	Indexer	Logic
Sleep Mode	7V < V_M < 45V	nSLEEP = 0	Disabled	Disabled	Disabled	Disabled	Disabled
Run (Active)	7V < V_M < 45V	nSLEEP = 1 ENABLE = 1 or Hi-Z	Operating	Operating	Operating	Operating	Operating
Disabled	7V < V_M < 45V	nSLEEP = 1 ENABLE = 0	Disabled	Operating	Operating	Operating	Operating

APPLICATION INFORMATION

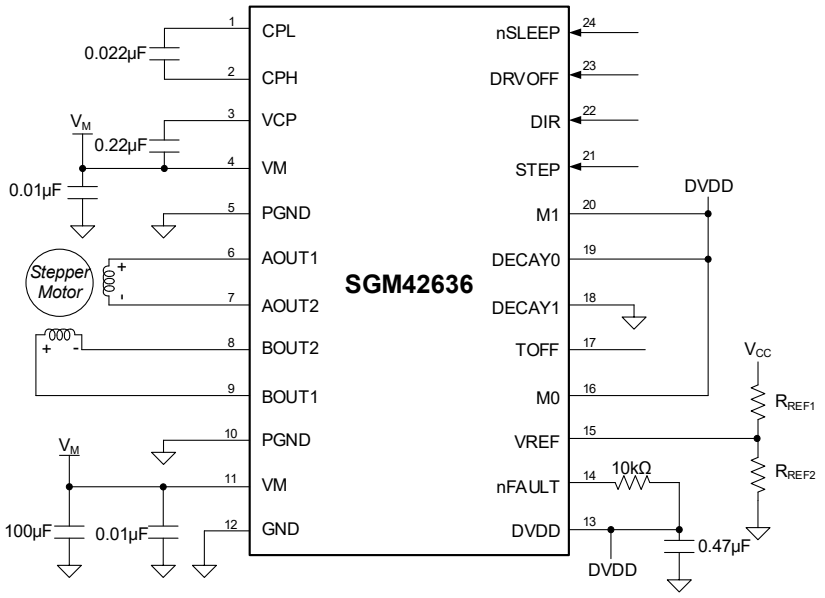


Figure 22. Typical Application Schematic

Configurations of the SGM42636 are explained in the following design examples.

Design Requirements

A list of design parameters for a typical motor drive system with the SGM42636 are provided in Table 10 as example.

Table 10. Design Parameters

Design Parameter	Reference	Example Value
Supply Voltage	V_M	24V
Motor Winding Resistance	R_L	2.6Ω/phase
Motor Winding Inductance	L_L	1.4mH/phase
Motor Full Step Angle	θ_{STEP}	1.8°/step
Target Microstepping Level	n_m	1/8 step
Target Motor Speed	v	120rpm
Target Full-Scale Current	I_{FS}	500mA

Stepper Motor Speed

The motor speed and microstepping requirements are the first parameters to consider in configuration of the stepper motor driver. If the application requires a constant speed, STEP pin must receive square pulses with f_{STEP} frequency.

Note that if the target speed is set too high, the motor may not be able to follow the STEP and won't spin, so, it is important to make sure the motor and load can support that speed with the available torque/power.

Equation 1 can be used to calculate the required f_{STEP} frequency for driving the stepper motor at speed (v) based on the microstepping level (n_m) and the motor full step angle (θ_{STEP}):

$$f_{STEP}\left(steps/s\right)=\frac{v\left(rpm\right)\times 360\left(°/rot\right)}{\theta_{STEP}\left(°/step\right)\times n_m\left(steps/micro\text{-}step\right)\times 60\left(s/min\right)} \quad (1)$$

θ_{STEP} is a stepper motor parameter that is specified in its datasheet or on the motor body.

The microstepping level (n_m) is set by the MODE pins (M0 and M1) based on the list in Table 2. By choosing a finer microstepping value, smoother and quieter motor motion is achieved, but at the cost of increased switching losses and higher required f_{STEP} frequency for the same motor speed.

APPLICATION INFORMATION (continued)

For example, to get the a target speed of 120rpm for a 1.8°/step motor with 1/8 microstepping the required step pulse frequency is:

$$f_{STEP} = \frac{120(\text{rpm}) \times 360(°/\text{rot})}{1.8(°/\text{step}) \times 1/8(\text{steps/micro-step}) \times 60(\text{s/min})} = 3200\text{Pluse/sec} \quad (2)$$

Power Supply Considerations

The SGM42636 stepper driver is designed to operate from 7V to 45V supply voltage on their VM pins and can drive stepper motors with the same voltage rating. Each VM pin must be decoupled with at least one 0.01μF ceramic capacitor. These capacitors must be placed as close as possible to each VM pins and its adjacent PGND pin. A bulk capacitor should also be used between VM and PGND return near the device to limit voltage ripple on the VM and stabilize the supply line.

Bulk Capacitance Selection for Motor Drivers

Using local bulk capacitors near the motor driver is necessary even though they increase the size and cost of the system. This capacitor is selected based on several factors including the following:

• The required peak current of the system
• The power supply internal capacitance and its sourcing capability
• The parasitic supply line inductance between the source and motor driver
• The system maximum acceptable voltage ripple

If other motor types are used (like brushed or brushless DC) the selection can be different and motor braking method should also be considered.

The parasitic inductance of the supply line limits the rate of the current change. It can result in large voltage variations if the load current has sharp changes. The local bulk capacitance keeps the VM voltage stable by providing or absorbing the difference between sharp motor driver current variations and the available slow changing current through the supply line. This capacitor should be large enough to provide or absorb the difference and limit the voltage rise or fall within the acceptable ripple range.

Even though datasheets usually recommend a wide range for this capacitor, a system-level testing is highly recommended to find the proper bulk capacitance. The bulk capacitor voltage rating must be chosen sufficiently above the VM operating voltage, because with motor loads, the energy transfer is sometimes rapidly reversed from the motor to the supply bus that charges the capacitor. The transient voltage can be significantly above the supply voltage. Selection of a higher voltage rating for the capacitor also improves the capacitor reliability by reducing the stress on its dielectric and mitigating its aging effects.

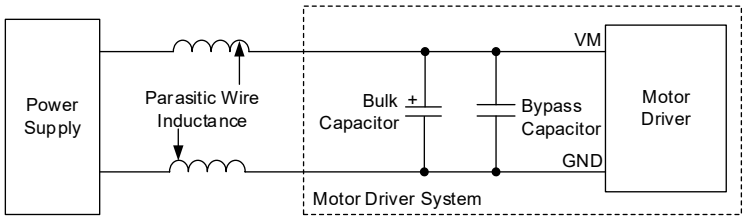


Figure 23. A Typical Motor Drive System with External Power Supply

APPLICATION INFORMATION (continued)

Layout Considerations

PCB layout has a significant impact on the performance of the drive system. The conductors must be sufficiently sized to carry large currents. Wide PGND planes are recommended for stable operation and better cooling.

The VM supply pins must be bypassed to their adjacent PGND pins using 0.01μF low-ESR ceramic capacitors with sufficient voltage rating with thick traces. PGND pins share large ground planes. The electrolytic bulk capacitor must be placed near the device on the VM and PGND traces as well.

Also, a low-ESR ceramic capacitor (0.022μF recommended) rated for VM voltage should be placed as charge pump flying capacitor between and close to the CPL and CPH pins. Same capacitor with 16V rating must be connected between and close to the VM and VCP pins for decoupling.

To bypass DVDD regulator output, it is recommended to use a low-ESR 0.47μF/6.3V capacitor between and as close as possible to the DVDD and GND pins.

The thermal PAD must be connected to system ground planes. This pad serves as a heat sinking path as well.

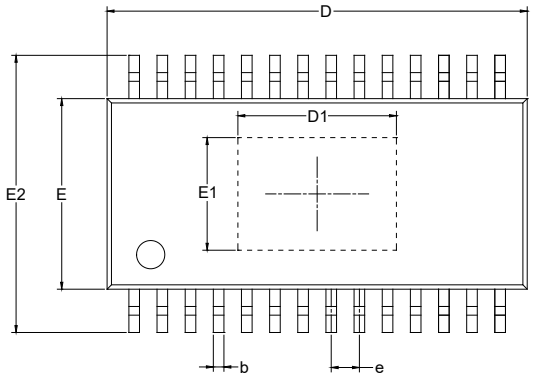
REVISION HISTORY

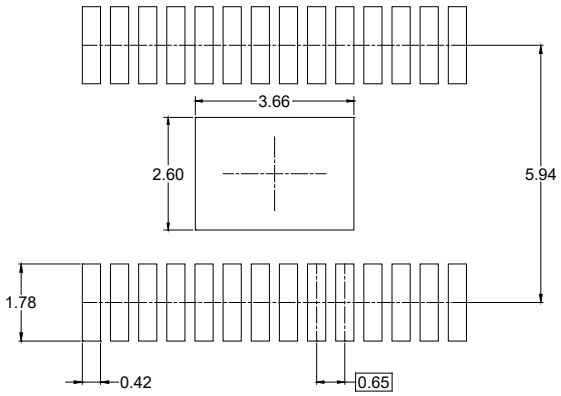
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (MARCH 2026)	Page
Changed from product preview to production data	All

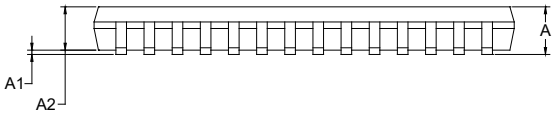
PACKAGE OUTLINE DIMENSIONS

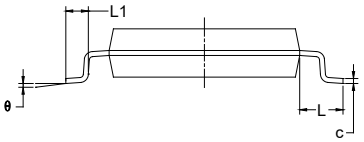
TSSOP-28 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)





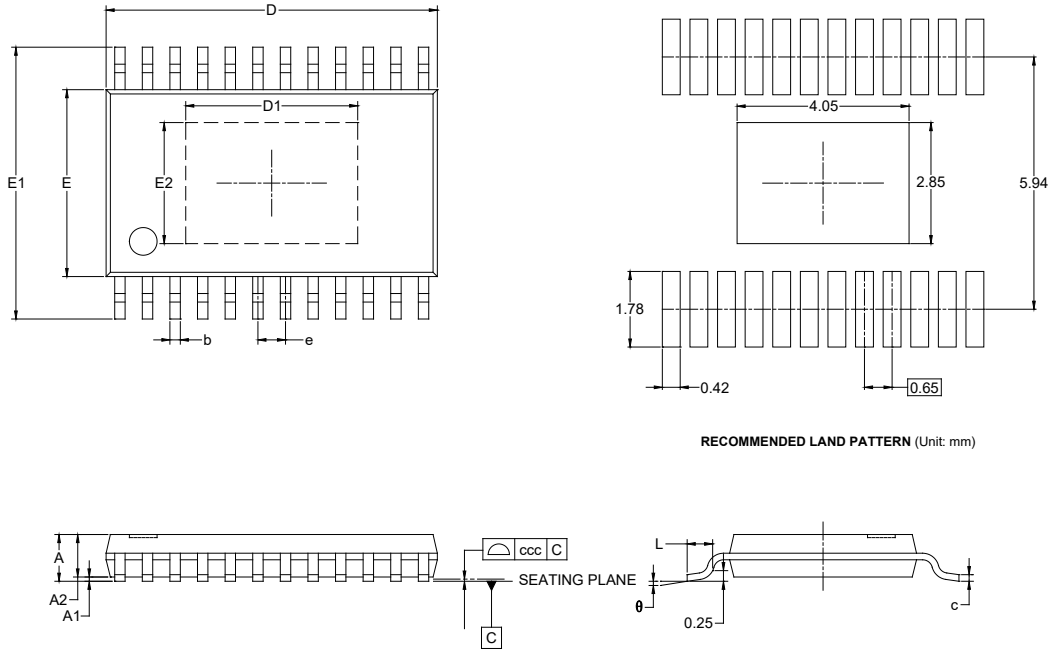
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
D1	3.460	3.860	0.136	0.152
E	4.300	4.500	0.169	0.177
E1	2.400	2.800	0.094	0.110
E2	6.200	6.600	0.244	0.260
e	0.650 BSC		0.026 BSC	
L	1.000 BSC		0.039 BSC	
L1	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

NOTES:

1. Body dimensions do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

TSSOP-24 (Exposed Pad)

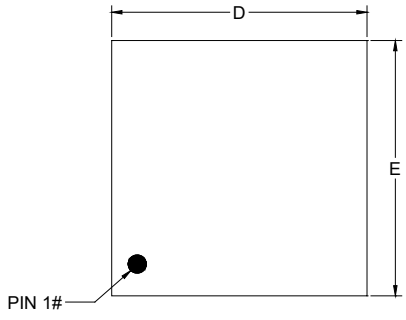


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	1.000 REF		
b	0.190	-	0.300
c	0.090	-	0.200
D	7.700	-	7.900
D1	3.850	-	4.250
E	4.300	-	4.500
E1	6.200	-	6.600
E2	2.650	-	3.050
e	0.650 BSC		
L	0.450	-	0.750
θ	0°	-	8°
ccc	0.100		

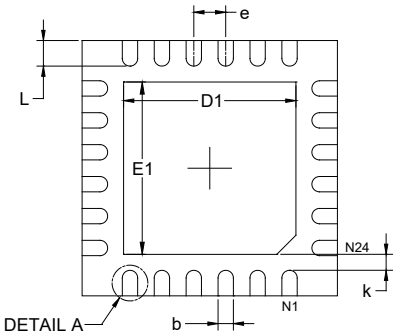
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

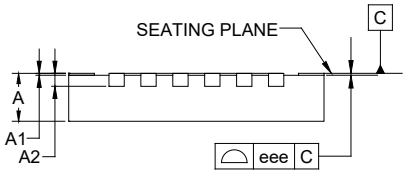
TQFN-4×4-24L



TOP VIEW

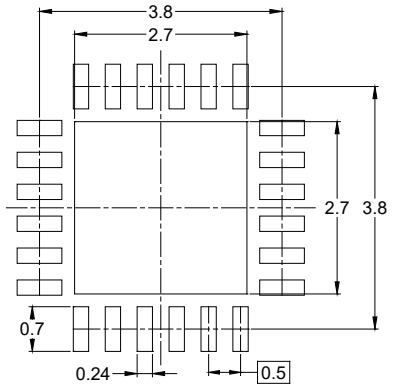


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



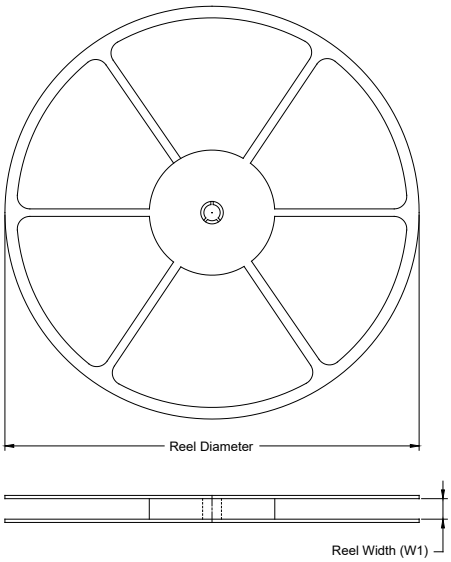
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.180	-	0.300
D	3.900	-	4.100
E	3.900	-	4.100
D1	2.600	-	2.800
E1	2.600	-	2.800
e		0.500 BSC	
k		0.200 MIN	
L	0.300	-	0.500
eee		0.080	

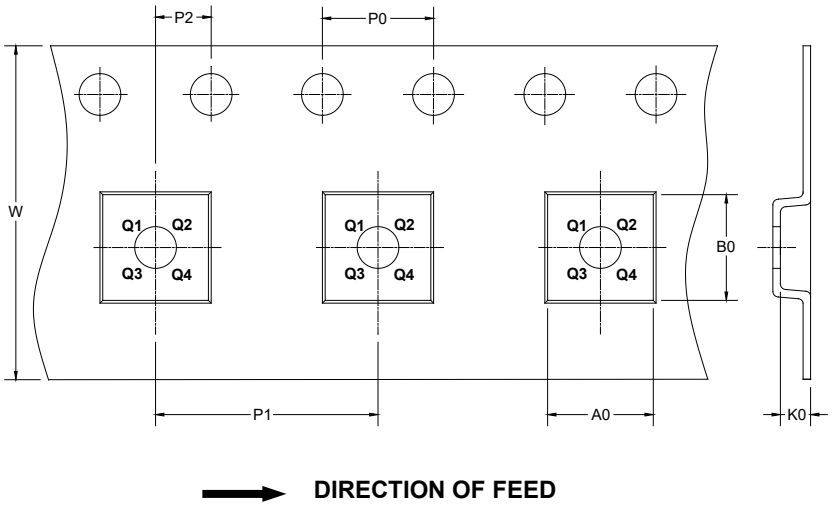
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



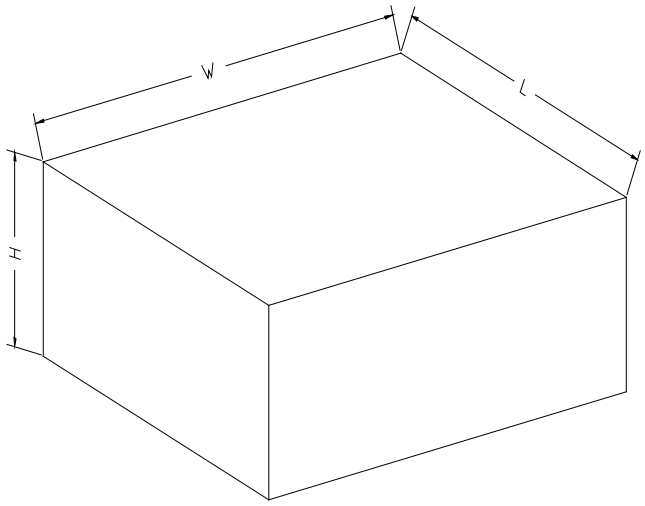
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-24 (Exposed Pad)	13"	16.4	6.80	8.30	1.60	4.0	8.0	2.0	16.0	Q1
TSSOP-28 (Exposed Pad)	13"	16.4	6.80	10.25	1.60	4.0	8.0	2.0	16.0	Q1
TQFN-4×4-24L	13"	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002