SGM64201
3V to 26V Input, ACOT Synchronous Buck Controller

GENERAL DESCRIPTION

The SGM64201 is a 4.5V to 25V controller with adaptive constant on-time (ACOT) control for synchronous Buck converters. It is capable to efficiently drive two N-MOSFETs over the whole voltage range. The SGM64201 exports the maximize power and limits the maximum valley current of the low-side MOSFET. The forced pulse width modulation (FPWM) mode or power saving mode (PSM) at light load is configurable through the voltage of MODE pin.

Eight preset switching frequency can be selected by an external resistor between the RF pin and GND or between the RF pin and the VREG pin.

The SGM64201 is available in a Green TQFN-3×3-16FL package.

APPLICATIONS

Server Computers
Storage Computers
Embedded Computing
Multi-Function Printers

FEATURES

- **Wide Conversion Input Voltage: 3V to 26V**
- **Wide VDD Input Voltage: 4.5V to 25V**
- **Adjustable Output Voltage: 0.6V to 5.5V**
- **Continuous Output Current: > 20A**
- **Precise Reference of 600mV: ±0.7%**
- **5.2V Built-in LDO**
- **Power Saving Mode for Light-Load Efficiency**
- **Adaptive Constant On-Time Mode Control**
- **8 Selectable Frequency Settings**
- **4700ppm/℃ R_{DSON} Current Sensing**
- **4 Selectable Soft-Start Time Settings with Pre-Biased Capability**
- **Power Good (PG) Indicator**
- **Output OVP and UVP Protections**
- **Over Temperature Protection (OTP) with Auto Recovery**
- **Available in a Green TQFN-3×3-16FL Package**

TYPICAL APPLICATION

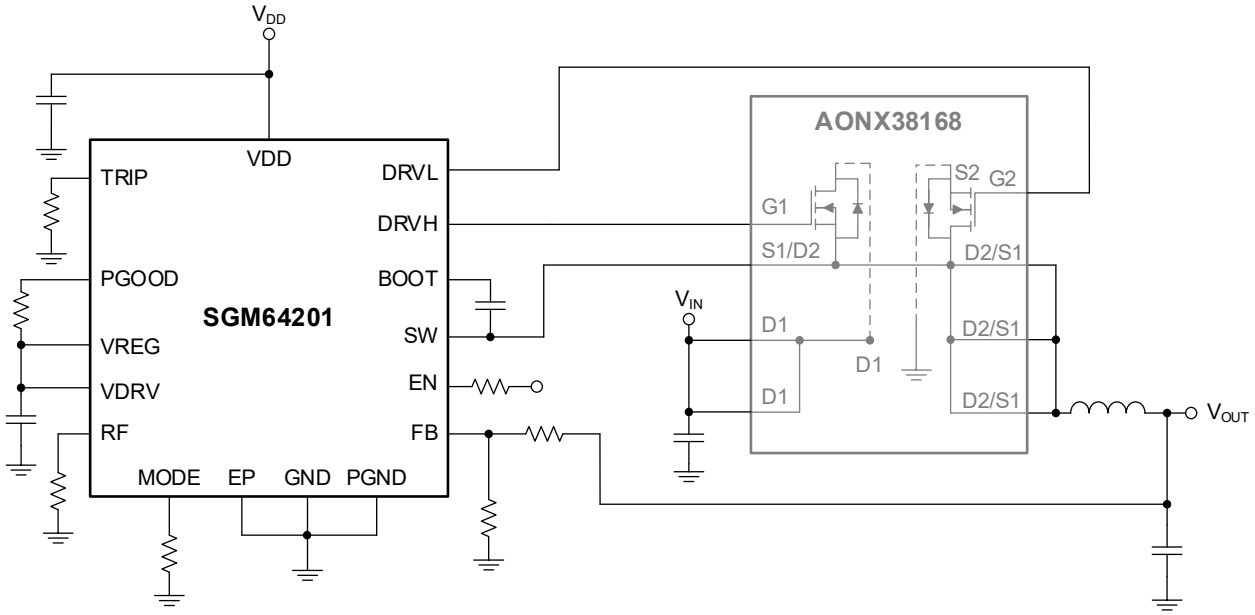


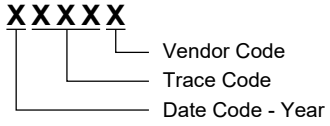
Figure 1. Simplified Schematic Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM64201	TQFN-3×3-16FL	-40℃ to +125℃	SGM64201YTUZ16G/TR	0TKUZ XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- BOOT ..... -0.3V to 34.5V
- BOOT (with Respect to the SW Terminal) ..... -0.3V to 6.5V
- VDD ..... -0.3V to 28V
- SW (DC) ..... -2V to 28V
- SW (Pulse < 20ns, E = 5μJ) ..... -6.5V
- VDRV, EN, TRIP, FB, RF, MODE ..... -0.3V to 6.5V

Output Voltage
- DRVH ..... -2V to 34.5V
- DRVH (with Respect to the SW Terminal) ..... -0.3V to 6.5V
- DRVL, VREG ..... -0.5V to 6.5V
- PGOOD ..... -0.3V to 6.5V

Package Thermal Resistance
- TQFN-3×3-16FL, θ_{JA} ..... 62.7℃/W
- TQFN-3×3-16FL, θ_{JB} ..... 30.8℃/W
- TQFN-3×3-16FL, $\theta_{JC(TOP)}$ ..... 51℃/W
- TQFN-3×3-16FL, $\theta_{JC(BOT)}$ ..... 5.8℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage
BOOT ..... -0.1V to 31V
BOOT (with Respect to the SW Terminal) ..... -0.1V to 5V
VDD ..... 4.5V to 25V
SW ..... -1V to 26V
VDRV, EN, TRIP, FB, RF, MODE ..... -0.1V to 5V

Output Voltage
DRVH ..... -1V to 31V
DRVH (with Respect to the SW Terminal) ..... -0.1V to 5V
DRVL, VREG ..... -0.3V to 5V
PGOOD ..... -0.1V to 5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

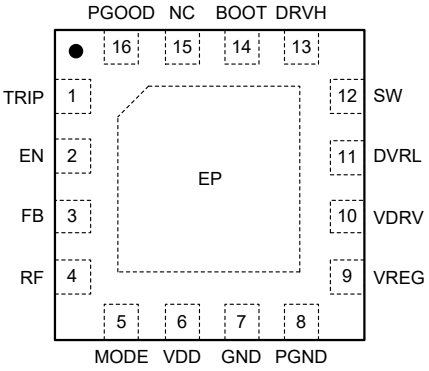
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×3-16FL

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	TRIP	I	Set Pin for Over-Current Threshold. Place a resistor from this pin to GND, $V_{TRIP} = I_{TRIP} \times R_{TRIP}$, $V_{OCL} = V_{TRIP}/8$.
2	EN	I	Active-High Enable Input Pin. Pull it up to a logic high voltage to enable, pull it down to disable the device. Place a 100kΩ resistor in series with EN pin if the source voltage is higher than 5.5V. The input UVLO level can be programmed using a resistor divider from VIN.
3	FB	I	Output Feedback Input Pin. Tap an output feedback resistor divider to this pin.
4	RF	I	Switching Frequency Setting Pin. The switching frequency can be set by an external resistor connected between RF and GND or RF and VREG.
5	MODE	I	Set Pin for Selection of FPWM mode or Power Saving Mode (PSM). For FPWM mode, place a resistor from this pin to PGOOD. For PSM, place a resistor from this pin to GND. The soft-start time varies when choosing different resistor.
6	VDD	I	4.5V to 25V Power Supply Input Pin. Place a decoupling ceramic capacitor between this pin and PGND.
7	GND	G	Analog Ground. Reference for internal analog signals and logic. Connect it to system ground.
8	PGND	G	Power Ground. Connect it to system ground, exposed pad and GND together.
9	VREG	O	Internal Bias Supply Rail. Decouple this pin to PGND with a ceramic capacitor.
10	VDRV	I	Gate Drive Supply Voltage Input. Connect it to VREG if using LDO output as gate drive supply.
11	DRVL	O	Gate Driving Output for the Low-side MOSFET (the External Synchronous N-MOSFET).
12	SW	I	Switching Node. Connect it to the switching node of the converter and act as the return of bootstrap supply, and provide a path for the high-side MOSFET high bootstrapping currents.
13	DRVH	O	Gate Driving Output for the High-side MOSFET. Drive the high-side N-MOSFET. The DRVH is powered from the bootstrap (BOOT) capacitor (returned to SW) that is a floating supply.
14	BOOT	I	Bootstrap Input. Bootstrap supply for high-side driver. Connect a 100nF ceramic capacitor between BOOT and SW pins.
15	NC	–	No Connection.
16	PGOOD	O	Open-Drain Power Good Flag Output. Connect it to suitable voltage supply through a 10kΩ resistor. High = power good, Low = power not good. Flag pulls low when EN = Low.
Exposed Pad	EP	–	Thermal Exposed Pad. It is the main thermal relief path of the die connected to the ground plane on the PCB.

NOTE: I = input, O = output, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 12V, T_J = -40℃ to +85℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current						
VDD Supply Current	I_{VDD}	VDD current, no load, V_{EN} = 5V, V_{FB} = 0.630V, V_{TRIP} = 0.5V, T_J = +25℃		380	590	μA
VDD Shutdown Current	I_{VDDSDN}	VDD current, no load, V_{EN} = 0V, T_J = +25℃			5	μA
Internal Reference Voltage						
Feedback Reference Voltage	V_{FB}	T_J = +25℃	597	600	603	mV
		T_J = -40℃ to +85℃	596	600	604	
Feedback Input Current	I_{FB}	V_{FB} = 0.630V, T_J = +25℃		0.002	0.2	μA
Output Drivers						
DRVH Resistance	R_{DRVH}	Source, I_{DRVH} = -50mA		1.5	3	Ω
		Sink, I_{DRVH} = 50mA		0.8	1.5	
DRVL Resistance	R_{DRVL}	Source, I_{DRVL} = -50mA		1	2	Ω
		Sink, I_{DRVL} = 50mA		0.6	1.2	
Dead Time	t_{DEAD}	DRVH-off to DRVL-on		18		ns
		DRVL-off to DRVH-on		22		
LDO Output						
LDO Output Voltage	V_{VREG}	0mA ≤ I_{VREG} ≤ 50mA	4.74	5.2	5.65	V
LDO Output Current (1)	I_{VREG}	Maximum current allowed from LDO			50	mA
LDO Drop Output Voltage	V_{DO}	V_{DD} = 4.5V, I_{VREG} = 50mA			500	mV
Bootstrap Switch						
Forward Voltage	V_{BOOT_F}	V_{VREG} - V_{BOOT}, I_F = 10mA		0.05	0.12	V
BOOT Leakage Current	I_{BOOT_LK}	V_{BOOT} = 22V, V_{SW} = 17V		0.01	1	μA
Duty and Frequency Control						
Minimum Off-Time	t_{OFF_MIN}		154	250	342	ns
Minimum On-Time (1)	t_{ON_MIN}	V_{IN} = 25V, V_{OUT} = 0.6V, R_{RF} = 0Ω to VREG		45		ns
Soft-Start						
Internal Soft-Start Time	t_{SS}	0V ≤ V_{OUT} ≤ 95%, R_{MODE} = 39kΩ		0.6		ms
		0V ≤ V_{OUT} ≤ 95%, R_{MODE} = 100kΩ		1.2		
		0V ≤ V_{OUT} ≤ 95%, R_{MODE} = 200kΩ		2.4		
		0V ≤ V_{OUT} ≤ 95%, R_{MODE} = 470kΩ		4.8		
Power Good						
Power Good Threshold, V_{OUT} Rising	V_{THPG}	PG becomes high, T_J = +25℃	92	96	99.8	%
Power Good Hysteresis, V_{OUT} Falling		PG becomes low, T_J = +25℃	2	4.5	7	
Power Good Threshold, V_{OUT} Falling		PG becomes high, T_J = +25℃	106.5	110.5	114.5	
Power Good Hysteresis, V_{OUT} Rising		PG becomes low, T_J = +25℃	3	6.5	8.5	
PG Transistor On-Resistance	R_{PG}		15	30	50	Ω
PG Delay after Soft-Start	t_{PG_DEL}	T_J = +25℃	0.6	1	1.3	ms
Logic Threshold and Setting Conditions						
EN Input Level Required to Start Switching	V_{EN_H}		1.1	1.2	1.3	V
EN Input Level Required to Stop Switching	V_{EN_L}		1	1.1	1.2	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 12V, T_J = -40℃ to +85℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EN Input Level Required to Turn on Internal LDO	$V_{EN-VREG\_H}$			0.7	0.85	1	V
EN Input Level Required to Turn off Internal LDO	$V_{EN-VREG\_L}$			0.6	0.75	0.9	V
EN Input Current	I_{EN}	V_{EN} = 5V				1	μA
Switching Frequency (2)	f_{SW}	T_J = +25℃	R_{RF} = 0Ω to GND	230	280	330	kHz
			R_{RF} = 187kΩ to GND	280	330	380	
			R_{RF} = 619kΩ to GND	370	420	470	
			R_{RF} = Open	450	500	550	
			R_{RF} = 866kΩ to VREG	540	650	760	
			R_{RF} = 309kΩ to VREG	580	720	860	
			R_{RF} = 124kΩ to VREG	620	800	980	
			R_{RF} = 0Ω to VREG	655	875	1095	
V_O Discharge							
V_O Discharge Current	I_{DISCHG}	V_{EN} = 0V, V_{SW} = 0.5V, V_{VREG} = 5V		8	13.4		mA
Protection: Current Sense							
TRIP Source Current	I_{TRIP}	V_{TRIP} = 1V, T_J = +25℃		9	10	11	μA
TRIP Current Temp. Coef. (1)	TC_{ITRIP}	T_J = +25℃			4700		ppm/°C
Current Limit Threshold Setting Range	V_{TRIP}	V_{TRIP} - GND voltage		0.2		3	V
Current Limit Threshold	V_{OCL}	V_{TRIP} = 3V		300	360	420	mV
		V_{TRIP} = 1.6V		160	195	230	
		V_{TRIP} = 0.2V		17	25	33	
Negative Current Limit Threshold	V_{OCLN}	V_{TRIP} = 3V		-420	-360	-300	mV
		V_{TRIP} = 1.6V		-230	-195	-160	
		V_{TRIP} = 0.2V		-42	-25	-7	
Auto Zero Cross Adjustable Range	V_{AZC_ADJ}	Positive, T_J = +25℃		1.5	6.5		mV
		Negative, T_J = +25℃			-6.5	-1.5	
Protection: UVP and OVP							
OVP Trip Threshold Voltage	V_{OVP}	OVP detect		115	121	127	%
OVP Propagation Delay Time (1)	t_{OVP_DEL}	FB delay with 50mV overdrive			1		μs
Output UVP Trip Threshold Voltage	V_{UVP}	UVP detect		65	70	75	%
Output UVP Propagation Delay Time	t_{UVP_DEL}	T_J = +25℃		0.6	1	1.3	ms
Output UVP Enable Delay Time	t_{UVP_EN}	From EN to UVP workable, R_{MODE} = 39kΩ		1.5	2.6	3.7	ms
UVLO							
VREG UVLO Threshold	V_{UVVREG}	Wake up		3.65	4.1	4.5	V
		Hysteresis			0.2		
Thermal Shutdown							
Thermal Shutdown Threshold (1)	T_{SDN}	Shutdown temperature			140		℃
		Hysteresis			10		

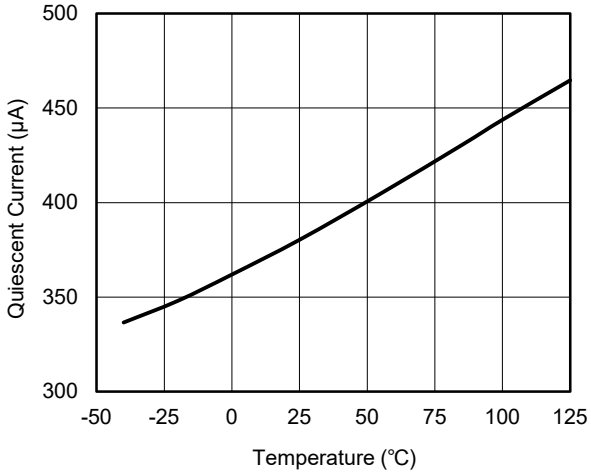
NOTES:

1. Ensured by design. Not production tested.
2. Not production tested. Test conditions are V_{IN} = 12V, V_{OUT} = 1.35V, I_{OUT} = 10A and using the application circuit.

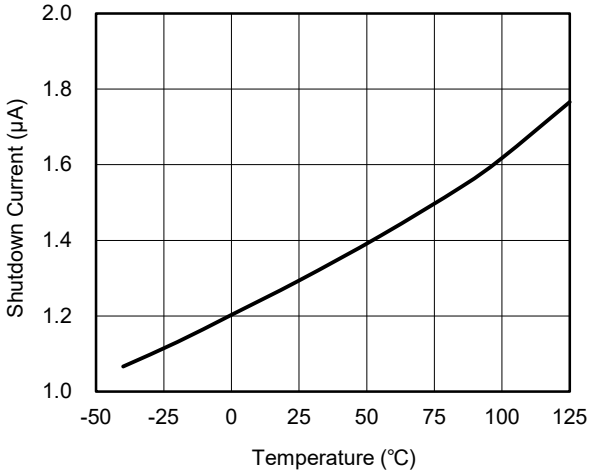
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.35V, f_{SW} = 500kHz , L = 0.44μH and C_{OUT} = 100μF × 4, unless otherwise noted.

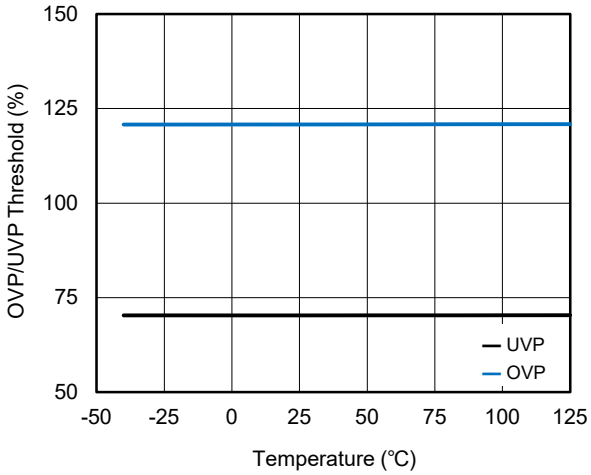
Quiescent Current vs. Temperature



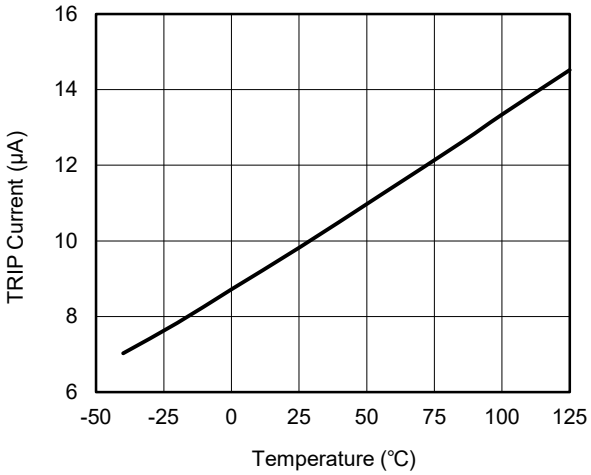
Shutdown Current vs. Temperature



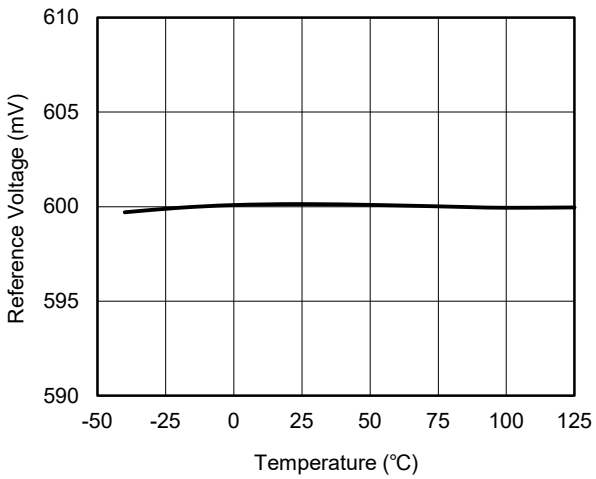
OVP/UVP Threshold vs. Temperature



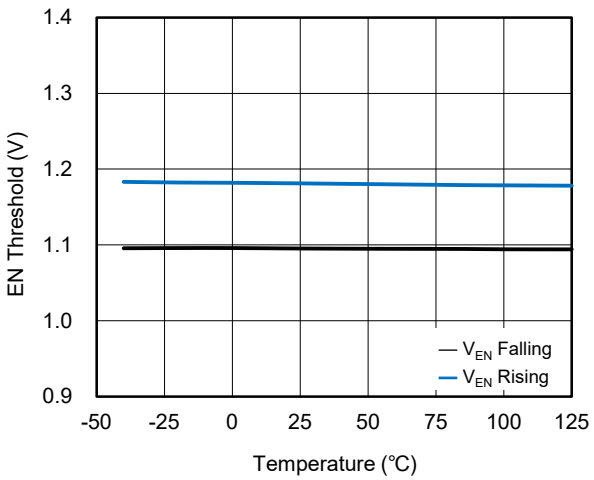
TRIP Current vs. Temperature



Reference Voltage vs. Temperature



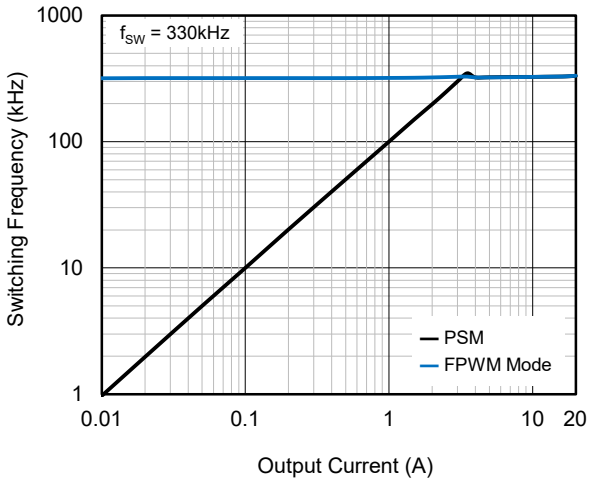
EN Threshold vs. Temperature



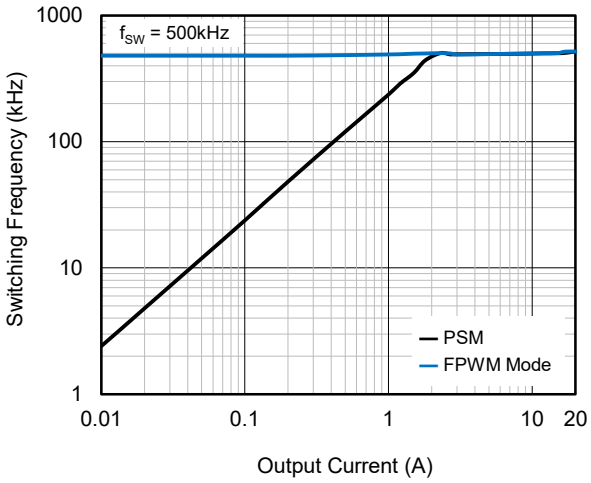
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.35V, f_{SW} = 500kHz , L = 0.44μH and C_{OUT} = 100μF × 4, unless otherwise noted.

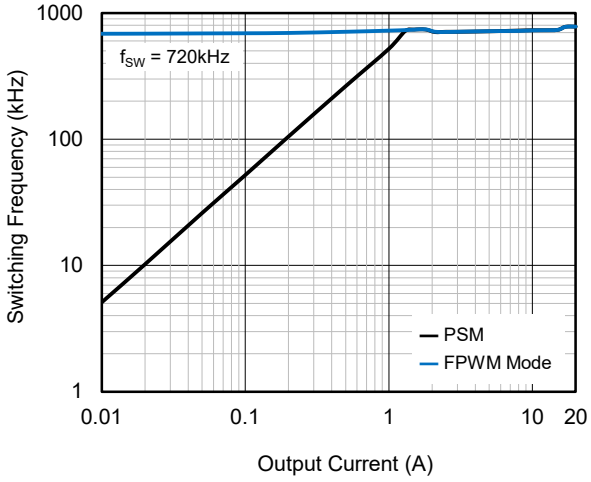
Switching Frequency vs. Output Current



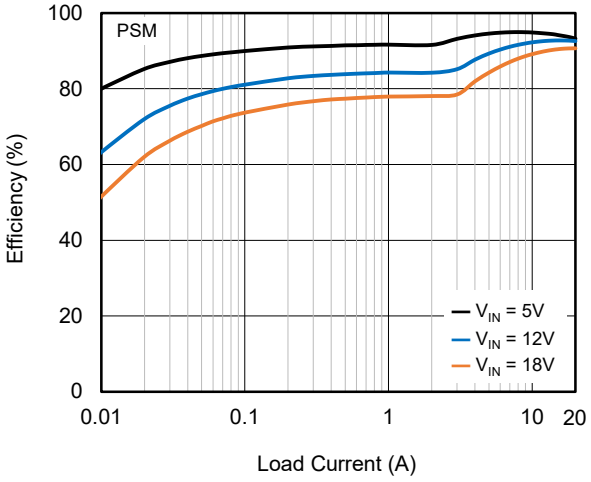
Switching Frequency vs. Output Current



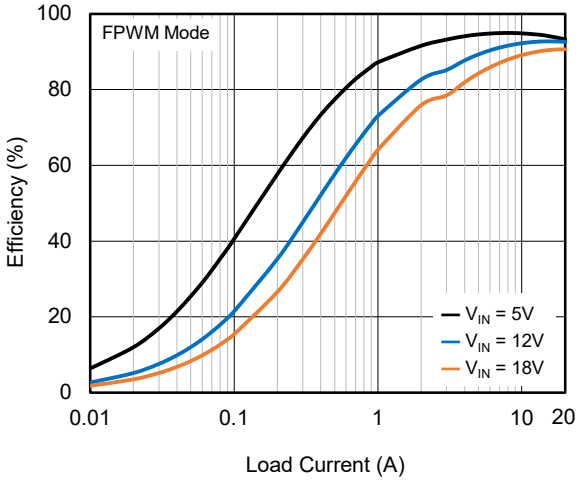
Switching Frequency vs. Output Current



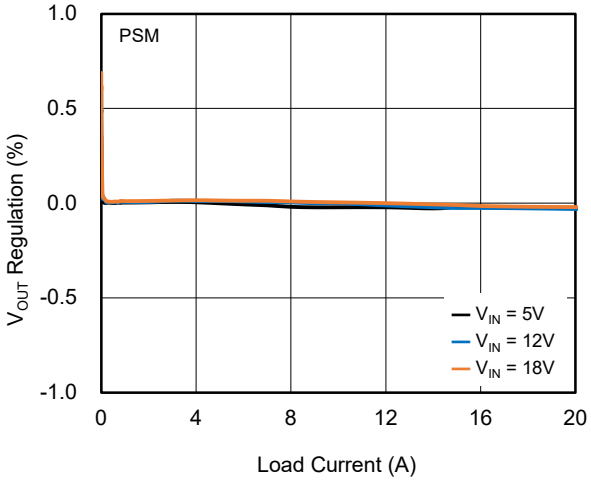
Efficiency vs. Load Current



Efficiency vs. Load Current



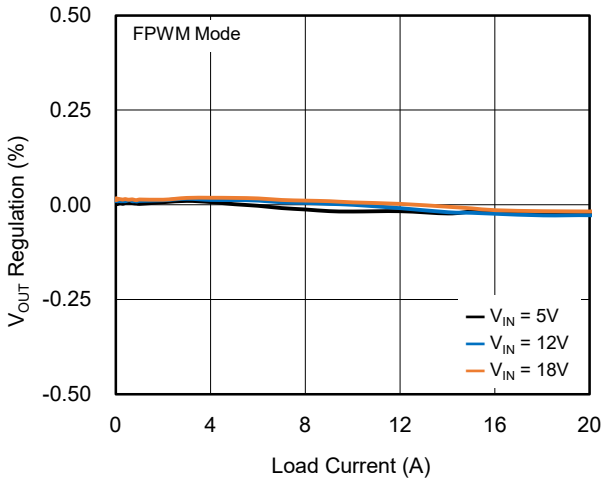
VOUT Regulation vs. Load Current



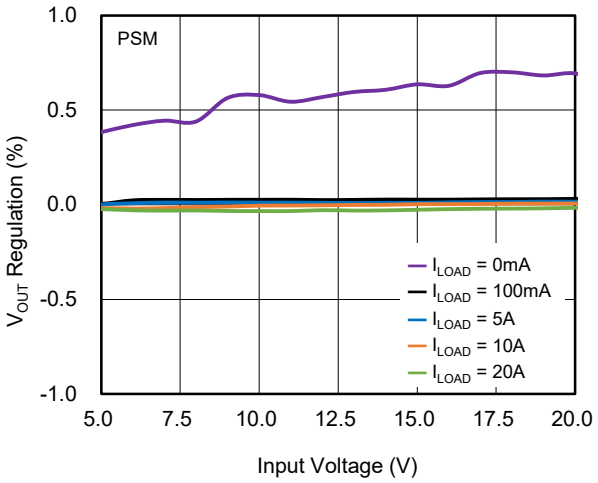
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.35V, f_{SW} = 500kHz , L = 0.44μH and C_{OUT} = 100μF × 4, unless otherwise noted.

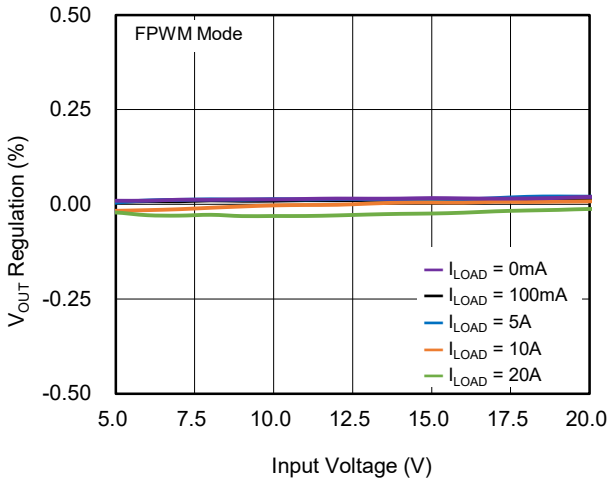
V_{OUT} Regulation vs. Load Current



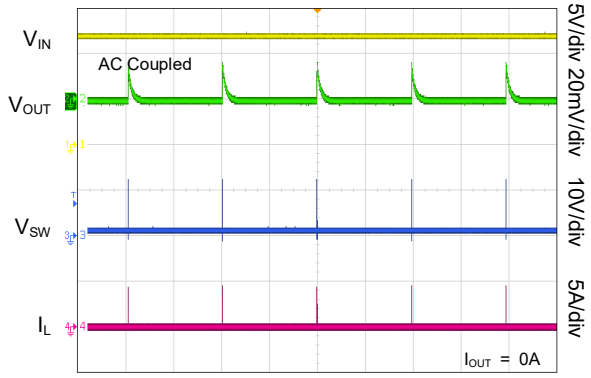
V_{OUT} Regulation vs. Input Voltage



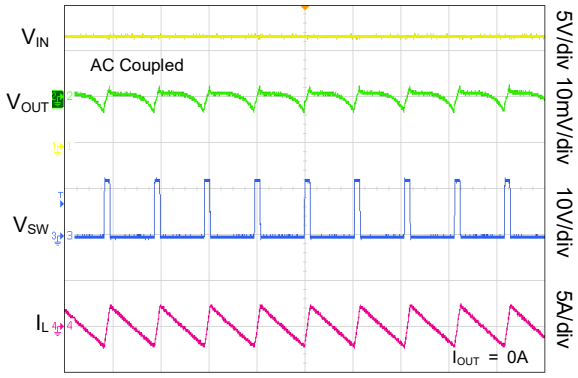
V_{OUT} Regulation vs. Input Voltage



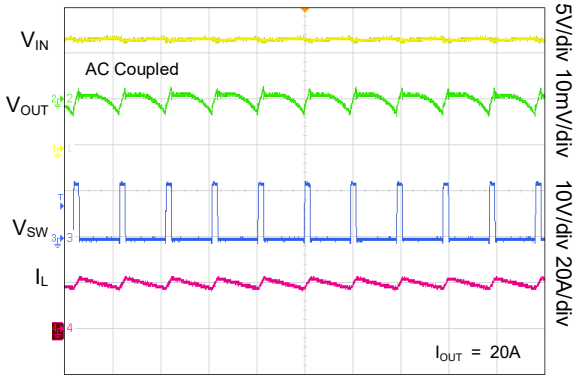
Output Voltage Ripple (PSM)



Output Voltage Ripple (FPWM Mode)



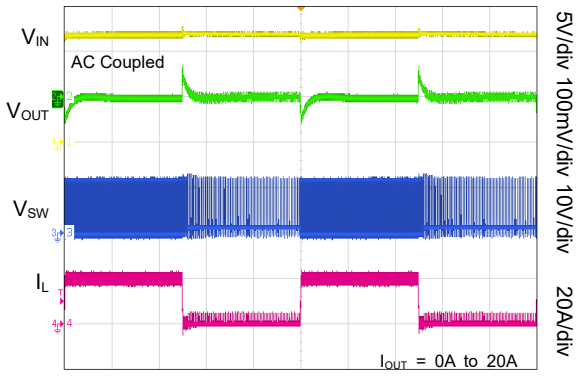
Output Voltage Ripple



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

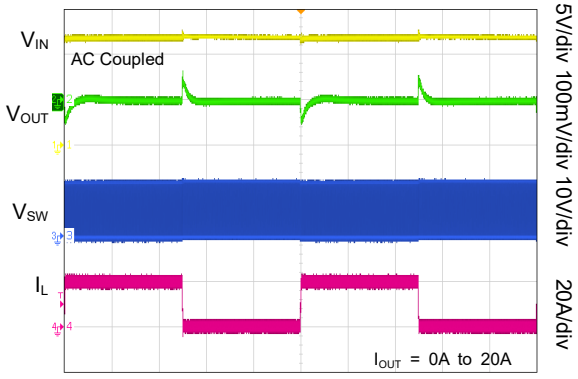
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.35V, f_{SW} = 500kHz , L = 0.44μH and C_{OUT} = 100μF × 4, unless otherwise noted.

Load Transient (PSM)



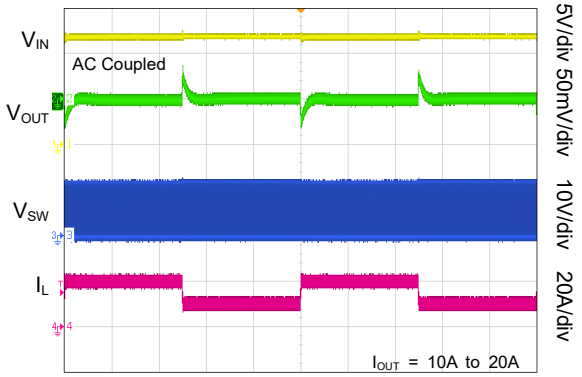
Time (1ms/div)

Load Transient (FPWM Mode)



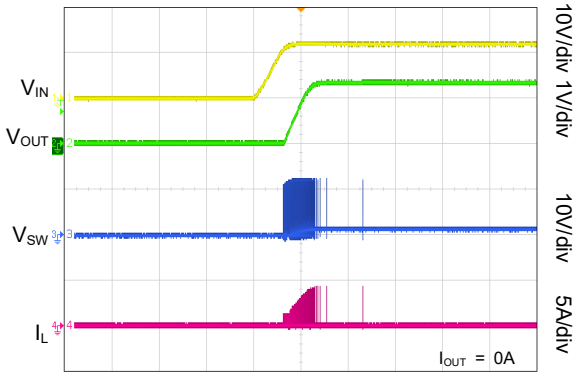
Time (1ms/div)

Load Transient



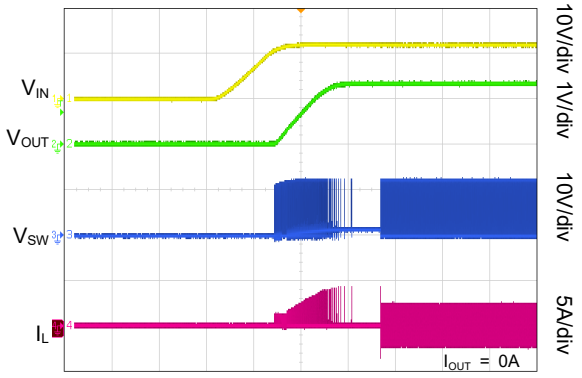
Time (1ms/div)

Startup by V_{IN} (PSM)



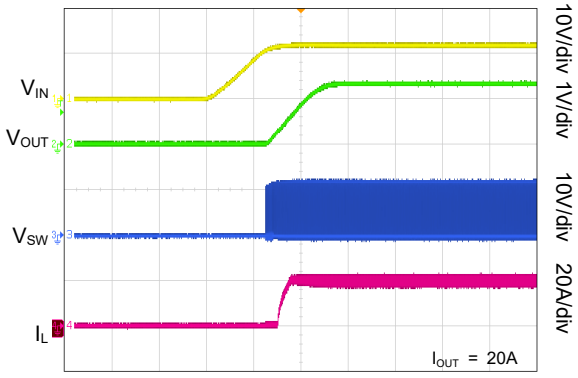
Time (2ms/div)

Startup by V_{IN} (FPWM Mode)



Time (1ms/div)

Startup by V_{IN}

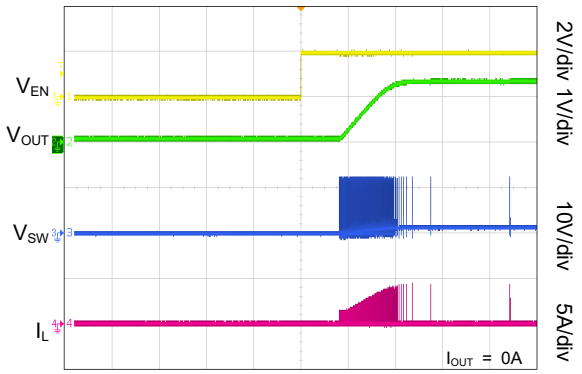


Time (1ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

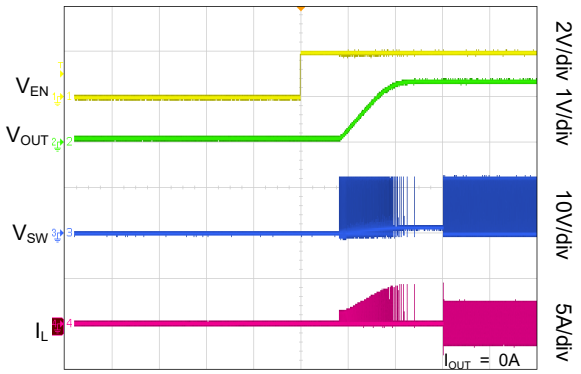
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.35V, f_{SW} = 500kHz , L = 0.44μH and C_{OUT} = 100μF × 4, unless otherwise noted.

Startup by EN (PSM)



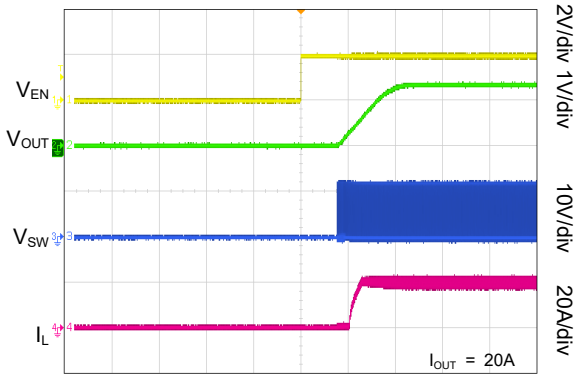
Time (1ms/div)

Startup by EN (FPWM Mode)



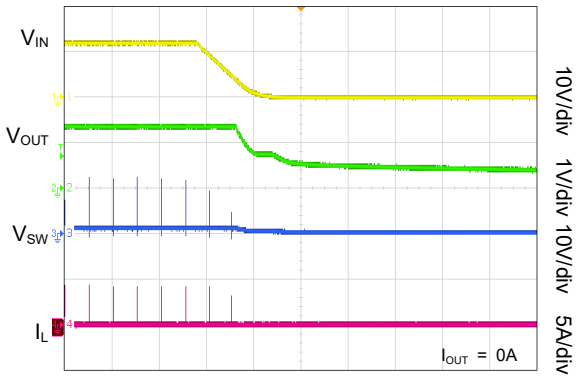
Time (1ms/div)

Startup by EN



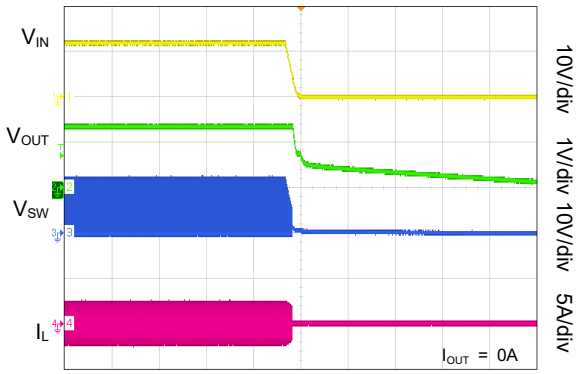
Time (1ms/div)

Shutdown by V_{IN} (PSM)



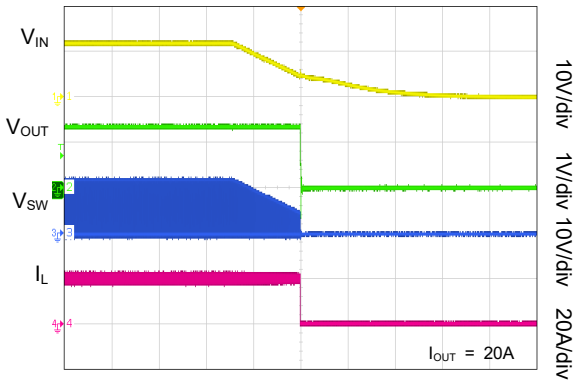
Time (20ms/div)

Shutdown by V_{IN} (FPWM Mode)



Time (5ms/div)

Shutdown by V_{IN}

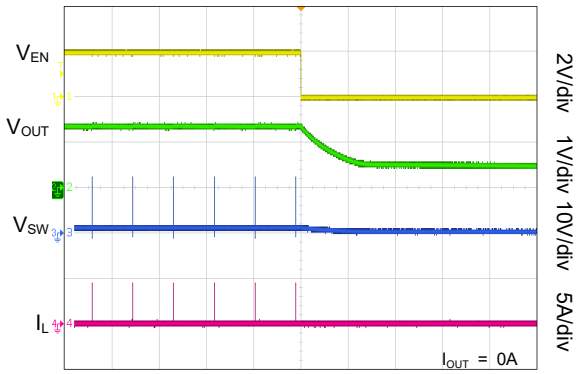


Time (5ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

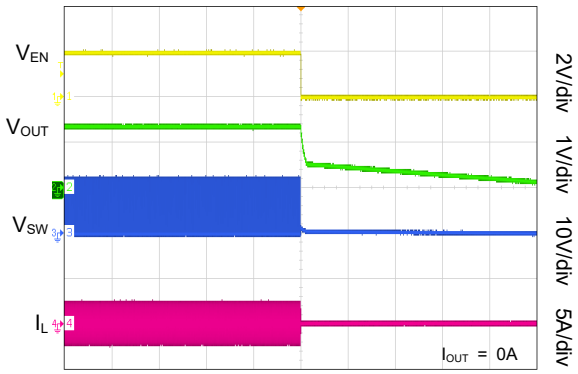
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.35V, f_{SW} = 500kHz , L = 0.44μH and C_{OUT} = 100μF × 4, unless otherwise noted.

Shutdown by EN (PSM)



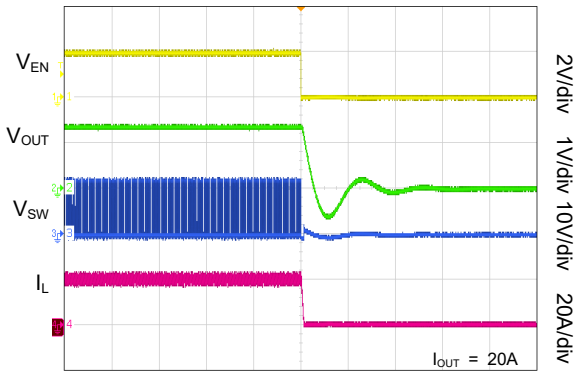
Time (10ms/div)

Shutdown by EN (FPWM Mode)



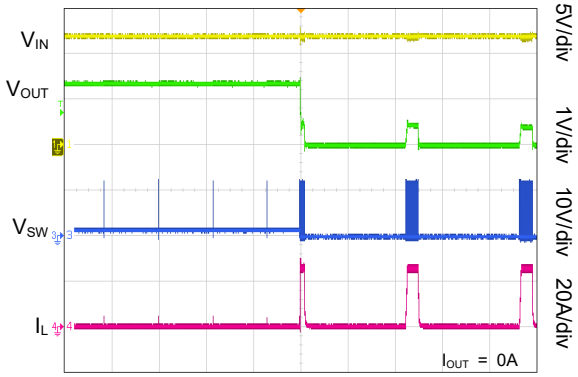
Time (100ms/div)

Shutdown by EN



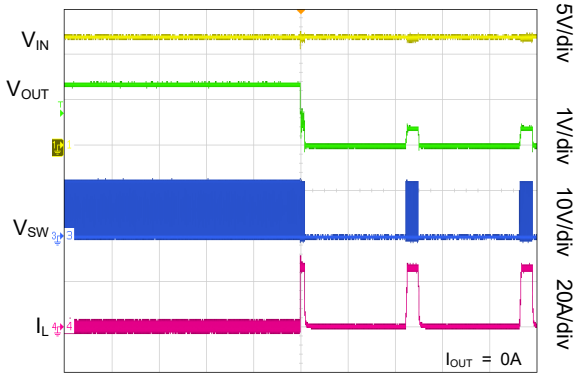
Time (100μs/div)

Short-Circuit Entry (PSM)



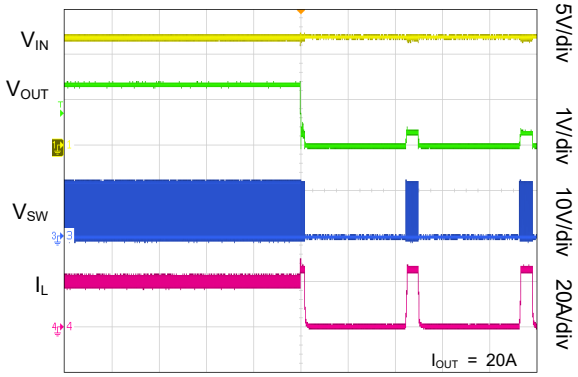
Time (10ms/div)

Short-Circuit Entry (FPWM Mode)



Time (10ms/div)

Short-Circuit Entry

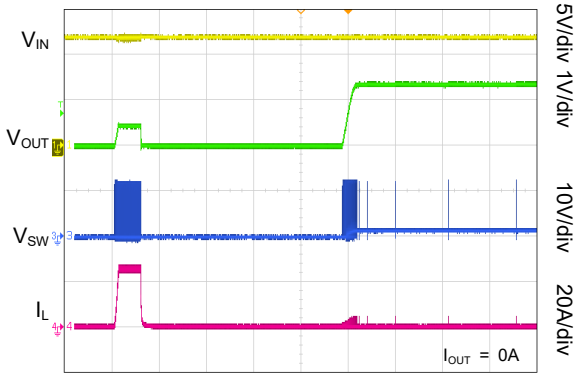


Time (10ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

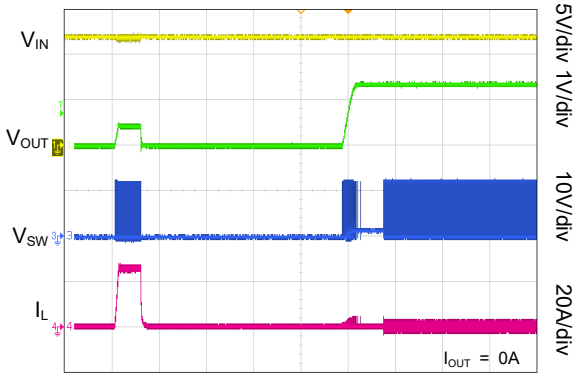
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.35V, f_{SW} = 500kHz , L = 0.44μH and C_{OUT} = 100μF × 4, unless otherwise noted.

Short-Circuit Recovery (PSM)



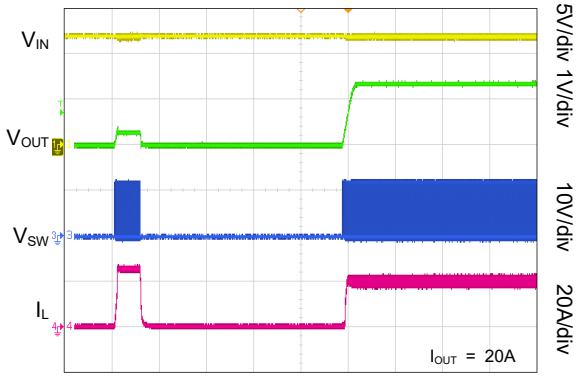
Time (5ms/div)

Short-Circuit Recovery (FPWM Mode)



Time (5ms/div)

Short-Circuit Recovery



Time (5ms/div)

FUNCTIONAL BLOCK DIAGRAM

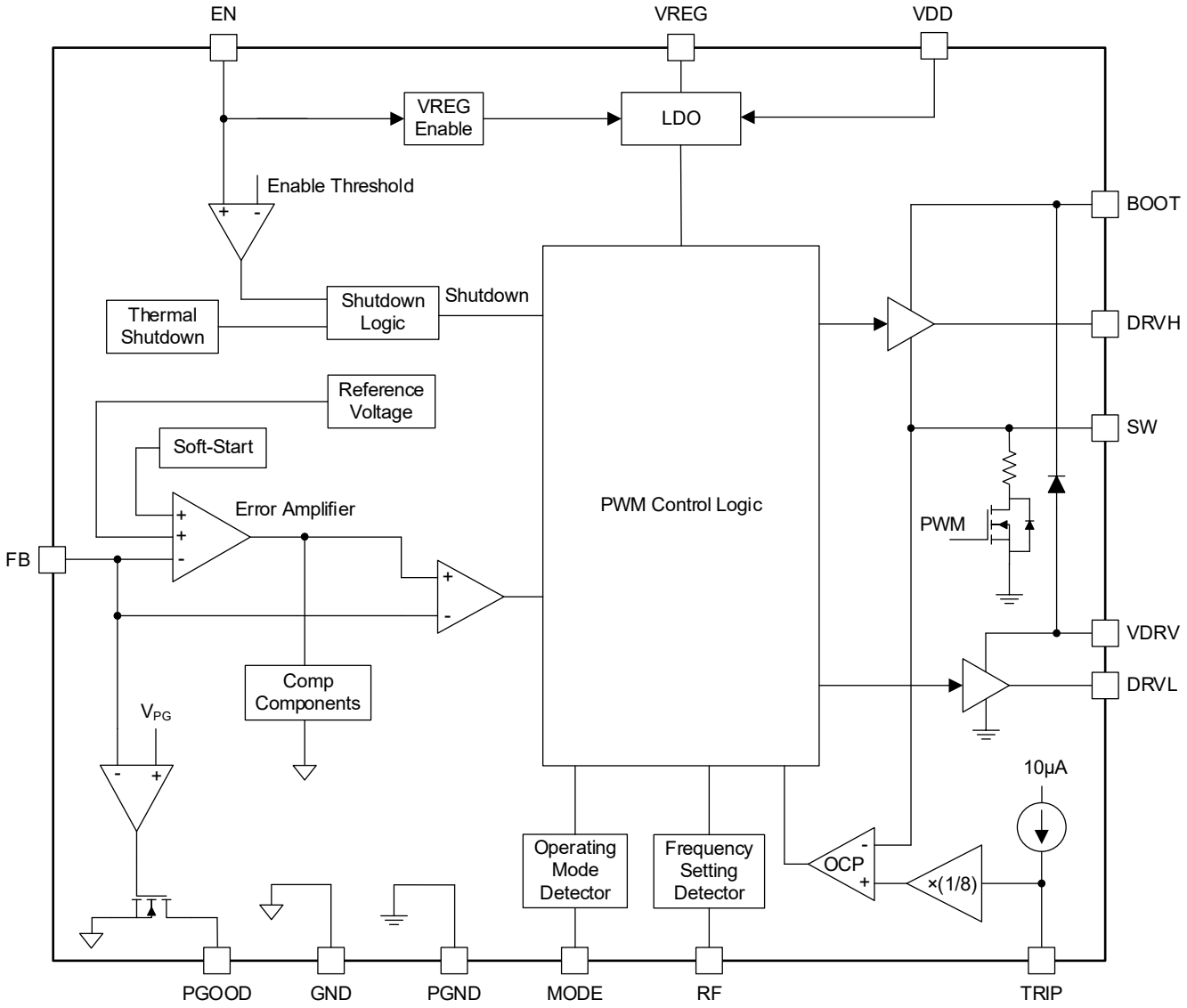


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM64201 is a 4.5V to 25V wide input controller with adaptive constant on-time (ACOT) control for synchronous Buck converters. The SGM64201 can provide adjustable output voltage in range of 0.6V to 5.5V. It is capable to driver external N-MOSFET efficiently with the conversion input voltage from 3V to 26V.

Eight preset switching frequency values from 280kHz to 875kHz can be selected through a resistor connected from the RF pin to ground or RF pin to VREG. The switching frequency is determined before soft-start and ACOT control can dynamically adjust the on-time duration based on the input and output voltage, achieving a relatively constant frequency during steady-state operation.

The SGM64201 features a MODE pin. At light load, power saving mode (PSM) can be selected to improve the efficiency by connecting a resistor from MODE pin to ground, or forced pulse width modulation (FPWM) mode can be selected to decrease the output ripple by connecting a resistor from MODE pin to a voltage higher than 1.3V. SGMICRO recommends to connect the MODE pin to the PGOOD pin if FPWM mode is desired. Additionally, the MODE pin facilitates the selection of four preset soft time between 0.6ms, 1.2ms, 2.4ms and 4.8ms when using different resistor.

Cycle-by-cycle over-current limiting control is integrated in SGM64201, and over-current threshold is configured using a resistor connect from TRIP pin to ground.

UVLO Protection

The under-voltage lockout protection (UVLO) is necessary to avoid device malfunction due to insufficient supply voltage. The SGM64201 incorporates VREG UVLO as a safety mechanism. Whenever the VREG voltage drops below 3.9V, the device automatically shuts down to prevent damage. Conversely, when the VREG voltage exceeds 4.1V, a new startup sequence begins seamlessly.

Enable and Soft-Start

The EN pin can be used to turn the device on and off or to change the UVLO thresholds. The device is enabled if the EN pin voltage exceeds the enable threshold and VREG exceeds 4.1V. The device is disabled if the EN voltage is externally pulled low or the VREG pin voltage falls below 3.9V. The EN pin cannot be left floating and can be connected to V_{IN} to enable the device. A resistor large than 100kΩ is needed if EN voltage is higher than 5.5V.

The startup sequence initiates when the voltage of EN pin rises above the enable threshold voltage. The internal LDO regulator startup after a deglitch time and regulates VREG to 4.6V first. After VREG is ready, the controller then uses the next calibrate time to determine the operation mode, soft-start (SS) time through resistor attached to the MODE pin and switching frequency through resistor attached to the RF pin. This information is encoded in internal registers, remaining unchanged until a new startup sequence begins.

During the second phase, an internal ramp voltage begins to rise from 0V to 0.6V with a ramp time varies from 0.6ms to 4.8ms, depending on the MODE pin resistor. The soft-start is needed to avoid high inrush currents caused by rapid increase of output voltage across output capacitors and the load.

Table 1. Soft-Start and MODE

Mode Selection	Action	Soft-Start Time (ms)	R_{MODE} (kΩ)
PSM	Pull MODE pin down to GND	0.6	39
		1.2	100
		2.4	200
		4.8	470
FPWM	Connect MODE pin to PGOOD	0.6	39
		1.2	100
		2.4	200
		4.8	470

Adaptive Constant On-Time Control and Frequency Selection

The adaptive constant on-time (ACOT) control differs from voltage mode control (VMC) or current mode control (CMC) in that it operates without clock signal and instead uses hysteretic mode control. At the start of each switching cycle, the ACOT control generates a relatively constant on-time pulse when the internal comparator detects that the output voltage has dropped below the desired level. The feedback (FB) pin senses the output voltage through a resistor divider and compares it to the internal reference voltage (V_{REF}) using an error amplifier. The amplifier output is then sent to a comparator.

DETAILED DESCRIPTION (continued)

When the feedback voltage (V_{FB}) falls below the amplifier output, the on-time control logic is triggered which turns on the high-side MOSFET. ACOT control can dynamically adjust the on-time duration based on the input and output voltage ($t_{on} \propto V_{OUT}/V_{IN}$), achieving a relatively constant frequency during steady-state operation over a wide input voltage range.

Eight preset switching frequency range of 280kHz to 875kHz is programmed by a resistor connected between the RF pin and GND or VREG pin. Please refer to Table 2. The switching frequency is default 500kHz if the RF pin is left open.

Table 2. Resistor and Switching Frequency

Resistor (R_{RF}) Connections	Switching Frequency (kHz)
0Ω to GND	280
187kΩ to GND	330
619kΩ to GND	420
Open	500
866kΩ to VREG	650
309kΩ to VREG	720
124kΩ to VREG	800
0Ω to VREG	875

Light Load Condition with Power Saving Mode (PSM)

SGM64201 operates in power saving mode (PSM) with light loads when the MODE pin is pulled low through R_{MODE} in which internal power dissipation is significantly reduced. Moreover, the operating frequency starts to drop depending on the load.

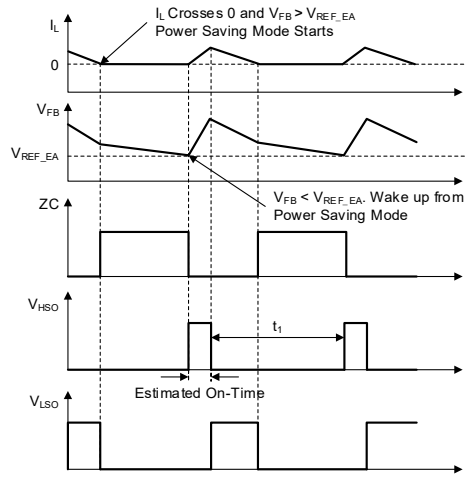


Figure 3. Power Saving Mode (PSM) in DCM

The details are explained in Figure 3 that shows the timings of the ACOT control in discontinuous conduction mode (DCM). Inductor current (I_L) is monitored with a zero-crossing detector and when I_L crosses the zero and $V_{FB} > V_{REF\_EA}$ (the output of the error amplifier), both high-side and low-side MOSFETs are turned off. They will not turn on again until the V_{FB} falls below V_{REF_EA} and triggers a new on-time pulse. During this off-time period, the load is supplied by the output capacitor stored energy.

Light Load Condition with Forced Pulse Width Modulation (FPWM) Mode

The SGM64201 is locked in continuous current mode from full load to no load when the MODE pin is pulled high to PGOOD through a resistor. Negative inductor currents are allowed at light load to keep continuous inductor current operation. It is a tradeoff that sacrifices light load efficiency in order to keep switching frequency relatively fixed, achieve lower output ripple, and ensure better output regulation.

Ramp Signal

The SGM64201 enhances jitter performance by incorporating a ramp signal into V_{REF}. According to the ACOT, the feedback voltage (V_{FB}) is continuously compared with the output of error amplifier, ensuring that the output voltage remains regulated. By incorporating a slight ramp signal into the reference, the relative slope rate of V_{FB} is significantly improved, thereby reducing jitter and promoting operational stability.

Output Voltage Programming

The output voltage is set by a resistor divider between V_{OUT} and GND that is tapped to the FB pin. It is recommended to use 1% or higher quality resistors with low thermal tolerance for an accurate and thermally stable output voltage.

Use Equation 1 to calculate the output voltage. Lower divider resistor values increase loss and reduce light load efficiency. Consider larger resistors to improve efficiency at light load. Note that if R_1 is too high (> 1MΩ), the FB pin leakage current and other noises can easily affect the accuracy and performance of the regulator.

$$V_{OUT} = V_{REF} \times \left(\frac{R_1 + R_2}{R_2} \right) \quad (1)$$

DETAILED DESCRIPTION (continued)

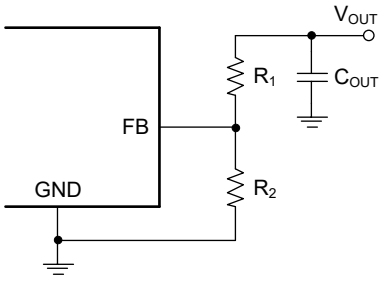


Figure 4. Adjustable Output Voltage

Adaptive Zero Crossing Detection

The SGM64201 features an adaptive zero-crossing circuit that optimizes the detection of zero inductor current during PSM operation at light load.

Based on the voltage of switching node when the low-side MOSFET is turned off, the threshold current for the zero-crossing circuit detection in the next cycle is adaptively adjusted to achieve the ideal turn off time for the low-side MOSFET, resulting in higher light load efficiency and better electromagnetic interference (EMI) performance.

Output Discharge Control

When EN is low, the SGM64201 utilizes an internal MOSFET connected between the SW pin and the PGND pin to discharge the output capacitor stored energy, while ensuring that both the high-side and low-side MOSFETs remain in the OFF state. The typical discharge resistance is 40Ω. The internal MOSFET turns off and the discharge function is disabled once VREG becomes low.

Floating Driver and Bootstrap Charging

The low-side driver is specifically crafted to efficiently power high-current, low on-resistance N-channel MOSFET. The driving voltage VDRV can be supplied either from 5.2V VREG power source or an external source ranging from 4.5V to 6V.

The high-side driver is specifically crafted to efficiently power high-current, low on-resistance N-channel MOSFET. To power the high-side MOSFET gate driver, a voltage higher than V_{IN} is needed. Bootstrap technique is used to provide this voltage from the switching node by using a 0.1μF bootstrap capacitor (C_{BOOT}) between SW and BOOT pins along with an internal bootstrap diode. An X5R or X7R ceramic capacitor is recommended for C_{BOOT} to have stable capacitance against temperature and voltage variations. C_{BOOT} is normally charged by VDRV when the high-side MOSFET turns off.

Power Good

The SGM64201 features a power-good (PG) pin that indicates whether the output voltage is at the desired level. This pin is an open-drain output that requires a resistor of 10kΩ pulled up to a DC voltage. Figure 5 illustrates that when the FB voltage is within the power-good range, the PG switch is turned off, and the PG pin is pulled up to high after 1ms internal delay. Conversely, when the FB voltage is outside the power-good range, the PG switch is turned on, and the PG pin is pulled down to low after 2μs internal delay. When EN is pulled low, the flag output will also be forced low.

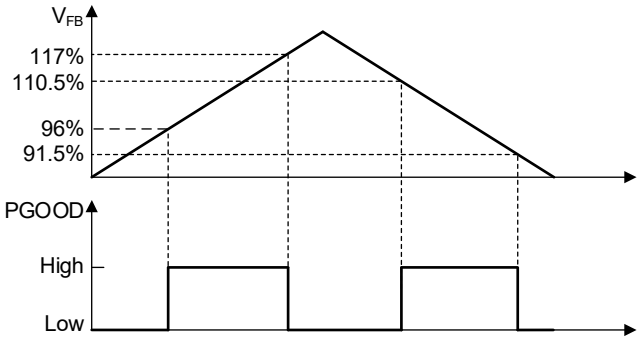


Figure 5. Power-Good Flag

Current Sense and Over-Current Protection

The SGM64201 supports overload mode. When the output current continues overload while the system is powered up, the SGM64201 exports the maximum power and limits the maximum valley current of the low-side MOSFET. The device keeps in cycle-by-cycle limit to meet the system's power request. The SGM64201 does not shut down until the device heats and then goes to thermal shutdown. As the load increases continuously, the output voltage decreases. If the FB pin voltage drops to 70% of V_{REF} for 1ms delay, the hiccup current-protection mode will be activated. In hiccup mode, the regulator is shut down and kept off for 16ms (with 0.6ms soft-start configuration) typically before the SGM64201 tries to start again. If over-current or a short-circuit fault condition still exists, the hiccup mode will repeat until the fault condition is removed. Hiccup mode can help to reduce power dissipation and prevent overheating and potential damage to the device.

DETAILED DESCRIPTION (continued)

The over-current threshold can be adjusted by the voltage of TRIP pin. V_{TRIP} is programmed by a resistor R_{TRIP} connected from TRIP pin to GND. The V_{TRIP} can be calculated from Equation 2:

$$V_{TRIP}(mV) = R_{TRIP}(k\Omega) \times I_{TRIP}(\mu A) \quad (2)$$

Where:

I_{TRIP} is 10μA typically at room temperature.

V_{TRIP} sets the valley level of the inductor current. Use Equation 3 to calculate the over-current threshold.

$$I_{OCP} = \frac{V_{TRIP}}{8 \times R_{DSON\_LS}} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times V_{IN} \times f_{SW}} \quad (3)$$

Where:

R_{DSON_LS} is low-side MOSFET on-resistance at room temperature.

When FPWM is chosen, to avoid fatal negative current in the low-side MOSFET, the negative current limit (NCL) is limited as the same absolute value as positive I_{OCP}, but with a negative polarity.

Under-Voltage and Over-Voltage Protection

The output voltage is monitored through FB pin voltage. If soft-start is ready and the FB voltage drops to 70% of V_{REF}, hiccup current-protection mode is activated after 1ms UVP delay. In hiccup mode, the regulator is shut down and kept off for 16ms (with 0.6ms soft-start configuration) typically before the SGM64201 tries to start again.

An over-voltage protection is included in the device to minimize the output voltage overshoots that may occur after recovery from an output fault or a large unloading transient. The FB pin voltage is compared with the OVP thresholds. If the V_{FB} exceeds 121% of the V_{REF}, the high-side MOSFET driver is forced to turn off, and the low-side MOSFET driver is turned on until negative current limit is triggered. The output voltage decreases. The device enters hiccup mode and high-side and low-side MOSFETs driver will be OFF if FB voltage drops to 70% of V_{REF}.

Thermal Shutdown

The SGM64201 monitors junction temperature and will stop switching if it becomes too high. If the junction temperature exceeds +140℃ (TYP), the device is forced to stop switching. It will recover automatically when T_J the junction temperature decreases by approximately 10℃.

Ripple Injection

The SGM64201 is an ACOT control device in which the PWM timing is based on the output voltage ripple feedback to the FB pin. As explained before, every time the V_{FB} voltage falls below the amplifier output voltage, the high-side MOSFET is turned on and the inductor current starts to rise. High-side MOSFET is kept on for a constant on-time. At the end of on-time, the high-side MOSFET is turned off and after a very short dead-time, the low-side MOSFET is turned on (off-time) and current in the inductor starts to decrease. The next on-time and current rise in the inductor start when the V_{FB} falls below the amplifier output voltage threshold again. Therefore, in ACOT control the ripple initiates each cycle and there is no clock signal for switching.

The required V_{FB} peak-to-peak ripple range for stable PWM operation is at least 20mV. At high output voltage applications (typically V_{OUT} > 5V), the natural output ripple is usually large enough for proper PWM operation because the output filter is usually designed such that the output ripple magnitude is roughly 1% to 2% of the output voltage. However, in some design conditions like low output voltage applications, such as a 1V, the output voltage ripple is usually low (e.g. 10mV) and it will not be possible to get enough in phase ripple on the FB pin without a new strategy.

In fact, the ripple feedback is even lower than output ripple due to the voltage divider. If the FB ripple is small, the internal amplifier and comparator are not able to sense that and the control will be lost. In such condition, the output voltage is either not regulated or has large ripple due to missing or wrong multiple pulses. With the low ESR output capacitors such as ceramic ones, the ripple is also small. Therefore ripple injection methods are proposed for low output ripple applications to avoid instability.

Remember that naturally, the output ripple (ΔV_{OUT}) has two main components. One is in phase with inductor ripple and is produced by the inductor AC current going through the output capacitors (V_{rr} = ESR × ΔI_L), and the other one that has a lag phase is due to the charge and discharge of capacitor by ΔI_L current in each cycle (estimated by $V_{cr} \approx \Delta I_L / 8 f_{SW} C_{OUT}$).

DETAILED DESCRIPTION (continued)

The output capacitor C_{OUT} is usually designed large enough to filter switching ripples such that ΔV_{OUT} and output peak transients in response to load changes, remain within the acceptable range in the application. Too large output capacitor may result in startup issues.

Three main cases can be classified based on the amount of peak-to-peak feedback ripple (ΔV_{FB}) and the ripple injection technique used for ACOT converters.

Case 1: If the output capacitor has large ESR, the output ripple at the FB pin is mainly due to the ESR that carries the inductor current ripple (see Figure 6). If the output voltage is small (R_2 is large compared to R_1) the ripples seen by FB pin are large enough and with proper phase. In this case converter has a stable operation without any ripple injection. The stability criterion is:

$$ESR \times C_{OUT} > \frac{t_{ON}}{2} \quad (4)$$

The feedback voltage ripple is given by Equation 5:

$$\Delta V_{FB} \approx \frac{R_2}{R_1 + R_2} \times ESR \times \Delta I_L \quad (5)$$

where:
ΔI_L = peak-to-peak value of the inductor current ripple.

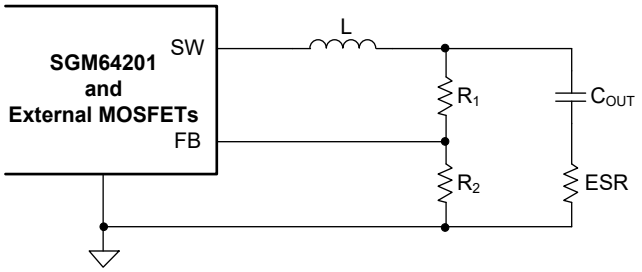


Figure 6. Feedback Circuit when Enough Ripple at FB Pin

Case 2: In this case, the in-phase ripple of the output is large enough, but it is weakened by the resistor divider. As shown in Figure 7, a small feed-forward capacitor (C_{FF}), across the upper resistor (R_1) bypasses the resistor divider at the ripple frequency (f_{SW}) and the ripple seen on the FB pin is essentially the same as the output voltage ripple (not weakened by the divider). The other advantage of using C_{FF} is the improvement of the converter transient response, because feeding back the actual over/under-voltage transients of the output with no weakening helps a quicker reaction and faster response to transients. In fact, it is sometimes used for applications like Case 1 for better transient response. However, the drawback of C_{FF} is that it may worsen the regulation of the converter output. The time constant seen by C_{FF} should be much longer than switching period, and Equation 6 defines the minimum feed-forward capacitance, C_{FF}.

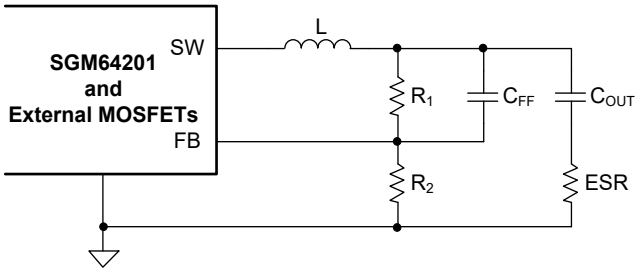


Figure 7. Use of Feed-Forward Capacitor when Inadequate Ripple at FB Pin

With the feed-forward capacitor, the feedback voltage ripple is very close to the output voltage ripple, giving in Equation 7.

$$C_{FF} > \frac{1}{2 \times \pi \times f_{SW} \times (R_1 \,||\, R_2)} \quad (6)$$

$$\Delta V_{FB} \approx ESR \times \Delta I_L \quad (7)$$

Case 3: In modern designs, ceramic capacitors are extensively used due to their small size and good stability. Due to very low ESR of the output capacitors, there is virtually no ripple at the FB pin. This is usually more critical at low output voltage in which lower output ripple is required. Therefore, additional ripple (in phase with inductor current) needs to be injected artificially into the FB pin to keep stable switching. The additional ripple can be injected by only two capacitors and one resistor. The ripple is generated by R_r and C_r using DCR of the inductor. And then coupled into the FB pin through C_d.

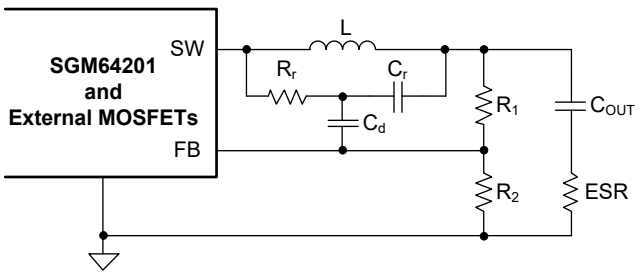


Figure 8. Ripple Injection from SW Pin

DETAILED DESCRIPTION (continued)

Note that if too much ripple is injected, the transient response will get worse, because the impact of the actual output variations on the feedback signal is reduced. The key point is that the ripple should be kept as small as possible without losing the stability.

The process of sizing the ripple injection resistor and capacitors in Figure 8 is as follows:

• Select R_r and C_r. Set R_r range from 10kΩ to 100kΩ and ensure R_rC_r satisfies the loop stability condition:

$$\frac{L \times C_{OUT}}{R_r \times C_r} > \frac{t_{ON}}{2} \quad (8)$$

• Select C_d to couple the ripples into the FB pin. The impedance of C_d should be small compared to the feedback divider impedance at the desired switching frequency. The impedance of the feedback network is the parallel combination of $R_1||R_2$. The impedance of C_d at the switching frequency can be taken to be about one tenth of this value.

$$C_d > \frac{10}{2 \times \pi \times f_{SW} \left(R_1 \,||\, R_2\right)} \quad (9)$$

Note that C_d should be smaller than C_r, also the selection of capacitance of C_d will influence the transient response of the converter. The transient is faster and undershoot is smaller if C_d is small. The transient is slower and undershoot is bigger if C_d is large.

With the ripple injection network, the feedback voltage ripple is calculated in Equation 10.

$$\Delta V_{FB} = \frac{V_{IN} - V_{OUT}}{R_r C_r} \times t_{ON} \quad (10)$$

APPLICATION INFORMATION

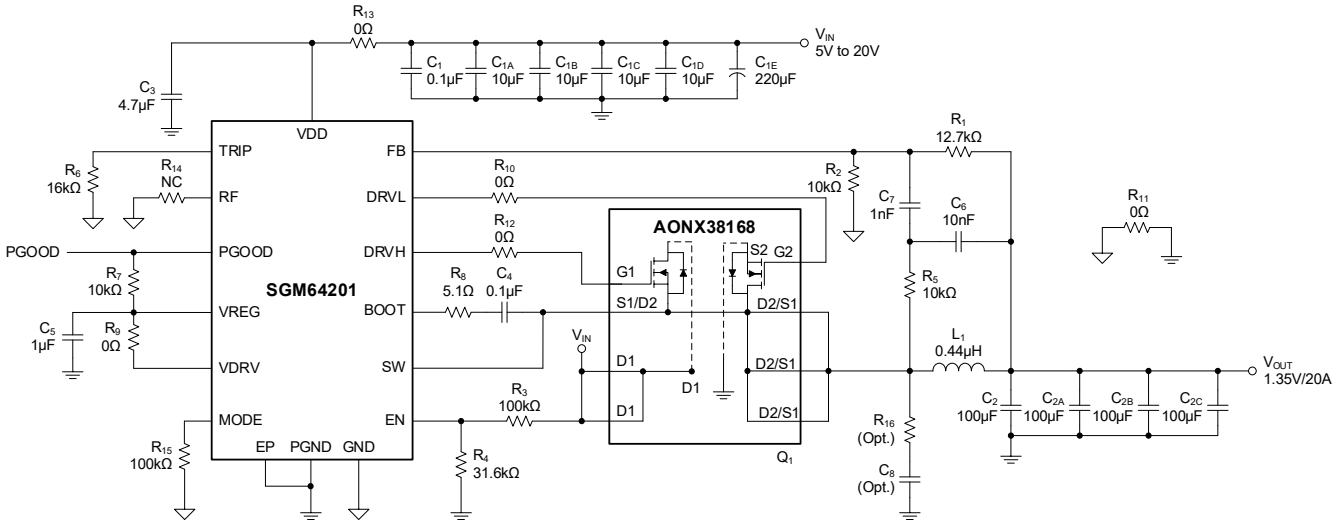


Figure 9. Typical Application Circuit Diagram

Design Requirements

This section describes the design calculations and device selection for applications with all ceramic output capacitors. Table 3 shows the design objectives.

Table 3. Design Specifications

Design Parameters	Example Values
Input Voltage	12V (TYP), 5V to 20V
Start Input Voltage (Rising V_{IN})	5V
Output Voltage	1.35V
Output Voltage Ripple	13.5mV, 1% of V_{OUT} (CCM)
Output Current Rating	20A
Over-Current Threshold	25A
Transient Response, 0A to 20A Load Step	67.5mV, 5% of V_{OUT}
Operation Frequency	500kHz
Operation Mode	PSM
Soft-Start Time	1.2ms

Input Capacitor Selection (C_1, C_{1A}, C_{1B}, C_{1C}, C_{1D}, C_{1E})

The input capacitor is necessary to circulate the high frequency ripples and switching currents of the converter and keep them away from the input line and the source. The selected capacitors must have enough RMS current rating to absorb all AC currents on the input. The input capacitors must deliver the RMS current according to:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (11)$$

Where the duty cycle is $D = V_{OUT}/V_{IN}$. For example, at D = 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 20A of steady-state load current, the input capacitor(s) must support an RMS current of 8A (0.40 × 20A).

The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 12. In this example, a 220μF/35V electrolytic capacitor and four 10μF/50V ceramic capacitors are used.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (12)$$

It recommended placing an additional small size 0.1μF ceramic capacitor right beside V_{IN} and GND pins for high frequency filtering.

Inductor Selection (L_1)

Equation 13 is conventionally used to calculate the output inductance of a Buck converter. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductance is typically selected such that K_{IND} is between 20% to 40%. The DC current rating of the selected inductor should be at least 25% above the maximum load current. The inductor saturation current must be high enough such that it does not saturate in any normal or transient operating condition. ΔI_L can be selected equal to 30% of maximum load current.

APPLICATION INFORMATION (continued)

$$L = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{V_{IN\_MAX} \times I_{OUT} \times K_{IND} \times f_{SW}} \quad (13)$$

In this example, the calculated inductance will be 0.42μH with K_{IND} = 0.3, so the nearest inductance of 0.44μH is selected.

The maximum inductor peak current and inductor ripple are calculated by Equation 14 and 15:

$$I_{L\_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (14)$$

$$\Delta I_L = \frac{V_{IN\_MAX} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (15)$$

Output Capacitor Selection (C_2, C_{2A}, C_{2B}, C_{2C})

The output capacitors and inductor filter the AC part of the PWM switching voltage and provide an acceptable level of output voltage ripple superimposed on the desired output DC voltage. Capacitors also store energy to help maintain of the output voltage regulation during a load transient. The output voltage ripple (ΔV_{OUT}) depends on the output capacitor value at the operating voltage and temperature (℃) and its parasitics (ESR and ESL):

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{V_{IN} - V_{OUT}}{L} \times ESL + \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} \quad (16)$$

The voltage rating of the output capacitors should be selected with enough margins to ensure that capacitance drop (voltage and temperature derating) is not significant. The type of output capacitors will determine which terms of Equation 16 are dominant. For ceramic output capacitors, the ESR and ESL are virtually zero so the output voltage ripple will be dominated by the capacitive term.

$$\Delta V_{OUT} \approx \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} \quad (17)$$

To reduce the voltage ripple either switching frequency or the total capacitance is increased. Inductance may also be increased to reduce the inductor current ripple. For electrolytic output capacitors, the value of capacitance is relatively high, and the third term in Equation 16 can be ignored compared to the ESR and ESL terms:

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{V_{IN} - V_{OUT}}{L} \times ESL \quad (18)$$

Higher quality capacitors, larger inductance or using parallel capacitors can help reduce the output ripple in a design using electrolytic output capacitors. The ESR of some commercial electrolytic capacitors can be quite high, and it is recommended to use quality capacitors with the ESR or the total impedance clearly documented in their datasheet. ESR of an electrolytic capacitor may increase significantly at cold ambient temperatures with a factor of 10 or so, which increases the ripple and can deteriorate the regulator stability.

The design of the output capacitor typically satisfies the typical ±1% ripple requirement. The appropriate output capacitor value can be selected through calculations based on the capacitor ripple and ESR ripple. However, in scenarios involving low voltage and high current, it is crucial to consider the overshoot and undershoot of the output voltage during load transient. Additionally, with the same output capacitor, the COT control response is faster than voltage mode control or current mode control. Therefore, the design of the output capacitor must always take into account the load transient response. Equation 19 and Equation 20 calculate the minimum capacitor required to keep the output voltage overshoot or undershoot to a desired value.

$$C_{OUT} > \frac{I_{MAX}^2}{2 \times V_{OVER}} \left(\frac{L}{V_{OUT}} - \frac{1}{I_{SR\_FALLING}} \right) \quad (19)$$

$$C_{OUT} > \frac{I_{MAX}^2}{2 \times V_{UNDER}} \left(\frac{1}{I_{SR\_eq}} - \frac{1}{I_{SR\_RISING}} \right) \quad (20)$$

Where:

$I_{SR\_FALLING}$ is the load current drop slew rate (5A/μs, TYP) during load transient from full load to no load.

I_{SR_RISING} is the load current rise slew rate (5A/μs, TYP) during load transient from no load to full load.

I_{SR_eq} is the equivalent slew rate of inductor current during load transient from no load to full load.

V_{OVER} is the output overshoot during load transient from full load to no load.

V_{UNDER} is the output undershoot during load transient from no load to full load.

In this case according to Table 3, 4 × 100μF/10V ceramic capacitors can meet the above conditions.

APPLICATION INFORMATION (continued)

MOSFET Selection (Q_1)

Select the AONX38168. The device integrates two MOSFETs at the size of 5mm × 6mm, and flows through 20A. The R_{ON} of the high-side MOSFET is 3.6mΩ, and the R_{ON} of the low-side MOSFET is 0.85mΩ.

VIN UVLO Setting (R_3, R_4)

The input UVLO can be programmed by using an external voltage divider on the EN pin of the SGM64201. In this design, R_3 is connected between V_{IN} pin and EN pin, and R_4 is connected between EN pin and GND (see Figure 9). The UVLO has two thresholds (hysteresis), one for power-up (turn-on) when the input voltage is rising and one for power-down (turn-off) when the voltage is falling. In this design, the turn-on (enable to start switching) occurs when V_{IN} rises above V_{UV_H}. When the regulator is working, it will not stop switching (disabled) until the input falls below V_{UV_L}. The enable rising threshold voltage V_{EN_H} is 1.2V (TYP) and enable hysteresis voltage V_{EN_HYS} is 0.1V (TYP). Given V_{UV_H} as 5.0V, select R_3 to be 100kΩ to minimize input current from the supply, then R_4 and V_{UV_L} can be calculated by following equations.

$$V_{UV\_H} = V_{EN\_H} \times \frac{R_3 + R_4}{R_4} \quad (21)$$

$$V_{UV\_L} = \left(V_{EN\_H} - V_{EN\_HYS}\right) \times \frac{R_3 + R_4}{R_4} \quad (22)$$

By Equation 21, R_4 is calculated to be 31.58kΩ, and a standard value of 31.6kΩ is selected. Based on the value of R_3 and R_4, V_{UV_L} can be calculated to be 4.58V according to Equation 22.

Output Voltage Setting (R_1, R_2)

Use an external resistor divider (R_1 and R_2) to set the output voltage using Equation 23:

$$R_1 = R_2 \times \frac{V_{OUT} - V_{REF}}{V_{REF}} \quad (23)$$

where V_{REF} = 0.6V is the internal reference. For example, by choosing R_2 = 10kΩ, the R_1 value for 1.35V output will be calculated as 12.5kΩ, so the nearest resistance of 12.7kΩ is selected.

TRIP Resistor Selection (R_6)

The over-current threshold of the SGM64201 can be set using a resistor placed between TRIP and GND pins. Equation 24 can be used to calculate the R_{TRIP} to set the desired over-current threshold.

$$R_{TRIP} = \frac{8 \times R_{DSON\_LS} \times \left(I_{OCP} - \Delta I_L / 2\right)}{I_{TRIP}} \quad (24)$$

In this example, the calculated inductance will be 15.5kΩ with I_{OCP} = 25A, so the nearest resistance of 16kΩ is selected.

Ripple Injection Selection (C_6, C_7, R_5)

For application with all ceramic output capacitor. Due to very low ESR of the output capacitors, additional ripple needs to be injected artificially into the FB pin to keep stable switching using C_r, C_d and R_r. In this example, according to Equation 8, Equation 9 and Equation 10, C_r, C_d and R_r are calculated as 10nF, 1nF, 10kΩ respectively.

LAYOUT

Layout Guidelines

PCB layout is an important part of the converter design. A weak layout can result in poor performance, resistive losses, EMI issues and instability problems. SGMICRO recommends that the PCB should be designed with at least 4 layers, Figure 10 and Figure 11 only shows the top and bottom layers of the 4-layer board. The following guidelines are helpful for designing a good layout for the SGM64201:

- Place the input capacitors as close as possible to the switches (drain of the high-side MOSFET and the source of the low-side MOSFET) to keep the input AC current loop as small as possible.
- Use small size high frequency decoupling capacitors near input and ground pins.
- Place the inductor pins as close as possible to the switching nodes. Keep the switching node connections short and wide with minimal copper area to minimize capacitive coupling noise and radiation. Keep them away from sensitive traces.
- Keep the BOOT-SW voltage path as short as possible.
- Sensitive signals such as FB, MODE, PGOOD and TRIP should be away from noisy traces and components such as SW node, gate driver and switching side of the inductor body. Place divider resistor as close as possible to the FB and GND pins. Use internal layers as ground planes and shield sensitive signals from noisy traces.
- Place decoupling capacitors on VREG and VDRV as close as possible to those pins.
- Keep the device close to the switch gate pins to minimize gate drive trace lengths. The device can be placed on the opposite side of the PCB. Connect the gates with some parallel vias to minimize gate connection impedance.
- Use separate routes for analog and power grounds. Use a 0Ω resistor as connection to separate analog and power ground nets in the layout.
- Please connect the frequency setting resistor from the RF pin either to GND or to the PGOOD pin, and make sure that the connections are made as close to the device as possible. Additionally, connect the over-current setting resistors from the TRIP pin to GND, also make sure that the connections are made as close to the device as possible.
- Use large copper areas on all layers and stich them with thermal vias for better heat transfer and dissipation especially for heavy load applications.

Layout Example

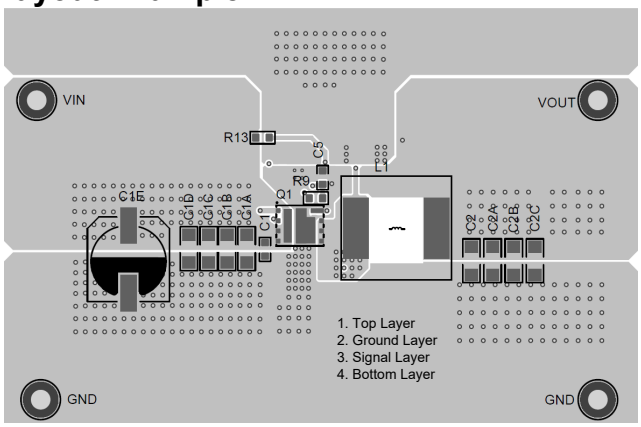


Figure 10. Layout Example (Top Layer)

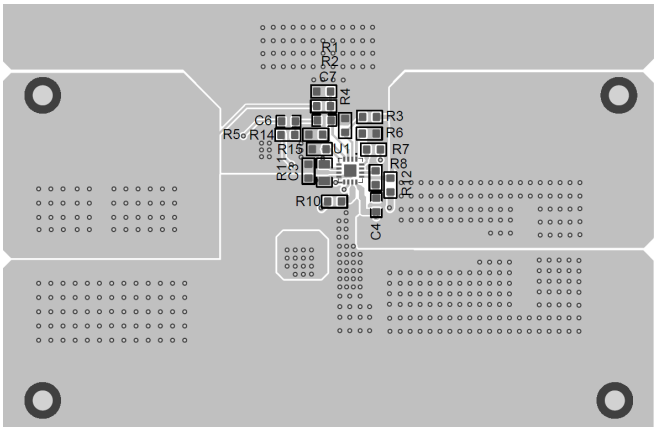


Figure 11. Layout Example (Bottom Layer)

REVISION HISTORY

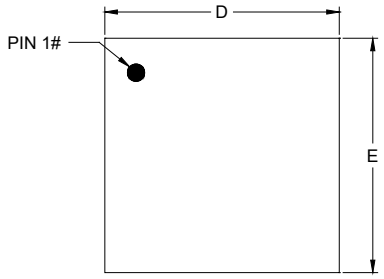
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JUNE 2025 – REV.A to REV.A.1	Page
Updated Typical Performance Characteristics section	7, 8
Updated Application Information section	20

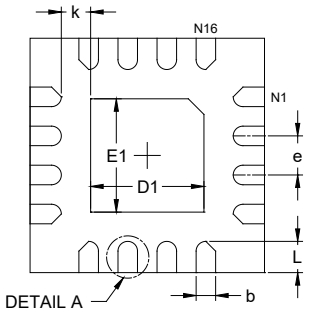
Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

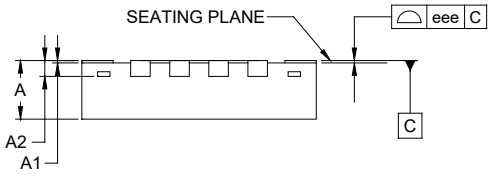
TQFN-3×3-16FL



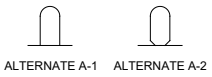
TOP VIEW



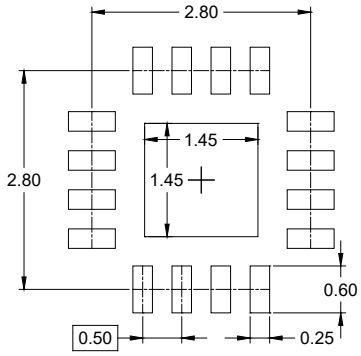
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



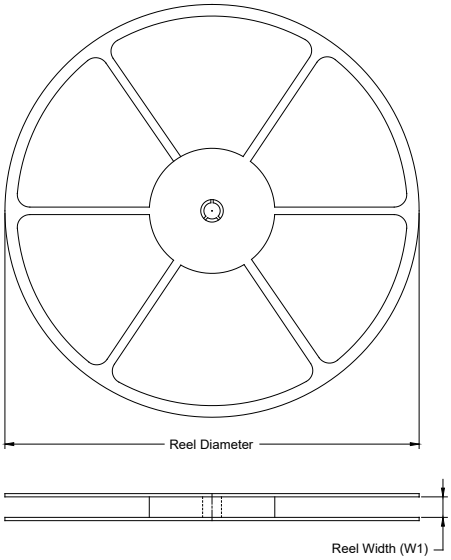
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.180	-	0.300
D	2.900	-	3.100
E	2.900	-	3.100
D1	1.300	-	1.550
E1	1.300	-	1.550
e	0.500 BSC		
k	0.200	-	-
L	0.300	-	0.500
eee	0.080		

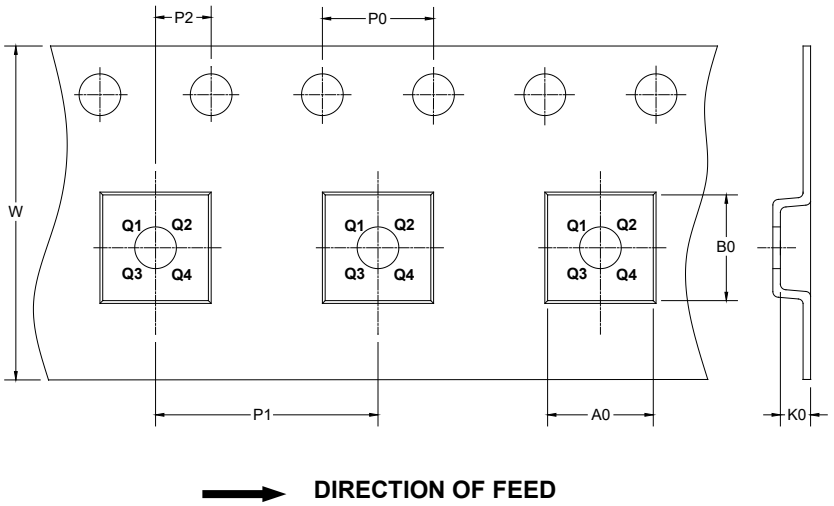
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



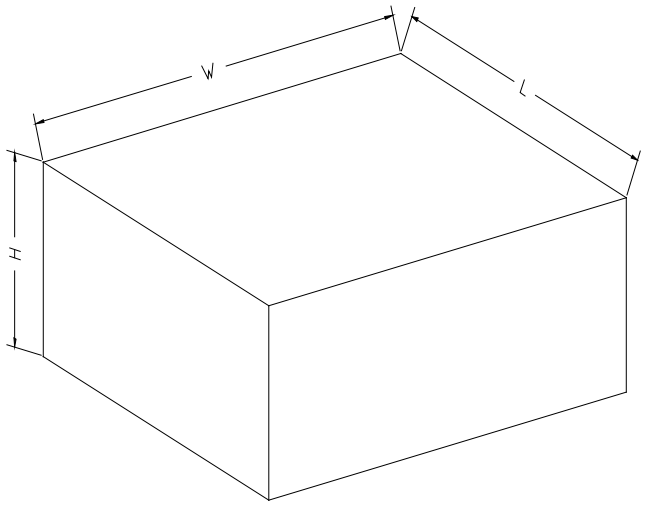
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-16FL	13"	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002