SGM25711B
2.5V to 18V High-Efficiency Hot Swap Controller with Power-Limiting

GENERAL DESCRIPTION

The SGM25711B is a hot swap controller that allows a board to be safely inserted or removed from a live backplane. An internal circuit drives an external N-MOSFET switch to control supply voltage from 2.5V to 18V.

The SGM25711B offers programmable current limit, power-limiting and fault time to ensure that the external MOSFET is always working within its safe operating area. If the load current is higher than the set current for more than the programmed time, the external MOSFET will be shutdown. The SGM25711B restarts automatically after a fault timeout delay. The low current sense threshold of 25mV is very accurate, which allows the use of smaller detection resistors resulting in lower power losses and smaller size.

This feature allows the user to easily design a high reliability system. The device has power and fault output functions to provide condition monitoring and load protection.

SGM25711B is available in a Green MSOP-10 package.

FEATURES

- **Input Voltage Range from 2.5V to 18V**
- **Programmable MOSFET SOA Protection**
- **Accurate Current Limit at All Times**
- **Accurate 25mV Current Sense Threshold**
- **Power Good Output**
- **Fast Circuit-Breaker for Short-Circuit Protection**
- **Programmable Fault Timer**
- **Programmable Under-Voltage Threshold**
- **Active-Low for nPG and nFLT Pins**
- **Available in a Green MSOP-10 Package**

APPLICATIONS

Medical Systems
Storage Area Networks (SAN)
Plug-In Modules
Base Stations

TYPICAL APPLICATION

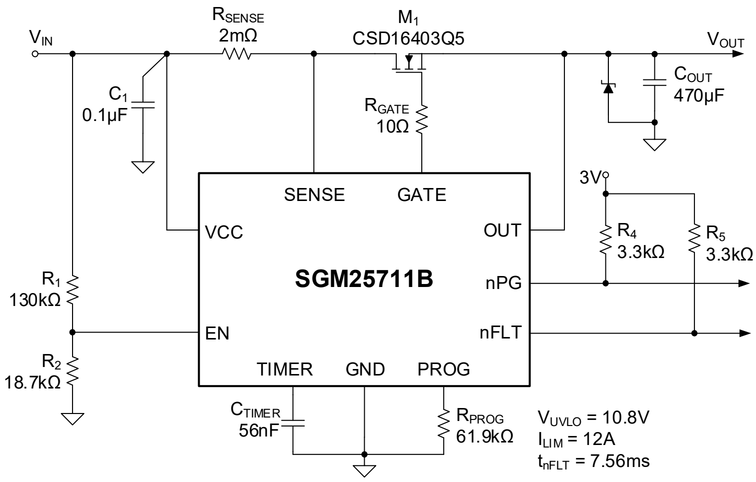


Figure 1. Typical Application Circuit (12V/10A)

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25711B	MSOP-10	-40℃ to +125℃	SGM25711BXMS10G/TR	SGMRB7 XMS10 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

X X X X X
- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range
- EN, nFLT (1), nPG (1), GATE, OUT, SENSE, VCC .... -0.3V to 27V
- VCC, SENSE (transient < 1ms, 10mA limited)............30V
- PROG (1).. -0.3V to 3.6V
- SENSE to VCC .... -0.3V to 0.3V
- TIMER .... -0.3V to 5V

Sinking Current
- nFLT, nPG...5mA

Sourcing Current
- PROG... Internally limited

Package Thermal Resistance
- MSOP-10, θ_{JA}... 164℃/W
- MSOP-10, θ_{JB}... 98.9℃/W
- MSOP-10, θ_{JC} .... 51.3℃/W

Junction Temperature...+150℃
Storage Temperature Range ....-65℃ to +150℃
Lead Temperature (Soldering, 10s)............................+260℃
ESD Susceptibility
HBM...4000V
CDM 1000V

NOTE: 1. Do not apply voltage directly to the pin.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range
- SENSE, VCC ....2.5V to 18V
- EN, nFLT, nPG, OUT ....0V to 18V

Sinking Current
- nFLT, nPG...0mA to 2mA

Resistance, R_{PROG} .... 4.99kΩ to 500kΩ
External Capacitance, C_{TIMER}................................. 1nF (MIN)
Operating Junction Temperature Range......-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

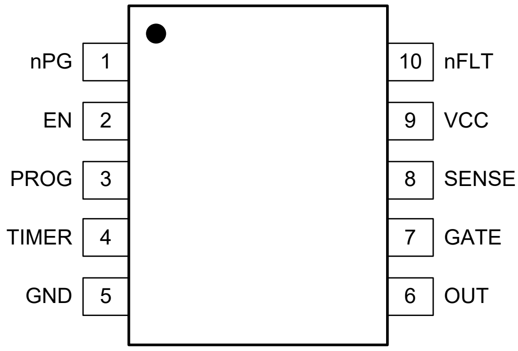
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



MSOP-10

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	nPG	Power Good Indicator Pin (Active-Low, Open-Drain). The voltage of the external MOSFET determines its state.
2	EN	Enable Pin. Active-high enable input. Connect to resistor divider.
3	PROG	Power-Limiting Programmable Pin. The power-limiting resistor connected to this pin determines the maximum allowable dissipation of the external MOSFET.
4	TIMER	Fault Timer Pin. An external capacitor on this pin sets the insertion delay time and fault time delay. The chip's restart time is also controlled by this capacitor.
5	GND	Ground.
6	OUT	Power Output Pin. Connect this pin to output (i.e., external MOSFET source). The chip monitors MOSFET V_{DS} voltage through this pin to limit the MOSFET power and control the nPG signal accordingly.
7	GATE	Gate Driver Output. This pin is connected to the gate of the external MOSFET.
8	SENSE	Current Sense Pin. The voltage from the input pin to this pin is measured by the current flowing into the sense resistor.
9	VCC	Power Input Pin. It is recommended to place a small bypass capacitor close this pin.
10	nFLT	Fault Event Indicator Pin. Go low when the external MOSFET has been turned off by the overload fault timer.

ELECTRICAL CHARACTERISTICS

($-40℃ \le T_J \le +125℃$, V_{CC} = 12V, V_{EN} = 3V and R_{PROG} = 50kΩ to GND. Typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC					
UVLO Threshold Voltage, Rising		2.25	2.35	2.45	V
UVLO Threshold Voltage, Falling		2.17	2.27	2.37	V
Hysteresis			85		mV
Supply Current, Enabled	$I_{OUT} + I_{VCC} + I_{SENSE}$		0.32	0.5	mA
Supply Current, Disabled	V_{EN} = 0V, $I_{OUT} + I_{VCC} + I_{SENSE}$		4		μA
EN					
Enable Threshold Voltage, Falling		1.25	1.3	1.35	V
Hysteresis			55		mV
Input Leakage Current	V_{EN} = 0V to 27V	-1	0	1	μA
nFLT					
Output Low Voltage	Sinking 2mA		35	65	mV
Input Leakage Current	V_{nFLT} = 0V or 27V	-1	0	1	μA
nPG					
nPG Threshold Voltage	$V_{(SENSE - OUT)}$ rising, nPG going high	235	315	395	mV
Hysteresis	$V_{(SENSE - OUT)}$ falling, nPG going low		85		mV
Output Low Voltage	Sinking 2mA		35	65	mV
Input Leakage Current	V_{nPG} = 0V or 27V	-1	0	1	μA
PROG					
Bias Voltage	Sourcing 10μA	0.65	0.68	0.71	V
Input Leakage Current	V_{PROG} = 1.5V	-0.2	0	0.2	μA
TIMER					
Sourcing Current	V_{TIMER} = 0V	8	10	12	μA
Sinking Current	V_{TIMER} = 2V	8	10	12	μA
	V_{EN} = 0V, V_{TIMER} = 2V	4.5	7	9.5	mA
TIMER Threshold Voltage, Rising		1.3	1.35	1.4	V
TIMER Threshold Voltage, Falling		0.33	0.35	0.38	V
Timer Activation Voltage	Raise GATE until I_{TIMER} sinking, measure $V_{(GATE - VCC)}$, V_{CC} = 12V	5.3	5.6	5.9	V
OUT					
Input Bias Current	V_{OUT} = 12V		1		μA
GATE					
Output Voltage	V_{OUT} = 12V	24.5	25.5	26.5	V
Clamp Voltage	Inject 10μA into GATE, measure $V_{(GATE - VCC)}$	12	13.5	15	V
Sourcing Current	V_{GATE} = 12V	20	33	46	μA
Sinking Current	Fast turn-off, V_{GATE} = 0.2V	33	63	93	mA
	Sustained, V_{GATE} = 4V to 23V	6	11	16	mA
Pull-Down Resistance	Thermal shutdown	11.5	17.5	23.5	kΩ
SENSE					
Input Bias Current	V_{SENSE} = 12V, sinking current		15	25	μA
Current Limit Threshold	V_{OUT} = 12V, $-20℃ \le T_J \le +125℃$	23	25	27	mV
	V_{OUT} = 12V, $-40℃ \le T_J \le +125℃$	22.5	25	27.5	
Power-Limiting Threshold	V_{OUT} = 7V, R_{PROG} = 50kΩ	10	14	18	mV
	V_{OUT} = 2V, R_{PROG} = 25kΩ	10	14	18	
Fast-Trip Shutdown Threshold		52.3	61.5	70.7	mV
Over-Temperature Shutdown (OTSD)					
Threshold, Rising			145		℃
Hysteresis			15		℃

TIMING REQUIREMENTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
EN					
Deglitch Time	EN↑	10	39.5	80	μs
Disable Delay Time ($t_{pff50\text{-}90}$)	EN↓ to GATE↓, C_{GATE} = 0, see Figure 2	0.33	0.665	1	μs
nPG					
Delay (Deglitch) Time	Rising or falling edge	2	4	6	ms
GATE					
Fast Turn-Off Duration		9	13.5	18	μs
Turn-On Delay Time ($t_{prr50\text{-}50}$)	V_{CC} rising to GATE sourcing, see Figure 3		125	250	μs
SENSE					
Fast Turn-Off Duration		9	13.5	18	μs
Fast Turn-Off Delay Time ($t_{prf50\text{-}50}$)	$V_{(VCC - SENSE)}$ = 80mV, C_{GATE} = 0pF, see Figure 4		250		ns

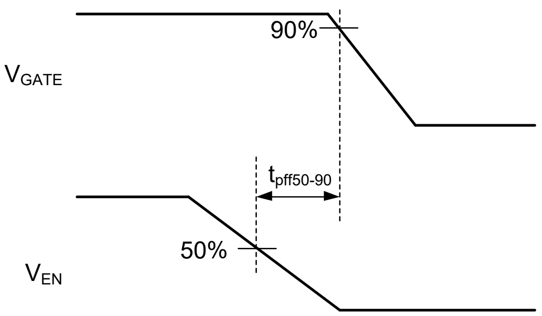


Figure 2. $t_{pff50\text{-}90}$ Timing Waveform

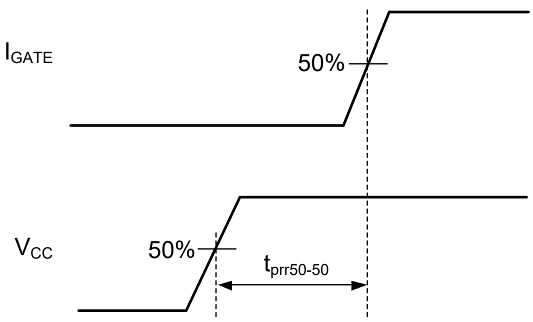


Figure 3. $t_{prr50\text{-}50}$ Timing Waveform

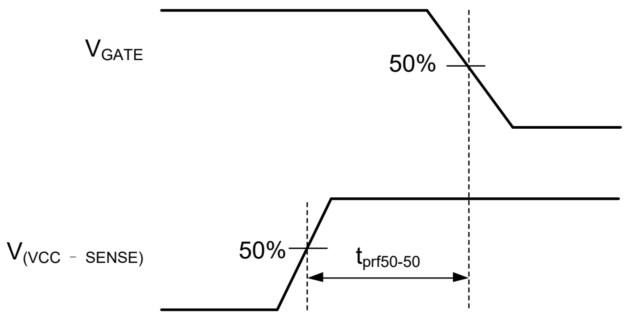
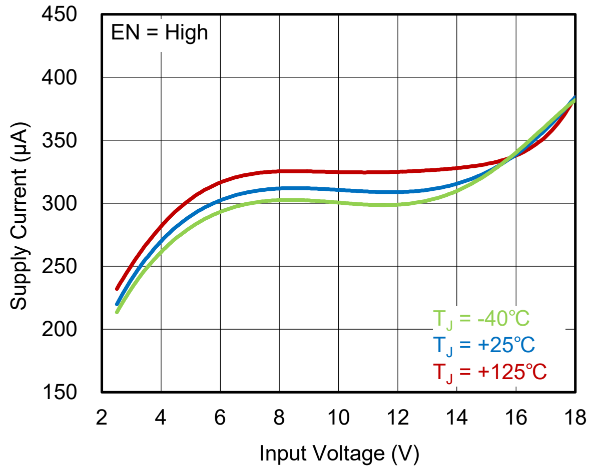


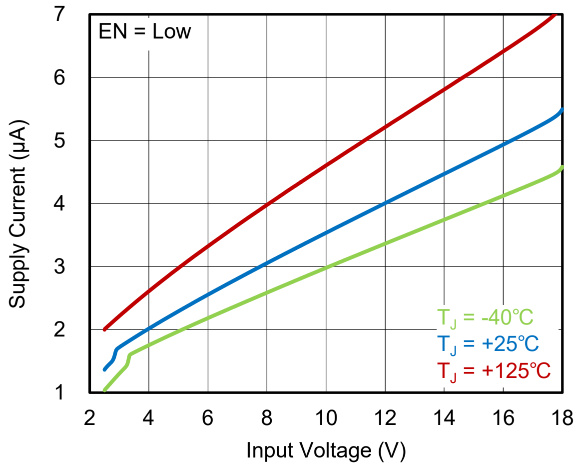
Figure 4. $t_{prf50\text{-}50}$ Timing Waveform

TYPICAL PERFORMANCE CHARACTERISTICS

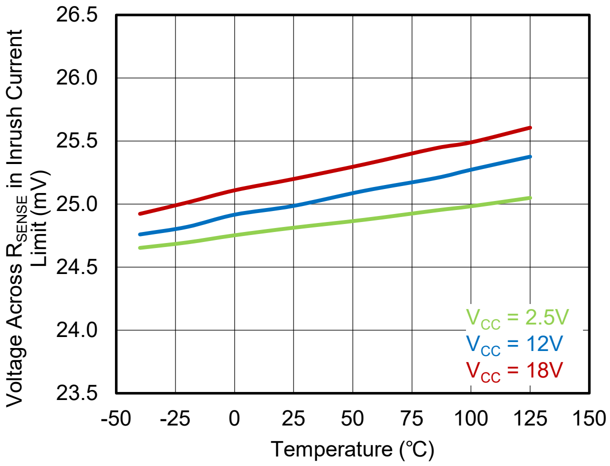
Supply Current vs. Input Voltage at Normal Operation



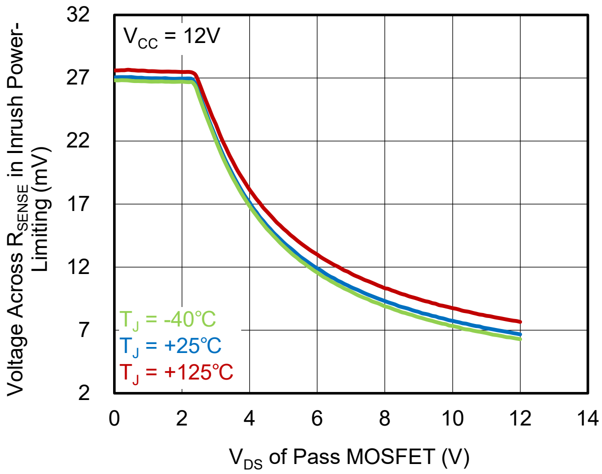
Supply Current vs. Input Voltage at Shutdown



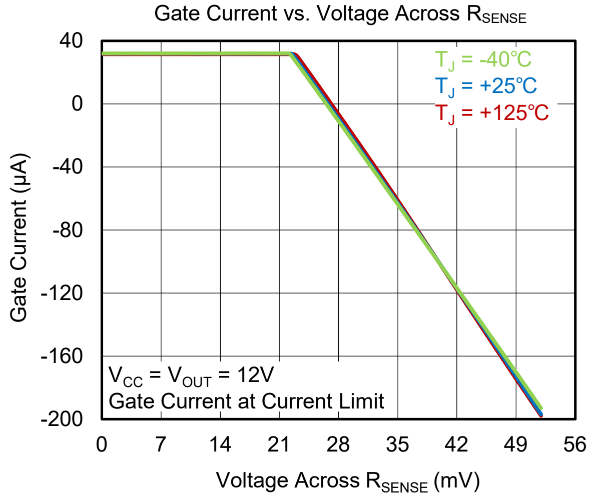
Voltage Across R_{SENSE} in Inrush Current Limit vs. Temperature



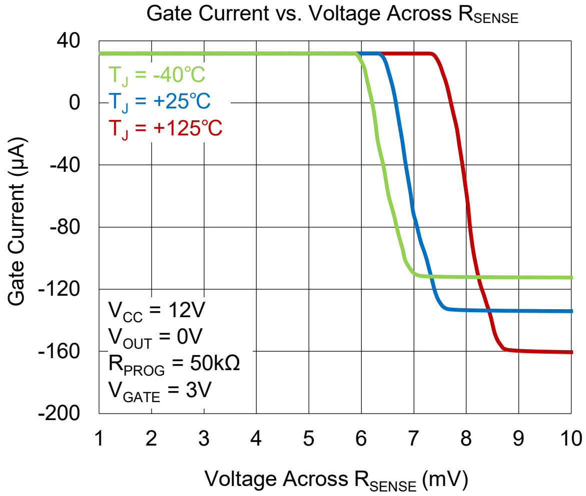
Voltage Across R_{SENSE} in Inrush Power-Limiting vs. V_{DS} of Pass MOSFET



Gate Current vs. Voltage Across R_{SENSE}

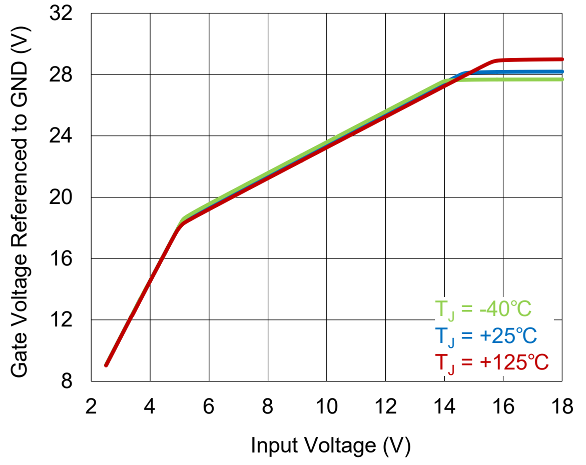


Gate Current vs. Voltage Across R_{SENSE}

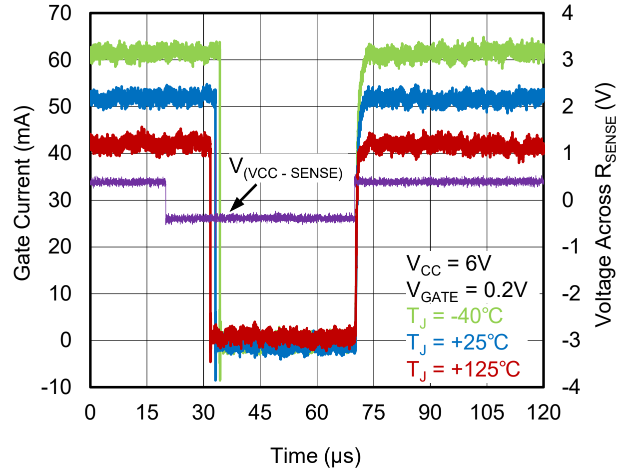


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

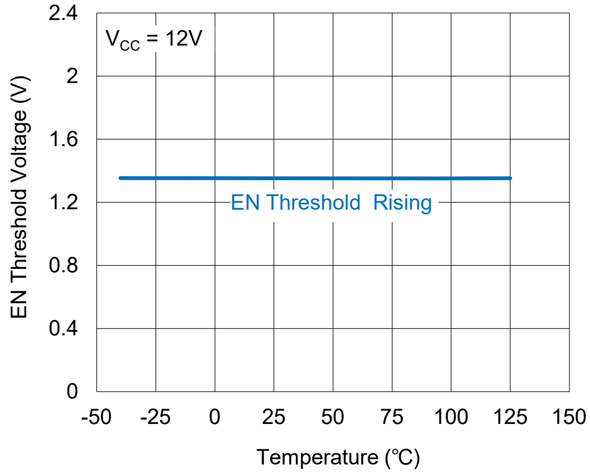
Gate Voltage with Zero Gate Current vs. Input Voltage



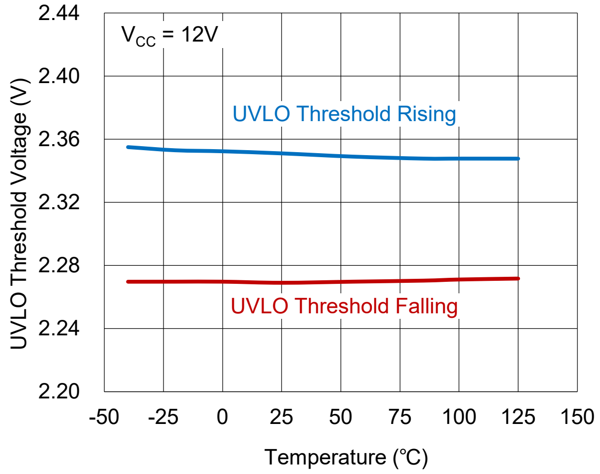
Gate Current during Fast-Trip



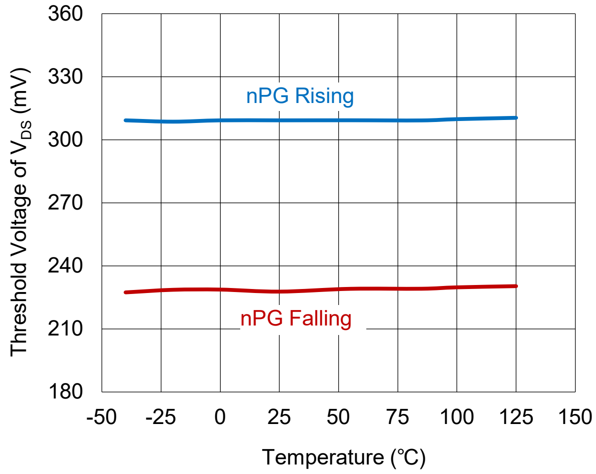
EN Threshold Voltage vs. Temperature



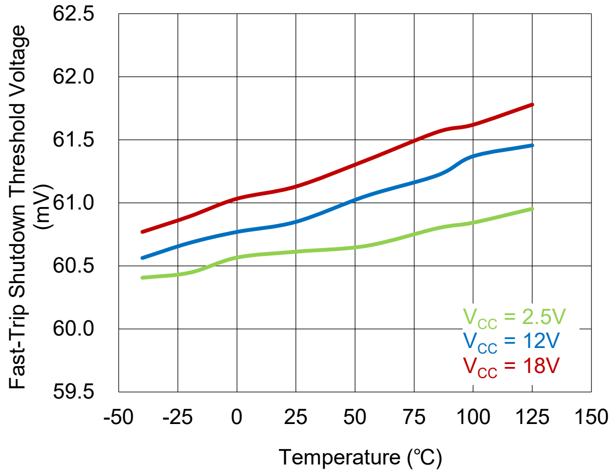
UVLO Threshold Voltage vs. Temperature



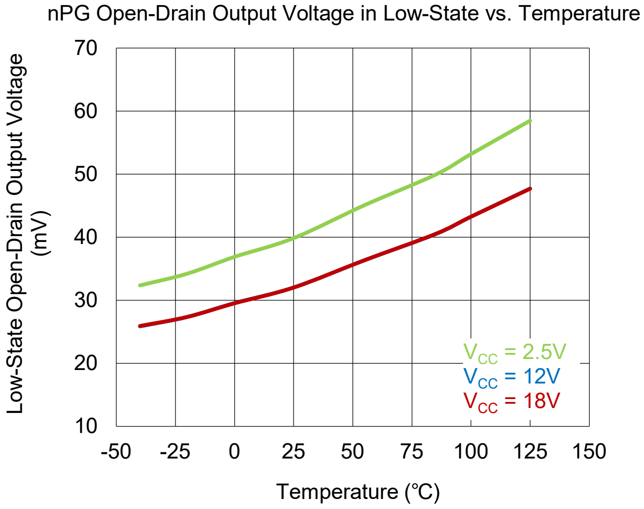
Threshold Voltage of V_{DS} vs. Temperature

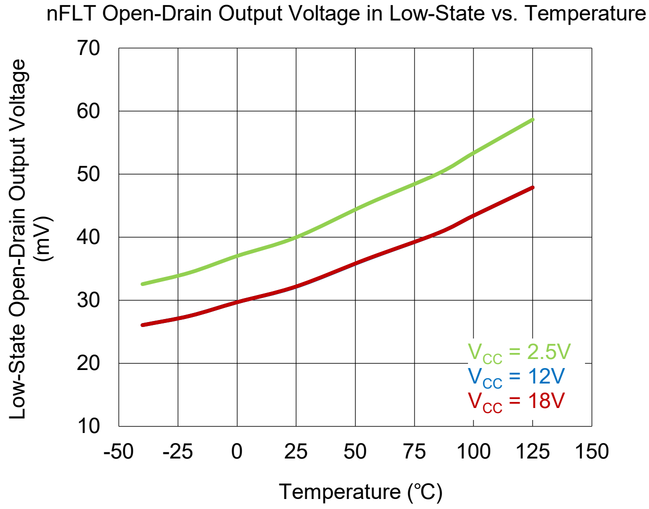


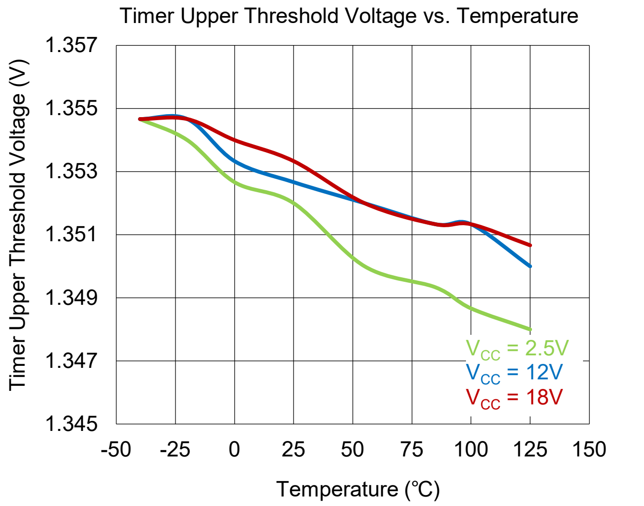
Fast-Trip Shutdown Threshold Voltage vs. Temperature

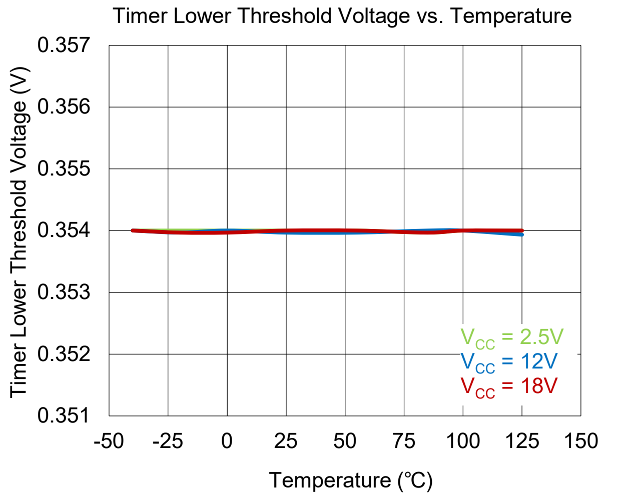


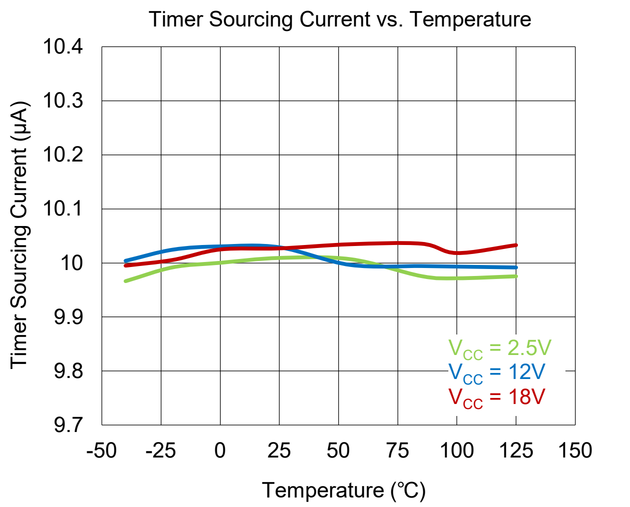
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

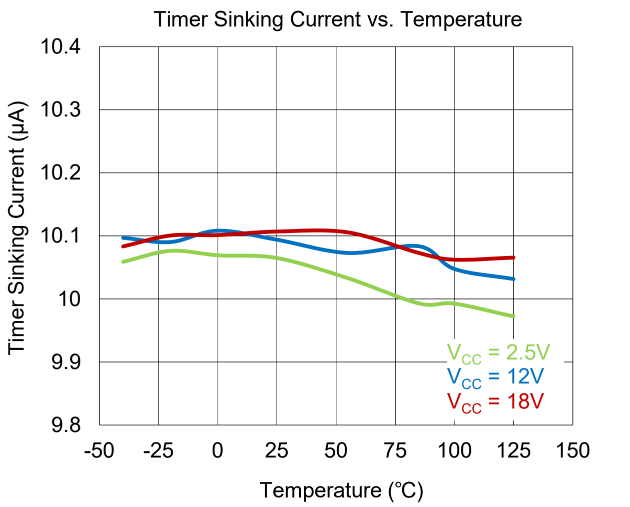




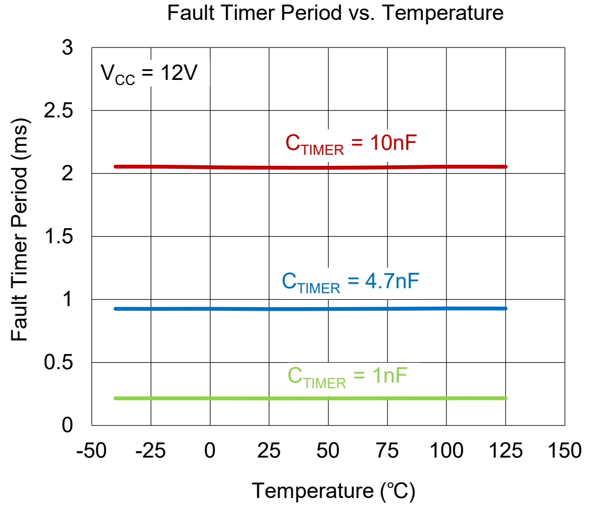


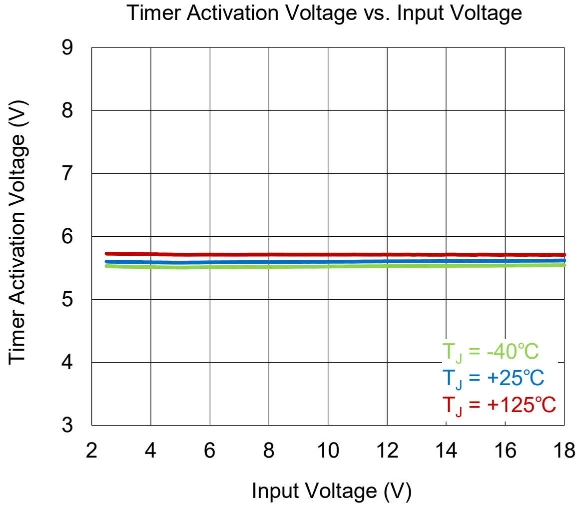






TYPICAL PERFORMANCE CHARACTERISTICS (continued)





FUNCTIONAL BLOCK DIAGRAM

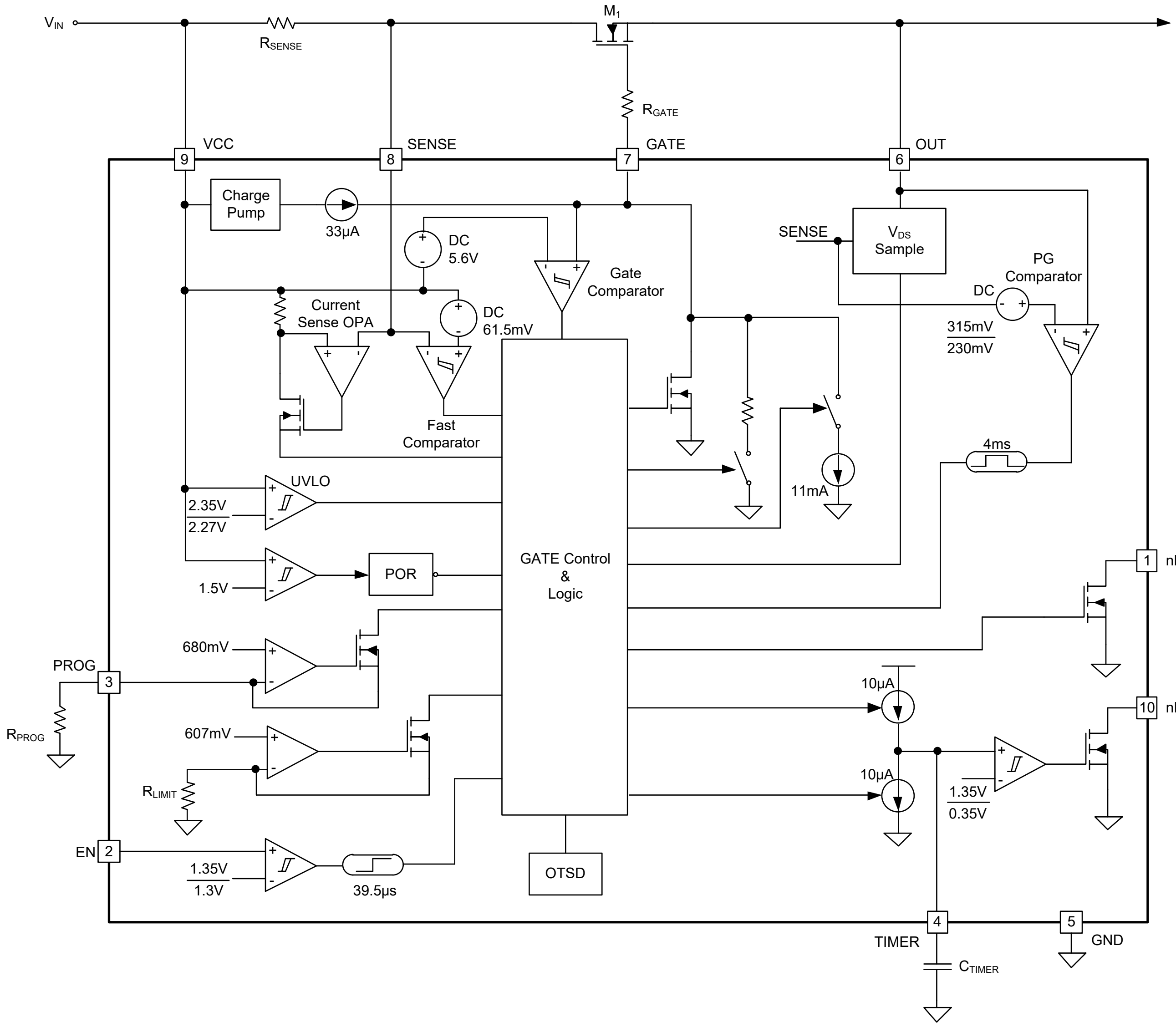


Figure 5. Block Diagram

DETAILED DESCRIPTION

VCC

There are three functions for the VCC pin. First, power the chip. Second, this pin is the input terminal of power on reset (POR) and under-voltage lockout (UVLO) functions. Third, the lead of the VCC should be directly connected to the positive end of the sense resistor, so that the current flowing through the resistor can be more accurately detected. A 0.1μF capacitor is recommended.

EN

When the voltage of EN pin is greater than 1.35V, the gate driver starts to work. An external divide resistor can be added to monitor the input under-voltage. When the chip is locked, pull down and then up EN to restart the chip. Do not float this pin.

GATE

This pin is the MOSFET (M_1) gate drive. The charge pump charges the gate with a current of 33μA. Since V_{CC} is approximately equal to V_{OUT} during normal operation, the $V_{(GATE\ -\ VCC)}$ is clamped to a maximum of 13.5V. During startup, the amplifier regulates the output current to control the gate voltage and to limit the inrush current. During the surge, the TIMER pin charges the capacitor with a current of 10μA until the $V_{(GATE\ -\ VCC)}$ voltage exceeds the set voltage (5.6V when V_{CC} = 12V), if $V_{(GATE\ -\ VCC)}$ is greater than the timer set voltage, the TIMER pin stops sourcing current and starts sinking current. This pin is disabled in three situations:

1. Under the following circumstances, the 11mA current sink will pull down the GATE voltage:

- $V_{(VCC\ -\ SENSE)}$ > 25mV.
- V_{EN} is lower than the falling threshold voltage.
- V_{CC} reaches the lower threshold of UVLO.

2. The GATE pin is pulled down through a 3.2Ω resistor when V_{EN} is less than its falling threshold or when an output short occurs and $V_{(VCC\ -\ SENSE)}$ exceeds 61.5mV, the chip trips shutdown quickly, and there is still 11mA pull-down current to turn off the MOSFET.

3. If the chip temperature exceeds the threshold, the chip discharges the GATE charge to GND through a 17.5kΩ resistor. In the auto-retry mode, the chip will restart periodically. No resistance should be connected between the GATE and GND (or OUT) pins.

nFLT

The nFLT pin is assigned for SGM25711B. When the SGM25711B remains within the current limit long enough for the fault timer to expire, the low open-drain output will be pulled low. The SGM25711B operates in auto-retry mode. In the auto-retry mode, the fault timeout will stop the operation of the external MOSFET (M_1) and try to restart after 16 hiccup cycles. When the fault is not eliminated, the hiccup continues. At this time, this pin will be pulled low. If M_1 is disabled by EN, OTSD or UVLO, the nFLT pin will not be asserted. The pin can remain suspended when not needed.

OUT

This pin can measure the voltage between drain and source of MOSFET. Power-limiting also needs the function of this pin. It is recommended to place Schottky diode to prevent negative pressure. At the same time, this pin needs to connect the low ESR ceramic capacitor to the ground to bypass the high-frequency signal.

nPG

When the voltage across drain and source of MOSFET is less than 230mV and a deglitch time of 4ms elapses, the drain of this pin is pulled down. When V_{DS} > 315mV, it becomes open-drain output. That is, when the V_{DS} of M_1 rises, the pin assumes a high resistance state after the same deglitch time.

DETAILED DESCRIPTION (continued)

PROG

The resistance between PROG and GND pins sets the maximum power allowed by MOSFET. Do not apply voltage directly to the PROG pin. When the constant power-limiting function is not used, connect this pin to the ground with a 4.99kΩ resistance. If it is necessary to set the constant power, please refer to Equation 1.

$$R_{PROG} = \frac{3600}{P_{LIM} \times R_{SENSE}} \quad (1)$$

$$P_{LIM} = \frac{3600}{R_{PROG} \times R_{SENSE}} \quad (2)$$

where P_{LIM} is the power-limiting value of the M_1, R_{SENSE} is the detection resistor between VCC and SENSE pins, and P_{LIM} can calculate the maximum thermal stress of M_1.

$$P_{LIM} < \frac{T_{J(MAX)} - T_{C(MAX)}}{R_{\theta JC(MAX)}} \quad (3)$$

where $T_{J(MAX)}$ is the expected maximum junction temperature, $T_{C(MAX)}$ is the maximum shell temperature, and $R_{\theta JC\ (MAX)}$ is the junction shell thermal resistance.

SENSE

This pin is the other end of the sense resistor. The current can be limited by detecting the voltage across sense resistor, refer to Equation 4.

$$I_{LIM} < \frac{25mV}{R_{SENSE}} \quad (4)$$

when $V_{(VCC\ -\ SENSE)}$ > 61.5mV, fast-trip shutdown occurs.

TIMER

A C_{TIMER} capacitor is connected between TIMER and GND to time the fault time. When the overload occurs, the TIMER charges the C_{TIMER} with 10μA current, otherwise discharges the C_{TIMER} with 10μA current. If V_{TIMER} reaches 1.35V, the MOSFET will be turned off. The capacitor sets the restart time after failure. It is recommended to place a minimum capacitance of 1nF to ensure the normal operation of the timer. The value of this capacitor can be calculated by the following formula.

$$C_{TIMER} = \frac{10\mu A}{1.35V} \times t_{nFLT} \quad (5)$$

If the load current is higher than the current setting value or a fast-trip shutdown occurs, the MOSFET will be stopped for 16 charging and discharging cycles. After the time counting, the TIMER pin will be pulled to GND by the 7mA sinking current, and then the MOSFET will be restarted. In any of the following cases, the C_{TIMER} charge will also be put to GND by the 7mA current source:

- V_{EN} is less than the lower threshold.
- V_{CC} is less than the lower threshold of UVLO.

DETAILED DESCRIPTION (continued)

Device Functional Modes

SGM25711B has all the functions of the forward hot plug controller, mainly including: start surge suppression, under-voltage lockout, external MOSFET driving and power-limiting, overload timeout shutdown and indication functions.

Figure 6 to Figure 8 and Figure 10 to Figure 12 respectively show the typical application (12V/10A) and oscilloscope plots. Many of the previously described capabilities are shown in these figures.

Board Plug-In

Figure 6 and Figure 7 show the surge current of SGM25711B during hot plug. When V_{CC} > 1.5V, power on reset (POR) initializes and the chip is ready to start.

If the internal voltage is higher than the EN threshold, GATE, PROG, TIMER, nPG, nFLT begin to release. The chip starts to drive the MOSFET (M_1) through the GATE pin. At the same time, monitor the current and voltage at both ends (DS) of M_1 to limit the current and power. The current increases with the decrease of V_{DS} until the current limit value is reached.

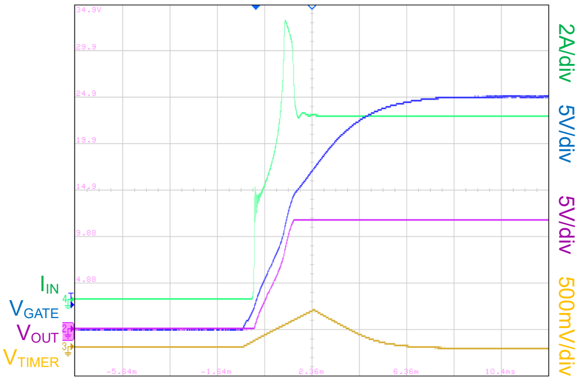


Figure 6. Inrush Mode at Hot Swap Circuit Insertion

Inrush Operation

After the enable of SGM25711B is activated, the GATE pin starts to flow current and the V_{GATE} rises. When it reaches the opening threshold of M_1, M_1 has current flowing into the output capacitor. When the current is higher than the limit value, the negative feedback system will adjust the turn-on degree of the MOSFET to keep the current at the limit value. Constant power process is a more complex process. When the constant power occurs, the TIMER pin starts charging the C_{TIMER} with a current of 10μA until $V_{(GATE - VCC)}$ = 5.6V. Then discharge C_{TIMER} with 10μA. When $V_{(GATE - VCC)}$ < 5.6V, V_{TIMER} exceeds the upper limit value of 1.35V, the GATE is pulled down, and the chip enters the auto-retry process.

When the surge ends, the power-limiting function will be disabled. When the load current is higher than the limit value, the chip will turn off the MOSFET after the timing period.

DETAILED DESCRIPTION (continued)

The Action of a Constant Power Engine

Figure 7 shows the operation of constant power function. After the PROG is connected to a resistor, it is used to program the power-limiting of 54W. At this time, the current starts to flow through the MOSFET. When the V_{DS} of MOSFET is 12V, the maximum allowable current is 4.5A (54W divided by 12V). As the V_{DS} voltage decreases, the current will gradually increase. Figure 7 shows the measured power of MOSFET. The power remains essentially constant during operation until the current limit is reached. The constant power function allows the MOSFET to work close to its SOA area, thereby reducing the constant power time and the size of the MOSFET.

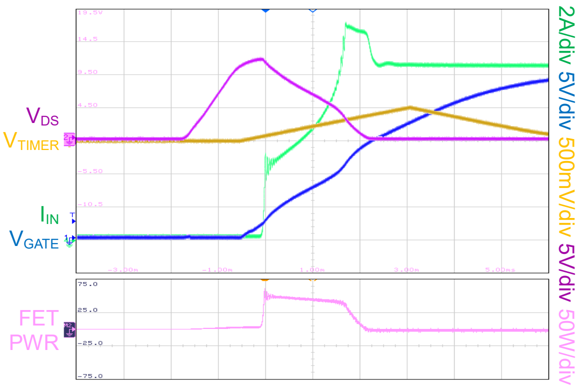


Figure 7. Computation of M_1 Power Stress during Startup

Circuit-Breaker and Fast-Trip

By monitoring the voltage across R_{SENSE}, the SGM25711B measures load current. The SGM25711B offers two limit thresholds: a current limit threshold and a fast-trip shutdown threshold.

The circuit-breaker mode and fast-trip turn-off are shown in Figure 8 through Figure 11.

Figure 8 shows the performance of the chip when the load current is higher than the current limit but below the fast-trip shutdown threshold. When this happens, the controller adjusts the gate voltage to adjust the current flowing through R_{SENSE} to the set current. At the same time, the C_{TIMER} is charged with a 10μA current source. When the V_{TIMER} reaches the upper limit of 1.35V, the MOSFET is turned off, and the chip is restarted cyclically. At the same time, the nFLT pin is pulled down to indicate a fault.

Figure 10 and Figure 11 show the behavior when a fast-trip shutdown occurs. The function of fast-trip shutdown is to prevent the system from being cut off quickly in case of serious failure. When the R_{SENSE} voltage exceeds the fast-trip shutdown threshold, the gate charge is immediately pulled down to GND by the large current source, and the resistance is about 3.2Ω at this time. The turn-off current can be changed by a low value resistance connected in series between GATE pin and gate of the MOSFET. After a few milliseconds of fast-trip, the gate voltage rises again and the circuit restarts.

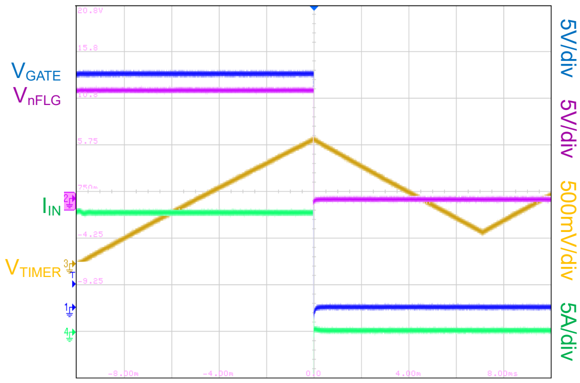


Figure 8. Circuit-Breaker Mode during Overload

DETAILED DESCRIPTION (continued)

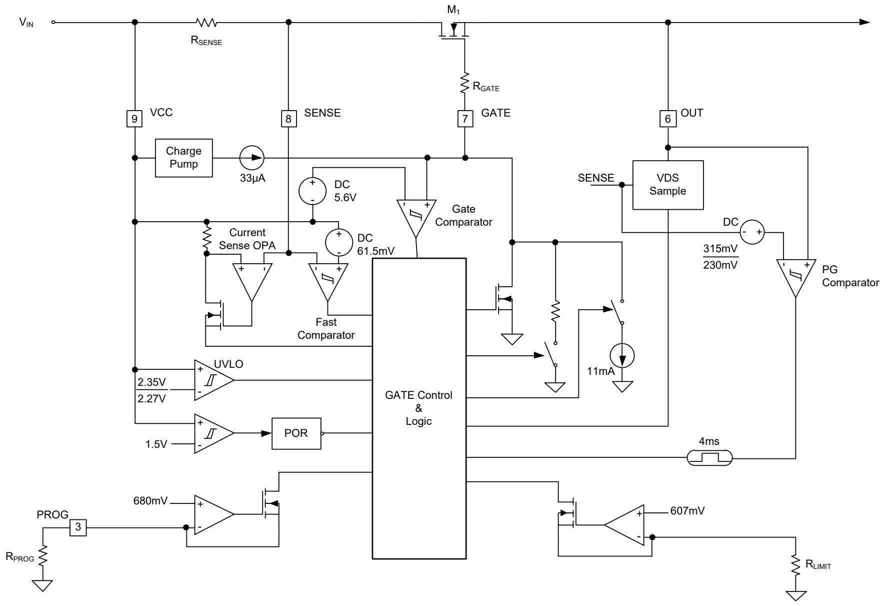


Figure 9. Partial Diagram of the SGM25711B with Selected External Components

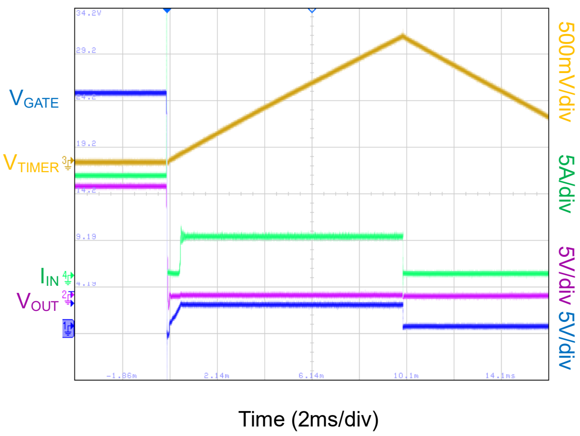


Figure 10. Current Limit during Output Short-Circuit (Overview)

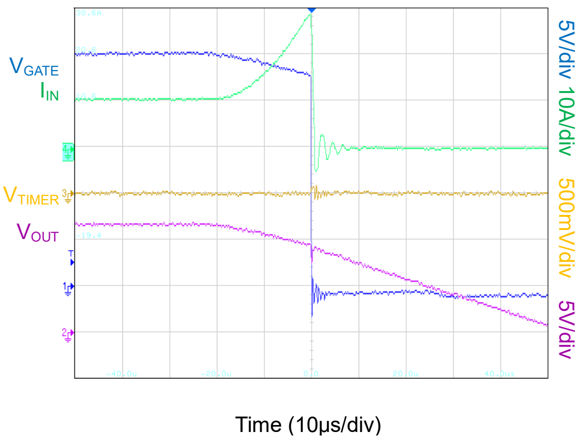


Figure 11. Current Limit during Output Short-Circuit (Onset)

Auto-Retry

SGM25711B will turn off the MOSFET and restart automatically when a fault occurs. Restart the MOSFET after 16 timing cycles, as shown in Figure 12. When the fault still exists, the timing and restart will continue. At this time, the charging and discharging currents are the same. In the first cycle, the TIMER voltage rises from 0V to 1.35V and then drops to 0.35V. For the next 16 counting cycles, 0.35V is used as low threshold cycle. This will reduce the thermal stress caused to MOSFET restarting.

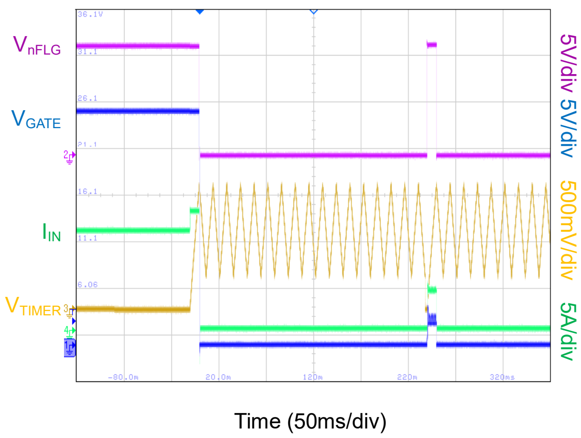


Figure 12. Auto-Retry Cycle Timing

DETAILED DESCRIPTION (continued)

nPG, nFLT and TIMER Operations

The nPG adds the deglitched design inside, which changes to active-low after C_{OUT} is fully charged for 4ms, providing sufficient margin for various unstable situations at power-up.

Make sure that the chosen MOSFET on-resistance is as small as possible, and in order for the system to operate in a safe temperature or electrical environment, the nPG will change to a high-impedance state when the on-voltage drop of the MOSFET is greater than 315mV to send a warning to the downstream device.

When the over-current condition occurs, an internal 10μA current source charges the C_{TIMER} and starts fault timing, and when the voltage of the C_{TIMER} reaches 1.35V, the nFLT pin is pulled low, otherwise the high-impedance state continues.

The fault timer starts counting at any of the following moments:

1. During start-up, if $V_{(GATE - VCC)}$ rises to the voltage of timer activation before V_{TIMER} reaches 1.35V, the device assumes that the MOSFET can start normally, the fault timer will shut down. If the $V_{(GATE - VCC)}$ is less than the voltage of timer activation within the fault time set by the C_{TIMER}, the MOSFET will be shut down and enter an auto-retry.

2. When the over-current condition occurs, the C_{TIMER} is charged from 0V to 1.35V starting with the GATE pin which is pulled low. After fault timer period, the TIMER will enter the auto-retry mode.

3. After an output short-circuit causes an over-current, the MOSFET is quickly shut down. The C_{TIMER} is charged from 0V to 1.35V starting the GATE pin which is pulled low. After fault timer period, the TIMER will enter the auto-retry mode.

If the load returns below the programmed current limit value during the restart period, the MOSFET turns on after the V_{TIMER} drops to 0V.

During the restart period, C_{TIMER}'s 16^{th} discharge until V_{TIMER} is pulled down to 0V, after the GATE pin briefly opens for the first half-cycle of the charge. This cyclical process continues until the failure is recovered or the device is disabled by EN or UVLO.

Over-Temperature Shutdown (OTSD)

Over-temperature protection circuitry has also been added inside the device, and when the temperature exceeds +145℃, the MOSFET will be turned off and the nFLT, nPG pins will enter into high-impedance state. The recovered temperature hysteresis is 15℃.

Startup of Hot Swap Circuit by VCC or EN

When EN or UVLO reaches the upper threshold, the device charges the GATE pin, and after the inrush process, M_1 is fully turned on.

M_1 will be shut down when EN under-voltage, load over-current, short-circuit, or over-temperature occurs.

1. If the following happens, the GATE is pulled low by an 11mA current source.

- The fault timer expires during an overload current fault ($V_{(VCC - SENSE)}$ > 25mV).
- The value of V_{EN} is less than the falling threshold voltage.
- The value of V_{CC} is lower than the UVLO threshold.

2. When the output hard short occurs and the $V_{(VCC - SENSE)}$ is higher than the fast-trip shutdown threshold (61.5mV), the GATE is pulled down through an N-MOSFET (3.2Ω when V_{DS} = 0.2V) by 13.5μs. After the fast-trip shutdown is complete, a continuous current of 11mA ensures that the external MOSFET remains shutdown.

3. If the die temperature is higher than the OTSD rising threshold, GATE pin is discharged to GND by a 17.5kΩ resistor.

APPLICATION INFORMATION

SGM25711B is a hot swap controller used to limit inrush current and protect loads device. Please take special care of below factors before designing.

- Startup.
- Output shorted to ground when hot swap controller is on.
- Start-into-shorted.
- SOA of MOSFET.

Typical Application

Please refer to the detailed design procedure of this section as a calculating example. Related parameters are shown in the following table.

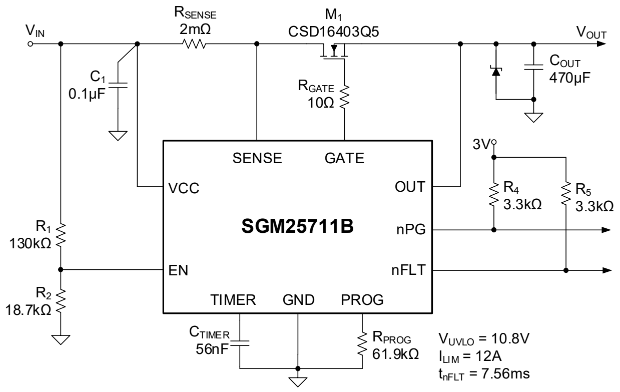


Figure 13. Typical Application (12V at 10A)

Design Requirements

Table 1 lists the necessary parameters which are needed to know before designing.

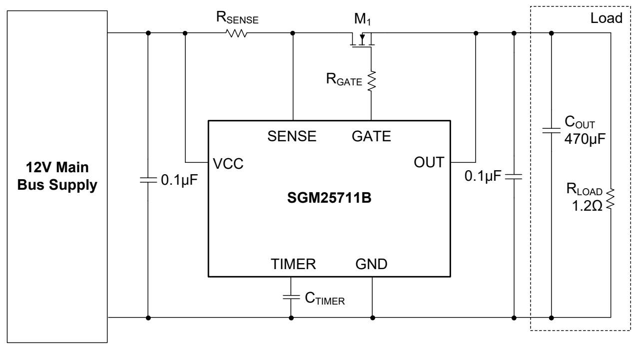
Table 1. Design Parameters

Parameter	Value
Input Voltage	12V
Operating Load Current (MAX)	10A
Operating Temperature	+20℃ to +50℃
Fault Trip Current	12A
Load Capacitance	470μF

Power-Limiting Startup

This application example assumes 12V system power supply with the swinging range of ±2V, 10A stable output current with over-current limit value of 12A with the +20℃ to +50℃ operating temperature range. A 470μF output capacitor is set. Please refer to Figure 14 for more details.

Take all factors and conditions of M_1 such as the operating temperature, package, R_{DSON}, fault timeout, current limit and power-limiting into consideration. The design procedure is intend to keep the MOSFET operating in safe area and restart in time after power-limiting. Please adapt this design procedure to fit the application.



Specifications (at Output): Peak Current Limit: 12A, Nominal Current: 10A.

Figure 14. Simplified Block Diagram of the System Constructed

APPLICATION INFORMATION (continued)

Choose R_{SENSE}

The current limit voltage threshold is about 25mV according to the electrical characteristics table. Choose a resistance of 2mΩ to realize the peak current limit of 12A. Please take care of the power loss of the resistance and choose suitable specifications.

$$R_{SENSE} = \frac{V_{(VCC\text{ - }SENSE)}}{I_{LIM}}$$

therefore,

$$R_{SENSE} = \frac{25mV}{12A} \approx 2m\Omega \quad (6)$$

Choose M_1

The SGM25711B is designed for MOSFET with a gate-source voltage rating of 20V.

Lower gate-source voltage MOSFET can be used with an external Zener diode to keep the peak value of gate-source voltage in absolute ratings.

Another factor must be considered is drain-to-source voltage. So it is recommended that add an external TVS to the input end. Extreme conditions of abrupt shutoff or short-circuit will cause the surge in input voltage. Besides, please use MOSFET with the $V_{DS(MAX)}$ rating at least twice as the power supply value.

Voltage across the MOSFET should less than minimum nPG threshold of 235mV. A maximum on-resistance of 19mΩ is required under the condition of 12A current limit. Besides, please refer to Equation 7 to calculate the maximum on-resistance at the corresponding ambient temperature.

$$R_{DSON(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{I_{MAX}{}^2 \times R_{\theta JA}}$$

therefore,

$$R_{DSON(MAX)} = \frac{150℃\text{ - }50℃}{(12A)^2 \times 51℃/W} = 13.6m\Omega \quad (7)$$

Considering all these factors, choose CSD16403Q5 as the switch device for the example. This transistor has a $V_{GS(MAX)}$ rating of 16V, a $V_{DS(MAX)}$ rating of 25V, and a maximum R_{DSON} of 2.8mΩ at room temperature. The device can hold up to 10A current flowing through during normal operation. The power dissipation of the MOSFET is about 0.24W and a 9.6℃ rise in junction temperature.

Power dissipation of the MOSFET must be kept in SOA as the power consumption during a fault is much larger than it in steady-state.

Choose P_{LIM} and R_{PROG}

The M_1 consumes large power during start-up. Please avoid the device rising temperature to an absolute maximum value ($T_{J(MAX)2}$) for a short period of time. Assuming the value is 130℃, refer to the Equation 8 to calculate the minimum P_{LIM}.

$$P_{LIM} \le 0.8 \times \frac{T_{J(MAX)2} - \left[\left(I_{MAX}{}^2 \times R_{DSON} \times R_{\theta CA}\right) + T_{A(MAX)}\right]}{R_{\theta JC}}$$

therefore,

$$P_{LIM} \le 0.8 \times \frac{130℃ - \left[\left(12A^2 \times 0.002\Omega \times (51℃/W\text{-}1.8℃/W)\right) + 50℃\right]}{1.8℃/W} = 29.3W \quad (8)$$

If the operating temperature is 50℃, the P_{LIM} (MAX) is 29.3W. The minimum R_{PROG} can be calculated using Equation 9.

$$R_{PROG} = \frac{3600}{P_{LIM} \times R_{SENSE}}$$

therefore,

$$R_{PROG} = \frac{3600}{29.3W \times 0.002\Omega} = 61.4k\Omega \quad (9)$$

Choose a resistor that is closer but larger than the calculated value. In this case, it is recommended to choose a 61.9kΩ (1%) resistor, which sets a power limit of 29.1W.

Choose Output Voltage Rise Time (t_{ON}), C_{TIMER}

Please make sure the load capacitance is fully charged before the timing period set by timer capacitor stops. So that the system will not trigger the fault circuit. Please refer to Equation 10 for more details.

Assuming that there is no resistive load at the startup time.

$$t_{ON} = \begin{cases} \frac{C_{OUT} \times P_{LIM}}{2 \times I_{LIM}{}^2} + \frac{C_{OUT} \times V_{CC(MAX)}{}^2}{2 \times P_{LIM}} - \frac{C_{OUT} \times V_{CC(MAX)}}{I_{LIM}} & \text{if } P_{LIM} < I_{LIM} \times V_{CC(MAX)} \\ \frac{C_{OUT} \times V_{CC(MAX)}}{I_{LIM}} & \text{if } P_{LIM} > I_{LIM} \times V_{CC(MAX)} \end{cases}$$

therefore,

$$t_{ON} = \frac{470\mu F \times 29.3W}{2 \times (12A)^2} + \frac{470\mu F \times (12V)^2}{2 \times 29.3W} - \frac{470\mu F \times 12V}{12A} = 0.73ms \quad (10)$$

APPLICATION INFORMATION (continued)

The t_{ON} calculated in Equation 10 only takes the voltage rise in OUT capacitor into consideration. Besides, when consider the time margin set by the timing capacitor, add up the time which takes to charge the GATE pin voltage to 5.6V above the input voltage. Please refer to the Equation 11.

$$t_{nFLT} = t_{ON} + \frac{5.6V \times C_{ISS}}{I_{GATE}}$$

therefore,

$$t_{nFLT} = 0.73ms + \frac{5.6V \times 2040pF}{20\mu A} = 1.3ms \quad (11)$$

It should learn about the I_{GATE} is 20μA and C_{ISS} is 2040pF through respective electrical characteristic. By using the example parameters, it is easy to get that the CSD16403Q5 takes 1.3ms as the fault time. Please also kindly refer to the SOA curves of MOSFET for circuit safety. The fault timer should be set higher than 1.3ms to avoid power loss during startup and below the corresponding time of the SOA curve at the specified operating temperature.

Factors such as temperature, component tolerance and load characteristics, choose 7ms as the fault time to reserve sufficient margin. Choose the second highest capacitor specification is 56nF and the final failure time is 7.56ms.

$$C_{TIMER} = \frac{10\mu A}{1.35V} \times t_{nFLT}$$

therefore,

$$C_{TIMER} = \frac{10\mu A}{1.35V} \times 7ms = 52nF \quad (12)$$

Calculate the Auto-Retry Mode Duty Ratio

Learn about the device will be charged and discharged 16 times as Figure 12. Note that the timer capacitor will charge from 0V to 1.35V and discharge from 1.35V to 0.35V. So, the total time is 7.56ms + 33 × 5.6ms = 192.36ms. The auto-retry mode duty cycle is 7.56ms/192.36ms = 3.93%.

Select the R_1 and R_2 for Under-Voltage

Next, select the value of the divider resistance of the UVLO pin as Figure 1 according to the V_{ENTH} value of 1.35V in electrical specifications.

$$V_{ENTH} = \frac{R_2}{R_1 + R_2} \times V_{CC} \quad (13)$$

If R_1 is 130kΩ, the value of R_2 can be calculated as 18.7kΩ.

Select R_4, R_5, R_{GATE} and C_1

Choose the appropriate gate resistor based on the actual input capacitance value of MOSFET, and if the C_{ISS} of the MOSFET is less than 200pF, a gate resistance of 33Ω is recommended. In addition, if required, assign 3.3kΩ pull-up resistors to the nFLT and nPG pins, as they are open-drain outputs. C_1 is a bypass capacitor and ceramic capacitors which are smaller than 100nF are recommended.

Use of nPG

To avoid undesired latch-up of the downstream DC/DC converter, please use nPG to control the enable pin of the DC/DC converter instead of connect the C_{OUT} of the hot swap controller to the VIN pin of the downstream device directly. It also can use a long time delay to make sure the fully charge of the C_{OUT}.

Output Clamp Diode

To avoid inverting condition of the OUT pin caused by inductive loads transients or current limit, please connect a Schottky diode to the OUT end.

Gate Clamp Diode

To keep the V_{GS} of M_1 in absolute rating, connect an external clamp Zener to the gate and source of the M_1 if it is needed. Please also connect a series resistance or a silicon diode to cut off the output capacitance discharging path through GATE pin.

High Gate Capacitance Applications

Once the gate capacitance (total) of the MOSFET is larger than 4000pF, use an external Zener diode to gate voltage overstress or fault current spikes.

Bypass Capacitors

To avoid large inrush current during plug-in period, please use suitable low-impedance ceramic capacitor (10nF to 0.1μF is recommended).

APPLICATION INFORMATION (continued)

Using Soft-Start with SGM25711B

It can connect a capacitor from GATE to GND if the constant output slew rate of the hot swap controller is needed. The ramp rate of the GATE pin voltage is also reflected at the output.

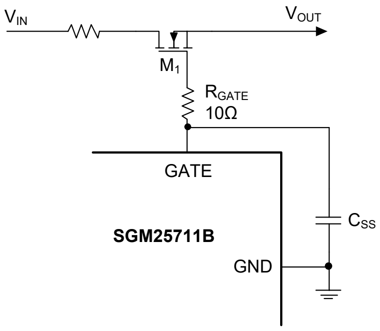


Figure 15. Simplified Schematic for Using Soft-Start

Power Supply Recommendations

Use a 10nF to 1μF ceramic capacitor and a TVS to bypass the VCC to GND.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

MAY 2025 – REV.A.2 to REV.A.3	Page
Updated Absolute Maximum Ratings section	2
Updated Electrical Characteristics Section	4

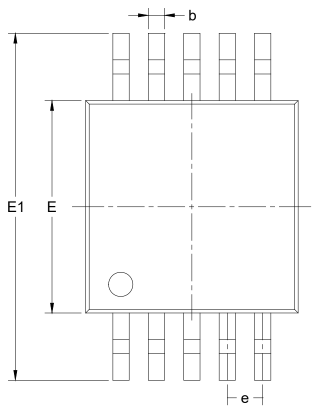
OCTOBER 2024 – REV.A.1 to REV.A.2	Page
Updated Typical Application section	1
Updated Absolute Maximum Ratings section	2
Updated Application Information section	17, 18, 19
Updated Package Outline Dimensions section	21

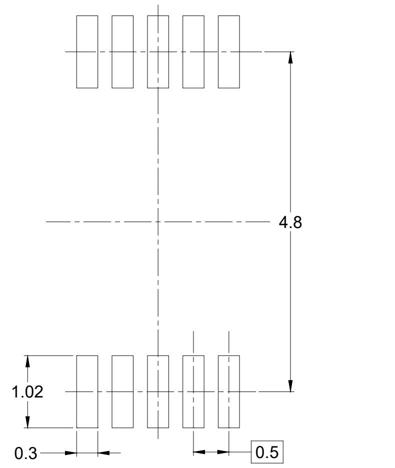
OCTOBER 2022 – REV.A to REV.A.1	Page
Update Detailed Description	All
Update Application Information section	12, 18

Changes from Original (OCTOBER 2021) to REV.A	Page
Changed from product preview to production data	All

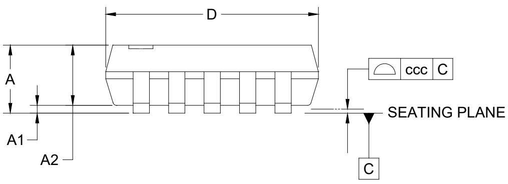
PACKAGE OUTLINE DIMENSIONS

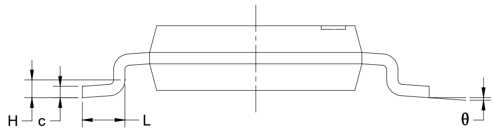
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)



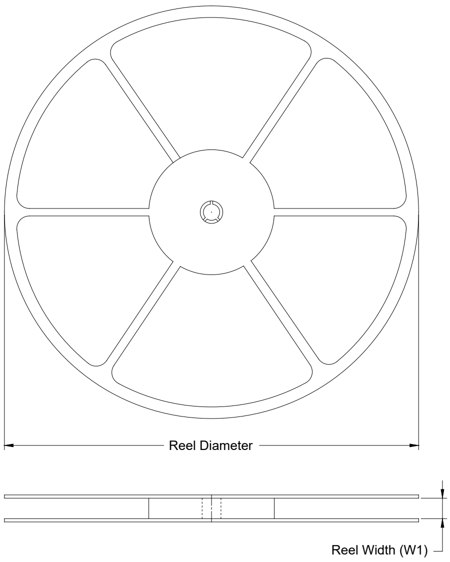


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.170	-	0.330
c	0.080	-	0.230
D	2.900	-	3.100
E	2.900	-	3.100
E1	4.750	-	5.050
e	0.500 BSC		
H	0.250 TYP		
L	0.400	-	0.800
θ	0°	-	8°
ccc	0.100		

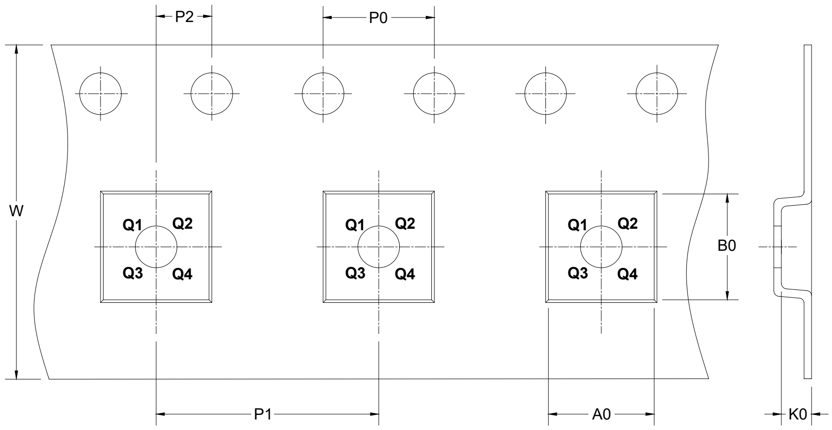
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

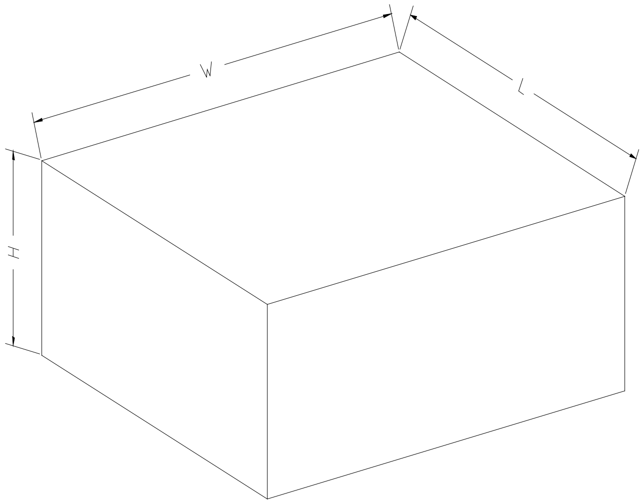
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002