# SGM8607-2 1.2MHz, High Precision, Rail-to-Rail I/O, Dual SGM1CRO CMOS Operational Amplifier in WLCSP Package

#### **GENERAL DESCRIPTION**

The SGM8607-2 integrates a dual, high precision, low noise, low voltage and low power CMOS operational amplifier in a small, 9-ball WLCSP package. It can operate from 1.8V to 5.5V power supply over the -40°C to +125°C temperature range or operate from 1.7V to 5.5V power supply over the 0°C to +70°C temperature range. The SGM8607-2 supports rail-to-rail input and output operation. The input common mode voltage range is from (-V<sub>S</sub>) - 0.1V to (+V<sub>S</sub>) + 0.1V, and the output range is from (-V<sub>S</sub>) + 0.032V to (+V<sub>S</sub>) - 0.05V with 600 $\Omega$  load resistor.

The SGM8607-2 features an input offset voltage of  $30\mu V$  (MAX), a gain-bandwidth product of 1.2MHz, and a slew rate of  $0.6V/\mu s$ .

The SGM8607-2 is available in a Green WLCSP-1.2×1.2-9B-A package. It is specified over the extended industrial temperature range (-40°C to +125°C).

#### **APPLICATIONS**

Sensors

Audio

Active Filters

A/D Converters

Communications

Test Equipment

Cellular and Cordless Phones

Laptops and PDAs

Photodiode Amplification

#### **FEATURES**

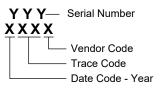
- Low Input Offset Voltage: 30μV (MAX)
- Low Input Bias Current: 70pA (TYP)
- Input Voltage Noise Density: 27nV/√Hz at 10kHz
- Gain-Bandwidth Product: 1.2MHz
- Gain = +20 Stable for C<sub>L</sub> = 1nF
   Unity-Gain Stable for C<sub>L</sub> = 100pF
- Slew Rate: 0.6V/μs
- Settling Time to 0.1% with 200mV Step: 1µs
- Overload Recovery Time: 0.5μs
- Rail-to-Rail Input and Output
- Power Supply Voltage:
  - Low 1.8V Supply Rail over the -40°C to +125°C Range
- Low 1.7V Supply Rail over the 0°C to +70°C Range
- High Supply Voltage: 5.5V
- Input Signal Range: (-V<sub>S</sub>) 0.1V to (+V<sub>S</sub>) + 0.1V
- Low Power:
  - 140µA (TYP) Quiescent Current
  - 0.6µA (MAX) Supply Current in Shutdown
- Available in a Green WLCSP-1.2×1.2-9B-A Package

#### PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8607-2	WLCSP-1.2×1.2-9B-A	-40°C to +125°C	SGM8607-2XG/TR	01I XXXX	Tape and Reel, 3000

#### MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, +V <sub>S</sub> to -V <sub>S</sub>	6.0V
Input Common Mode Voltage Range	
(-V <sub>S</sub> ) -	$0.3V$ to $(+V_S) + 0.3V$
Package Thermal Resistance	
WLCSP-1.2×1.2-9B-A, θ <sub>JA</sub>	109.2°C/W
WLCSP-1.2×1.2-9B-A, θ <sub>JB</sub>	43.2°C/W
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility (1)(2)	
HBM	±4000V
CDM	±1000V

#### NOTES:

- 1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
- 2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

#### RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range .....-40°C to +125°C

#### **OVERSTRESS CAUTION**

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

#### **ESD SENSITIVITY CAUTION**

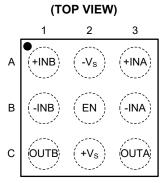
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

#### **DISCLAIMER**

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.



# **PIN CONFIGURATION**



WLCSP-1.2×1.2-9B-A

# **PIN DESCRIPTION**

PIN	NAME	FUNCTION
A1	+INB	Non-Inverting Input of Amplifier B.
A2	-Vs	Negative Power Supply.
A3	+INA	Non-Inverting Input of Amplifier A.
B1	-INB	Inverting Input of Amplifier B.
B2	EN	Active High Enable Input. When EN = High, the SGM8607-2 is in active status. When EN = Low, the SGM8607-2 is in shutdown status.
В3	-INA	Inverting Input of Amplifier A.
C1	OUTB	Output of Amplifier B.
C2	+V <sub>S</sub>	Positive Power Supply.
C3	OUTA	Output of Amplifier A.

# **ELECTRICAL CHARACTERISTICS**

 $(V_S = 3.3V, V_{CM} = V_S/2, V_{EN} = +V_S, Full = -40^{\circ}C$  to +125°C, typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted.)

PARAMETER	CONDITIO	ONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage ()/	\/ - E\/		+25°C		±5	±30	\/
Input Offset Voltage (Vos)	V <sub>S</sub> = 5V		Full			±90	μV
Input Offset Voltage Drift ( $\Delta V_{OS}/\Delta T$ )			Full		120	600	nV/°C
Input Bias Current (I <sub>B</sub> )	V <sub>S</sub> = 1.8V to 5.5V		+25°C		±70	±2000	pА
input Bias Current (IB)	V <sub>S</sub> = 1.6V to 5.5V		Full			±9	nA
Input Offset Current (I <sub>OS</sub> )	V <sub>S</sub> = 1.8V to 5.5V		+25°C		±140		pА
Input Common Mode Voltage Range ( $V_{\text{CM}}$ )			Full	(-V <sub>S</sub> ) - 0.1		$(+V_S) + 0.1$	V
Common Mode Pointing Patie (CMPP)	( ) ( ) ( ) ( ) ( ) ( ) ( ) ( ) ( )	) ± 0 1)/	+25°C	98	114		٩D
Common Mode Rejection Ratio (CMRR)	$(-V_S) - 0.1V \le V_{CM} \le (+V_S)$	5) + 0.10	Full	95	±5  120 ±70  ±140		dB
	(-V <sub>S</sub> ) + 0.25V < V <sub>OUT</sub> < (-	+V <sub>s</sub> ) - 0.25V,	+25°C	101	114		
Open-Loop Voltage Gain (A <sub>OL</sub> )	$R_L = 600\Omega$		+25°C Full +25°C Full +25°C Full +25°C Full +25°C Full	98			dB
Open-Loop Voltage Gaill (AoL)	$(-V_S) + 0.1V < V_{OUT} < (+)^{-1}$	s) - 0.1V, +25°C Full	102	120		ub	
	$R_L = 10k\Omega$	,	Full	99			
Input Capacitance (C <sub>IN</sub> )			+25°C		30		pF
Output Characteristics							
	V <sub>OL</sub> = V <sub>OUT</sub> - (-V <sub>S</sub> )	D = 6000	+25°C		32	50	- mV
Output Voltage Law		RL - 60002	Full			70	
Output Voltage Low	VOL - VOUT - (-Vs)	B = 10k0	+25°C		2	5	
		K 10K22	Full			7	
		B = 6000	+25°C	(-V <sub>s</sub> ) - 0.1 98 95 101 98 102 99 102 99 103 104 105 106 107 108 109 109 109 109 109 109 109 109	50	65	
Output Voltage Lligh	$V_{OH} = (+V_S) - V_{OUT}$	KL - 00022	Full			92	mV
Output Voltage High	VOH - (+Vs) - VOUT	D = 10k0	+25°C		3	7	IIIV
		Kr - 10K2	Full			9	
Output Short-Current Limited (I <sub>LIM</sub> )	Short to +V <sub>S</sub> or -V <sub>S</sub>		+25°C		±28		mA
Power Supply							
			Full	1.8		5.5	
Operating Voltage Range (V <sub>S</sub> )				1.7		5.5	<b>V</b>
Power Supply Rejection Ratio (PSRR)	$V_{\rm S}$ = 1.8V to 5.5V, $V_{\rm CM}$ =	( ) ( ) + 0.5)/	+25°C	100	124		dB
1 ower oupply rejection read (Form)	vs - 1.0v to 5.5v, v <sub>CM</sub> -	(-vs) · 0.5v	Full	97			שט
Quioscont Current (I-)	J = 0A		+25°C		140	195	^
Quiescent Current (I <sub>Q</sub> )	I <sub>OUT</sub> = 0A		Full			235	μA
Shutdown Supply Current (I <sub>SHDN</sub> )	I <sub>OUT</sub> = 0A, V <sub>EN</sub> = -V <sub>S</sub>		+25°C			0.6	μA

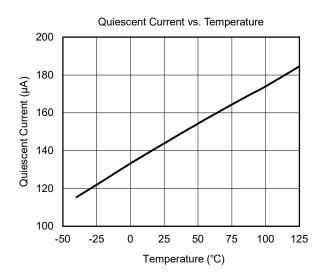
# **ELECTRICAL CHARACTERISTICS (continued)**

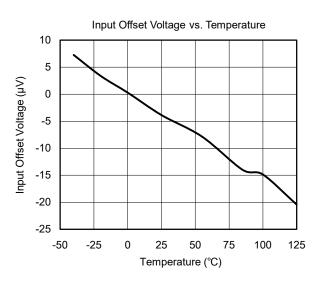
 $(V_S = 3.3V, V_{CM} = V_S/2, V_{EN} = +V_S, Full = -40^{\circ}C$  to +125°C, typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted.)

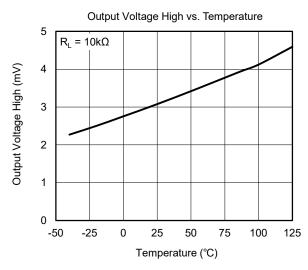
PARAMETER	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Dynamic Performance	•					•
Gain-Bandwidth Product (GBP)		+25°C		1.2		MHz
Phase Marain (a.)	$G = +20$ , $R_L = 10kΩ$ , $C_L = 1nF$	+25°C		56		۰
Phase Margin (φ <sub>0</sub> )	$G = +1$ , $R_L = 10$ kΩ, $C_L = 100$ pF	+25°C		55		
Slew Rate (SR)	G = +1, 2V output step	+25°C		0.6		V/µs
Settling Time to 0.1% (t <sub>S</sub> )	G = +1, 200mV output step	+25°C		1		μs
Overload Recovery Time (ORT)	V <sub>IN</sub> × G = V <sub>S</sub>	+25°C		0.5		μs
Noise Performance						
Input Voltage Noise	f = 0.1Hz to 10Hz	+25°C		0.4		μV <sub>P-P</sub>
Input Voltage Noise Density (e <sub>n</sub> ) (1)	f = 10kHz	Full		27	55	nV/√Hz
EN Control	•					
Input Voltage Low (V <sub>IL</sub> )	+V <sub>S</sub> = 1.8V to 5.5V, -V <sub>S</sub> = GND	Full			0.4	V
Input Voltage High (V <sub>IH</sub> )	$+V_{S}$ = 1.8V to 5.5V, $-V_{S}$ = GND	Full	1.7			V
Turn On Time from Shutdown (4——)		+25°C		275	420	
Turn-On Time from Shutdown (t <sub>SHDN</sub> )		Full			600	μs
Power-Up Time (t <sub>ON</sub> ) (1)		Full		0.6	1.2	ms

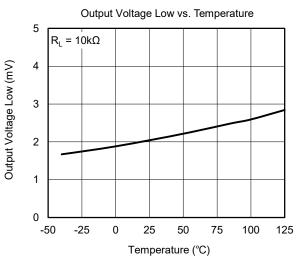
NOTE: 1. Limits are specified by design and characterization, not production tested.

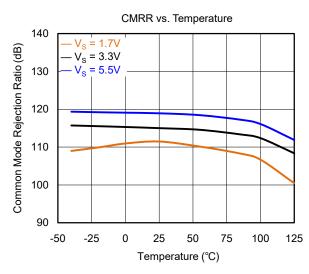
#### TYPICAL PERFORMANCE CHARACTERISTICS

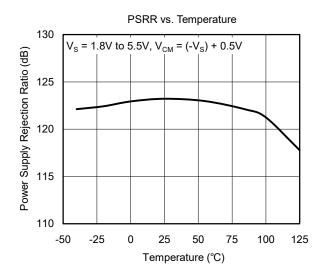


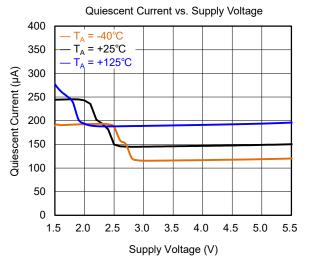


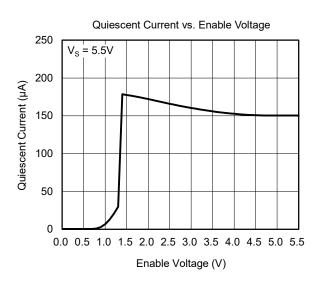


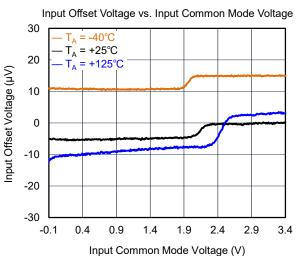


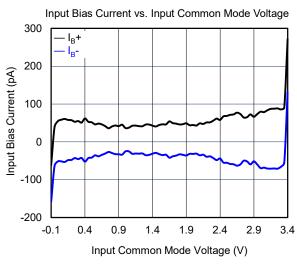


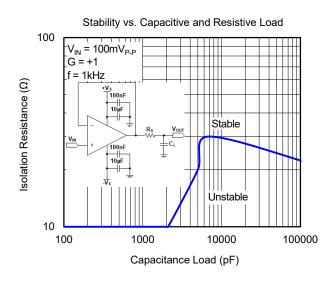


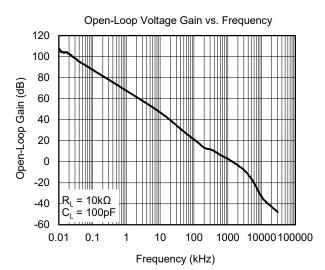


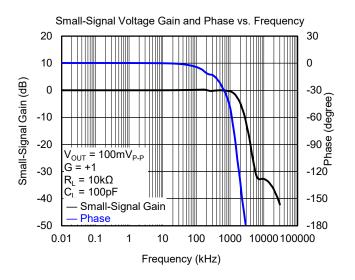


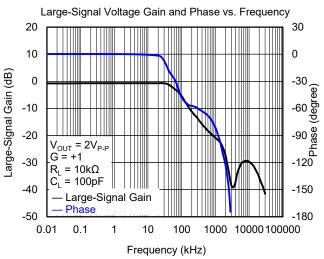


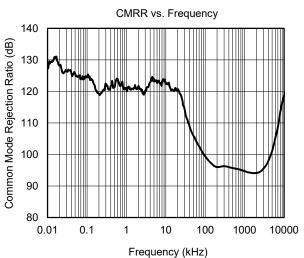


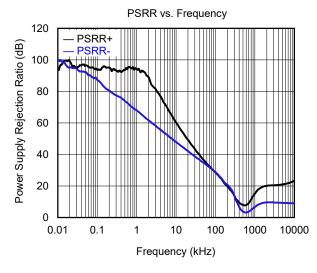


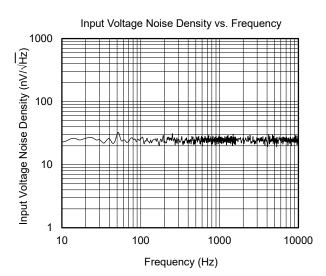


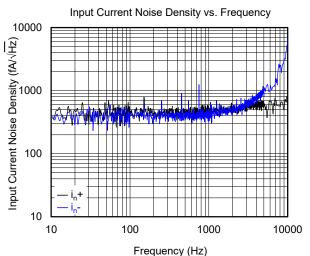


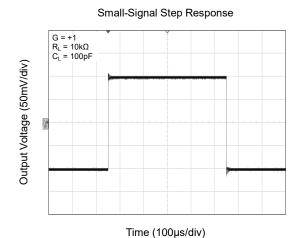


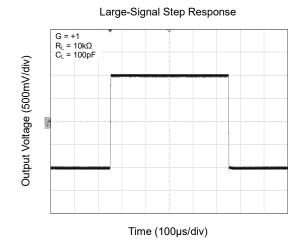


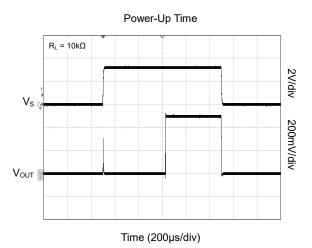


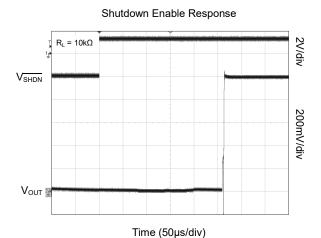


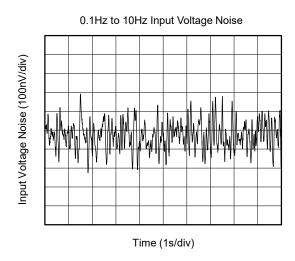


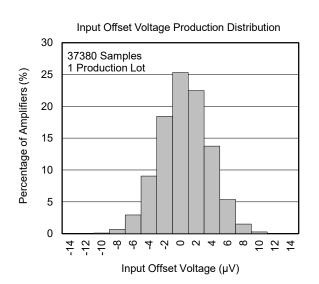


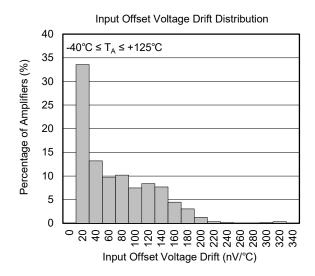












#### APPLICATION INFORMATION

#### Rail-to-Rail Input

The input common mode voltage range of the SGM8607-2 extends 100mV beyond the supply rails for the full supply voltage range. In Figure 1, the ESD diodes between the inputs and the power supply rails will clamp the input voltage so that it does not exceed the rails.

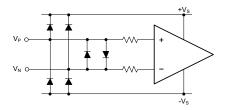


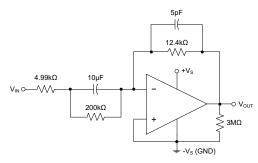
Figure 1. Input Equivalent Circuit

#### **Input Current-Limit Protection**

For ESD diode clamping protection, when the current flowing through ESD diode exceeds the maximum rating value, the ESD diode and amplifier will be damaged, so current-limit protection will be added in some applications. One resistor is selected to limit the current not to exceed the maximum rating value. In Figure 2, a series input resistor is used to limit the input current, but the drawback of this current-limit resistor is that it contributes thermal noise at the amplifier input. If this resistor must be added, its value must be selected as small as possible.

In addition, a clamping circuit on its inputs can sink current (up to 20mA) when the input is (+V<sub>S</sub>) + 0.3V. This is for protecting from a worst  $V_{\rm IN}$  short-circuit condition, and any alternate would need to have some sort of clamping behavior on its inputs. But in the shutdown mode, the clamping circuit does not work.

In the circuit (Figure 2), the operational amplifier inputs can handle a  $V_{\text{IN}}$  pulse (20V pulses width 1 $\mu$ s, rise and fall times 1ns).



NOTE: A current-limit resistor is required if the input voltage exceeds the supply rails by  $\geq 0.3V$ .

Figure 2. Input Current-Limit Protection

#### Rail-to-Rail Output

The SGM8607-2 supports rail-to-rail output operation. In single power supply application, for example, when  $+V_S = 3.3V$ ,  $-V_S = GND$ ,  $600\Omega$  load resistor is tied from OUT pin to ground, the typical output swing range is from 0.032V to 3.25V.

#### **Driving Capacitive Loads**

The SGM8607-2 can directly drive a 1nF capacitor at Gain =  $\pm$ 20 or a 100pF capacitor at Gain =  $\pm$ 1 without oscillation. If greater capacitive load must be driven in application, the circuit in Figure 3 can be used. In this circuit, the IR drop voltage generated by R<sub>ISO</sub> is compensated by feedback loop.

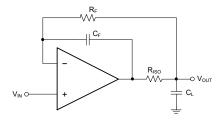


Figure 3. Circuit to Drive Heavy Capacitive Load

#### Power Supply Decoupling and Layout

A clean and low noise power supply is very important in amplifier circuit design. Besides of input signal noise, the power supply is one of important source of noise to the amplifiers through  $+V_S$  and  $-V_S$  pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. In application,  $10\mu F$  ceramic capacitor paralleled with  $0.1\mu F$  or  $0.01\mu F$  ceramic capacitor is used in Figure 4. The ceramic capacitors should be placed as close as possible to  $+V_S$  and  $-V_S$  power supply pins.

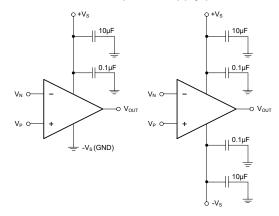


Figure 4. Amplifier Power Supply Bypassing

# **APPLICATION INFORMATION (continued)**

#### Grounding

In low speed application, one node grounding technique is the simplest and most effective method to eliminate the noise generated by grounding. In high speed application, the general method to eliminate noise is to use a complete ground plane technique, and the whole ground plane will help distribute heat and reduce EMI noise pickup.

#### **Reduce Input-to-Output Coupling**

To reduce the input-to-output coupling, the input traces must be placed as far away from the power supply or output traces as possible. The sensitive trace must not be placed in parallel with the noisy trace in the same layer. They must be placed perpendicularly in different layers to reduce the crosstalk. These PCB layout techniques will help to reduce unwanted positive feedback and noise.

# Typical Application Circuits Difference Amplifier

The circuit in Figure 5 is a design example of classical difference amplifier. If  $R_4/R_3 = R_2/R_1$ , then  $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$ .

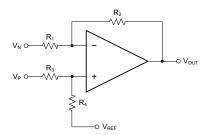


Figure 5. Difference Amplifier

#### **High Input Impedance Difference Amplifier**

The circuit in Figure 6 is a design example of high input impedance difference amplifier. The added amplifiers at the input are used to increase the input impedance and eliminate drawback of low input impedance in Figure 5.

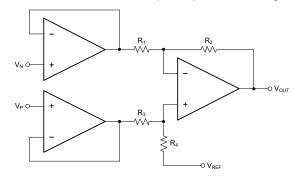


Figure 6. High Input Impedance Difference Amplifier

#### **Active Low-Pass Filter**

The circuit in Figure 7 is a design example of active low-pass filter, the DC gain is equal to  $-R_2/R_1$  and the -3dB corner frequency is equal to  $1/(2\pi R_2 C).$  In this design, the filter bandwidth must be less than the bandwidth of the amplifier, and the resistor values must be selected as low as possible to reduce ringing or oscillation generated by the parasitic parameters in PCB layout.

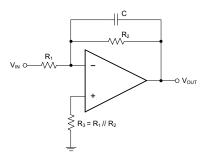


Figure 7. Active Low-Pass Filter

# SGM8607-2

# 1.2MHz, High Precision, Rail-to-Rail I/O, Dual CMOS Operational Amplifier in WLCSP Package

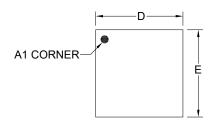
# **REVISION HISTORY**

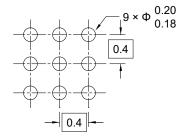
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JUNE 2025 – REV.A to REV.A.1	Page
Updated Absolute Maximum Ratings section	2
Updated Electrical Characteristics section	4, 5
Updated Typical Performance Characteristics section	
Changes from Original (DECEMBER 2023) to REV.A	Page
Changed from product preview to production data	All



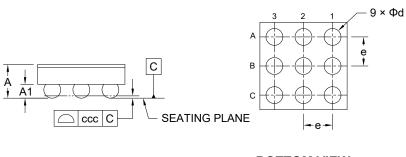
# PACKAGE OUTLINE DIMENSIONS WLCSP-1.2×1.2-9B-A





**TOP VIEW** 

RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW

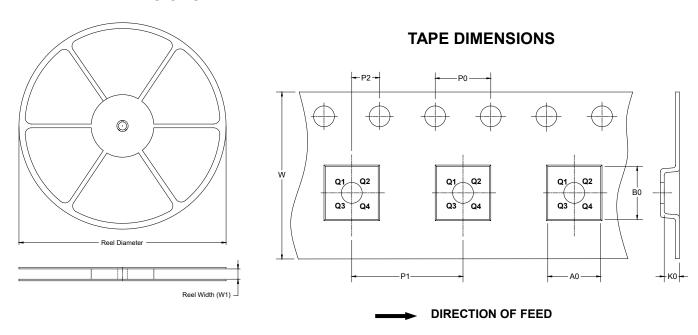
**BOTTOM VIEW** 

Symbol	Dimensions In Millimeters						
Symbol	MIN	MIN NOM					
Α	-	-	0.500				
A1	0.169	-	0.209				
D	1.170	-	1.230				
E	1.170	-	1.230				
d	0.202	-	0.262				
е	0.400 BSC						
ccc	0.050						

NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

#### **REEL DIMENSIONS**

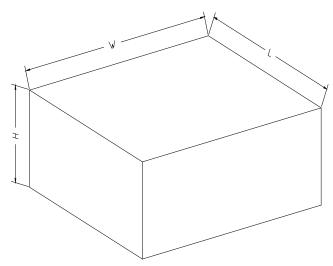


NOTE: The picture is only for reference. Please make the object as the standard.

#### **KEY PARAMETER LIST OF TAPE AND REEL**

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.2×1.2-9B-A	7"	9.2	1.31	1.31	0.58	4.0	4.0	2.0	8.0	Q1

### **CARTON BOX DIMENSIONS**



NOTE: The picture is only for reference. Please make the object as the standard.

# **KEY PARAMETER LIST OF CARTON BOX**

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18