SGM25890
High Efficiency 90A Integrated Internal Current Sense Power Stage

GENERAL DESCRIPTION

The SGM25890 consists of an integrated driver, a control MOSFET, and a synchronous MOSFET. Due to the short distance connection between the internal driver and MOSFET, SGM25890 has better timing control and smaller switch node ringing while further improving its heat dissipation capability in terms of packaging. Appropriate driver and MOSFET size allocation enables SGM25890 to have better efficiency performance in low output voltage related applications such as CPU, GPU, and DDR Memory.

Compared to traditional DCR detection schemes, the internal MOSFET current detection scheme has higher current detection accuracy to help multiphase controllers obtain more accurate current information. The SGM25890 also has universal protection functions: OTP, OCP, HSS (high-side short detection), and VDRV under-voltage protection.

The SGM25890 supports a maximum switching frequency of 1.5MHz to ensure excellent dynamic performance when paired with multiphase controllers. Reasonable area allocation of both control MOSFET and synchronous MOSFET ensures optimal efficiency for SGM25890 in applications such as CPU, GPU, and DDR memory.

The SGM25890 is available in a Green TQFN-5×6-39L package.

FEATURES

- **Integrated Driver, Synchronous MOSFET and Control MOSFET**
- **On-Chip MOSFET Current Sensing and Reporting at 5μA/A**
- **Input Voltage Range: 4.25V to 16V**
- **V_{CC} and V_{DRV} Supply: 4.5V to 5.5V**
- **Output Voltage Range: 0.225V to 5.5V at V_{IN} = 12V**
- **Output Current Capability: 90A**
- **Operation up to 1.5MHz**
- **Enhanced Fault Reporting and Identification**
- **VDRV Under-Voltage Lockout (UVLO)**
- **Temperature Analog Output: 8mV/℃**
- **Over-Temperature Protection (OTP) and Thermal Shutdown**
- **Cycle-by-Cycle Over-Current Protection (OCP) and Flag**
- **Control MOSFET Short (HSS) Detection and Flag**
- **Compatible with 3.3V Tri-State PWM Input**
- **Body-Braking Load Transient Support**
- **Deep-Sleep Mode (EN = Low)**
- **Available in a Green TQFN-5×6-39L Package**

APPLICATIONS

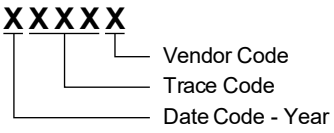
High Frequency, Low Profile DC/DC Converters
Voltage Regulators for CPUs, GPUs and DDR Memory Arrays
Telecom Controlled and Uncontrolled

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25890	TQFN-5×6-39L	-40℃ to +125℃	SGM25890XTVR39G/TR	SGM25890 XTVR39 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... -0.3V to 20V
Logic Supply Voltage ..... -0.3V to 6.5V
High and Low-side Driver Voltage ..... -0.3V to 6.5V
Switch Node Voltage, V_{SW} (DC) ..... -1V to 20V
PHASE Voltage, V_{PHASE} (DC) ..... -1V to 20V
VIN-PHASE Voltage, $V_{IN-PHASE}$ (DC) ..... -1V to 20V
BOOT Voltage, V_{BOOT_PHASE} (DC) ..... -0.3V to 6.5V
GL, EN Voltage ..... -0.3V to 6.5V
PWM Voltage ..... -0.3V to 4V
TMON/FAULT, IMON, IMONREF Voltage ..... -0.3V to 3.6V
NC Pin Voltage ..... -0.3V to 0.3V
Maximum Average Load Current 90A
Package Thermal Resistance
TQFN-5×6-39L, θ_{JA} ..... 24.8℃/W
TQFN-5×6-39L, θ_{JB} ..... 2.2℃/W
TQFN-5×6-39L, $\theta_{JC\ (TOP)}$ ..... 13.9℃/W
TQFN-5×6-39L, $\theta_{JC\ (BOT)}$ ..... 1.1℃/W
Package Thermal Characterization Parameter
TQFN-5×6-39L, ψ_{JT} ..... 0.6℃/W
TQFN-5×6-39L, ψ_{JB} ..... 2℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±500V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage ..... 4.25V to 16V
MOSFET Driver, Logic Supply Voltage ..... 4.5V to 5.5V
Frequency of the PWM ..... 100kHz to 1500kHz
EN Voltage ..... 5.5V (MAX)
PWM Voltage ..... 3.6V (MAX)
Current Sense Reference Voltage ..... 1.1V to 1.9V

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

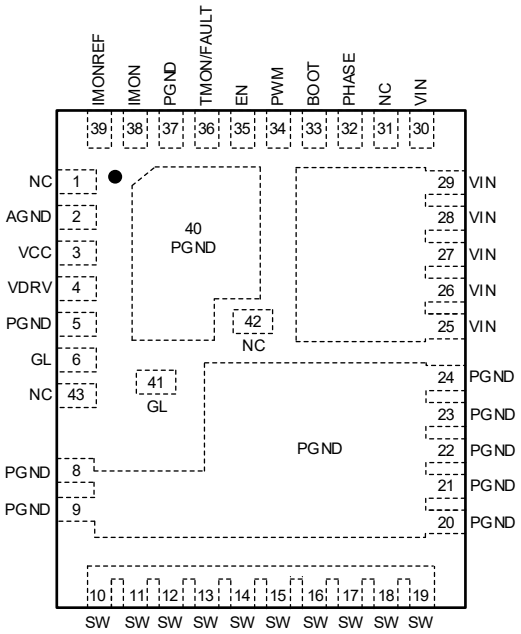
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-5×6-39L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1, 31, 42, 43	NC	—	No Connection.
2	AGND	AGND	Signal Ground.
3	VCC	P	The Supply of Control Circuit. Connect VCC to a 5V supply and a 1μF capacitor between VCC and AGND.
4	VDRV	P	The Supply of Driver. Connect VDRV to a 5V supply and a 1μF capacitor between VDRV and PGND.
5, 8, 9, 20, 21, 22, 23, 24, 37, 40	PGND	PGND	Power Ground Pin.
6, 41	GL	AIO	Low-side MOSFET Gate Pin. Test pin can be left floating
10 ~ 19	SW	AO	Switching Node.
25 ~ 30	VIN	P	Input Voltage. Place the input capacitor between VIN and PGND and try to get it as close to the chip as possible.
32	PHASE	AI	Switching Node Pin. Place the bootstrap capacitor between PHASE and BOOT.
33	BOOT	AI	Bootstrap Capacitor Connection. Connect a 0.22μF to 0.56μF ceramic capacitor between PHASE and BOOT. A bootstrap resistor in series with the bootstrap capacitor can reduce SW ringing and EMI when V_{IN} > 13.2V. Bootstrap resistor recommended value is 2Ω.
34	PWM	AIO	PWM Input Pin. PWM = high level: enables the control MOSFET. PWM = low level: enables the synchronous MOSFET. PWM = floating: tri-state mode, dual MOSFETs disabled.
35	EN	AI	Enable. EN = high level: enable the driver. EN = low level: shuts down the driver and enters ultra-low quiescent current operation mode. It is not recommended to float this pin.
36	TMON/FAULT	AO	Temperature Sense Output & Fault Indication.
38	IMON	AO	Current Sense Output.
39	IMONREF	AI	System Reference Voltage Input. It is recommended to the system reference voltage used for fault indication

NOTE: AI = analog input, AO = analog output, AIO = analog input output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{DRV} = V_{CC} = 5V, $V_{IMONREF}$ = 1.2V, typical values are at T_J = +25℃, unless otherwise noted.)

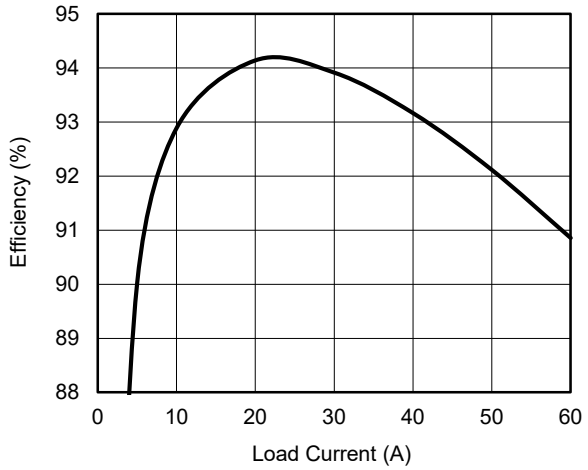
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Supply, Biasing Current						
V_{DRV} UVLO Threshold	V_{UVLO_R}	Rising		4.01	4.5	V
	V_{UVLO_F}	Falling	3.2	3.82		V
Driver Current	I_{VDRV}	EN = high, f_{SW} = 600kHz, D = 15%		33		mA
		EN = low		13		μA
Supply Current	I_{VCC}	EN = high, f_{SW} = 600kHz, D = 15%		8		mA
		EN = low		104		μA
VIN Current	I_{VIN}	EN = low, no switching			1	μA
Current Sense						
IMON Voltage Range	V_{IMON}	DC + AC components (1)	0.8		2.35	V
Current Sense Gain	A_{CS}			5		μA/A
IMON Gain Resistor Range	R_{IMON}	R_{IMON} (between IMON and IMONREF): 1kΩ (±1%) recommended (5mV/A)		1		kΩ
Temperature Sense and Fault Communication						
Temperature Sense Slope	$A_{TMPGAIN}$	T_J = +25℃ to +125℃ (1)		8		mV/℃
Temperature Sense Offset Voltage	$V_{TMPOFFSET}$	T_J = +25℃, 0.6V + 8mV/℃ × T_J		812		mV
Other Logic Functions, Inputs/Outputs and Thresholds						
Enable Power-On Delay	$t_{EN\_ONDELAY}$	Measured from EN rising edge to V_{GL} > 1V, PWM = 0		23		μs
Enable Power-Off Delay	$t_{EN\_OFFDELAY}$	Measured from EN falling edge to V_{GL} < 4V, PWM = 0		0.83		μs
Internal Pull-Down Resistance	R_{PD_EN}	EN = floating		246		kΩ
Input High Voltage	V_{EN_H}		2			V
Input Low Voltage	V_{EN_L}				0.95	V
PWM Input High Threshold	V_{IH}	PWM = low-level or tri-state to high	2.6			V
PWM Input Low Threshold	V_{IL}	PWM = high-level or tri-state to low			0.7	V
PWM Hysteresis	V_{PWM_HYS}	Tri-state to active or active to tri-state		180		mV
Protection						
Over-Temperature Rising Threshold	T_R	TMON/FAULT pulled high		140		℃
Over-Temperature Falling Threshold	T_F	TMON/FAULT released		128		℃
High-side MOSFET Short Threshold	V_{HSS_TH}	V_{SW} - V_{PGND}			800	mV
TMON/FAULT Delay Time	t_{HSS_DELAY}	TMON/FAULT pulled high after V_{HSS_TH} is detected (1)		860		ns
Over-Current Threshold	I_{OCP_TH}			130		A
Over-Current Delay	t_{OCP_DEL}	TMON/FAULT pulled high after PWM high-low cycles		10		Cycle

NOTE: 1. Guaranteed by design but not tested in production.

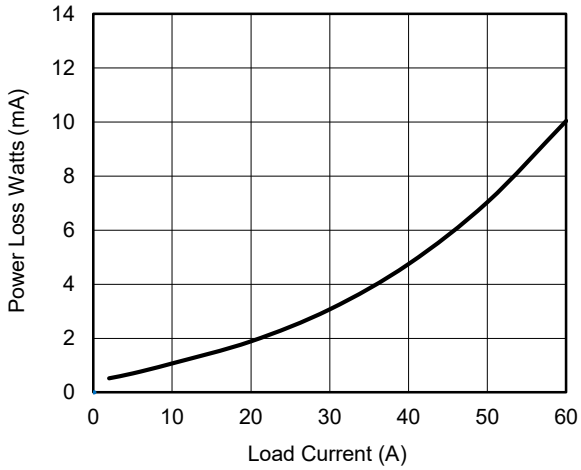
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 1MHz, L = 100nH, V_{CC} = V_{DRV} = 5V, T_A = +25℃, no heat sink, no air flow, 8-layer PCB board of 3.7" (L) × 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

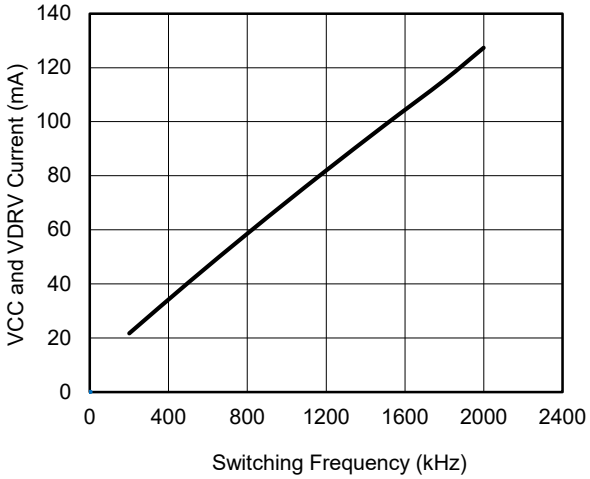
Power Stage Efficiency



Power Stage Loss



VCC and VDRV Current vs. Switching Frequency



FUNCTIONAL BLOCK DIAGRAM

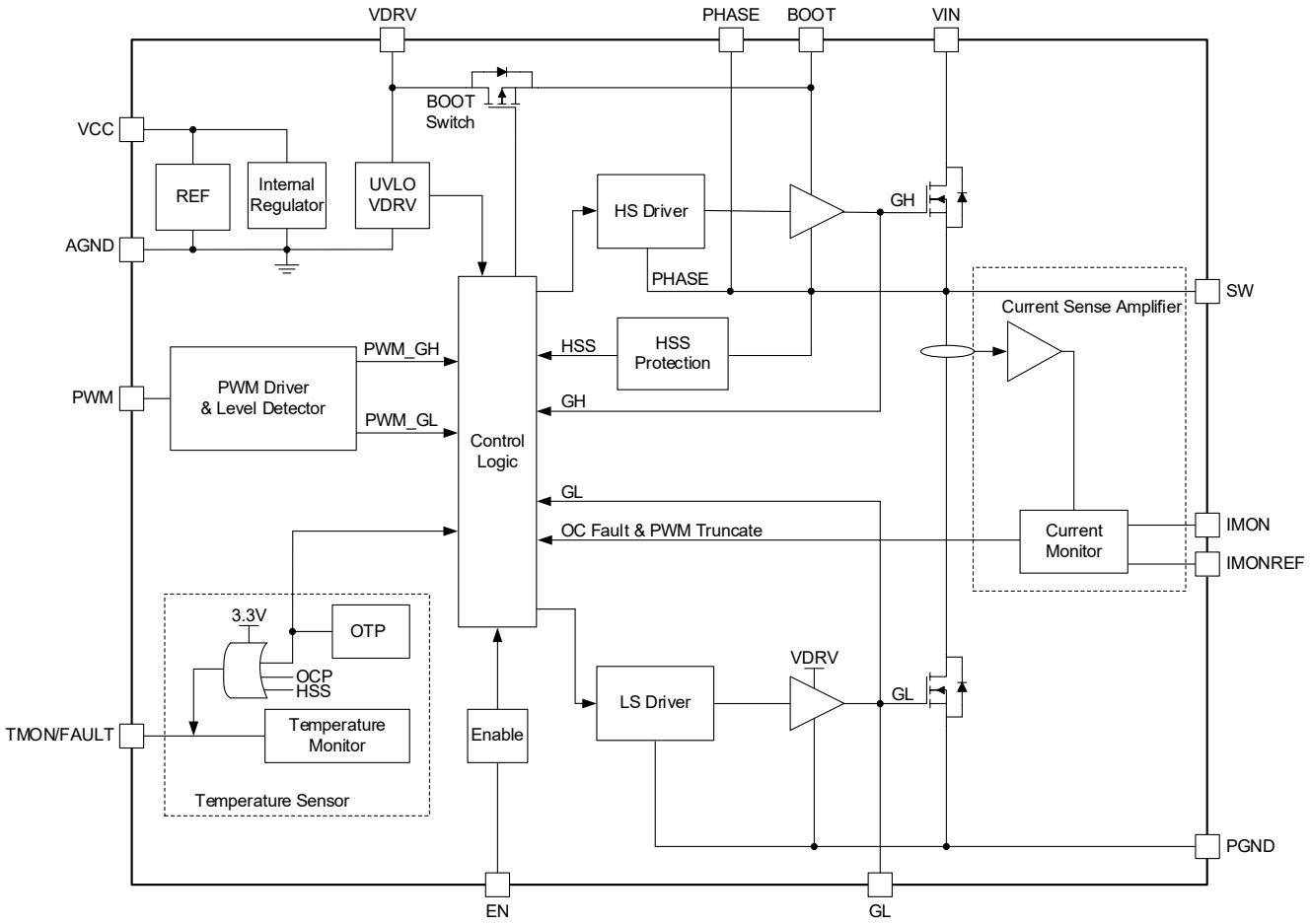


Figure 1. Block Diagram

TYPICAL APPLICATION

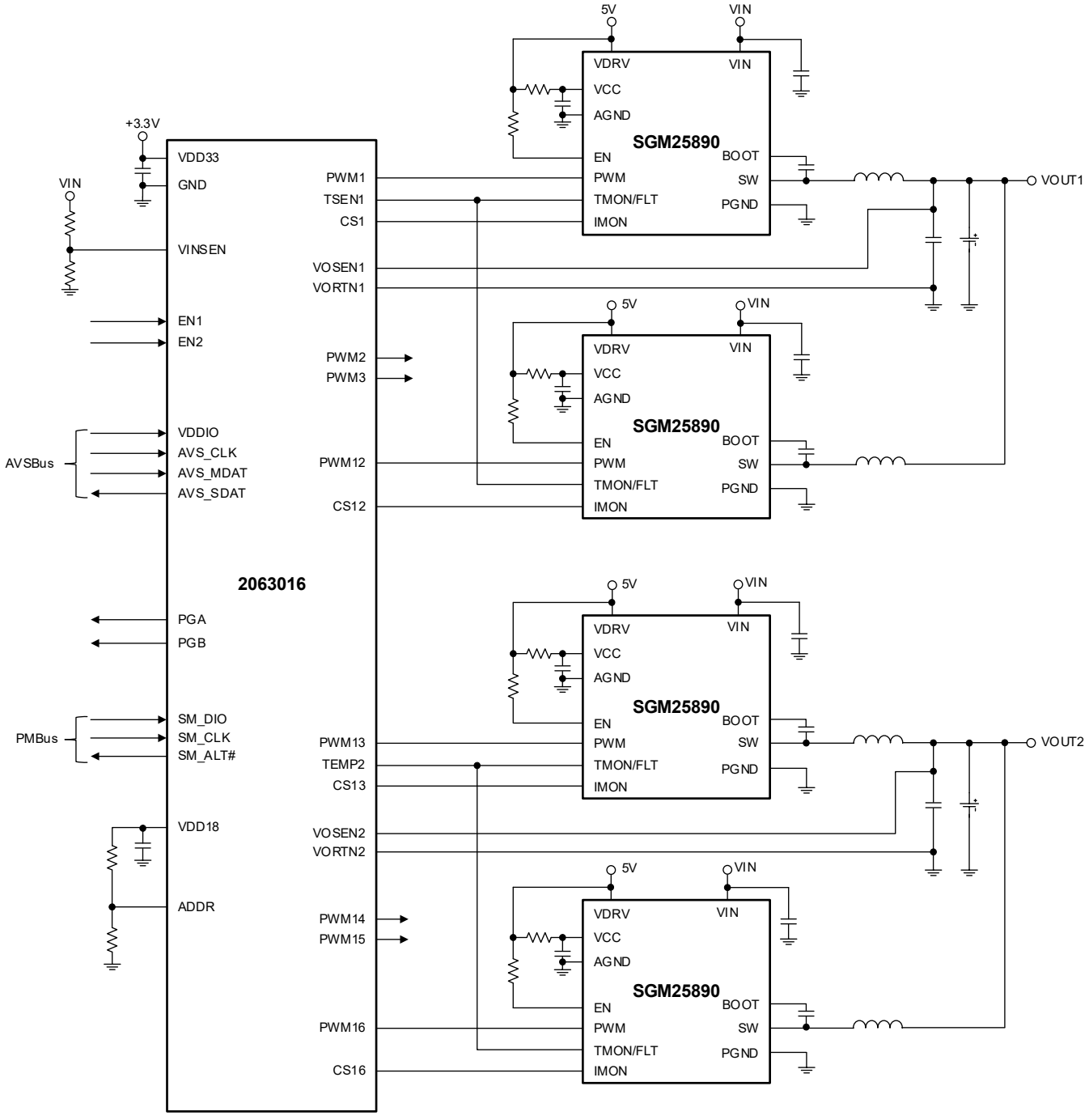


Figure 2. Typical Application Circuit

DETAILED DESCRIPTION

Overview

The SGM25890 has a pair of co-packaged high-side and low-side MOSFETs which is driven by an enhanced high-speed MOSFET driver, supporting operating frequencies up to 1.5MHz. The SGM25890 adopts advanced current-mirror sensing to achieve current report of IMON. Current on low-side MOSFET is mirrored on a sense MOSFET which is a part of the main low-side MOSFET device, no additional temperature compensation is required. And the current sense of the high-side MOSFET is difficult because SGM25890 mainly used in small duty, so the IMON of high-side MOSFET is generating through simulation. Real current sensing on low-side MOSFET ensures that the controller can get the relatively real output current.

The SGM25890 reports the temperature through TMON/FAULT pin with the gain of 8mV/℃. In multiphase systems, all TMON/FAULT pins of the power stage is connected together to generate the highest voltage to controller.

The SGM25890 cooperates with the controller can enter diode emulation mode through PWM tri-state signal to on/off the high-side MOSFET or low-side MOSFET. The diode emulation mode has higher light-load efficiency.

The SGM25890 will enter deep-sleep mode by pulling down the EN pin. The deep-sleep mode further reduces the power consumption of V_{DRV}.

The SGM25890 supports multiple protections: V_{CC}/ V_{DRV} under-voltage lockout (UVLO), over-temperature protection (OTP), high-side MOSFET short (HSS), and over-current protection (OCP).

Deep-Sleep Mode

The SGM25890 will enter deep-sleep mode by pulling down the EN pin. In the deep-sleep mode, the most of the logic circuitry will be shut down and the driver will also be shut down. At the same time, IMON output will equal to IMONREF in deep-sleep mode.

When EN is toggled high to exit deep-sleep mode, the power stage becomes ready to accept PWM signals after a 23μs delay.

Current Sensing and Reporting

The SGM25890 adopts advanced current-mirror sensing to achieve current report of IMON. Current on low-side MOSFET is mirrored on a sense MOSFET which is a part of the main low-side MOSFET device. The IMON pin outputs in proportion to the actual inductor current at a ratio of 5μA/A.

An IMON voltage range of 0.8V to 2.35V is required to achieve an accurate IMON current reporting. In general, there is a resistor connected from IMON to IMONREF. The recommended voltage range for IMONREF application is 1.1V to 1.9V. The selection of this resistor needs to be based on the IMONREF voltage while ensuring that the operating current range meets the requirements of IMON.

Advanced Fault Reporting

The SGM25890 can report all types of faults by TMON/FAULT pin, and through different voltage combinations of the IMON pin and TMON/FAULT pin to distinguish fault type. When the SGM25890 cooperates with controller, all TMON/FAULT pins are connected together and IMON pins are separately connected to the controller. So the controller identifies the occurrence of faults through the TMON/FAULT pin. And the controller detects the IMON voltage to distinguish fault types. A summary of fault reporting is given in the Table 1.

V_{DRV} Under-Voltage Lockout (UVLO)

The SGM25890 has a V_{DRV} under-voltage lockout fault protection that is monitored by the logic circuitry. As shown in Table 1, V_{DRV} UVLO is a non-catastrophic fault and the TMON/FAULT pin will be pulled low when the fault happened. If the SGM25890 has not started up, the PWM pin is also pulled down to 0V. When V_{DRV} is over the UVLO threshold, the PWM pin will change to PWM tri-state. At the same time, The IMON generates a voltage equal to IMONREF.

Once the SGM25890 is in normal operation, and then occurs a V_{DRV} UVLO condition, SGM25890 will stop working, and both TMON/FAULT and IMON pins will be pulled down to 0V. Because controller can only get the highest voltage of the TMON/FAULT, so controller can't identify the TMON/FAULT at V_{DRV} UVLO. But controller can identify the 0V from the IMON to confirm the type of fault.

DETAILED DESCRIPTION (continued)

Temperature Reporting and Over-Temperature Protection

SGM25890 reported the temperature through the voltage of TMON/FAULT pin. The relationship between voltage and temperature follows Equation 1.

$$V_{TMON\_FAULT}(V) = 0.6V + 0.8V/℃ \times T_J(℃) \quad (1)$$

When a fault occurs, the TMON/FAULT pin is pulled to 3.3V or pulled down to 0V as a fault pin, as shown in Table 1.

When OTP happened (the temperature rises above 140℃), the TMON/FAULT will be pulled to 3.3V, but SGM25890 will continue responding to the PWM signals if controller continues to send PWM signals. If controller stops sending the PWM signal, then the TMON/FAULT will return to normal state and continue to report the temperature after the junction temperature falls below the recovery threshold (+128℃).

Over-Current Protection and Flag

The SGM25890 has cycle-by-cycle current limit. If the current through low-side MOSFET exceeds the over-current threshold, the PWM high pulse will be set to the minimum on-time until the current through low-side MOSFET is below the current limit before PWM is pulled to high. When SGM25890 detects 10 consecutive PWM cycle over-current events, the TMON/FAULT pin will be pulled to 3.3V.

Table 1. Advanced Fault Reporting and Identification

Fault Severity Level	Type of Fault	Power Stage PWM Response	Power Stage IMON Response	Power-Stage TMON/FAULT Response	Recommended Controller Identification Criteria
Non-Catastrophic	V_{DRV} UVLO (power-up)	Weak pull-down to 0V (PWM pin voltage can be driven by controller, no switching on power stage)	= IMONREF	Weak pull-down to 0V (or V_{TMON} from other power stages in same loop)	$V_{TMON/FAULT}$ < 2V, PWM < 0.8V
	V_{DRV} UVLO (normal operation)		= 0V		$V_{TMON/FAULT}$ < 2V, V_{IMON} < 0.4V
Catastrophic	OTP	Power stage stops switching until OTP clears	= IMONREF	= 3.3V	$V_{TMON/FAULT}$ > 2.6V, V_{IMON} = $V_{IMONREF}$, 1V < V_{IMON} < 2V
	OCP (10 events without 3 consecutive good cycles)	Power stage continues responding to PWM signal from controller. Truncates high-side pulse until power stage is in OCP.	Continues reporting current	= 3.3V	$V_{TMON/FAULT}$ > 2.6V, V_{IMON} - $V_{IMONREF}$ > CTRL_OCP, V_{IMON} < 2.6V
	HSS (1st event)	Power stage continues responding to PWM signal from controller.	= 3.3V (latched)	= 3.3V	$V_{TMON/FAULT}$ > 2.6V, V_{IMON} > 2.6V

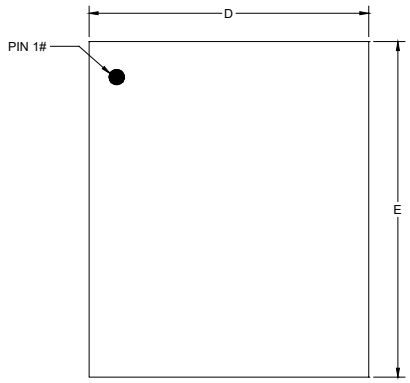
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

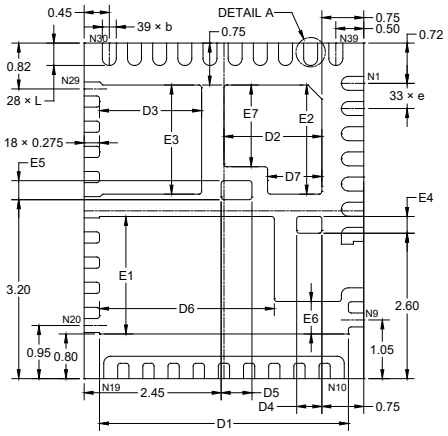
Changes from Original to REV.A (APRIL 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

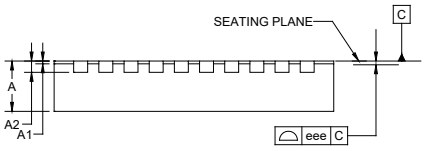
TQFN-5×6-39L



TOP VIEW

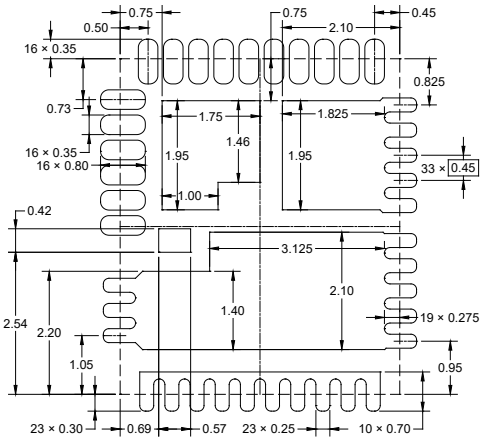


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



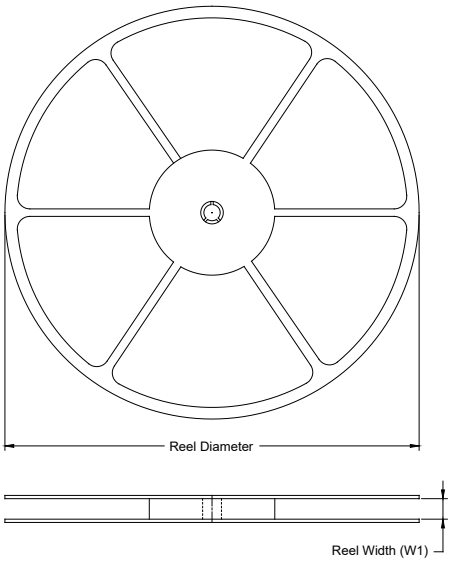
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.800	-	1.000
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
D	4.900	-	5.100
D1	4.350	-	4.550
D2	1.650	-	1.850
D3	1.720	-	1.920
D4	0.350	-	0.550
D5	0.450	-	0.650
D6		3.125 REF	
D7		0.970 REF	
E	5.900	-	6.100
E1	2.000	-	2.200
E2	1.850	-	2.050
E3	1.850	-	2.050
E4	0.200	-	0.400
E5	0.240	-	0.440
E6		0.580 REF	
E7		1.460 REF	
e		0.450 BSC	
L	0.300	-	0.500
eee		0.080	

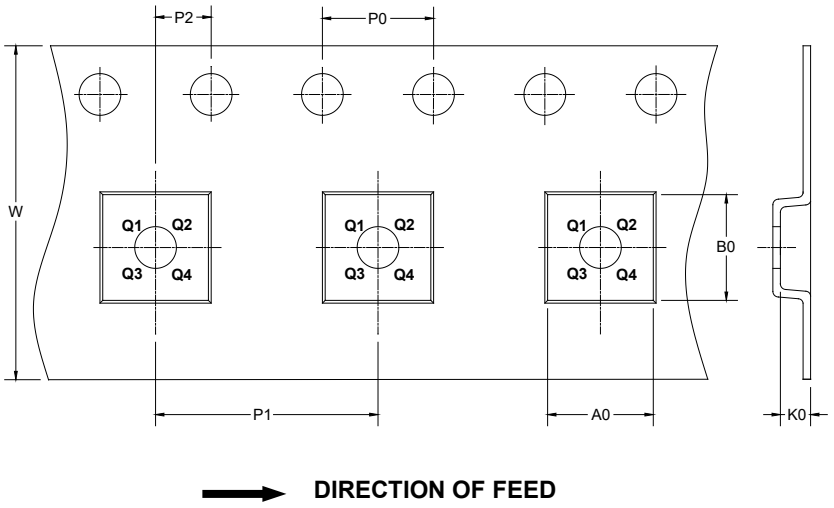
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



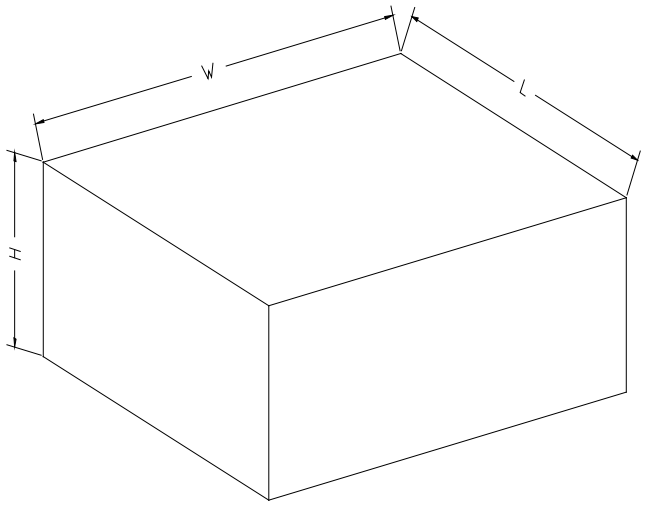
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-5×6-39L	13"	12.4	5.30	6.30	1.20	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002