SGM5200Q
12-Bit, 1MSPS, 16 Channels, Single-Ended, Serial Interface ADC

GENERAL DESCRIPTION

The SGM5200Q is a 12-bit, multi-channel input, successive approximation (SAR) analog-to-digital converter (ADC).

The SGM5200Q analog power supply range is 2.7V to 5.25V. The SGM5200Q has an SPI-compatible interface that digital power supply range is 1.7V to 5.25V. The input signal is sampled on the nCS falling edge. The ADC conversion is droved by external clock SCLK.

The SGM5200Q supports manual channel selection and two kinds of auto channel scan modes. The input range of SGM5200Q is software configurable, 0V to reference voltage or 0V to two times of reference voltage. It also supports two programmable alarm thresholds for each channel. The SGM5200Q provides power-down mode.

The SGM5200Q is AEC-Q100 qualified (Automotive Electronics Council Standard Q100 Grade 1) and the use of this device is suitable for automotive applications.

The SGM5200Q is available in a Green TSSOP-38 package. It operates over an ambient temperature range -40℃ to +125℃.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **12-Bit Resolution**
- **16 Channels**
- **Sampling Rate: Up to 1MHz**
- **Supply Voltage Ranges:**
  - **Analog Supply: 2.7V to 5.25V**
  - **Digital Supply: 1.7V to 5.25V**
- **Two Software Selectable Unipolar Input Ranges:**
  - **Range 1: 0V to V_{REF}**
  - **Range 2: 0V to 2 × V_{REF}**
- **Support Auto and Manual Channel Selections**
- **Individually Configurable GPIOs Function:**
  Four GPIOs
- **20MHz SPI-Compatible Serial Interface**
- **Power-Down Current: 1.4μA (TYP)**
- **Input Bandwidth: 45MHz (TYP) at -3dB**
- **Typical Power Consumption:**
  24mW at 1MSPS (V_A = 5V, V_{BD} = 3V)
- **Available in a Green TSSOP-38 Package**

APPLICATIONS

Automotive Applications
PLC
Optical Module Signal Monitoring
Digital Power Supplies
Industrial Automation Systems

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5200Q	TSSOP-38	-40℃ to +125℃	SGM5200QTS38G/TR	03Q TS38 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX
- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to AGND)
+VA .... -0.3V to 6V
AINP or CHx .... -0.3V to V_A + 0.3V
Voltage Range (with Respect to BGND)
+VBD .... -0.3V to 6V
Digital Input Voltage .... -0.3V to 6V
Digital Output Voltage .... -0.3V to V_A + 0.3V
Input Current to Any Pin except Supply Pins
.... -10mA to 10mA
Junction Temperature .... +150℃
Storage Temperature Range .... -65℃ to +150℃
Lead Temperature (Soldering, 10s) .... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Analog Supply Voltage Range .... 2.7V to 5.25V
Digital I/O Supply Voltage Range .... 1.7V to V_A
Reference Voltage Range... 2V to 3V
SCLK Frequency 20MHz
Operating Temperature Range .... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

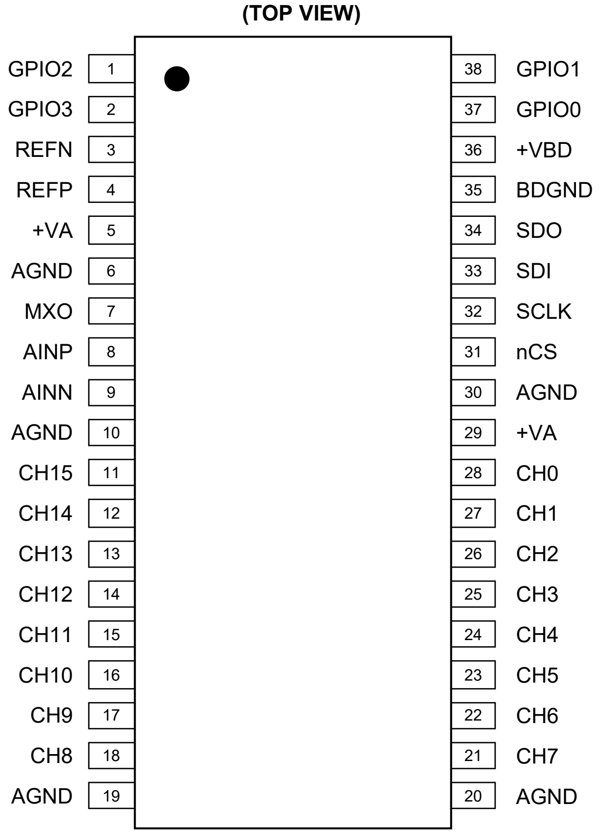
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



TSSOP-38

PIN DESCRIPTION

<table>
<tr><th>PIN</th><th>NAME</th><th>TYPE [1]</th><th>FUNCTION</th></tr>
<tr><td rowspan="2">1</td><td>GPIO2</td><td>DIO</td><td>General-Purpose Input or Output.</td></tr>
<tr><td>Range</td><td>DI</td><td>Selects ADC Input Range.
High (1): select Range 2 (0V to 2 × V_{REF}).
Low (0): select Range 1 (0V to V_{REF}).</td></tr>
<tr><td rowspan="2">2</td><td>GPIO3</td><td>DIO</td><td>General-Purpose Input or Output.</td></tr>
<tr><td>nPD</td><td>DI</td><td>Power-Down Input. Active low.</td></tr>
<tr><td>3</td><td>REFN</td><td>AI</td><td>Reference Ground.</td></tr>
<tr><td>4</td><td>REFP</td><td>AI</td><td>Reference Input.</td></tr>
<tr><td>5, 29</td><td>+VA</td><td>–</td><td>Analog Power Supply.</td></tr>
<tr><td>6, 10, 19, 20, 30</td><td>AGND</td><td>–</td><td>Analog Ground.</td></tr>
<tr><td>7</td><td>MXO</td><td>AO</td><td>Multiplexer Output.</td></tr>
<tr><td>8</td><td>AINP</td><td>AI</td><td>ADC Input Signal.</td></tr>
<tr><td>9</td><td>AINN</td><td>AI</td><td>ADC Input Ground.</td></tr>
<tr><td>11</td><td>CH15</td><td>AI</td><td rowspan="16">Analog Channel Inputs for Multiplexer.</td></tr>
<tr><td>12</td><td>CH14</td><td>AI</td></tr>
<tr><td>13</td><td>CH13</td><td>AI</td></tr>
<tr><td>14</td><td>CH12</td><td>AI</td></tr>
<tr><td>15</td><td>CH11</td><td>AI</td></tr>
<tr><td>16</td><td>CH10</td><td>AI</td></tr>
<tr><td>17</td><td>CH9</td><td>AI</td></tr>
<tr><td>18</td><td>CH8</td><td>AI</td></tr>
<tr><td>21</td><td>CH7</td><td>AI</td></tr>
<tr><td>22</td><td>CH6</td><td>AI</td></tr>
<tr><td>23</td><td>CH5</td><td>AI</td></tr>
<tr><td>24</td><td>CH4</td><td>AI</td></tr>
<tr><td>25</td><td>CH3</td><td>AI</td></tr>
<tr><td>26</td><td>CH2</td><td>AI</td></tr>
<tr><td>27</td><td>CH1</td><td>AI</td></tr>
<tr><td>28</td><td>CH0</td><td>AI</td></tr>
<tr><td>31</td><td>nCS</td><td>DI</td><td>Chip Select. Active low.</td></tr>
<tr><td>32</td><td>SCLK</td><td>DI</td><td>Serial Clock Input.</td></tr>
<tr><td>33</td><td>SDI</td><td>DI</td><td>Serial Data Input.</td></tr>
<tr><td>34</td><td>SDO</td><td>DI</td><td>Serial Data Output.</td></tr>
<tr><td>35</td><td>BDGND</td><td>–</td><td>Digital Ground.</td></tr>
<tr><td>36</td><td>+VBD</td><td>–</td><td>Digital Power Supply.</td></tr>
<tr><td rowspan="2">37</td><td>GPIO0</td><td>DIO</td><td>General-Purpose Input or Output.</td></tr>
<tr><td>Alarm</td><td>DO</td><td>Alarm Output. Active high. Refer to Programming section for a detailed configuration.</td></tr>
<tr><td rowspan="2">38</td><td>GPIO1</td><td>DIO</td><td>General-Purpose Input or Output.</td></tr>
<tr><td>Low Alarm</td><td>DO</td><td>Low Alarm Output Indication. Active high.</td></tr>
</table>

NOTE:
1. AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input or Output.

ELECTRICAL CHARACTERISTICS

(V_A = 2.7V to 5.25V, V_{BD} = 1.7V to V_A, V_{REF} = 2.5V ± 0.1V, f_{SAMPLE} = 1MHz, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Input							
Full-Scale Input Span (1)		Range 1		0		V_{REF}	V
		Range 2 while 2 × V_{REF} ≤ V_A		0		2 × V_{REF}	
Absolute Input Range		Range 1		-0.2		V_{REF} + 0.2	V
		Range 2 while 2 × V_{REF} ≤ V_A		-0.2		2 × V_{REF} + 0.2	
Input Capacitance					31		pF
Input Leakage Current		T_A = +125℃			60		nA
System Performance							
Resolution					12		Bits
No Missing Codes	NMC	Range 1		11			Bits
		Range 2		12			
Integral Nonlinearity	INL	Range 1		-3.7	-1.6/+0.6	2.7	LSB (2)
		Range 2		-1.32	±0.6	1.32	
Differential Nonlinearity	DNL	Range 1		-1	-1/+1.3	2.9	LSB
		Range 2		-0.99	±0.5	1	
Offset Error (3)	E_O	Range 1		-9.7	±2	6.8	LSB
		Range 2		-6.4	±1.8	3.5	
Gain Error	E_G	Range 1		-6	±0.1	5.8	LSB
		Range 2		-3.8	±0.1	3.8	
Total Unadjusted Error	TUE	Range 1			±2.5		LSB
		Range 2			±1.9		
Sampling Dynamics							
Conversion Time	t_{CONV}	20MHz SCLK			800		ns
Acquisition Time	t_{ACQ}				325		ns
Maximum Throughput Rate		20MHz SCLK				1	MHz
Aperture Delay					6		ns
Dynamic Characteristics							
Total Harmonic Distortion (4)	THD	100kHz	Range 1		-76		dB
			Range 2		-78		
Signal-to-Noise Ratio	SNR	100kHz	Range 1	66.4	71		dB
			Range 2	67.9	71.8		
Signal-to-Noise + Distortion	SINAD	100kHz	Range 1	65.6	70		dB
			Range 2	66.7	70.9		
Spurious Free Dynamic Range	SFDR	100kHz	Range 1		77		dB
			Range 2		80		
Small-Signal Bandwidth		At -3dB			45		MHz
Channel-to-Channel Crosstalk		Any off-channel with 100kHz, full-scale input to channel being sampled with DC input (isolation crosstalk)			-100		dB
		From previously sampled to channel with 100kHz, full-scale input to channel being sampled with DC input (memory crosstalk)			-84		

ELECTRICAL CHARACTERISTICS (continued)

(V_A = 2.7V to 5.25V, V_{BD} = 1.7V to V_A, V_{REF} = 2.5V ± 0.1V, f_{SAMPLE} = 1MHz, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External Reference Input						
Reference Voltage at REFP (5)	V_{REF}		2	2.5	3	V
Reference Input Resistance		f_{SAMPLE} = 1MHz		31		kΩ
Alarm Setting						
High Threshold Range			0		4092	LSB
Low Threshold Range			0		4092	LSB
Digital Input/Output						
High Input Voltage	V_{IH}	V_{BD} = 5.25V	3.20			V
		V_{BD} = 1.7V	1.25			
Low Input Voltage	V_{IL}	V_{BD} = 5.25V			1.90	V
		V_{BD} = 1.7V			0.45	
High Output Voltage	V_{OH}	I_{SOURCE} = 200μA	V_{BD} - 0.2			V
Low Output Voltage	V_{OL}	I_{SINK} = 200μA			0.4	V
Data Format MSB First				MSB First		
Power Requirements						
Analog Supply Voltage	V_A		2.7	3.3	5.25	V
Digital I/O Supply Voltage	V_{BD}		1.7	3.3	5.25	V
Analog Supply Current (Normal Mode)	I_A	V_A = 2.7V to 3.6V and 1MHz throughput		3		mA
		V_A = 2.7V to 3.6V static state		1.1		
		V_A = 4.7V to 5.25V and 1MHz throughput		4.1	5.5	
		V_A = 4.7V to 5.25V static state		1.1	2.2	
Power-Down State Supply Current				1.4		μA
Digital I/O Supply Current	I_{BD}	V_A = 5.25V, f_{SAMPLE} = 1MHz		1.3		mA
Power-Up Time				1		μs
Invalid Conversions after Power-Up or Reset				1		Conversion

NOTES:
1. Ideal input span, not consider gain error and offset error.
2. LSB = Least Significant Bit.
3. The measurement is performed relative to the ideal full-scale input.
4. The calculation is performed on the first nine harmonics of the input frequency.
5. The device is designed to operate at a reference voltage of 2V to 3V. However, when V_{REF} < 2.4V, it expects lower noise performance since SNR degradation results from lowered signal range.

TIMING CHARACTERISTICS

(V_A = 2.7V to 5.25V, Full = -40℃ to +125℃, unless otherwise noted.) [1] [2] (See Figure 1 and Figure 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Time	t_{CONV}	V_{BD} = 1.8V			16	SCLK
		V_{BD} = 3V			16	
		V_{BD} = 5V			16	
Delay Time (nCS Low to First Data DO15 Out)	t_1	V_{BD} = 1.8V			38	ns
		V_{BD} = 3V			27	
		V_{BD} = 5V			17	
Hold Time (SCLK Falling to SDO Data Bit Valid)	t_2	V_{BD} = 1.8V	8			ns
		V_{BD} = 3V	6			
		V_{BD} = 5V	4			
Delay Time (SCLK Falling to SDO Next Data Bit Valid)	t_3	V_{BD} = 1.8V			35	ns
		V_{BD} = 3V			27	
		V_{BD} = 5V			17	
Setup Time (SDI Valid to Rising Edge of SCLK)	t_4	V_{BD} = 1.8V	2			ns
		V_{BD} = 3V	3			
		V_{BD} = 5V	4			
Hold Time (Rising Edge of SCLK to SDI Valid)	t_5	V_{BD} = 1.8V	12			ns
		V_{BD} = 3V	10			
		V_{BD} = 5V	6			
Delay Time (16^{th} SCLK Falling Edge to SDO 3-State)	t_6	V_{BD} = 1.8V			26	ns
		V_{BD} = 3V			22	
		V_{BD} = 5V			16	
Minimum Quiet Sampling Time Needed from Bus 3-State to Start of Next Conversion	t_7	V_{BD} = 1.8V	40			ns
		V_{BD} = 3V	40			
		V_{BD} = 5V	40			
Pulse Duration nCS High	t_8	V_{BD} = 1.8V	20			ns
		V_{BD} = 3V	20			
		V_{BD} = 5V	20			
Setup Time (nCS Low to First Rising Edge of SCLK)	t_9	V_{BD} = 1.8V	8			ns
		V_{BD} = 3V	6			
		V_{BD} = 5V	4			
Pulse Duration SCLK High	t_{10}	V_{BD} = 1.8V	20			ns
		V_{BD} = 3V	20			
		V_{BD} = 5V	20			
Pulse Duration SCLK Low	t_{11}	V_{BD} = 1.8V	20			ns
		V_{BD} = 3V	20			
		V_{BD} = 5V	20			
SCLK Frequency	f_{CLK}	V_{BD} = 1.8V			20	MHz
		V_{BD} = 3V			20	
		V_{BD} = 5V			20	

NOTES:
1. 1.6V to 1.9V range is applied for 1.8V specifications. 2.7V to 3.6V range is applied for 3V specifications. 4.75V to 5.25V range is applied for 5V specifications.
2. With 50pF load.

TIMING DIAGRAMS

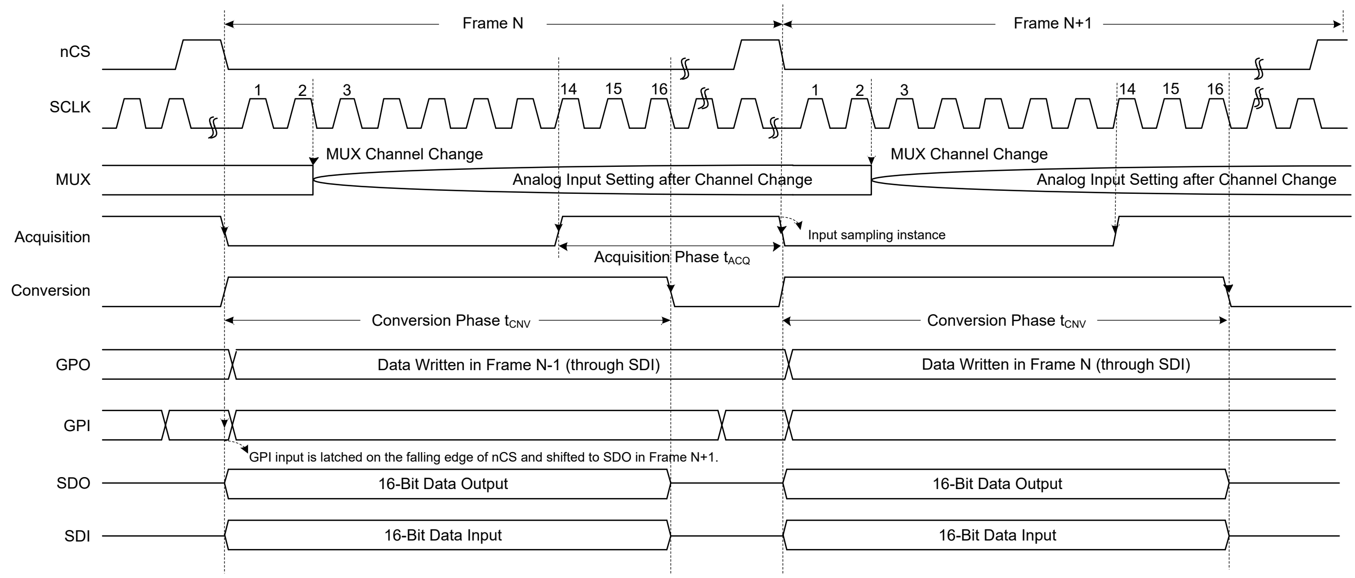


Figure 1. Device Operation Timing Diagram

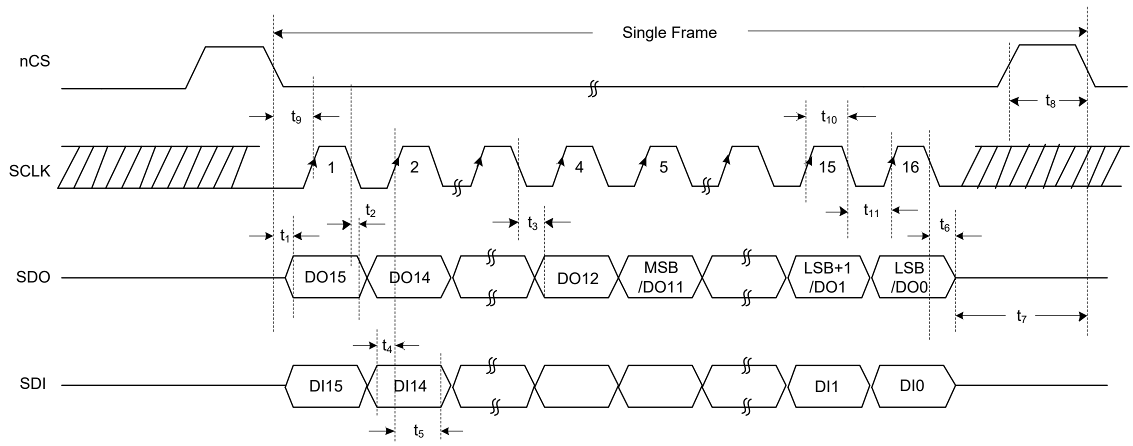
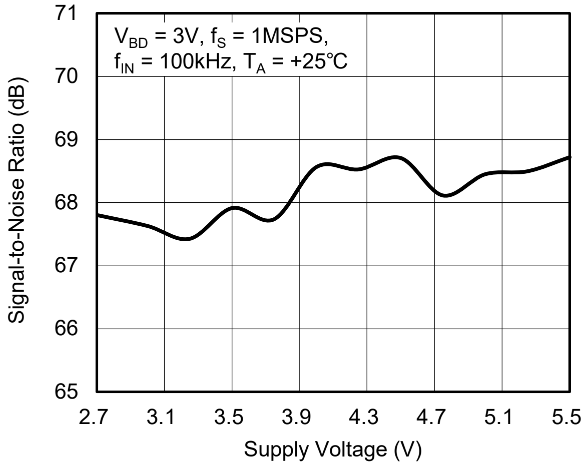


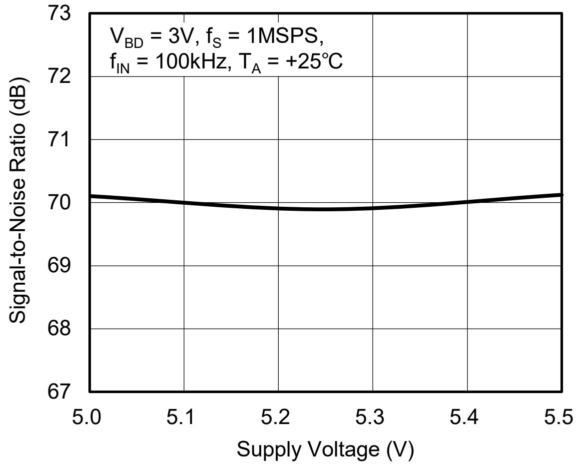
Figure 2. Serial Interface Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

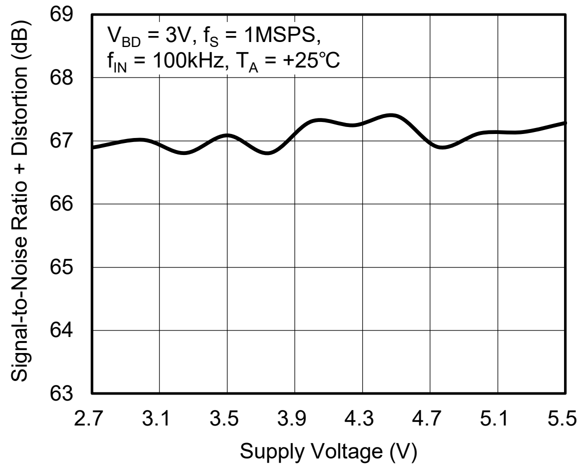
Signal-to-Noise Ratio vs. Supply Voltage (Range 1)



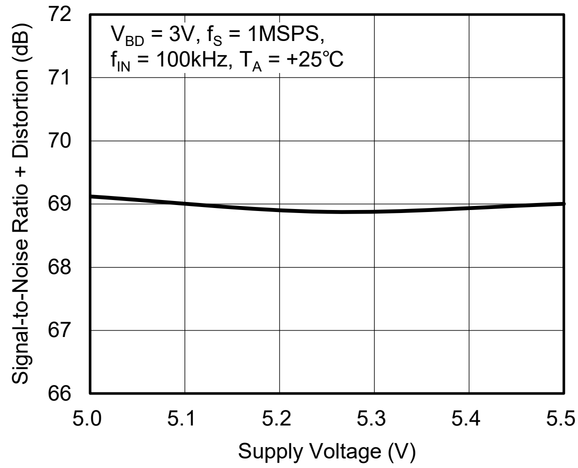
Signal-to-Noise Ratio vs. Supply Voltage (Range 2)



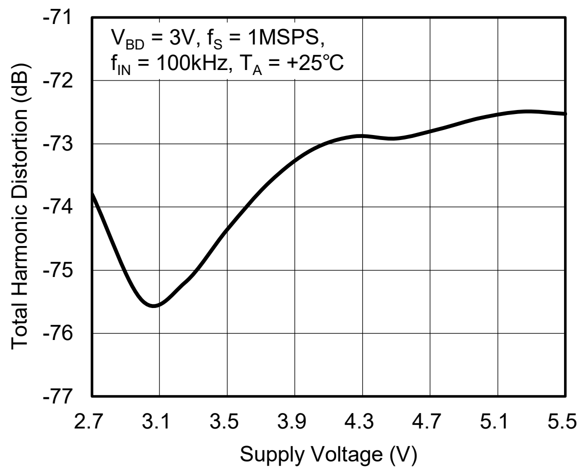
Signal-to-Noise + Distortion vs. Supply Voltage (Range 1)



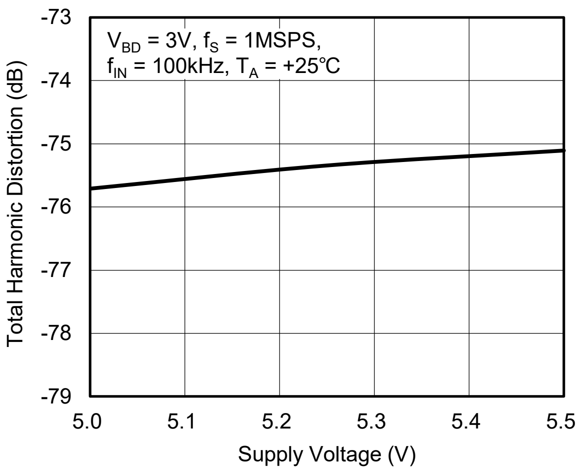
Signal-to-Noise + Distortion vs. Supply Voltage (Range 2)



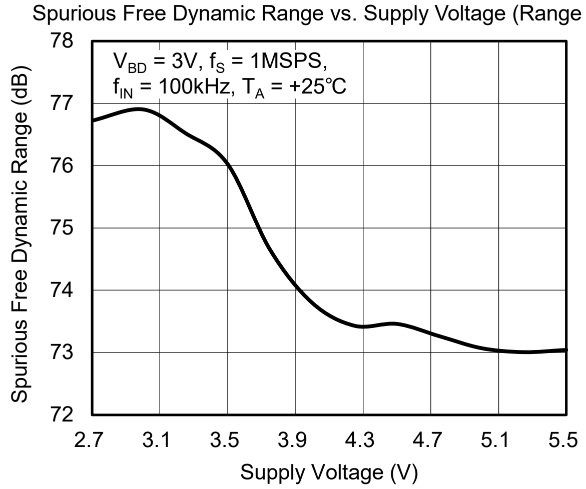
Total Harmonic Distortion vs. Supply Voltage (Range 1)

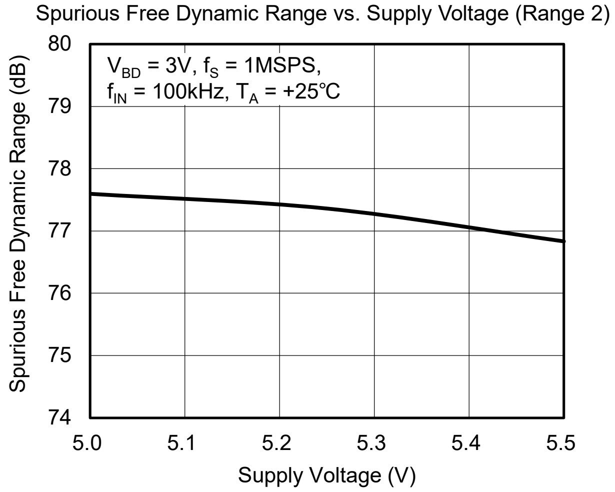


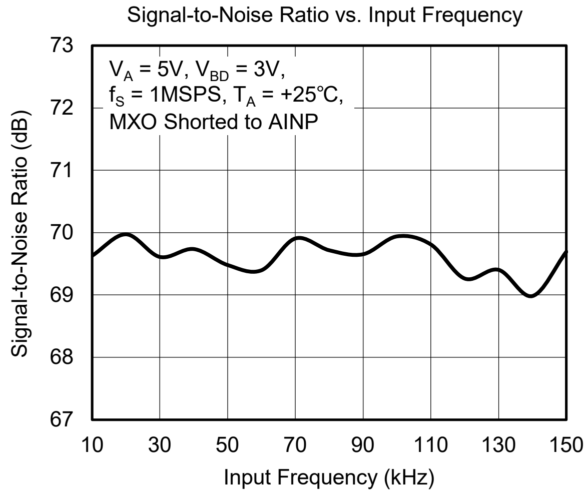
Total Harmonic Distortion vs. Supply Voltage (Range 2)

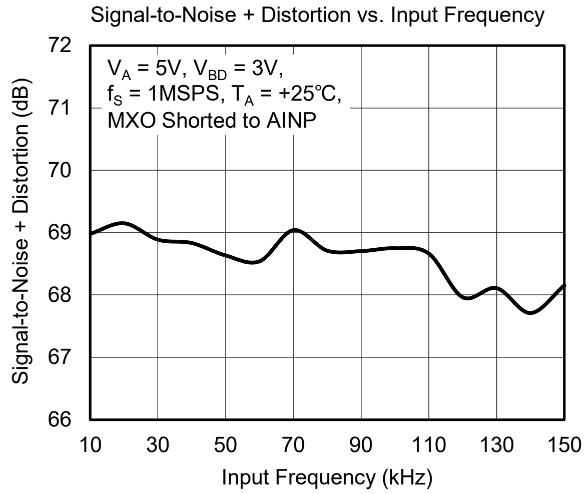


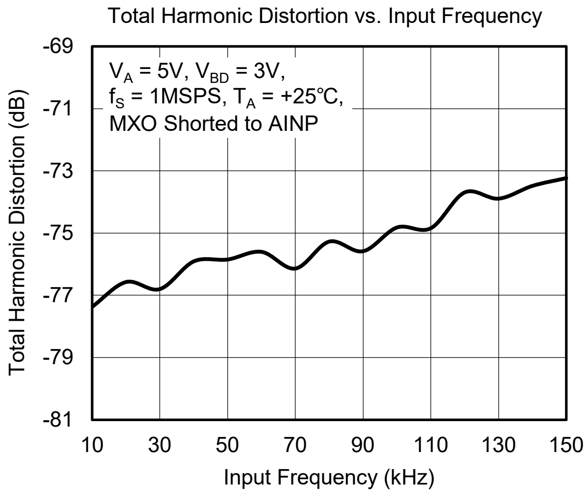
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

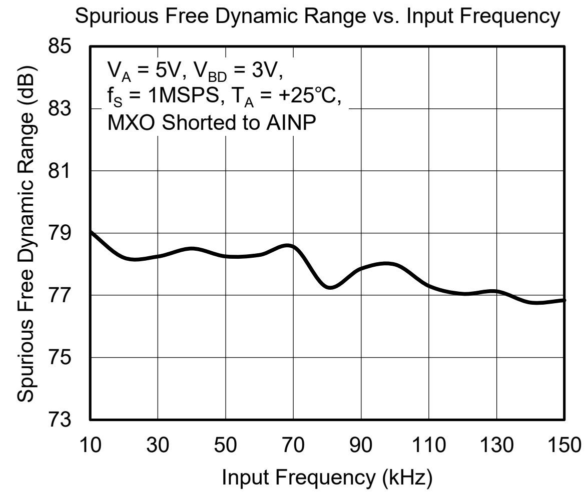






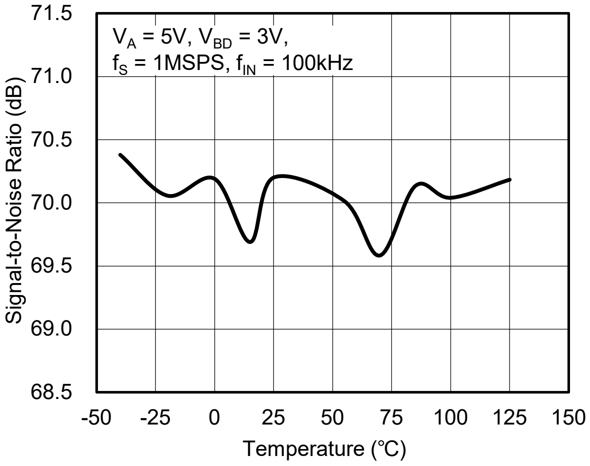




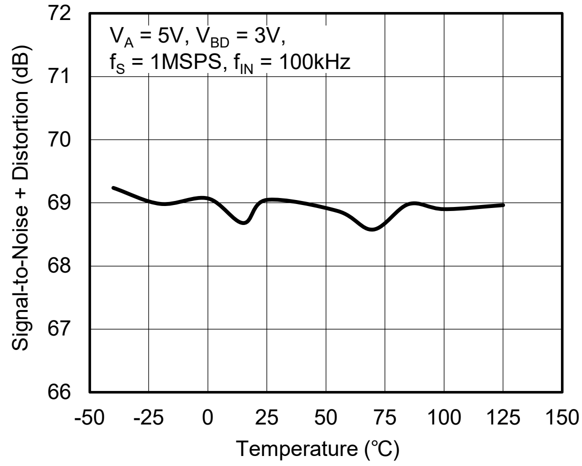


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

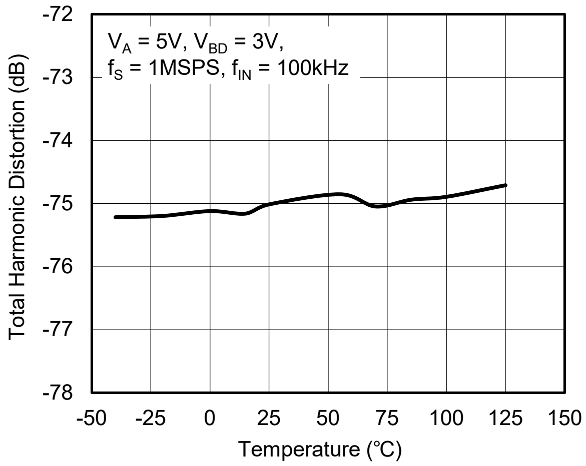
Signal-to-Noise Ratio vs. Temperature



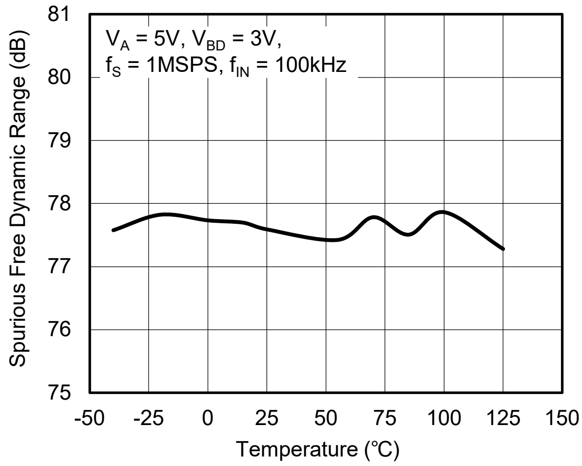
Signal-to-Noise + Distortion vs. Temperature



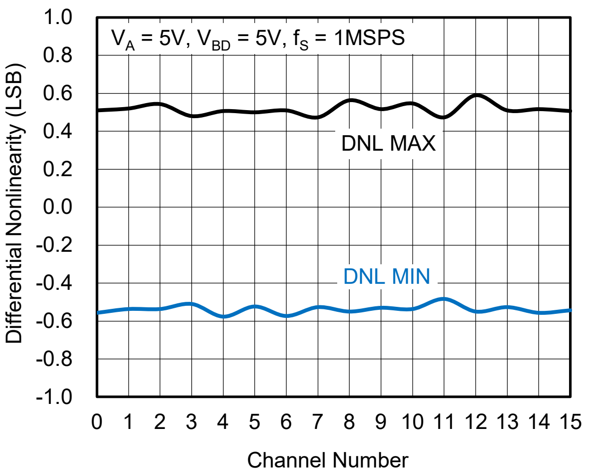
Total Harmonic Distortion vs. Temperature



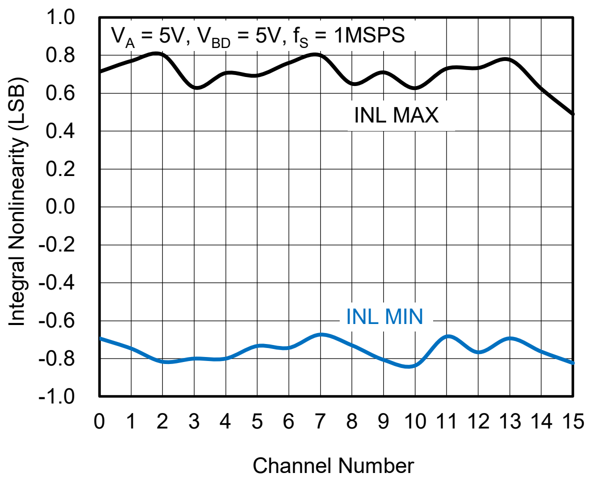
Spurious Free Dynamic Range vs. Temperature



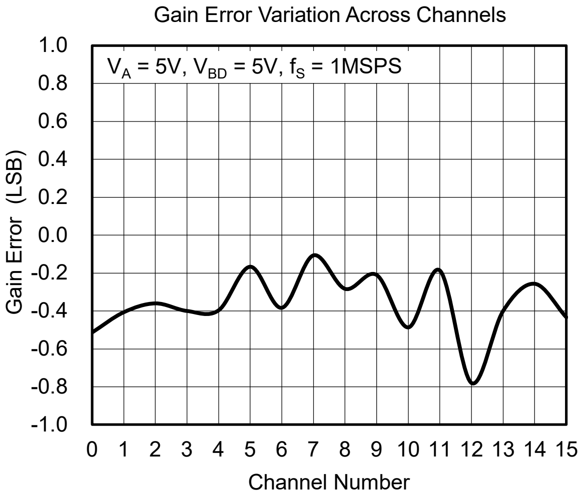
Differential Nonlinearity Variation Across Channels

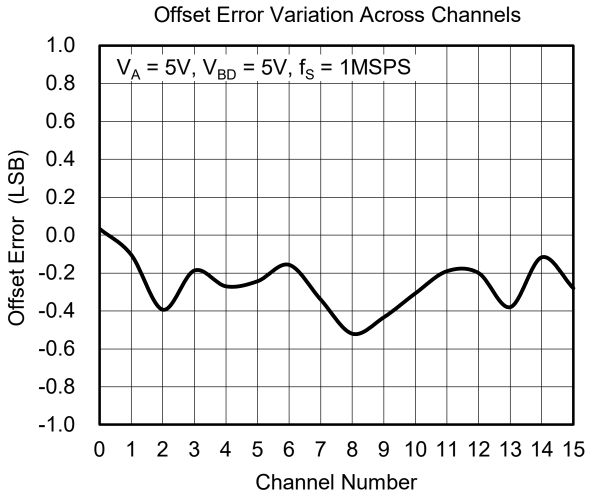


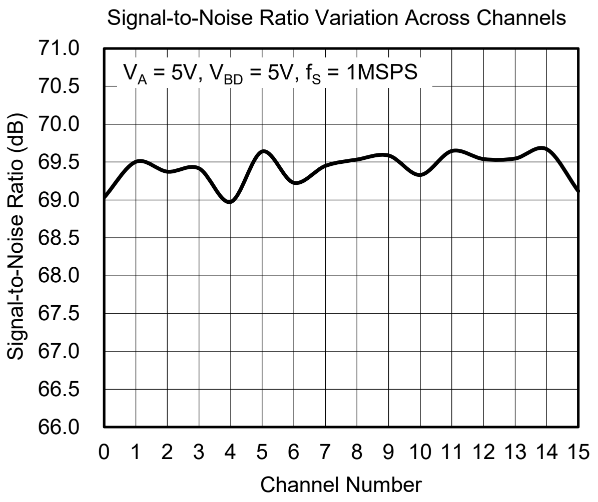
Integral Nonlinearity Variation Across Channels

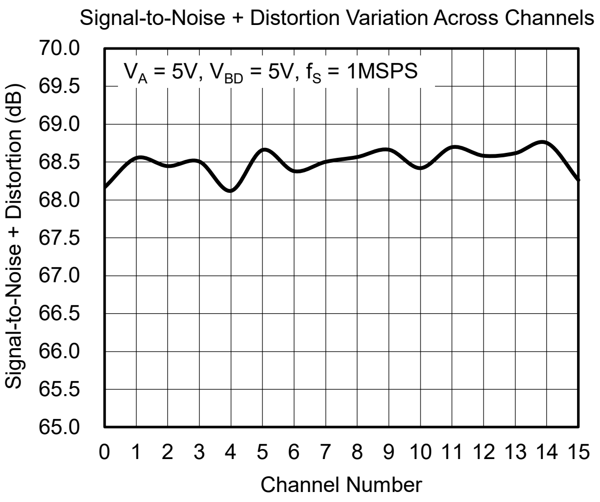


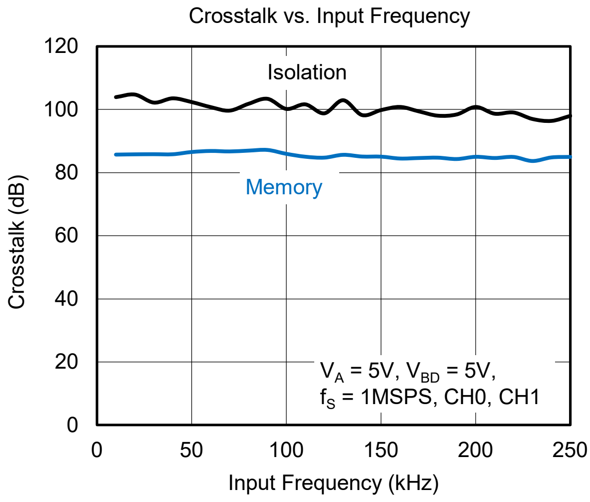
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

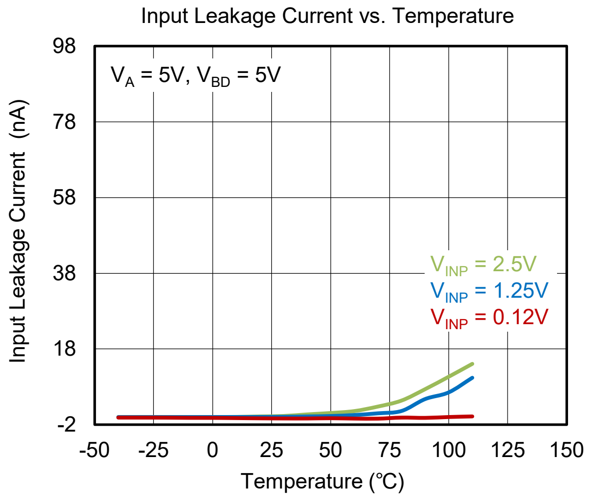






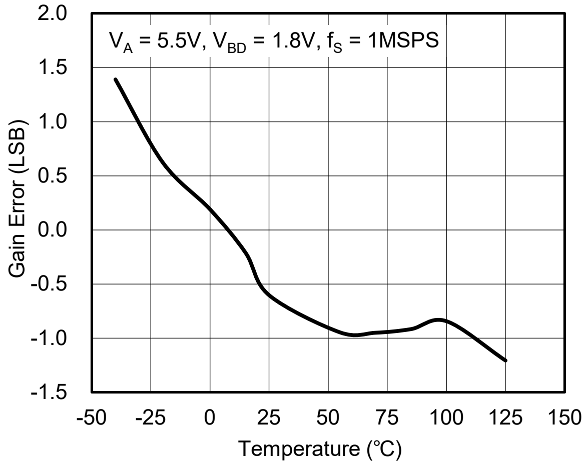




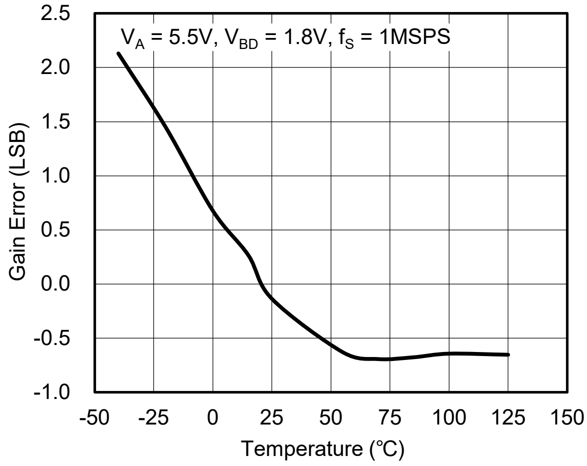


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

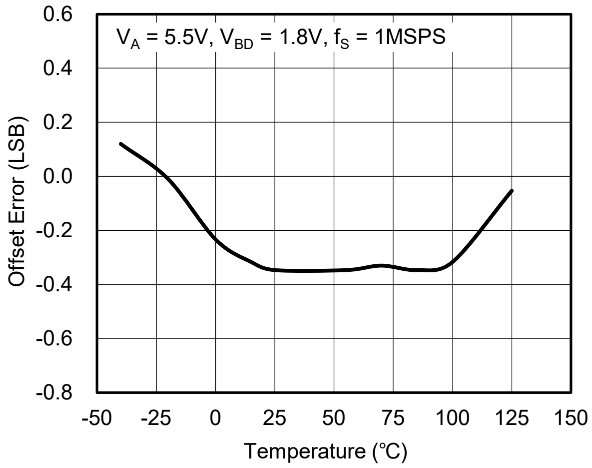
Gain Error vs. Temperature (Range 1)



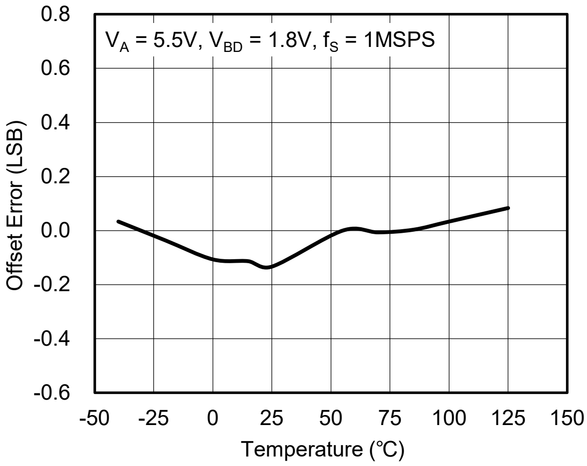
Gain Error vs. Temperature (Range 2)



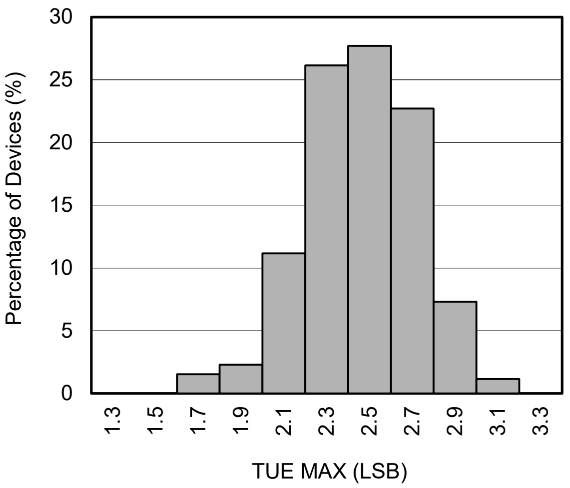
Offset Error vs. Temperature (Range 1)



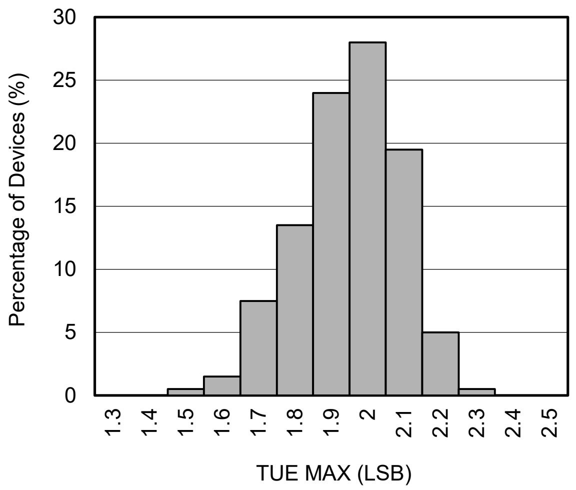
Offset Error vs. Temperature (Range 2)



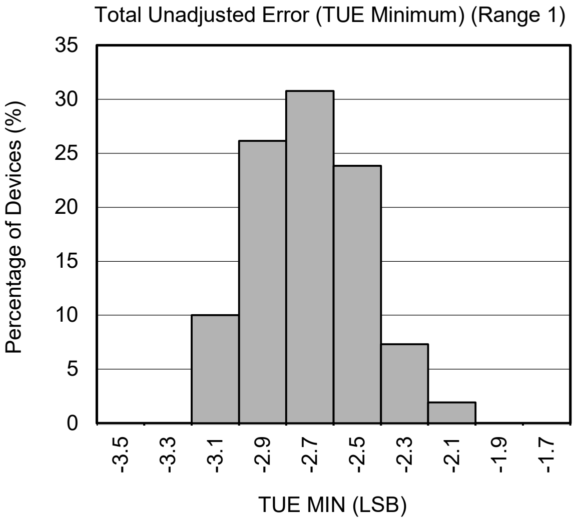
Total Unadjusted Error (TUE Maximum) (Range 1)

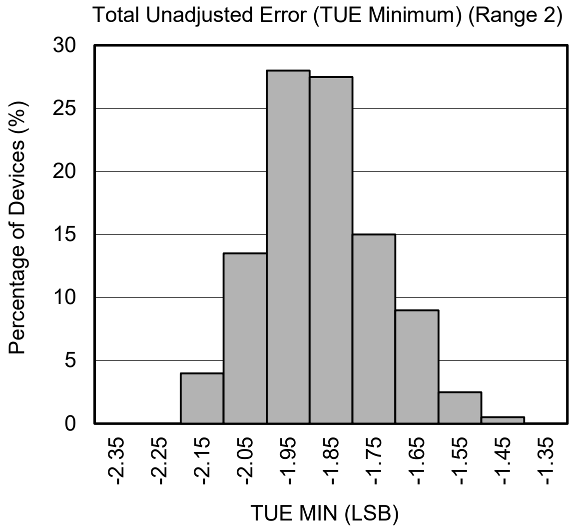


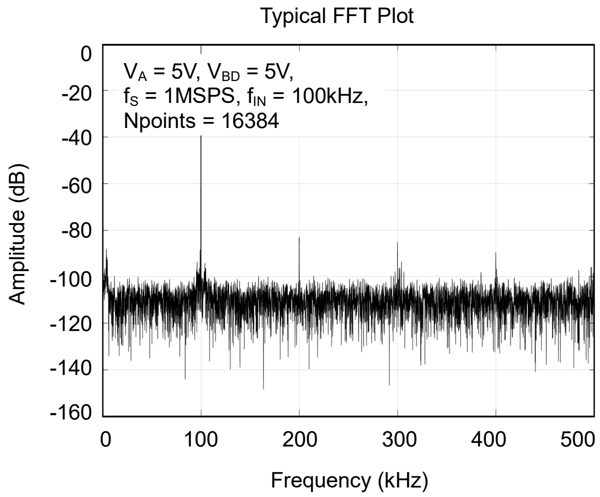
Total Unadjusted Error (TUE Maximum) (Range 2)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)







FUNCTIONAL BLOCK DIAGRAM

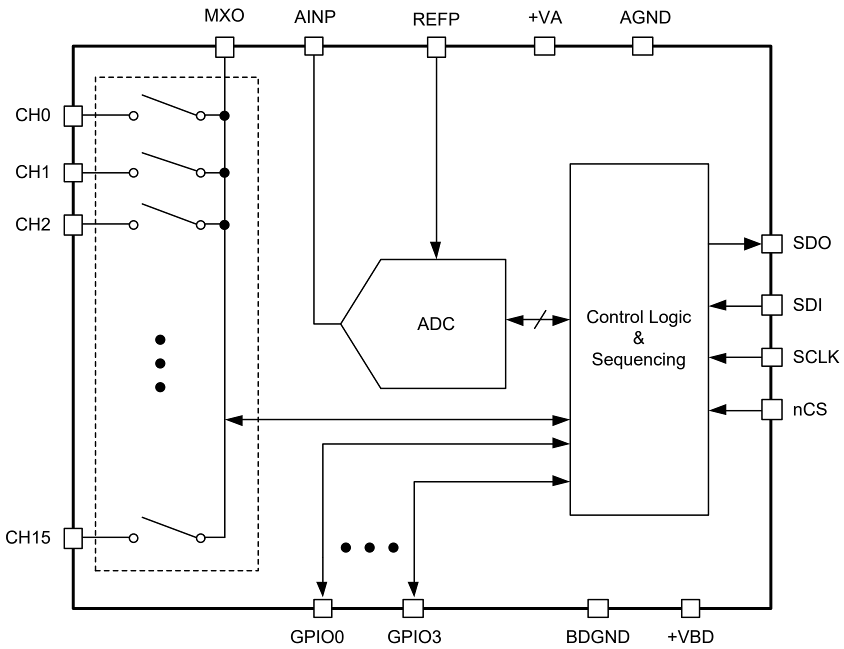


Figure 3. Block Diagram

TYPICAL APPLICATION CIRCUIT

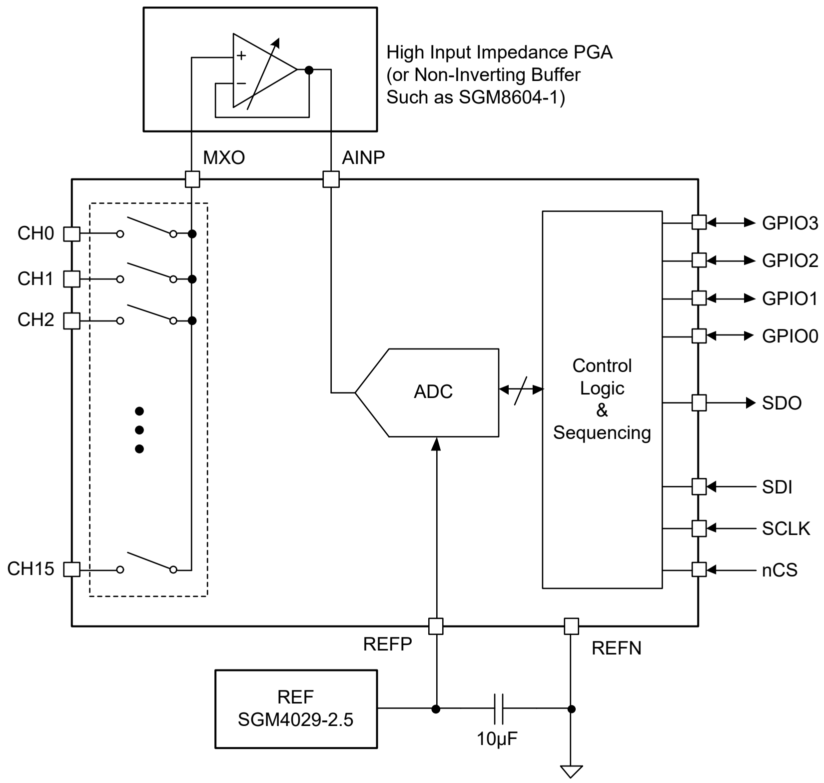


Figure 4. Typical Application Circuit

DETAILED DESCRIPTION

Overview

The SGM5200Q is a 12-bit, SAR ADC. It needs an external voltage reference. An Amplifier can be used between MXO and AINP for signal conditioning. Figure 1 and Figure 2 show the chip operating time sequences.

The SGM5200Q output data is composed of 4-bit channel address and 12-bit ADC conversion result. To read and write GPIOs, more details refer to Table 1, Table 2 and Table 5.

The SGM5200Q switches to new multiplexer channel on the 2nd falling edge of SCLK. The input acquisition phase (equal input capacitor starts charging) begins on the 14th rising edge of SCLK. The input signal is sampled on the nCS falling edge.

The chip refreshes the GPIO status (Input and output) at the nCS falling edge. The GPI data will be in the same frame starting with the nCS falling edge (if GPI read enabled).

The operating time sequence is shown in Figure 2. The falling edge of nCS clocks out DO15, and the remain bits are shifted out on the falling edge of SCLK. The ADC result is a 12-bit binary data, MSB is shifted out on the 4th falling edge of SCLK, and LSB is shifted out on the 15th falling edge of SCLK. Refer to Figure 2, when the ADC conversion ends on the 16th SCLK falling edge, SDO goes to 3-state. The chip 16-bit data (on SDI pin) is shifted in on the every rising edge of SCLK.

The SGM5200Q has threshold alarm function per channel. If ADC results exceed these limits (high and low), the chip can give alert on GPIO0/GPIO1 pins (detail configurations in Table 9). If there is an alarm, the alert will be set on the 12th SCLK falling edge in the same frame of ADC conversion in progress. It will reset on the 10th SCLK falling edge in the next frame.

Reference

The SGM5200Q needs an external reference.

Power Saving

The SGM5200Q provides two kinds of ways to power down the chip. The first way is command control. It depends on setting DI5 = '1', more details see Table 1, Table 2 and Table 5. If DI5 is set, the chip will be powered down on the 16th falling edge of SCLK in the next frame. If DI5 is reset, the chip will be powered up on the nCS falling edge. The second way is asynchronous control by GPIO3 pin. GPIO3 pin can be configured as an nPD input (see Table 9). Its output is active low. The chip goes to power-down at same time when nPD is '0'. The chip will be powered up when nPD is '1'.

Device Functional Modes

Channel Sequencing Modes

The SGM5200Q has three channel sequencing modes: manual mode, auto-1 mode and auto-2 mode. Mode selection is configured by the mode control register (see Table 1, Table 2 and Table 5). The new channel selection is valid on the 2nd SCLK falling edge in the next frame in all three modes (refer to Figure 1).

Once the chip is configured to work in a selected mode, it keeps working in this mode until the chip is powered down, reset or reprogrammed. Allow it to exit multiple times and re-enter this mode without disturbing program register settings.

Manual Mode

When power-up or after reset, the default channel is 'channel 0' and the default mode is manual mode.

Auto-1 Mode

In auto-1 mode, the chip scans all selected channels in ascending order. The selected channels are configured in a program register. The auto-1 program register setting is shown in Table 3 and Table 4. The auto-1 program register is reset to '0hFFFF'.

Auto-2 Mode

In auto-2 mode, the chip scans all selected channels from channel 0 to the last channel. The last channel is configured in a program register. The auto-2 program register setting is shown in Table 6. The auto-2 program register is reset to '0hF'.

Device Programming and Mode Control

The chip has two kinds of registers named mode registers and program registers.

Power-Up Sequence

After power-up, the chip is in default manual mode and channel 0 is set as default channel. User needs to configure program register and mode register to set the chip working in target mode.

DETAILED DESCRIPTION (continued)

Operating in Manual Mode

The mode control register settings for manual mode are shown in Table 1. In manual mode, no program register is required.

The example for the chip how to work in manual mode and scan channels CH3, CH5 and CH7 is shown in Figure 5. In this sequence, in the frame N, keep in manual mode and channel CH3 is selected. In the frame N+1, keep in manual mode and channel CH5 is selected, and the internal MUX is switched to channel CH3 on the 2nd falling edge of SCLK. In the frame N+2, keep in manual mode and channel CH7 is selected. On the falling edge of nCS, channel CH3 input signal is sampling and conversion result is sent out in this frame, and the internal MUX is switched to CH5. And the chip repeats this sequence and sends out ADC conversion result data of CH5 and CH7 in the following two frames.

Table 1. Mode Control Register Details for Manual Mode

<table>
<tr><th>BITS</th><th colspan="4">DESCRIPTION</th><th>RESET STATE</th></tr>
<tr><td>DI[15:12]</td><td colspan="4">0001 = Select manual mode</td><td>0001</td></tr>
<tr><td>DI11</td><td colspan="4">0 = Chip retains values of DI[6:0] from the previous frame
1 = Enables programming of bits DI[6:0]</td><td>0</td></tr>
<tr><td>DI[10:7]</td><td colspan="4">The 4-bit data means the next channel address to be selected in the next frame. DI10 is MSB and DI7 is LSB. For example, 0000 = channel 0, 0001 = channel 1 and so on.</td><td>0000</td></tr>
<tr><td>DI6</td><td colspan="4">0 = Select 0V to V_{REF} input range (Range 1)
1 = Select 0V to 2 × V_{REF} input range (Range 2)</td><td>0</td></tr>
<tr><td>DI5</td><td colspan="4">0 = Normal operation (no power-down).
1 = Power down on the 16th SCLK falling edge.</td><td>0</td></tr>
<tr><td rowspan="3">DI4</td><td colspan="4">0 = SDO outputs current channel address of the channel on DO[15:12], and the 12-bit conversion results on DO[11:0]
1 = GPIO3 to GPIO0 data (both input and output) corresponds to DO[15:12] in the following order as shown. Lower data bits DO[11:0] means 12-bit conversion result for the current channel</td><td rowspan="3">0</td></tr>
<tr><td>DO15</td><td>DO14</td><td>DO13</td><td>DO12</td></tr>
<tr><td>GPIO3</td><td>GPIO2</td><td>GPIO1</td><td>GPIO0</td></tr>
<tr><td rowspan="3">DI[3:0]</td><td colspan="4">GPIO data of the channels is used as output. The data of the channel configured as input will be ignored by the device. The SDI bits and corresponding GPIO are shown below.</td><td rowspan="3">0000</td></tr>
<tr><td>DI3</td><td>DI2</td><td>DI1</td><td>DI0</td></tr>
<tr><td>GPIO3</td><td>GPIO2</td><td>GPIO1</td><td>GPIO0</td></tr>
</table>

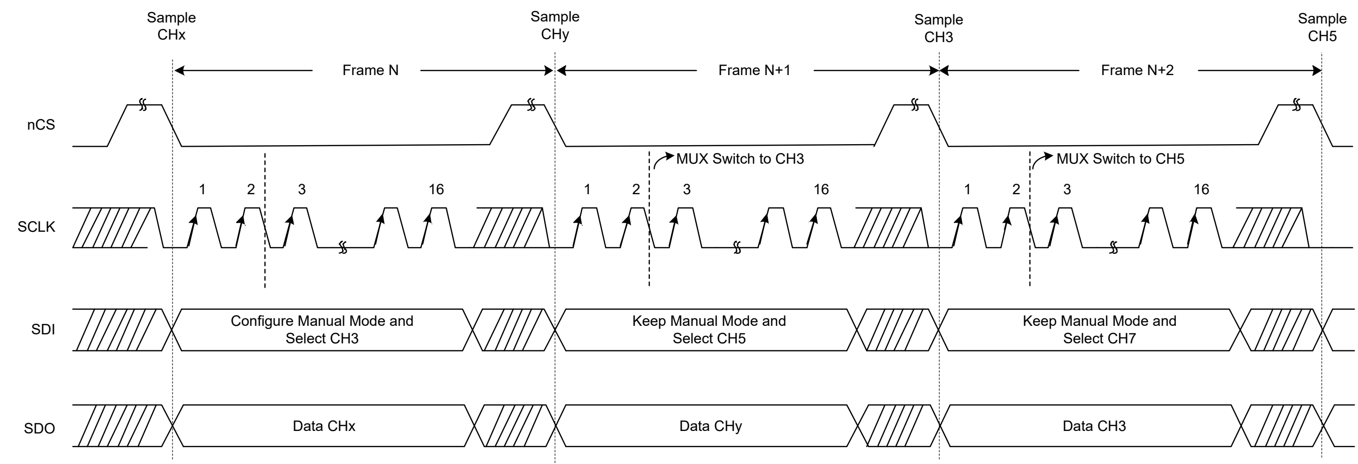


Figure 5. Example for Manual Mode Timing Diagram

DETAILED DESCRIPTION (continued)

Operating in Auto-1 Mode

The mode control register settings for auto-1 mode are shown in Table 2. There are both mode registers and program registers for auto-1 mode operation.

To let the chip work in auto-1 mode, it is necessary to configure auto-1 program register firstly to select which channels are going to be scanned.

The program register settings for auto-1 mode are shown in Table 3 and Table 4.

Before running in auto-1 mode, the target channels CH2, CH3 and CH5 (examples) must be configured in auto-1 program registers (see auto-1 program registers configuration sequence for details).

The example for the chip how to work in auto-1 mode and scan channels CH2, CH3 and CH5 automatically is shown in Figure 6. In this sequence, in the frame N, the chip enters auto-1 mode command and channel CH2 is selected automatically (the chip finds the first selected channel in ascending order automatically). In the frame N+1, the chip switches MUX to CH2. In the frame N+2, the chip samples the CH2 input and gives out ADC conversion result, and the MUX is switched to CH3 automatically. In the frame N+3, the chip samples CH3 and gives out ADC conversion results, and the MUX is switched to CH5 automatically, and so on. This process repeats until the last selected channel is reached, and the process loops back from the first selected channel.

In any case, re-entering auto-1 mode (it may be from auto-1 mode, manual mode and auto-2 mode) will cause the chip channel scan sequence restarts from the first selected channel.

Note that changing the auto-1 program register during the chip is working in auto-1 mode, the chip scan restarts from the first selected channel in ascending.

Figure 7 shows how the auto-1 program registers is configured. It is used to pre-select the channels for auto-1 scanning. It needs two operation frames for a complete configuration. More setting details are shown in Table 3 and Table 4.

Table 2. Mode Control Register Details for Auto-1 Mode

<table>
<tr><th>BITS</th><th colspan="4">DESCRIPTION</th><th>RESET STATE</th></tr>
<tr><td>DI[15:12]</td><td colspan="4">0010 = Select auto-1 mode</td><td>0001</td></tr>
<tr><td>DI11</td><td colspan="4">0 = Chip retains values of DI[10:0] from previous frame
1 = Enable programming of bits DI[10:0]</td><td>0</td></tr>
<tr><td>DI10</td><td colspan="4">0 = The channel counter increments every conversion (no reset)
1 = The channel counter is reset to the lowest programmed channel in the auto-1 program register</td><td>0</td></tr>
<tr><td>DI[9:7]</td><td colspan="4">xxx = Do not care</td><td>000</td></tr>
<tr><td>DI6</td><td colspan="4">0 = Select 0V to V_{REF} input range (Range 1)
1 = Select 0V to 2 × V_{REF} input range (Range 2)</td><td>0</td></tr>
<tr><td>DI5</td><td colspan="4">0 = Normal operation (no power-down).
1 = Power down on the 16th SCLK falling edge.</td><td>0</td></tr>
<tr><td rowspan="3">DI4</td><td colspan="4">0 = SDO outputs current channel address of the channel on DO[15:12], and the 12-bit conversion results on DO[11:0]
1 = GPIO3 to GPIO0 data (both input and output) corresponds to DO[15:12] in the following order as shown. Lower data bits DO[11:0] means 12-bit conversion result for the current channel</td><td rowspan="3">0</td></tr>
<tr><td>DO15</td><td>DO14</td><td>DO13</td><td>DO12</td></tr>
<tr><td>GPIO3</td><td>GPIO2</td><td>GPIO1</td><td>GPIO0</td></tr>
<tr><td rowspan="3">DI[3:0]</td><td colspan="4">GPIO data of the channels is used as output. The data of the channel configured as input will be ignored by the device. The SDI bits and corresponding GPIO are shown below.</td><td rowspan="3">0000</td></tr>
<tr><td>DI3</td><td>DI2</td><td>DI1</td><td>DI0</td></tr>
<tr><td>GPIO3</td><td>GPIO2</td><td>GPIO1</td><td>GPIO0</td></tr>
</table>

DETAILED DESCRIPTION (continued)

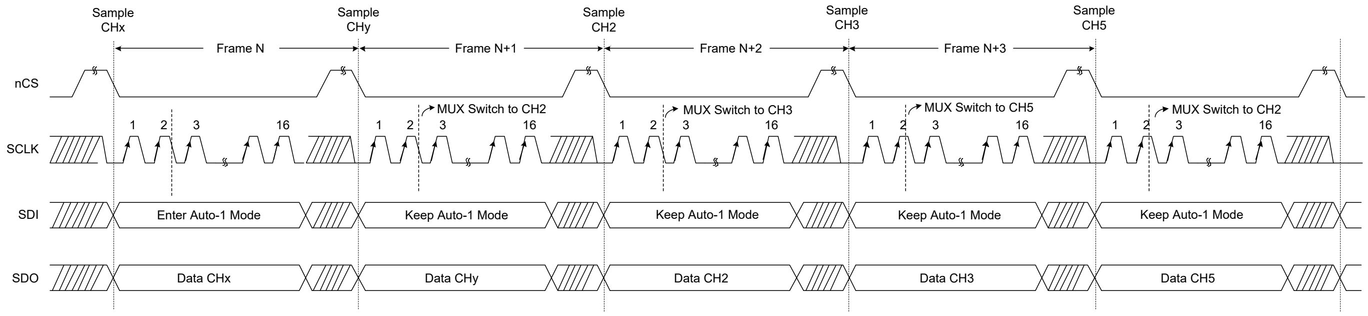
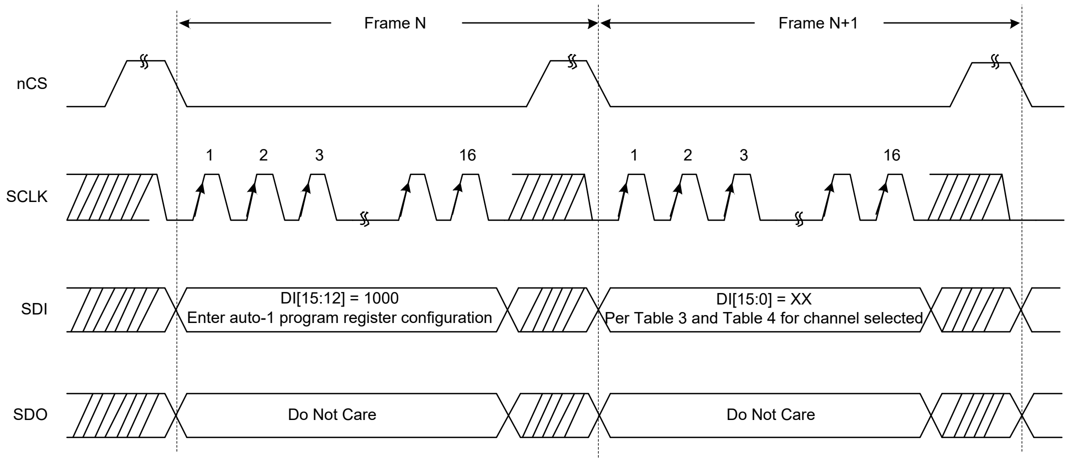


Figure 6. Example for Auto-1 Mode Timing Diagram



NOTE: During the programming process, the chip continues to run in the selected mode. The SDO is valid, but it is impossible to change the range or write GPIO data to the device during programming.

Figure 7. Auto-1 Program Register Setting

Table 3. Program Register Details for Auto-1 Mode

BITS	DESCRIPTION	RESET STATE
Frame 1		
DI[15:12]	1000 = Enter the sequence of auto-1 program. Configuration is done in the next frame	NA
DI[11:0]	Do not care.	NA
Frame 2		
DI[15:0]	1 (Individual Bit) = According bit is set to '1' means the according channel is selected in scanning sequence. The channel numbers are one-to-one associated with the SDI bits. For example, DI15 corresponds to CH15, DI14 corresponds to CH14 … DI0 corresponds to CH0 0 (Individual Bit) = According bit is set to '0' means the according channel is skipped in scanning sequence. The channel numbers are one-to-one associated with the SDI bits. For example, DI15 corresponds to CH15, DI14 corresponds to CH14 … DI0 corresponds to CH0	All '1'

Table 4. Channels Mapping to SDI Bits for the SGM5200Q

Device [1]	SDI Bits															
	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI0	DI4	DI3	DI2	DI1	DI0
16 Chan	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

NOTE:
1. The chip only scans the selected channels when in auto-1 mode.

DETAILED DESCRIPTION (continued)

Operating in Auto-2 Mode

The mode control register settings for auto-2 mode are shown in Table 5. There are both mode registers and program registers for auto-1 mode operation.

To let the chip work in auto-2 mode, it is necessary to configure auto-2 program register firstly to configure the last channel which is going to be reached.

The program register settings for auto-2 mode are shown in Table 6.

Before running in auto-2 mode, the last target channel CH2 (example) must be configured in auto-2 program registers (see auto-2 program registers configuration sequence for details).

The example about the chip how to work in auto-2 mode and scan channels CH0, CH1 and CH2 automatically is shown in Figure 8. In this sequence, in the frame N, the chip enters auto-2 mode command and channel CH0 is selected automatically (the chip switches to CH0 automatically). In the frame N+1, the chip switches MUX to CH02. In the frame N+2, the chip samples the CH0 input and gives out ADC conversion result, and the MUX is switched to CH1 automatically. In the frame N+3, the chip samples CH1 and gives out ADC conversion, and the MUX is switched to CH2 automatically, and so on. This process repeats until the last selected channel is reached (In this example, the last channel is CH2), and the process loops back from channel CH0.

In any case, re-entering auto-2 mode possibly from auto-1 mode, manual mode and auto-2 mode will cause the chip channel scan sequence to restart from the channel CH0.

Note that changing the auto-2 program register during the chip is working in auto-2 mode, the chip scan restarts from channel CH0.

Figure 9 shows how the auto-2 program registers is configured. It's for pre-select the last channel for auto-2 scanning. It needs one operation frames for a complete configuration. Refer to Table 6 for more setting details.

Table 5. Mode Control Register Details for Auto-2 Mode

BITS	DESCRIPTION				RESET STATE
DI[15:12]	0011 = Select auto-2 mode				0001
DI11	0 = Chip retains values of DI[10:0] from the previous frame 1 = Enable programming of bits DI[10:0]				0
DI10	0 = Channel counter increments every conversion (no reset) 1 = Channel number is reset to CH0				0
DI[9:7]	xxx = Do not care				000
DI6	0 = Select V_{REF} input range (Range 1) 1 = Select 2 × V_{REF} input range (Range 2)				0
DI5	0 = Normal operation (no power-down) 1 = Power down on the 16^{th} SCLK falling edge				0
DI4	0 = SDO outputs current channel address of the channel on DO[15:12], and the 12-bit conversion results on DO[11:0] 1 = GPIO3 to GPIO0 data (both input and output) corresponds to DO[15:12] in the following order as shown. Lower data bits DO[11:0] means 12-bit conversion result for the current channel				0
	DO15	DO14	DO13	DO12	
	GPIO3	GPIO2	GPIO1	GPIO0	
DI[3:0]	GPIO data of the channels is used as output. The data of the channel configured as input will be ignored by the device. The SDI bits and corresponding GPIO are shown below.				0000
	DI3	DI2	DI1	DI0	
	GPIO3	GPIO2	GPIO1	GPIO0	

DETAILED DESCRIPTION (continued)

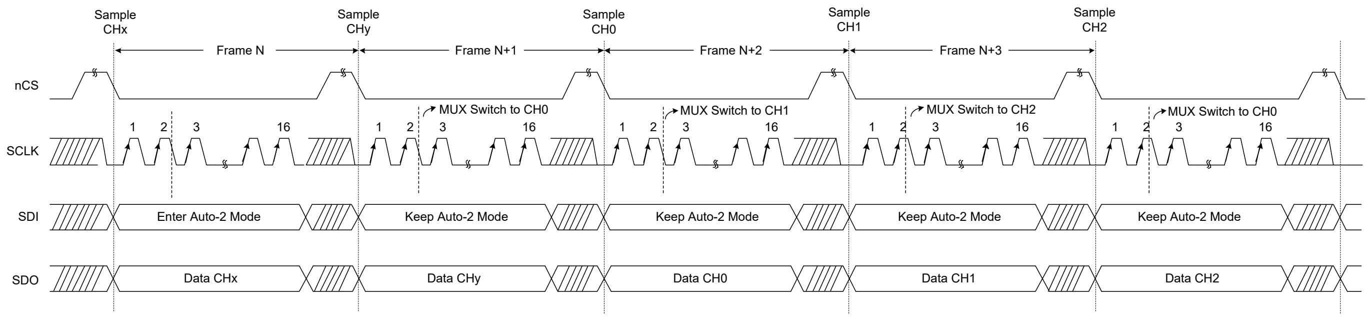
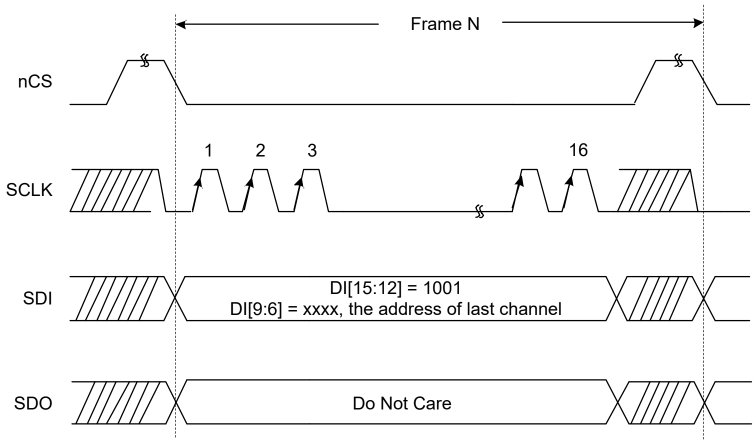


Figure 8. Example for Auto-2 Mode Timing Diagram



NOTE: During the programming process, the chip continues to run in the selected mode. The SDO is valid, but it is impossible to change the range or write GPIO data to the device during programming.

Figure 9. Auto-2 Program Register Setting

Table 6. Program Register Details for Auto-2 Mode

BITS	DESCRIPTION	RESET STATE
DI[15:12]	1001 = Configure auto-2 program register	NA
DI[11:10]	Do not care.	NA
DI[9:6]	aaaa = The 4-bit data means the address of the last channel in the scanning sequence. In auto-2 mode, the channel counter begins at CH0, increasing each frame until equal to 'aaaa'. The channel counter roles over to CH0 in the next frame	NA
DI[5:0]	Do not care.	NA

Continued Operation in a Selected Mode

When the chip is configured to working in one mode, the user may want to keep working in this mode. How to continue operating in a selected mode is shown in Table 7.

Table 7. Continued Operation in a Selected Mode

BITS	DESCRIPTION	RESET STATE
DI[15:12]	0000 = The chip continues to operate in current mode. When in auto-1 and auto-2 modes, the channel counter increments automatically. When in the manual mode, it continues with the last selected channel. The chip ignores datas on DI[11:0] and continues operating with the previous settings. SDI can be held low when there is no changes are required in the mode control register	0001
DI[11:0]	Chip ignores these bits when DI[15:12] is '0000'.	All '0'

DETAILED DESCRIPTION (continued)

Programming

Digital Output

Table 8 shows the theory output codes according to different input ranges. The ADC codes are in straight binary format.

GPIO Registers

The GPIO pins can be used as GPO (general-purpose output) or GPI (general-purpose input).

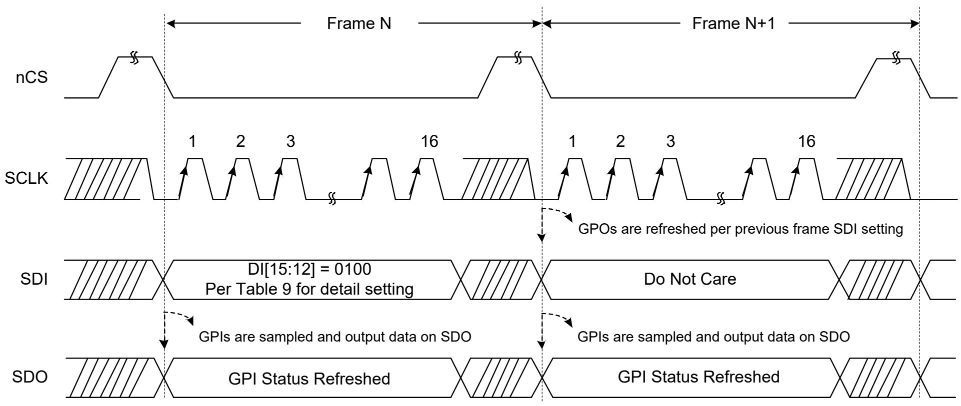
The GPIO functions and GPO status are set in GPIO program registers, more details refer to Table 9.

The GPO refresh includes two steps. The first step is to set the GPO data in the operation frame N, and the second step is to refresh the GPO data on the nCS falling edge in frame N+1. More details refer to Figure 10.

The chip samples the GPI input on the falling edge of nCS in frame N, and outputs GPI data on SDO in the same frame N.

Table 8. Ideal Input Voltages and Output Codes

Description	Analog Value		Digital Output Straight Binary	
Full Scale Range	Range 1 → V_{REF}	Range 2 → 2 × V_{REF}		
Least Significant Bit (LSB)	V_{REF}/4096	2 × V_{REF}/4096	**Binary Code**	**Hex Code**
Full Scale	V_{REF} - 1LSB	2 × V_{REF} - 1LSB	1111 1111 1111	FFF
Midscale	V_{REF}/2	V_{REF}	1000 0000 0000	800
Midscale - 1LSB	V_{REF}/2 - 1LSB	V_{REF} - 1LSB	0111 1111 1111	7FF
Zero	0V	0V	0000 0000 0000	000



NOTE: During the programming process, the chip continues to run in the selected mode. The SDO is valid, but it is impossible to change the range or write GPIO data to the device during programming.

Figure 10. GPIO Program Register Setting

DETAILED DESCRIPTION (continued)

Table 9. GPIO Program Register Details

BITS	DESCRIPTION	RESET STATE
DI[15:12]	0100 = Select GPIO program registers for programming	NA
DI[11:10]	00 = Reserved bits, must be '00'	00
DI9	0 = Normal operation 1 = Reset all registers in the next nCS frame to default value (it also resets itself)	0
DI8	0 = GPIO3 is still as general-purpose I/O 1 = Configure GPIO3 as the chip power-down input	0
DI7	0 = GPIO2 is still as general-purpose I/O 1 = Configure GPIO2 as device range input	0
DI[6:4]	000 = GPIO1 and GPIO0 are still as general-purpose I/Os xx1 = Configure GPIO0 as 'high or low' alarm output. It is an active high output. GPIO1 is still as general-purpose I/O 010 = Configure GPIO0 as high alarm output. It is an active high output. GPIO1 is still as general-purpose I/O 100 = Configure GPIO1 as low alarm output. It is an active high output. GPIO0 is still as general-purpose I/O 110 = Configure GPIO1 as low alarm output and GPIO0 as a high alarm output. These are active high outputs	000
DI3 (1)	0 = GPIO3 pin is configured as GPI (general-purpose input) 1 = GPIO3 pin is configured as GPO (general-purpose output)	0
DI2 (1)	0 = GPIO2 pin is configured as GPI 1 = GPIO2 pin is configured as GPO	0
DI1 (1)	0 = GPIO1 pin is configured as GPI 1 = GPIO1 pin is configured as GPO	0
DI0 (1)	0 = GPIO0 pin is configured as GPI 1 = GPIO0 pin is configured as GPO	0

NOTE:
1. The bits are valid for GPIOs that are not assigned a specific function by bits DI[8:4].

Alarm Thresholds for GPIO Pins

Each channel has separate high alarm threshold and low alarm threshold. To configure chip quickly, the input channels are divided into 4 groups, each group can be programmed consecutively (8 registers are programmed in one sequence).

In Table 10, the chip has its input channels divided into 4 groups.

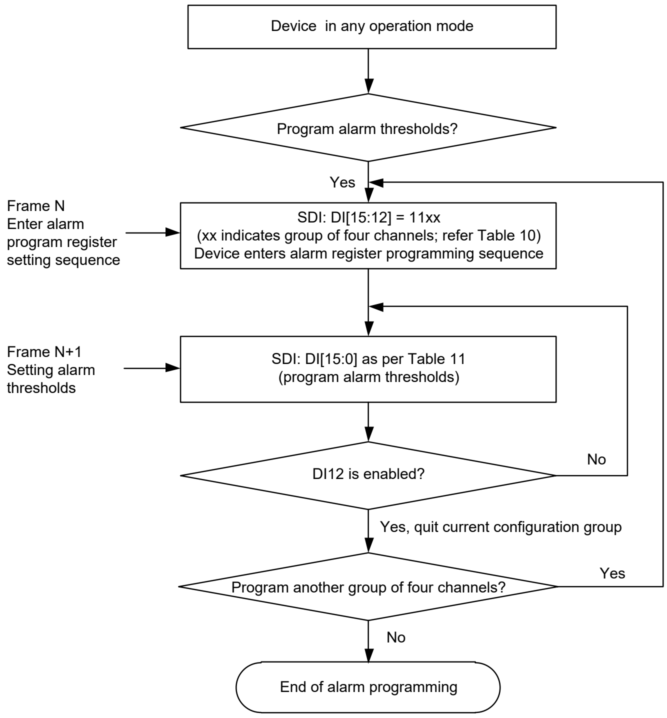
Table 11 shows details of the alarm program register.

Each group needs 9 operation frames to complete the alarm thresholds configuration. The chip supports to quit the configuration sequence in middle of progress (DI12 in alarm program register is enabled, and < 8 registers is configured). Once DI12 is enabled, the chip quits the configuration sequence in the next frame.

Table 10. Alarm Program Registers Groups

Group	Alarm Program Register DI[15:12]	Registers
0	1100	High and low alarm for CH0, CH1, CH2 and CH3
1	1101	High and low alarm for CH4, CH5, CH6 and CH7
2	1110	High and low alarm for CH8, CH9, CH10 and CH11
3	1111	High and low alarm for CH12, CH13, CH14 and CH15

DETAILED DESCRIPTION (continued)



NOTE: During the programming process, the chip continues to run in the selected mode. The SDO is valid, but it is impossible to change the range or write GPIO data to the device during programming.

Figure 11. Alarm Program Register Programming Flowchart

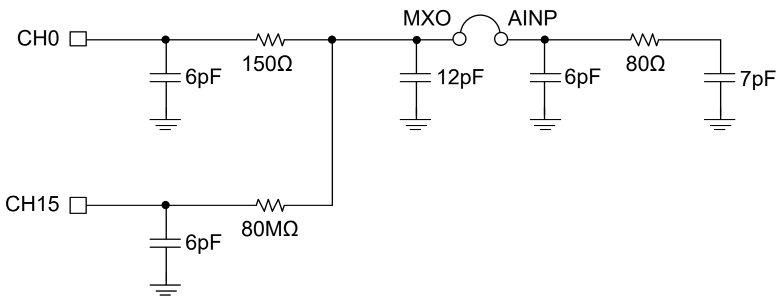
Table 11. Alarm Program Register Details

BITS	DESCRIPTION	RESET STATE
Frame 1		
DI[15:12]	1100 = Alarm programming sequence for group 0 1101 = Alarm programming sequence for group 1 1110 = Alarm programming sequence for group 2 1111 = Alarm programming sequence for group 3 Note: DI[15:12] = 11AA is the alarm programming request for group AA. "AA" means the alarm programming group number in binary format.	NA
DI[11:0]	Do not care.	NA
Frame 2 and Onwards		
DI[15:14]	CC = "CC" means the channel number in binary format in group AA (each group has 4 channels) The SGM5200Q programs the alarm for the channel represented by the binary number "AACC". "AA" is programmed in Frame 1.	NA
DI13	0 = Configure low alarm register 1 = Configure high alarm register	NA
DI12	0 = Continue alarm programming sequence in the next frame 1 = Exit alarm programming in the next frame Note: To quit the threshold configure sequence if all threshold registers have been configured, DI12 must be set to '1' to quit.	NA
DI[11:10]	Do not care.	NA
DI[9:0]	The 10-bit alarm threshold is compared with the upper 10-bit of the 12-bit conversion result.	'1111111111' for high alarm register and '0000000000' for low alarm register

DETAILED DESCRIPTION (continued)

Analog Input

Figure 12 shows the equivalent circuit model for the MUX and ADC.



NOTE: CH0 is assumed to be on, and CH15 is assumed to be off.

Figure 12. Equivalent Circuit for ADC and MUX

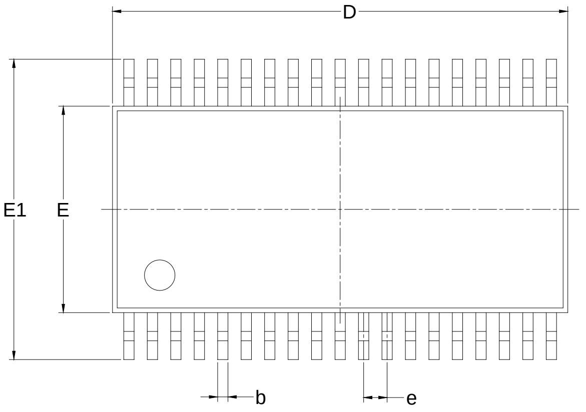
REVISION HISTORY

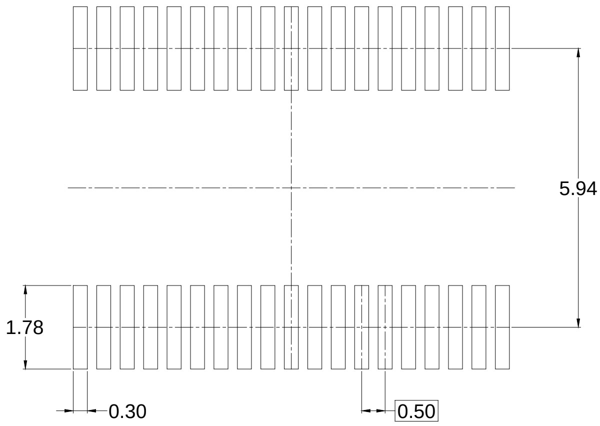
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (AUGUST 2023) to REV.A	Page
Changed from product preview to production data	All

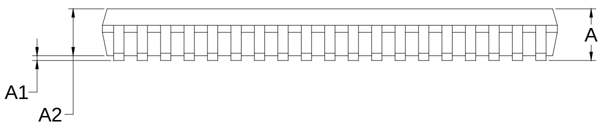
PACKAGE OUTLINE DIMENSIONS

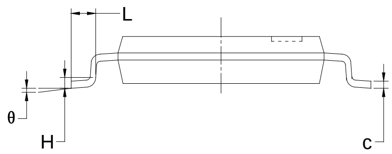
TSSOP-38





RECOMMENDED LAND PATTERN (Unit: mm)



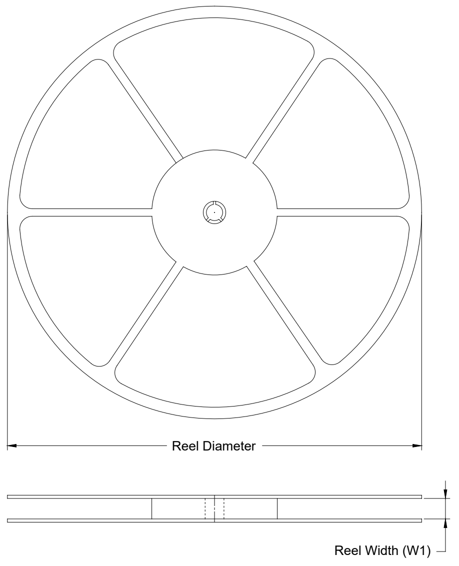


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.500 BSC		0.020 BSC	
H	0.250 TYP		0.010 TYP	
L	0.450	0.750	0.018	0.030
θ	1°	7°	1°	7°

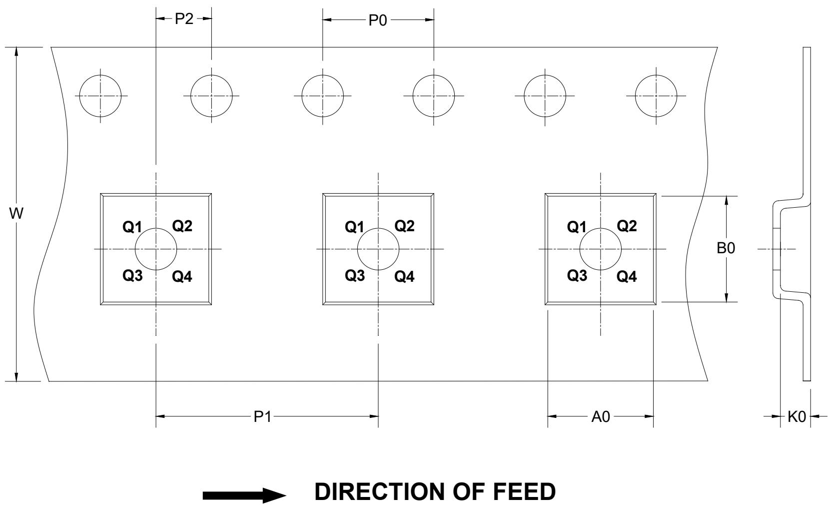
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



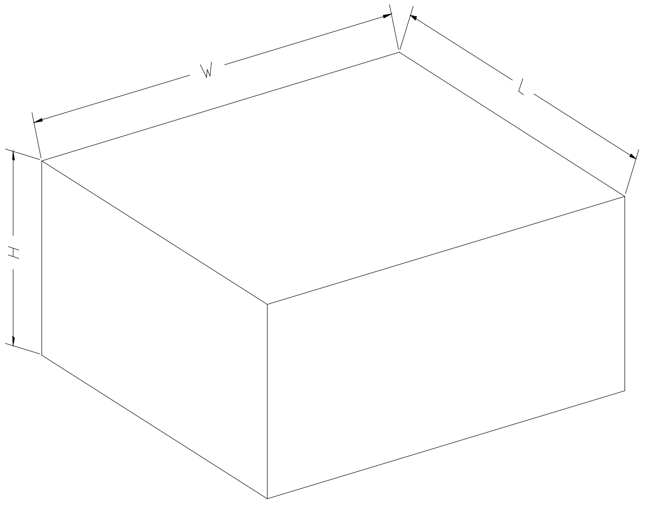
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-38	13″	16.4	6.80	10.25	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002