SGM52410C
Ultra-Small, Low-Power, 24-Bit Analog-to-Digital Converter with Internal Reference

GENERAL DESCRIPTION

The SGM52410C is a low-power, 24-bit, precision, sigma-delta (Σ-Δ) analog-to-digital converter (ADC). It operates from a 2V to 5.5V supply.

The SGM52410C contains a very low-drift on-chip reference and oscillator. It has an I^2C-compatible interface, and it can select four I^2C slave addresses. The data rate of the filter is up to 960SPS. The SGM52410C has an on-chip PGA, which can provide input ranges to as low as ±256mV from the power supply.

The input multiplexer supports 4 single-ended inputs or 2 differential inputs configuration.

The SGM52410C is available in Green MSOP-10 and UTQFN-2×1.5-10L packages. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Single-Supply Voltage Range: 2V to 5.5V**
  - **I^2C Bus Voltage Range: 2V to 5.5V**
- **Low Quiescent Current:**
  - **Continuous Mode: 310μA (TYP)**
  - **Power-Down Mode: 0.65μA (TYP)**
- **Selectable Data Rates: 5SPS to 960SPS**
- **Single-Cycle Settling**
- **50/60Hz Line Rejection**
- **Input Multiplexer**
  - **4 Single-Ended Inputs or 2 Differential Inputs**
- **Internal Programmable Gain Amplifier (PGA)**
- **Internal Voltage Reference and Oscillator**
- **Selectable Digital Comparator**
- **I^2C-Compatible Serial Interface**
- **Available in Green MSOP-10 and UTQFN-2×1.5-10L Packages**

APPLICATIONS

Portable Devices
Process Control
Battery Monitoring System
Temperature Measurement

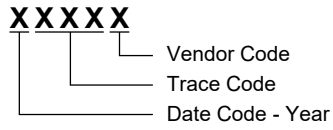
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM52410C	MSOP-10	-40℃ to +125℃	SGM52410CXMS10G/TR	SGM0KT XMS10 XXXXX	Tape and Reel, 4000
			SGM52410CXMS10SG/TR	SGM0KT XMS10 XXXXX	Tape and Reel, 500
	UTQFN-2×1.5-10L	-40℃ to +125℃	SGM52410CXURA10G/TR	0YU XXXX	Tape and Reel, 3000
			SGM52410CXURA10SG/TR	0YU XXXX	Tape and Reel, 500

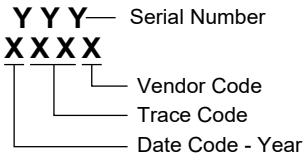
MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code. XXXXX = Date Code, Trace Code and Vendor Code.

MSOP-10



UTQFN-2×1.5-10L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)

V_{DD} ..... -0.3V to 5.5V

Analog Input Voltage..... -0.3V to 5.5V

SDA, SCL, ADDR, ALERT/RDY Voltage ..... -0.3V to 5.5V

Input Current (Momentary)..... 100mA

Input Current (Continuous) 10mA

Package Thermal Resistance

MSOP-10, θ_{JA} ..... 139.4℃/W

MSOP-10, θ_{JB} ..... 90.6℃/W

MSOP-10, θ_{JC} ..... 47.7℃/W

UTQFN-2×1.5-10L, θ_{JA} ..... 82.4℃/W

UTQFN-2×1.5-10L, θ_{JB} ..... 15.6℃/W

UTQFN-2×1.5-10L, θ_{JC} ..... 49.8℃/W

Junction Temperature.....+150℃

Storage Temperature Range .....-65℃ to +150℃

Lead Temperature (Soldering, 10s).....+260℃

ESD Susceptibility (1) (2)

HBM.....±4000V

CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

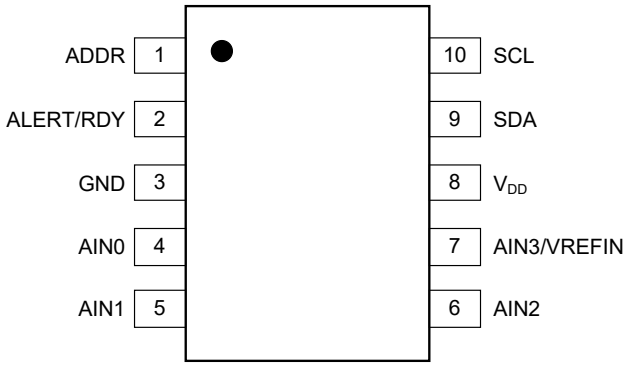
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

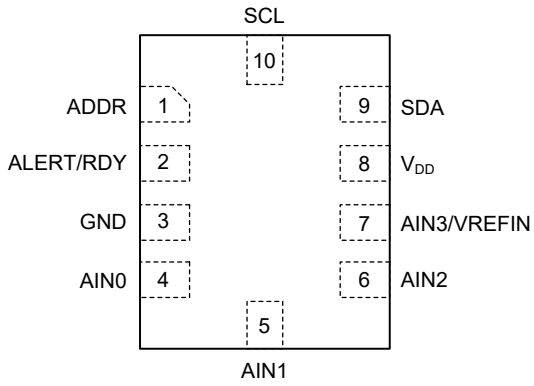
PIN CONFIGURATIONS

(TOP VIEW)



MSOP-10

(TOP VIEW)



UTQFN-2×1.5-10L

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
MSOP-10	UTQFN-2×1.5-10L			
1	1	ADDR	DI	I^2C Address Selection Pin.
2	2	ALERT/RDY	DO	Digital Comparator Output/Conversion Ready Pin.
3	3	GND	G	Ground.
4	4	AIN0	AI	Positive Input of Differential Channel 1 or Input of Single-Ended Channel 1.
5	5	AIN1	AI	Negative Input of Differential Channel 1 or Input of Single-Ended Channel 2.
6	6	AIN2	AI	Positive Input of Differential Channel 2 or Input of Single-Ended Channel 3.
7	7	AIN3/VREFIN	AI	Negative Input of Differential Channel 2 or Input of Single-Ended Channel 4, or External Reference Input.
8	8	V_{DD}	P	Power Supply Pin. It can be operated from 2V to 5.5V.
9	9	SDA	DIO	Serial Data Pin.
10	10	SCL	DI	Serial Clock Input Pin.

NOTE: AI = analog input, DI = digital input, DO = digital output, DIO = digital input and output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, DR = 5SPS, full-scale input voltage range (FSR) = ±2.048V, internal reference, maximum and minimum specifications apply from T_A = -40℃ to +125℃, typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Input							
Full-Scale Input Voltage (1)		V_{IN} = AIN_P - AIN_N			±4.096/PGA		V
Analog Input Voltage		AIN_P or AIN_N to GND		-0.1		V_{DD}	V
Differential Input Impedance					See Table 1		
System Performance							
Resolution		No missing codes		24			Bits
Data Rate	DR				See Table 5		SPS
Data Rate Variation		All data rates		-3.5		3.5	%
Output Noise				See Table 6 and Table 7			
Integral Nonlinearity	INL	DR = 5SPS, FSR = ±2.048V (2)			10	35	ppm
Offset Error	E_O	FSR = ±2.048V	Differential inputs		15	120	μV
			Single-ended inputs		15	150	
Offset Drift		FSR = ±2.048V			0.2	1	μV/℃
Offset Power Supply Rejection		FSR = ±2.048V			32		μV/V
Gain Error (3)	E_G	FSR = ±2.048V at +25℃			0.01	0.15	%
Gain Drift (3) (4)		FSR = ±0.256V			6		ppm/℃
		FSR = ±2.048V			6	15	
		FSR = ±6.144V (1)			6		
Gain Power Supply Rejection					80		ppm/V
PGA Gain Match (3)		Match between any two PGA gains			0.01	0.1	%
Gain Match		Match between any two inputs			0.01	0.08	%
Offset Match		Match between any two gains			45	400	μV
50/60Hz Rejection		FSR = ±2.048V			100		dB
Channel-to-Channel Crosstalk		At DC and FSR = ±2.048V, differential or single-ended inputs adjacent channels			110		dB
Common Mode Rejection Ratio	CMRR	At DC and FSR = ±0.256V			120		dB
		At DC and FSR = ±2.048V			120		
		At DC and FSR = ±6.144V (1)			120		

NOTES:

1. The full-scale range of the ADC scaling. In any event, it should not exceed V_{DD} + 0.3V applied to this device.

2. Best fit (99% of full-scale).

3. It includes all errors from on-chip PGA and reference.

4. Gain temperature drift is defined as the maximum change of gain error measured over the specified temperature range. The gain error drift is calculated using the box method, as described by Equation: Gain Error Drift = (GE_{MAX} - GE_{MIN})/(T_{MAX} - T_{MIN}).

Where:

- GE_{MAX} and GE_{MIN} are the maximum and minimum gain errors, respectively.
- T_{MAX} and T_{MIN} are the maximum and minimum temperatures, respectively, over the temperature range -40℃ to +125℃.

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, DR = 5SPS, full-scale input voltage range (FSR) = ±2.048V, internal reference, maximum and minimum specifications apply from T_A = -40℃ to +125℃, typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reference							
External Reference				0.5		2.5	V
External Reference Input Current		V_{REFIN} = 2.5V, continuous mode			2.35		μA
Digital Input/Output							
High Input Voltage (5)	V_{IH}			0.7 × V_{DD}			V
Low Input Voltage (5)	V_{IL}					0.3 × V_{DD}	V
Low Output Voltage	V_{OL}	I_{OL} = 3mA			0.13	0.4	V
High Input Leakage Current (6)	I_{IH}	V_{IH} = 5.5V			0.1	1	μA
Low Input Leakage Current (6)	I_{IL}	V_{IL} = GND			0.1	1	μA
Power Supply Requirements							
Power Supply Voltage	V_{DD}			2		5.5	V
Supply Current	I_{DD}	V_{DD} = 5.5V	Power-down current at +25℃		0.65	1.2	μA
			Power-down current up to +125℃			3.5	
			Operating current at +25℃		310	380	
			Operating current up to +125℃			400	
Power Dissipation	P_D	V_{DD} = 5V			1.5		mW
		V_{DD} = 3.3V			0.8		

NOTES:

5. There are two scenarios: V_{DD} = 5V, V_{BUS} can be 2V to 5V. V_{DD} = 3.3V, V_{BUS} should be 3.3V. Note that V_{BUS} = 2V may cause leakage in some extreme conditions, and it is better to make it higher than 3.1V. For V_{BUS} = V_{DD}, V_{IL}/V_{IH} = 30%/70% of V_{BUS}. For V_{BUS} = 3.3V and V_{DD} = 5V, V_{IL}/V_{IH} = 20%/80% of V_{BUS}.

6. Meet the "loss of V_{DD}" requirement of I^2C fast mode. When V_{DD} is lost, the leakage drawn from the pin is controlled.

TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	FAST MODE		HIGH-SPEED MODE		UNITS
			MIN	MAX	MIN	MAX	
SCL Operating Frequency	f_{SCL}		0.01	0.4	0.01	3.4	MHz
Bus Free Time between START and STOP Conditions	t_1		1300		160		ns
Hold Time after Repeated START Condition. After This Period, the First Clock is Generated	t_2		600		160		ns
SCL Clock Low Time	t_3		1300		160		ns
SCL Clock High Time	t_7		600		60		ns
Repeated START Condition Setup Time	t_9		600		160		ns
STOP Condition Setup Time	t_{10}		600		160		ns
Data Hold Time	t_5		0		0		ns
Data Setup Time	t_8		100		10		ns
Clock/Data Fall Time (1)	t_6			300		40	ns
Clock/Data Rise Time	t_4			300		80	ns

NOTE:

1. t_6 (MIN) for SDA output is 20ns for normal/fast mode and 10ns for high-speed mode. Glitch filter capability is 50ns for normal/fast mode and 10ns for high-speed mode.

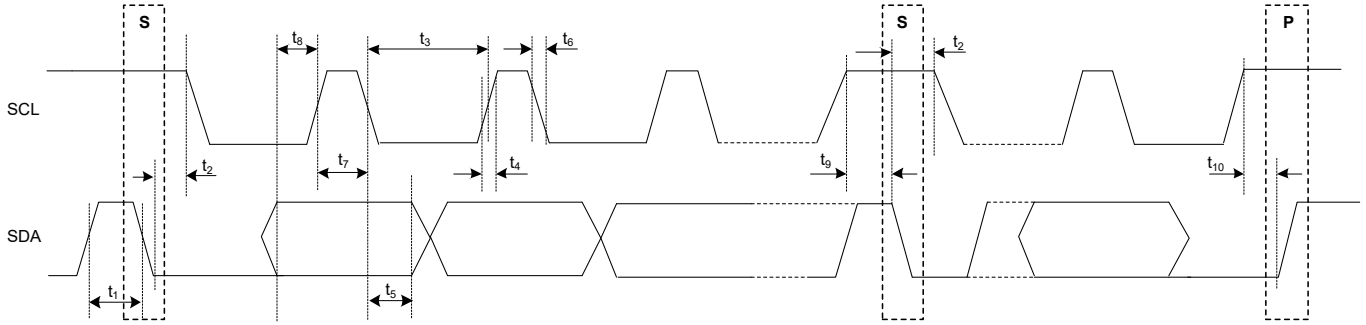
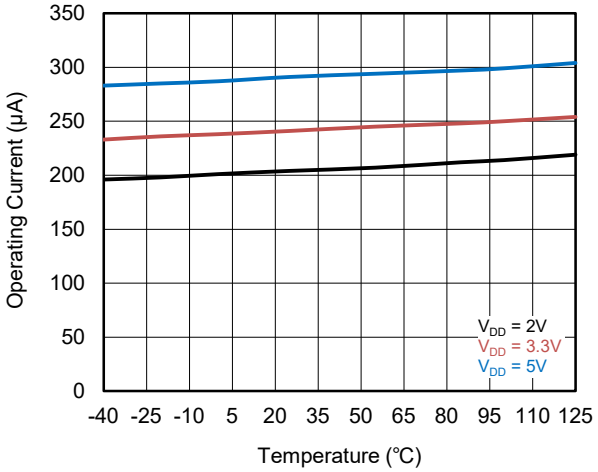


Figure 1. I²C Timing Diagram

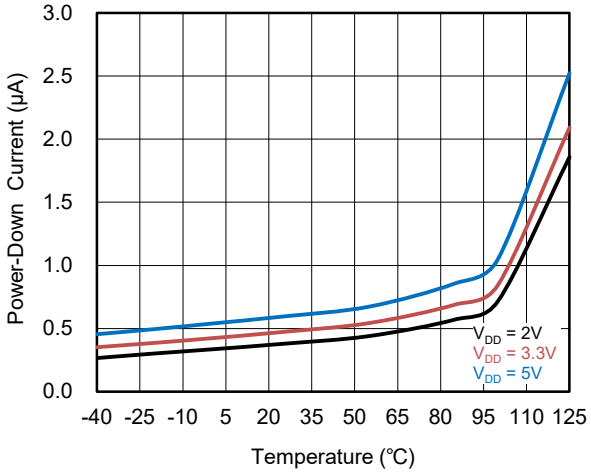
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{DD} = 3.3V, FSR = ±2.048V, DR = 5SPS, unless otherwise noted.

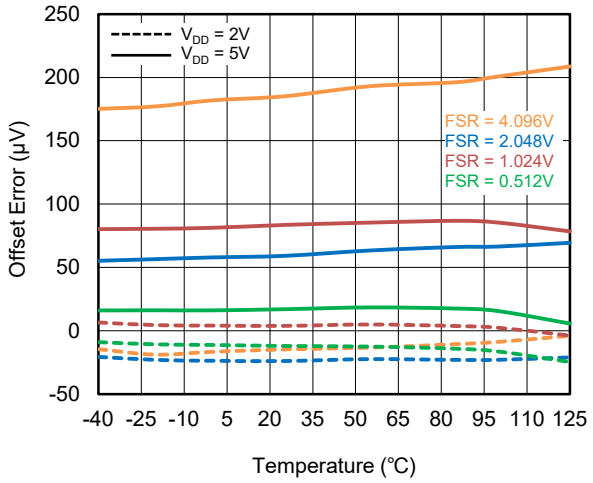
Operating Current vs. Temperature



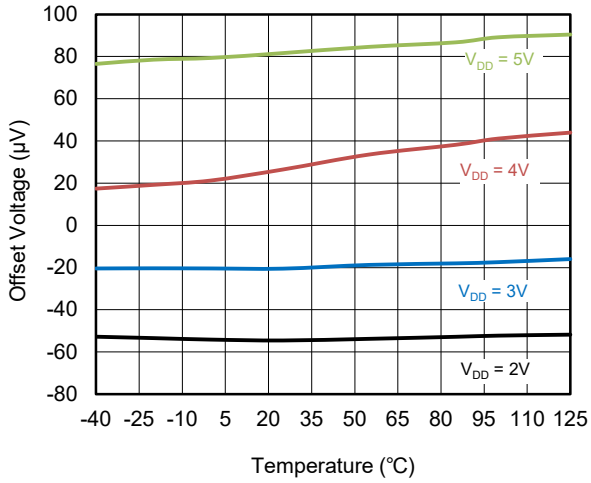
Power-Down Current vs. Temperature



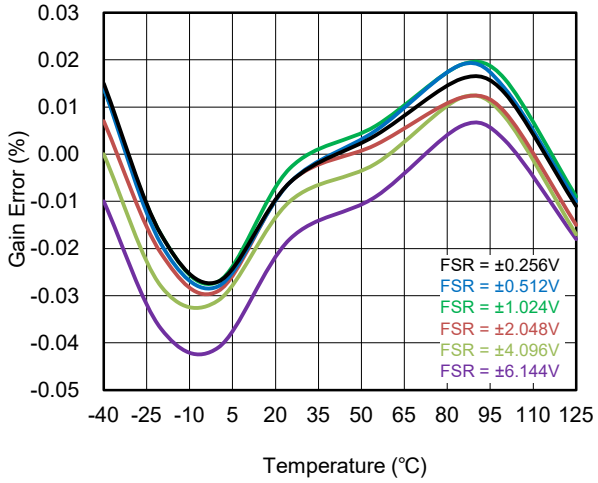
Single-Ended Offset Error vs. Temperature



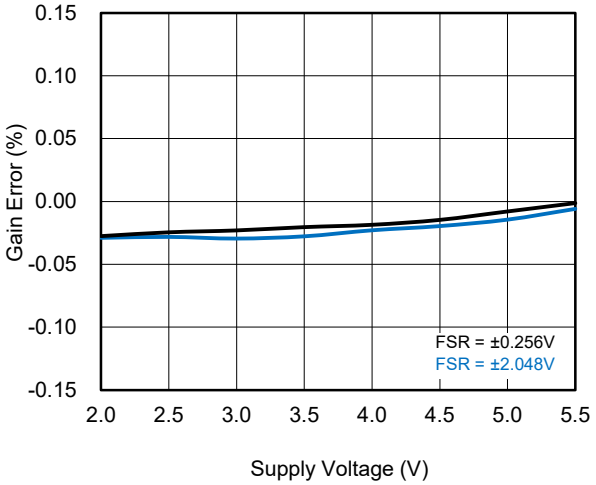
Differential Offset vs. Temperature



Gain Error vs. Temperature



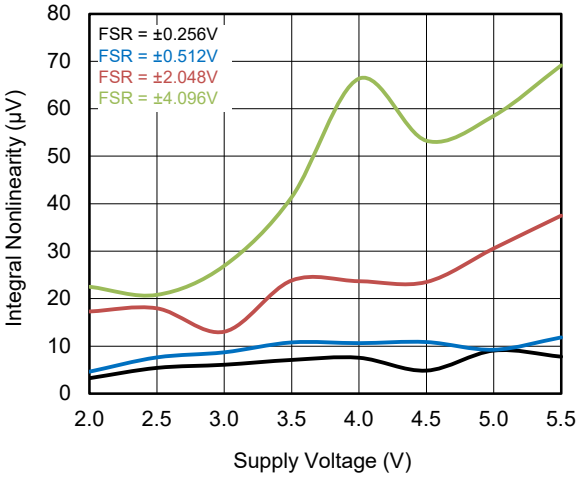
Gain Error vs. Supply Voltage



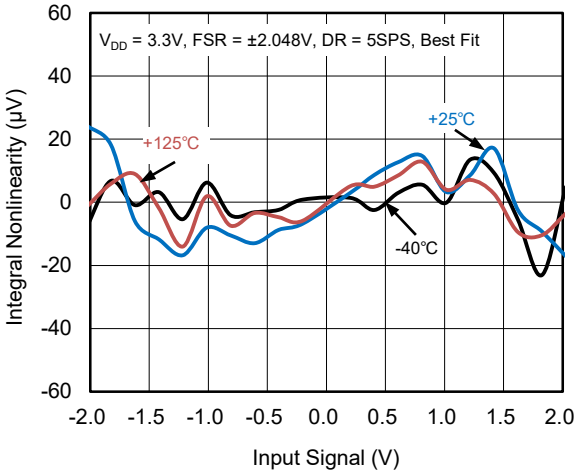
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 3.3V, FSR = ±2.048V, DR = 5SPS, unless otherwise noted.

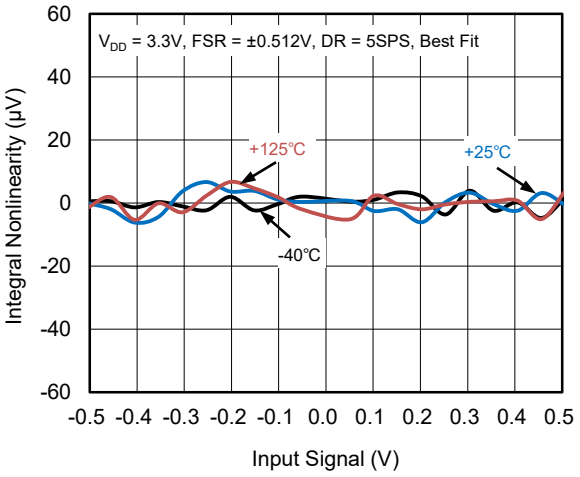
Integral Nonlinearity vs. Supply Voltage



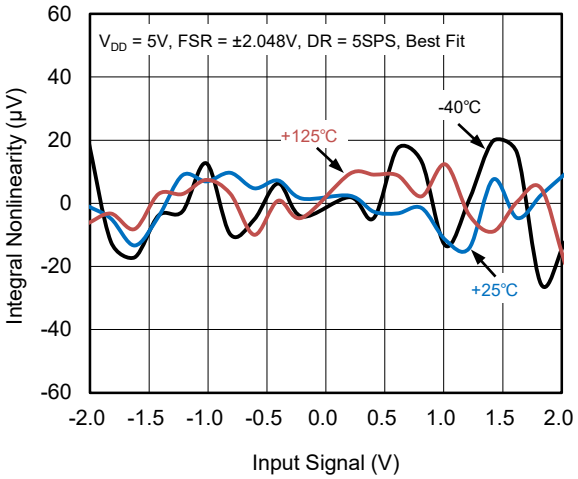
Integral Nonlinearity vs. Input Signal



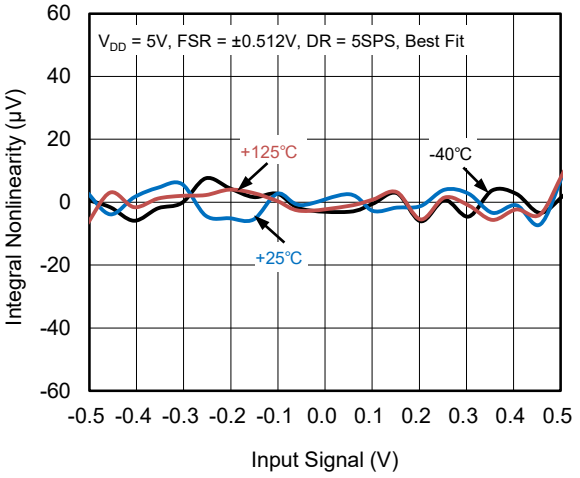
Integral Nonlinearity vs. Input Signal



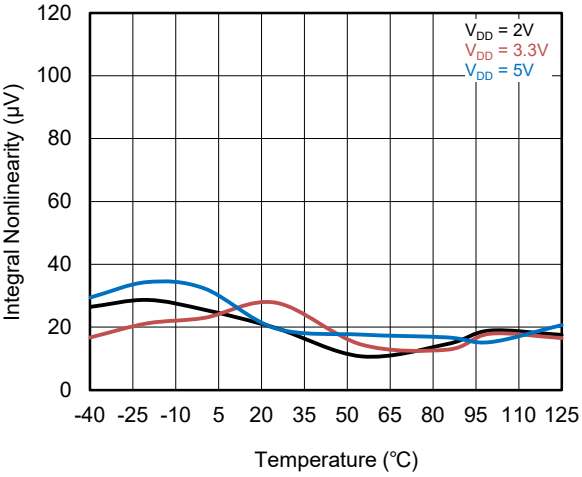
Integral Nonlinearity vs. Input Signal



Integral Nonlinearity vs. Input Signal



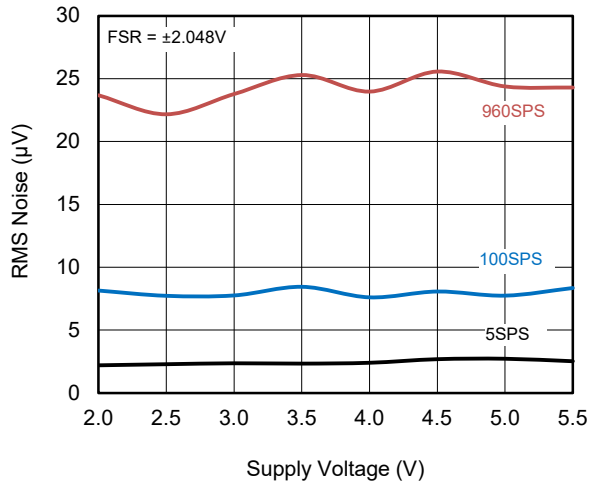
Integral Nonlinearity vs. Temperature



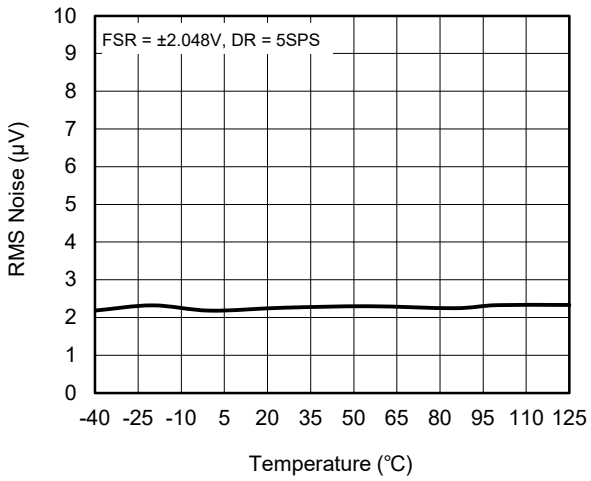
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 3.3V, FSR = ±2.048V, DR = 5SPS, unless otherwise noted.

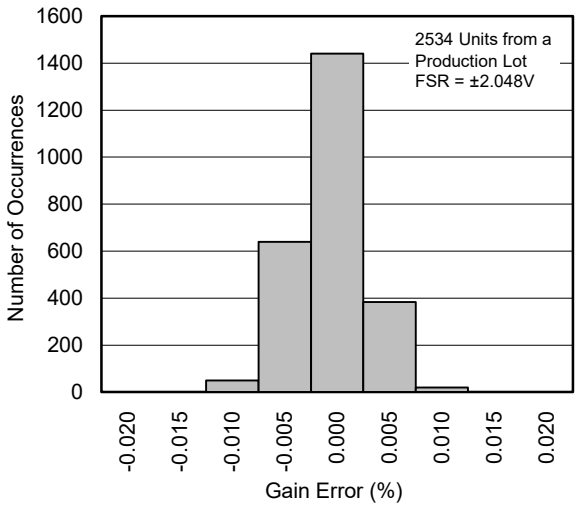
Noise vs. Supply Voltage



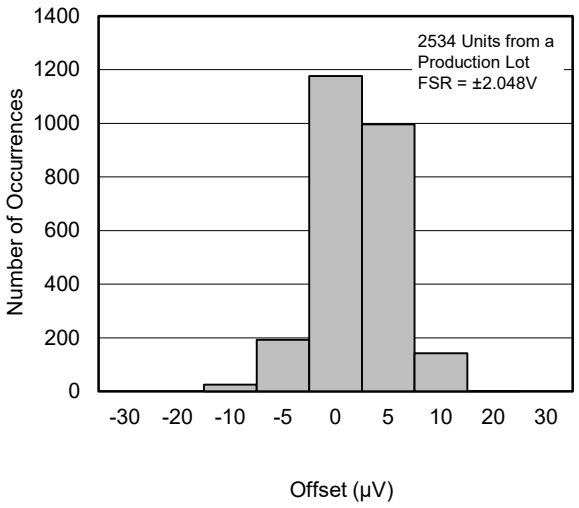
Noise vs. Temperature



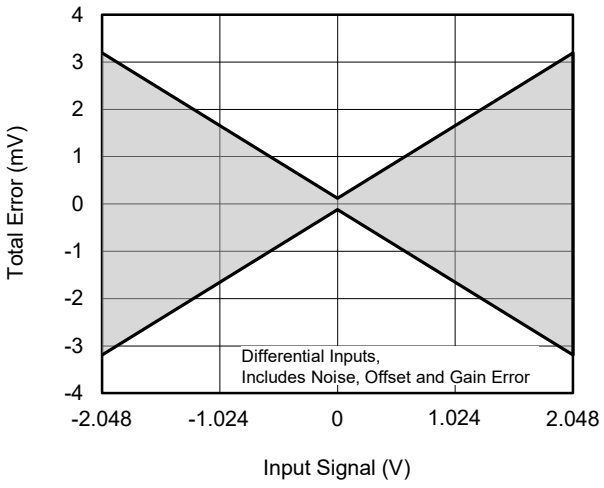
Gain Error Histogram



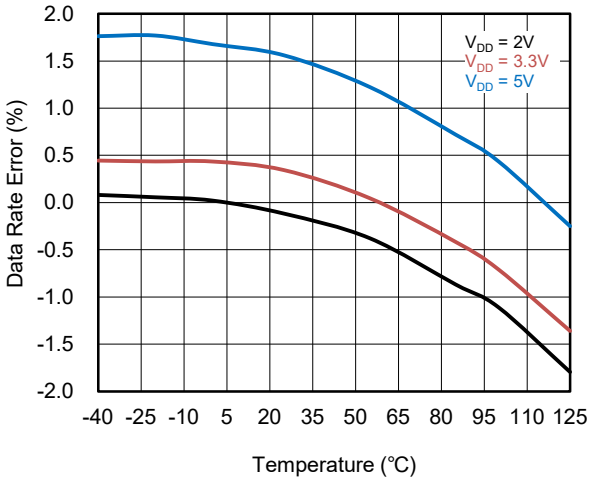
Offset Histogram



Total Error vs. Input Signal



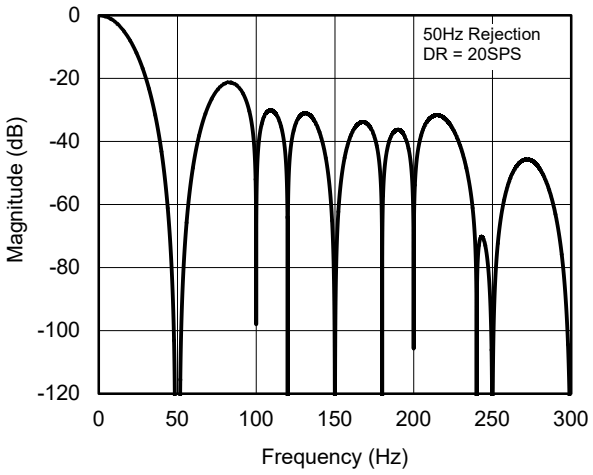
Data Rate vs. Temperature



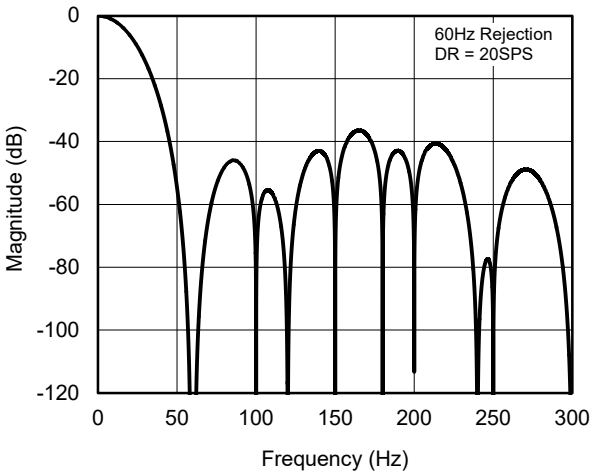
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 3.3V, FSR = ±2.048V, DR = 5SPS, unless otherwise noted.

Digital Filter Frequency Response



Digital Filter Frequency Response



FUNCTIONAL BLOCK DIAGRAM

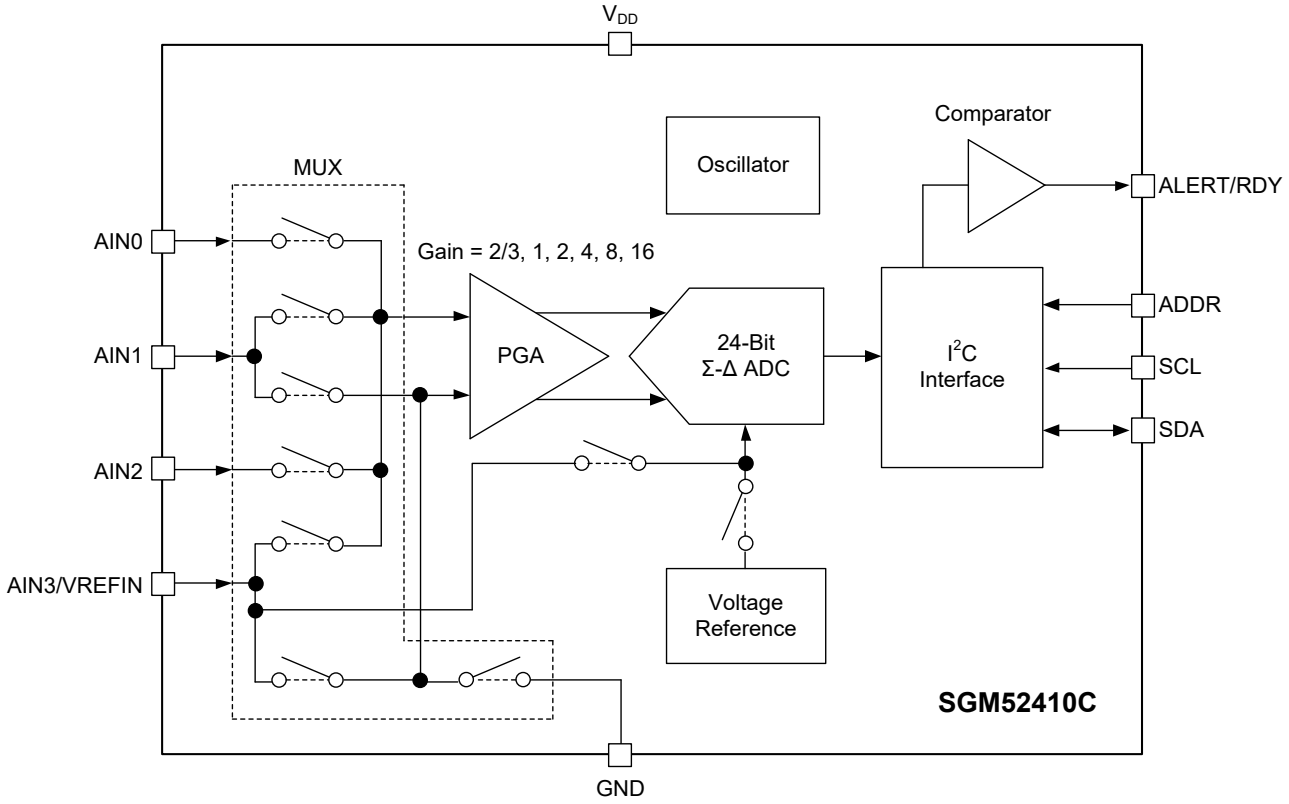


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Overview

The SGM52410C is a low-power, 24-bit, sigma-delta (Σ-Δ) analog-to-digital converter (ADC).

The SGM52410C supports both differential inputs and single-ended inputs.

The SGM52410C has two working modes: single-shot mode and continuous conversion mode.

In single-shot mode, the ADC performs one conversion and gives full settled data, no data needs to be discarded. Once ADC completes the conversion, it then goes to low-power shutdown mode.

In continuous mode, the ADC will achieve the first fully settled data without discarding any data, similar in single-shot mode. And the ADC begins a new conversion automatically after a previous conversion is completed. Every conversion result is given out. The data rate is equal to the configured data rate.

Quickstart Guide

The basic connection of ADC is shown in Figure 3. The communication interface is I^2C compatible. The SGM52410C works in slave mode. The I^2C address is configured as 0b1001000 (ADDR is connected to GND).

Figure 4, Figure 5 and Figure 6 show the demo read and write operation sequences.

For example, writing to the configuration register 0x1 sets the SGM52410C to continuous conversion mode, the following order can be followed:

1. The first byte, 0b1001000 (first 7-bit is I^2C address), the 8^{th} bit is read/write bit which is low writing now
2. The second byte, 0b00000001 (points to Config register 0x1)
3. The third byte, 0b10000100 (MSB of the Config register to be written, Bit[8] = '0' means the continuous mode)
4. The fourth byte, 0b10000011 (LSB of the Config register to be written, Bit[7:5] = '100' means data rate 100Hz)

For example, to read the conversion result from SGM52410C, the following order can be followed:

1. The first byte, 0b1001000 (first 7-bit is I^2C address), the 8^{th} bit is read/write bit which is low writing now
2. The second byte, 0b00000000 (points to Conversion register 0x0)
3. The third byte, 0b10010001 (first 7-bit is I^2C address), the 8^{th} bit is read/write bit which is high reading now
4. The fourth byte, the SGM52410C answers with the MSB of the Conversion register
5. The fifth byte, the SGM52410C answers with the M - LSB of the Conversion register
6. The sixth byte, the SGM52410C answers with the LSB of the Conversion register

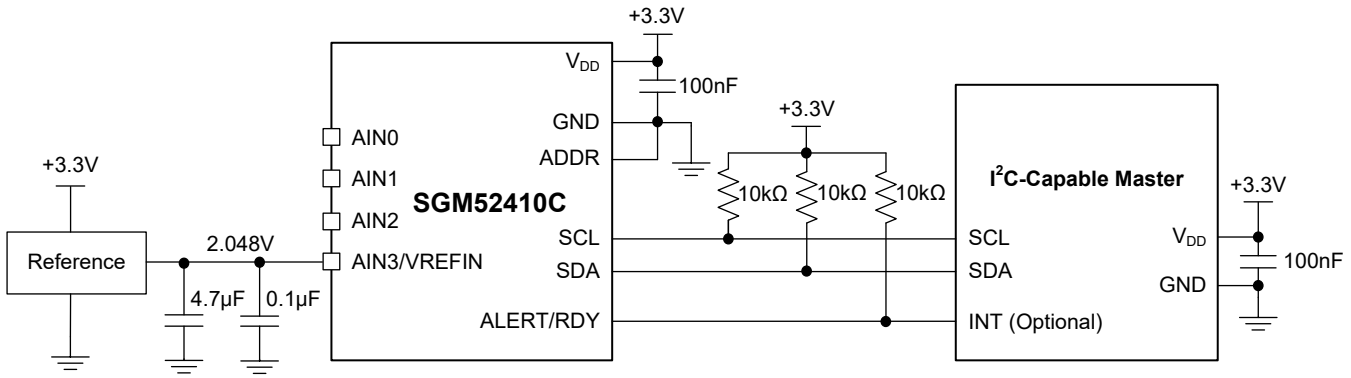
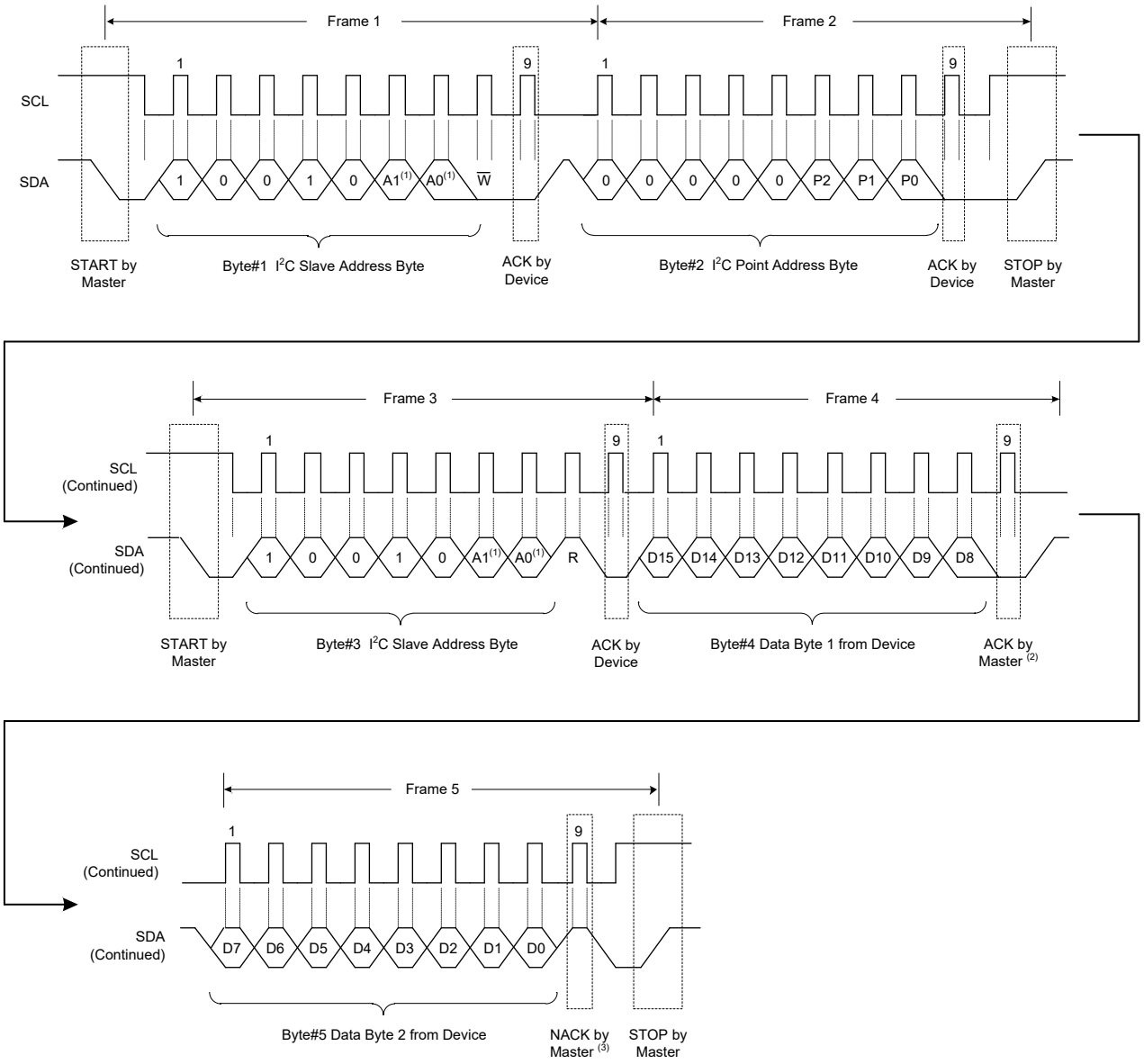


Figure 3. Basic Hardware Configuration

DETAILED DESCRIPTION (continued)

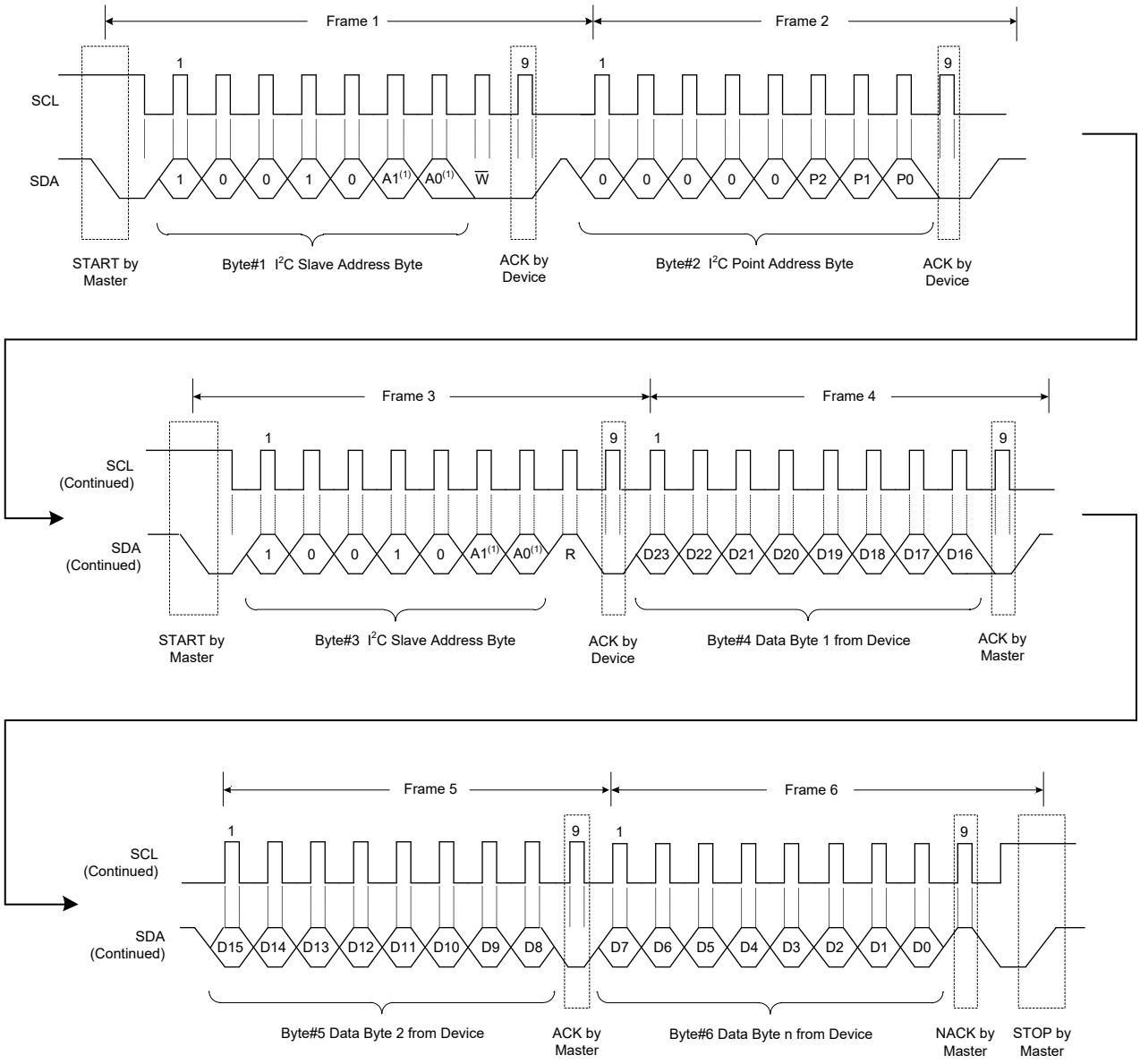


NOTES:

1. The A0 and A1 values depend on the ADDR pin.
2. SDA can be set high by master to terminate a single-byte read operation.
3. SDA can be set high by master to terminate a two-byte read operation.

Figure 4. Timing Diagram for Read Word Register

DETAILED DESCRIPTION (continued)

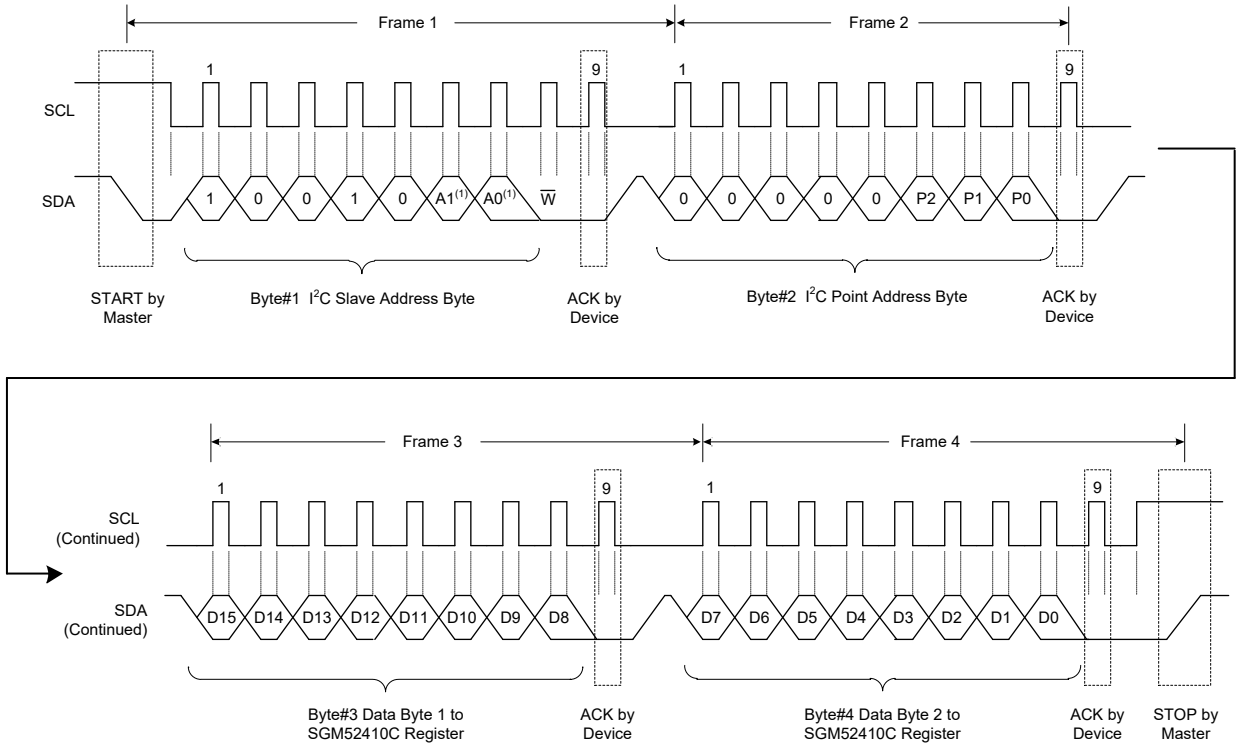


NOTES:

1. The A0 and A1 values depend on the ADDR pin.
2. SDA can be set high by master to terminate a single-byte read operation.
3. SDA can be set high by master to terminate a two-byte read operation.

Figure 5. Timing Diagram for Reading Three Bytes Register

DETAILED DESCRIPTION (continued)



NOTE:

1. The A0 and A1 values depend on the ADDR pin.

Figure 6. Timing Diagram for Write Word Register

Multiplexer

The SGM52410C has a flexible input multiplexer. It can be configured as 2 differential inputs or 4 single-ended inputs.

Whether the input is configured as differential inputs or single-ended inputs, the absolute voltage on any inputs pin must be in the range from GND to V_{DD}.

Analog Inputs

The SGM52410C has a switched capacitor input stage. There are charge and discharge current when ADC is working. The equal effective input impedance can be estimated by $R_{EFF} = V_{IN}/I_{AVERAGE}$.

The differential input impedance is Z_{DIFF} in Figure 7. Table 1 shows the typical differential input impedance.

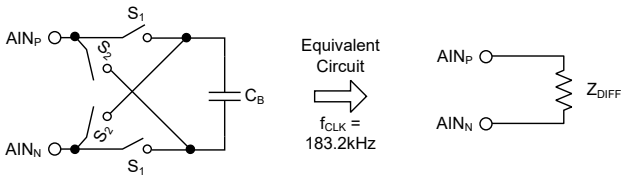


Figure 7. Simplified Analog Input Circuit

Table 1. Differential Input Impedance

FSR (V)	Differential Input Impedance (MΩ)
±6.144 (1)	2.3
±4.096 (1)	2.1
±2.048	1.4
±1.024	1.2
±0.512	0.752
±0.256	0.452

NOTE:

1. FSR = Full-scale range of the ADC scaling. In any event, it should not exceed V_{DD} + 0.3V applied to this device.

DETAILED DESCRIPTION (continued)

Full-Scale Input

The SGM52410C has an internal PGA. The PGA can be set to gains of 2/3, 1, 2, 4, 8 or 16. Table 2 and Table 3 show the corresponding full-scale ranges (FSR).

Analog input voltages can never exceed the analog input voltage limits.

Table 2. PGA Gain Full-Scale Range with Internal Reference

PGA Setting	FSR (V)
2/3	±6.144 (1)
1	±4.096 (1)
2	±2.048
4	±1.024
8	±0.512
16	±0.256

NOTE:
1. FSR = Full-scale range of the ADC scaling. In any event, it should not exceed V_{DD} + 0.3V applied to this device.

Table 3. PGA Gain Full-Scale Range with External Reference

PGA Setting	FSR (V)
2/3	±6.144 × V_{REF}/1.2
1	±4.096 × V_{REF}/1.2
2	±2.048 × V_{REF}/1.2
4	±1.024 × V_{REF}/1.2
8	±0.512 × V_{REF}/1.2
16	±0.256 × V_{REF}/1.2

Data Format

The SGM52410C conversion result data is in binary two's complement format.

Table 4 shows the ideal output codes for different input signals.

Table 4. Ideal Output Code for Different Input Signals

Input Signal V_{IN} (AIN_P - AIN_N)	Ideal Output Code (1)
≥ FS (2^{23} - 1)/2^{23}	7FFFFFh
+FS/2^{23}	000001h
0	0
-FS/2^{23}	FFFFFFh
≤ -FS	800000h

NOTE:

1. Except for effects of INL, noise, offset, and gain errors.

Aliasing

For some applications, an RC external filtering is recommended.

Operating Modes

The SGM52410C has two working modes, continuous mode and single-shot mode.

In continuous mode, the ADC begins a new conversion automatically after a previous conversion is completed. Every conversion result is given out.

In single-shot mode, if OS bit is written to '1', a single-shot conversion is started, during the conversion process, the OS bit is kept '0', and the chip doesn't response to OS bit operation. If conversion data is ready, the OS bit is set to '1' and the chip goes power-down automatically, and user can write '1' to OS bit to call a single-shot conversion again.

Power-Up and Reset

When the SGM52410C is powered up, all registers are reset to default values.

The SGM52410C supports I^2C general call reset command. See I^2C General Call section for details.

Duty Cycling for Low-Power

In some power sensitive application, the SGM52410C can work in sampling and power-down mode periodically. The duty cycle of working time and power-down time can be controlled by microcontroller flexibly.

For example, if the SGM52410C is configured as sample data rate at 960Hz, it can be operated with 125ms duty cycle. It means that if the chip is called to do single-shot conversion every 125ms, it will take the chip 1.2ms for sampling and then stay in power-down mode for 123.8ms. Under this working mode, it will reduce 103/104 power consumption compare with 960Hz operation in continuous mode.

Data Rate

Table 5. ADC Output Data Rate (SPS)

DR[2:0] Bits in Config Register	ODR
000	5Hz
001	10Hz
010	20Hz
011	50Hz
100	100Hz
101	200Hz
110	480Hz
111	960Hz

DETAILED DESCRIPTION (continued)

Comparator

The SGM52410C has an inside comparator that can be used to check ADC conversion results with high threshold and low threshold. When the result exceeds the limited setting, the chip can give an alert on the ALERT/RDY pin.

The comparator has two workings modes: traditional mode and window comparator mode. These modes are configurable. Under both working modes, the comparator can be configured as latch output or no-latch output (COMP_LAT bit in Config register). In latch output mode, the latched comparator output can be cleared by issuing an SMBus alert response or by reading the Conversion register. The ALERT/RDY pin output active polarity (low or high) can be configured by COMP_POL bit in Config register. Demos are shown in Figure 8 and Figure 9.

The comparator output trigger waiting times can be set by COMP_QUE[1:0] bits in Config register. It means comparator output can wait until the ADC results beyond the threshold configured times (which can be one, two, or four times). See Config Register section for details.

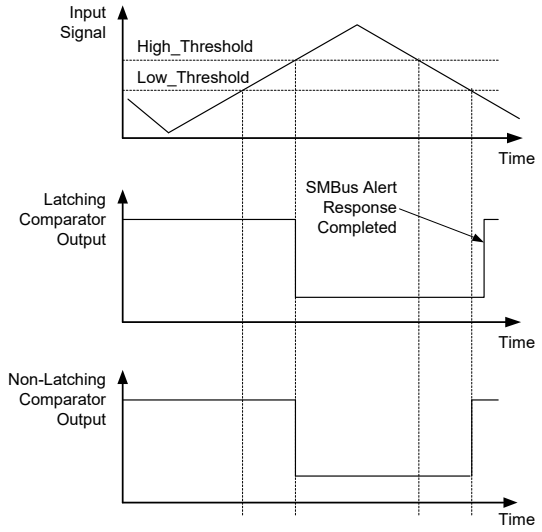


Figure 8. Alert Pin Timing Diagram when Configured as a Traditional Comparator

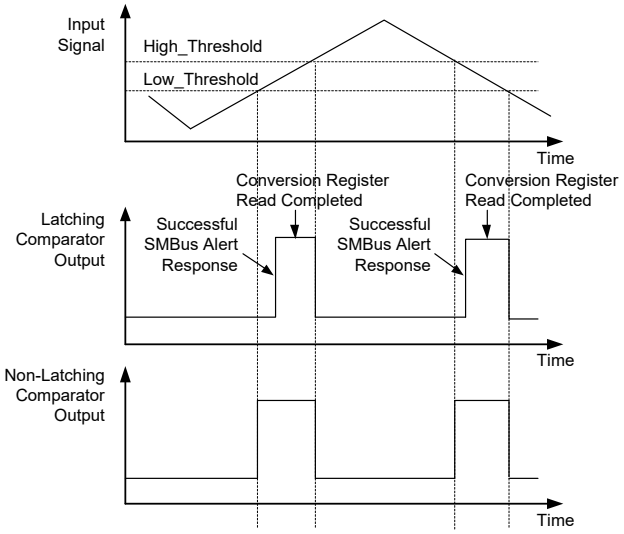


Figure 9. Alert Pin Timing Diagram when Configured as a Window Comparator

ADC Noise

Table 6. ADC Noise with Internal Reference (RMS in μV)

DR / FSR	960	480	200	100	50	20	10	5
6.144	77.08	49.71	33.43	25.44	17.53	13.74	9.84	6.68
4.096	52.21	33.72	23.05	16.15	12.11	9.24	6.47	4.36
2.048	23.65	16.53	11.67	8.45	5.60	4.66	3.27	2.17
1.024	13.86	9.64	6.06	4.63	3.45	2.74	1.78	1.26
0.512	7.30	4.81	3.20	2.45	1.70	1.39	0.91	0.65
0.256	3.89	2.67	1.75	1.27	0.98	0.70	0.49	0.35

Table 7. ADC ENOB (ENOB = ln(FSR/$V_{RMS\text{-}Noise}$)/ln(2))

DR / FSR	960	480	200	100	50	20	10	5
6.144	17.28	17.92	18.49	18.88	19.42	19.77	20.25	20.81
4.096	17.26	17.89	18.44	18.95	19.37	19.76	20.27	20.84
2.048	17.40	17.92	18.42	18.89	19.48	19.74	20.26	20.85
1.024	17.17	17.70	18.37	18.76	19.18	19.51	20.13	20.64
0.512	17.10	17.70	18.29	18.67	19.20	19.49	20.10	20.58
0.256	17.01	17.55	18.16	18.62	18.99	19.47	20.01	20.50

DETAILED DESCRIPTION (continued)

Digital Filter

The SGM52410C features a finite impulse response (FIR) digital filter with linear-phase characteristics. This filter serves a dual purpose, filtering and decimating the incoming digital data stream from the modulator. Notably, the digital filter automatically adapts to different data rates, ensuring a settling process within a single cycle. Operating at data rates of 5SPS, 10SPS and 20SPS, the filter configuration provides flexibility to reject either 50Hz or 60Hz line frequencies. One bit (DR_SEL) in the configuration register enables easy customization of the filter's behavior.

Conversion Ready Pin

If ALERT/RDY pin is used as a conversion ready pin, the following operations need to be followed, firstly set the MSB (Most Significant Bit) of the high threshold register to '1', secondly set the MSB of the low threshold register to '0', and select COMP_QUE[1:0] bits in '00'/'01'/'10' modes. It should be noted that COMP_QUE[1:0] bits can disable this pin function. The COMP_MODE and COMP_LAT bits have no affection on this function.

The ALERT/RDY pin is an open-drain output, it needs a pull-up resistor outside.

When the SGM52410C works in continuous mode, the ALERT/RDY pin gives a pulse (~8μs) at the end of every conversion completion.

When the SGM52410C works in single-shot mode, the ALERT/RDY pin goes low (COMP_POL bit is set to '0') when the conversion data is ready, and keeps low until the next conversion starts. Please see demos in Figure 10 and Figure 11.

SMBus Alert Response

The ALERT/RDY pin can output as an SMBus alert. When it is in latch mode, the COMP_LAT bit is set to '1'. And the pin output is latched, it can be cleared by reading ADC conversion data, or by issuing an SMBus alert response (reading the alerting device I^2C address).

If an alert is output at the ALERT/RDY pin and latched, the master controller accepts the alert, it sent an SMBus alert command (0b00011001) to I^2C bus. Any SGM52410C on the bus will response with their own address, the lowest I^2C address chip will occupy the bus and it will clear itself ALERT/RDY pin, the chip which loses I^2C bus will keep alert on ALERT/RDY pin. The master will repeat SMBus alert command until all salve chips clear their alert.

When ALERT/RDY pin is configured as window comparator mode, if ADC result is higher than upper threshold or ADC result is below the lower threshold, the pin is set (active low or active high).

Timing diagram for SMBus alert response is shown in Figure 12.

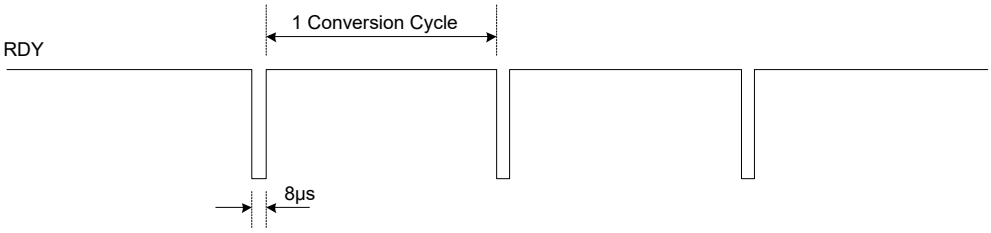


Figure 10. RDY in Continuous Mode

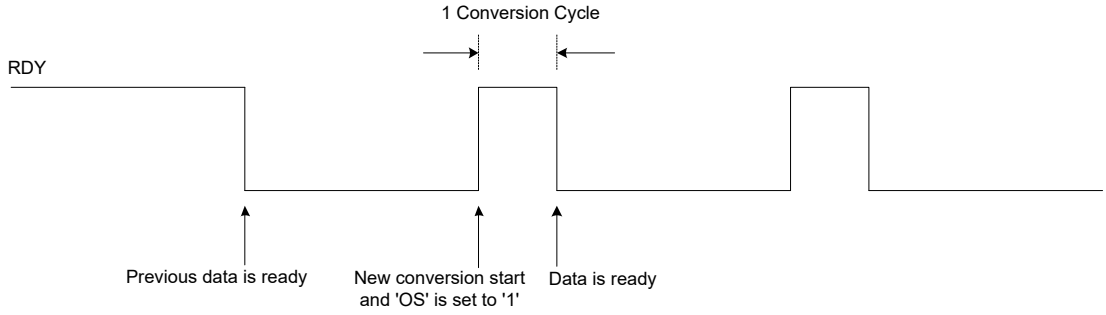
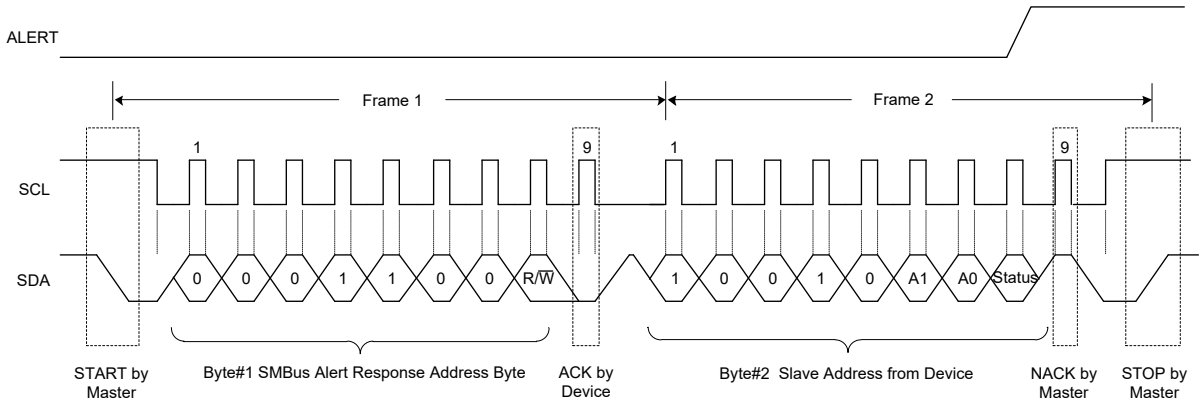


Figure 11. RDY in Single-Shot Mode

DETAILED DESCRIPTION (continued)



NOTE:

1. The A0 and A1 values depend on the ADDR pin.

Figure 12. Timing Diagram for SMBus Alert Response

I²C Interface

The SGM52410C communication interface is an I²C interface. The SGM52410C can only act as slave devices. An I²C timing diagram is shown in Figure 1.

I²C Address Selection

The SGM52410C has a separate address setting pin ADDR, which can be connected to GND, V_{DD}, SDA and SCL. Table 8 shows the four available addresses.

Table 8. ADDR Pin Connection and Corresponding Slave Address

ADDR Pin	Slave Address
GND	1001000
V_{DD}	1001001
SDA	1001010
SCL	1001011

I²C General Call

The SGM52410C supports I²C general call address (0000000) and the eighth bit must be '0'. The device acknowledges the general call address. And if the second byte is 00000110 (06h), the SGM52410C resets all registers and goes to power-down.

I²C Speed Modes

The I²C bus operation supports three speed modes: standard mode, fast mode, and high-speed mode. See Timing Characteristics section for more details.

To enter standard and fast mode, it needs no special operation.

To enter high-speed mode, send a special address byte of 00001XXX following the I²C start condition. The SGM52410C doesn't give an ACK (acknowledge) to this byte, the SGM52410C switches to high-speed mode after receiving this byte. The SGM52410C quits high-speed mode with the next STOP condition.

Slave Mode Operations

The SGM52410C works in slave mode and doesn't drive the SCL line.

REGISTER MAPS

Register Address

The SGM52410C has seven pointer registers. Table 9 and Table 10 show these register maps. Figure 4 shows how to access this pointer registers.

Table 9. Register Address

Address	Register
0x0	Conversion Register
0x1	Config Register
0x2	Low_Thresh Register
0x3	High_Thresh Register
0x4	Config1 Register
0x5	Chip_ID Register
0x6	GN_Trim1 Register for EXT_REF bit

Pointer Register

Table 10. Pointer Register Byte (Write-Only)

MSB LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	Register Address		

REG0x0: Conversion Register [Reset = 0x000000]

The ADC conversion result is 24-bit two's complement format. Table 11 shows the data format. Its reset default value is '0'.

Table 11. 24-Bit Conversion Register (Read-Only)

MSB LSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

REGISTER MAPS (continued)

REG0x1: Config Register [Reset = 0x8583]

The configuration register (Config Register) is shown in Table 12.

Table 12. Config Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	OS	1	R/W	Working Status/Single-Shot Conversion Start For a write status: 0 = No effect 1 = Start a single conversion (when in single-shot mode) For a read status: 0 = The chip is doing a conversion 1 = The chip is not doing a conversion This bit reports the status of the chip. It can only be written when the chip is in power-down.
D[14:12]	MUX[2:0]	000	R/W	Input Multiplexer (MUX) Configuration 000 = AIN_P = AIN0 and AIN_N = AIN1 (default) 001 = AIN_P = AIN0 and AIN_N = AIN3 010 = AIN_P = AIN1 and AIN_N = AIN3 011 = AIN_P = AIN2 and AIN_N = AIN3 100 = AIN_P = AIN0 and AIN_N = GND 101 = AIN_P = AIN1 and AIN_N = GND 110 = AIN_P = AIN2 and AIN_N = GND 111 = AIN_P = AIN3 and AIN_N = GND
D[11:9]	PGA[2:0]	010	R/W	Programmable Gain Amplifier (PGA) Configuration 000 = FSR = ±6.144V (1) 001 = FSR = ±4.096V (1) 010 = FSR = ±2.048V (default) 011 = FSR = ±1.024V 100 = FSR = ±0.512V 101 = FSR = ±0.256V 110 = FSR = ±0.256V 111 = FSR = ±0.256V
D[8]	MODE	1	R/W	Device Operating Mode 0 = Continuous conversion mode 1 = Power-down or single-shot mode (default)
D[7:5]	DR[2:0]	100	R/W	Data Rate These bits control the data rate setting. See Table 5.
D[4]	COMP_MODE	0	R/W	Comparator Mode 0 = A traditional comparator with hysteresis (default) 1 = A window comparator
D[3]	COMP_POL	0	R/W	Comparator Polarity 0 = Active low (default) 1 = Active high This bit sets the active polarity of the ALERT/RDY pin.
D[2]	COMP_LAT	0	R/W	Latching Comparator 0 = Non-latching comparator (default) 1 = Latching comparator This bit sets whether the ALERT/RDY pin latches once its outputs sets or resets when ADC conversion result is within the upper and lower threshold limitations.
D[1:0]	COMP_QUE[1:0]	11	R/W	Comparator Queue and Disable Function 00 = Assert after one conversion 01 = Assert after two conversions 10 = Assert after four conversions 11 = Disable comparator (default) These bits can disable the comparator. They can set the required times of successive ADC conversion beyond the threshold before an alert output on ALERT/RDY pin.

NOTE:

1. This is a theoretical full-scale range of the ADC scaling. The real input must be within the electrical limitation (0V to V_{DD} + 0.3V).

REGISTER MAPS (continued)

REG0x2 ~ REG0x3: Low_Thresh [Reset = 0x8000] and High_Thresh [Reset = 0x7FFF] Registers

The lower (Low_Thresh) and upper (High_Thresh) threshold registers are in 16-bit two's complement format, and aligned to conversion data D[23:8]. Table 13 shows these two register format.

Table 13. Low_Thresh and High_Thresh Registers Format (Read/Write)

Low_Thresh Register							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Low_Thresh[15:8]							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Low_Thresh[7:0]							
High_Thresh Register							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
High_Thresh[15:8]							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
High_Thresh[7:0]							

REG0x4: Config1 Register [Reset = 0x0000]

Table 14. 16-Bit Config1 Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:9]	Reserved	000 0000	R/W	
D[8]	PD	0	R/W	Writing '1' to PD powers down this part, and this PD bit is automatically cleared internally by any of the following continuous or single-shot conversion operations.
D[7]	DR_SEL	0	R/W	FIR Filter Configuration This specific bit is designated for the customization of filter coefficients dedicated to the internal finite impulse response (FIR) filter. Kindly employ these bits in conjunction with the 5SPS, 10SPS and 20SPS configuration. 0 = 50Hz rejection only (default) 1 = 60Hz rejection only
D[6:4]	Reserved	000	R/W	
D[3]	EXT_REF	0	R/W	0 = None (default) 1 = Use AIN3 as external reference for ADC
D[2:0]	Reserved	000	R/W	

REG0x5: Chip_ID Register [Reset = 0x0280]

Table 15. 16-Bit Chip_ID Register for Identifying Chip ID and Its Subversions (Read-Only)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:13]	Reserved	000	R	Reserved.
D[12:8]	ID[4:0]	0 0010	R	
D[7:5]	VER[2:0]	100	R	
D[4:0]	Reserved	0 0000	R	Reserved.

REGISTER MAPS (continued)

REG0x6: GN_Trim1 Register (When Using EXT_REF Bit) [Reset = 0x999A]

The ADC gain coefficient for user selecting Config1 register EXT_REF bit as reference. A default value is provided and the user is responsible for writing proper value to the register if they want to compensate external reference error. This register does not take effect when EXT_REF = 0 and the internal reference is selected.

Table 16. GN_Trim1 Register Format

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
GN15	GN14	GN13	GN12	GN11	GN10	GN9	GN8
1	0	0	1	1	0	0	1
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GN7	GN6	GN5	GN4	GN3	GN2	GN1	GN0
1	0	0	1	1	0	1	0

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

FEBRUARY 2025 – REV.A to REV.A.1 **Page**

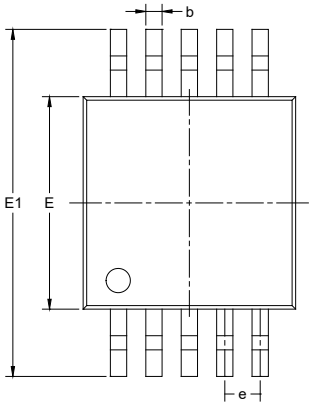
Updated Packing Option in Package/Ordering Information section 2
Updated Detailed Description section 13, 17, 18
Updated Register Maps section 21, 22

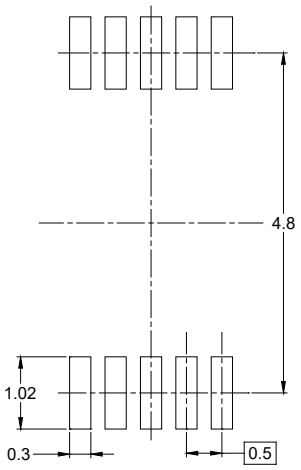
Changes from Original (DECEMBER 2024) to REV.A **Page**

Changed from product preview to production data ..... All

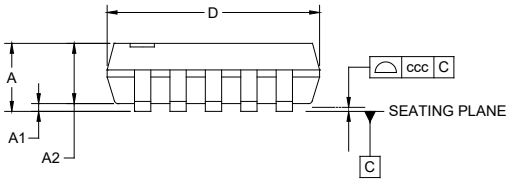
PACKAGE OUTLINE DIMENSIONS

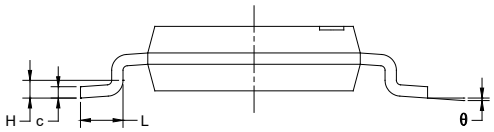
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)



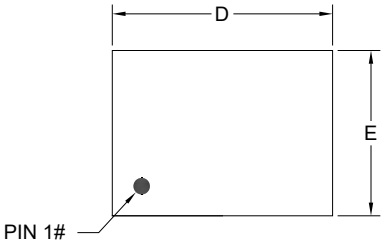


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.170	-	0.330
c	0.080	-	0.230
D	2.900	-	3.100
E	2.900	-	3.100
E1	4.750	-	5.050
e	0.500 BSC		
H	0.250 TYP		
L	0.400	-	0.800
θ	0°	-	8°
ccc	0.100		

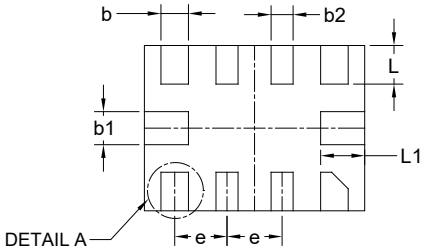
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

PACKAGE OUTLINE DIMENSIONS

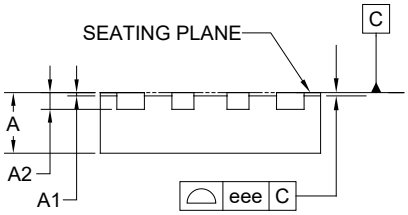
UTQFN-2×1.5-10L



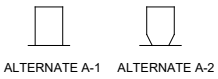
TOP VIEW



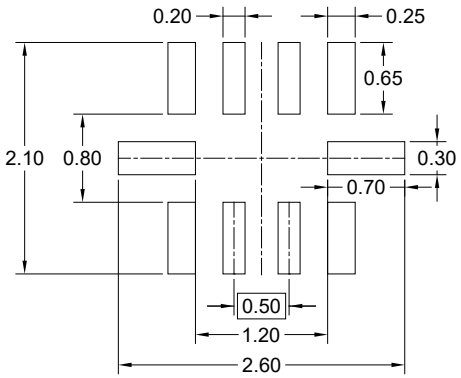
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



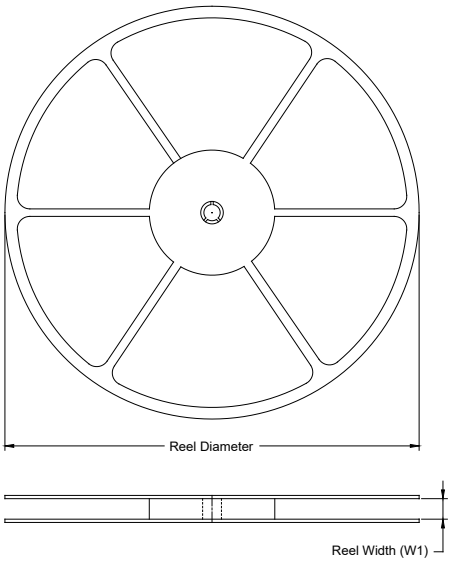
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.000	-	0.050
A2	0.152 REF		
b	0.200	0.250	0.300
b1	0.250	0.300	0.350
b2	0.150	0.200	0.250
D	1.900	2.000	2.100
E	1.400	1.500	1.600
L	0.250	0.350	0.450
L1	0.300	0.400	0.500
e	0.500 BSC		
eee	0.050		

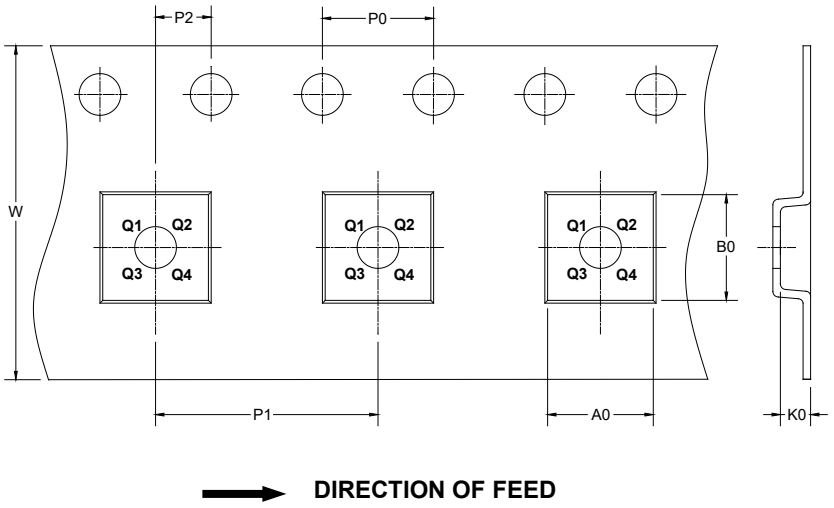
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



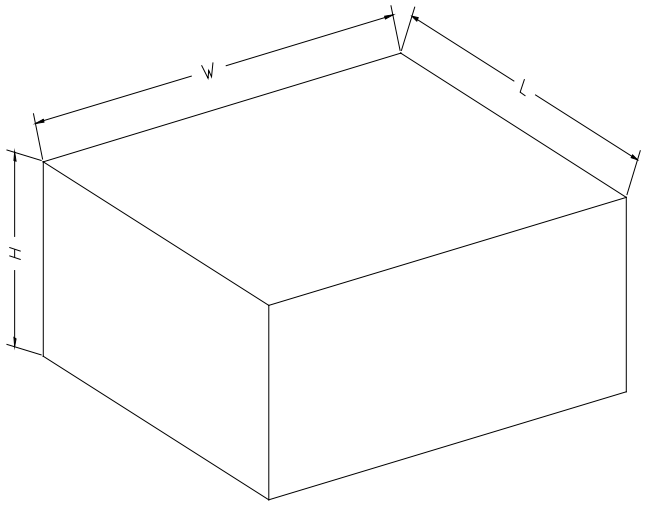
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
UTQFN-2×1.5-10L	7″	9.5	1.70	2.30	0.75	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002