SGM61021
2A High Efficiency Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61021 is a high efficiency synchronous Buck DC/DC converter with 2A output current capability and adjustable output voltage. The input supply voltage is in the range of 2.5V to 5.5V. Using adaptive off-time peak current control, the efficiency of this device reaches 95%.

This device operates with a quasi-fixed 2MHz pulse width modulation (PWM) mode for moderate or heavy loads. But at light loads, pulse skip modulation is used for power-save mode (PSM). The PSM operating quiescent current is very low, typically 48μA, which is well suitable for battery-powered applications to prolong battery life. Despite such low quiescent current, the transient response to large load variations is excellent. The device shutdown current is less than 0.8μA.

The SGM61021 provides an adjustable output voltage by an external resistor divider. The device is capable for low dropout operation with 100% duty cycle. Additional features include an internal soft-start function to limit inrush current, over-current and thermal shutdown protections, an enable input (EN), input under-voltage lockout (UVLO) protection and a power good (PG) output.

The SGM61021 is available in Green SOT-563-6 and UTDFN-1.6×1.6-6CL packages.

FEATURES

- **2.5V to 5.5V Input Voltage Range**
- **Adjustable Output Voltage from 0.6V to V_{IN}**
- **Up to 95% Efficiency**
- **Low R_{DSON} Switches (90mΩ/62mΩ)**
- **SGM61021A: Power-Save Mode**
- **SGM61021B: Forced PWM Mode**
- **SGM61021PA: Power-Save Mode and PG Pin**
- **SGM61021PB: Forced PWM Mode and PG Pin**
- **48μA (TYP) Operating Quiescent Current**
- **100% Duty Cycle for Low Dropout Operation**
- **2MHz PWM Switching Frequency**
- **Support 1.2V GPIO**
- **Active Output Discharge**
- **Over-Current Protection**
- **Thermal Shutdown Protection**
- **Input Under-Voltage Lockout (UVLO) Protection**
- **Available in Green SOT-563-6 and UTDFN-1.6×1.6-6CL Packages**

APPLICATIONS

Smart Phone
General Purpose POL Supply
Set-Top Box
Network Video Camera
Wireless Router
Hard Disk Driver

TYPICAL APPLICATION

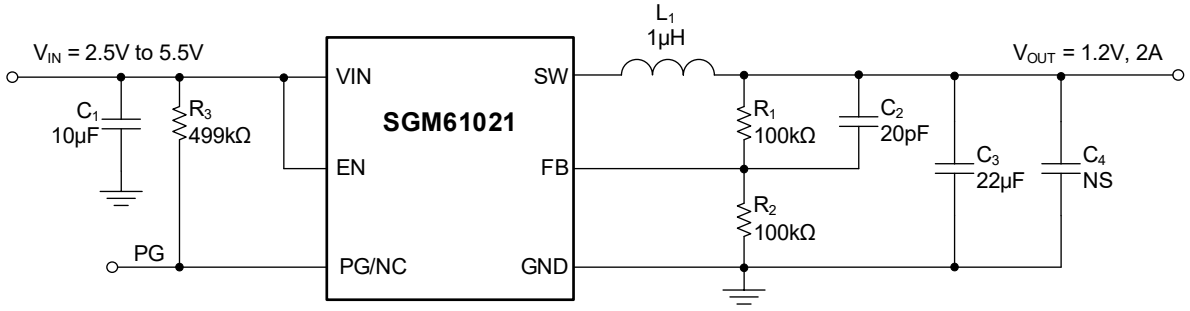


Figure 1. Typical Application Circuit

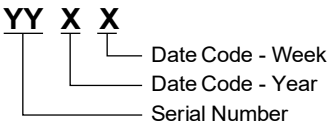
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61021A	SOT-563-6	-40℃ to +125℃	SGM61021AXKB6G/TR	0GXX	Tape and Reel, 5000
	UTDFN-1.6×1.6-6CL	-40℃ to +125℃	SGM61021AXUIE6G/TR	1LK XXX	Tape and Reel, 3000
SGM61021PA	SOT-563-6	-40℃ to +125℃	SGM61021PAXKB6G/TR	0EXX	Tape and Reel, 5000
	UTDFN-1.6×1.6-6CL	-40℃ to +125℃	SGM61021PAXUIE6G/TR	1LL XXX	Tape and Reel, 3000
SGM61021B	SOT-563-6	-40℃ to +125℃	SGM61021BXKB6G/TR	0FXX	Tape and Reel, 5000
SGM61021PB	SOT-563-6	-40℃ to +125℃	SGM61021PBXKB6G/TR	0DXX	Tape and Reel, 5000

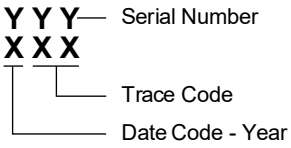
MARKING INFORMATION

NOTE: XX = Date Code. XXX = Date Code, and Trace Code.

SOT-563-6



UTDFN-1.6×1.6-6CL



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (1)
VIN, EN, PG ..... -0.3V to 6V
SW (DC) ..... -0.3V to V_{IN} + 0.3V
SW (AC, Less than 10ns) (2) ..... -2V to 9V
FB ..... -0.3V to 5.5V
Package Thermal Resistance
SOT-563-6, θ_{JA} ..... 124℃/W
SOT-563-6, θ_{JB} ..... 27.3℃/W
SOT-563-6, θ_{JC} ..... 71.8℃/W
UTDFN-1.6×1.6-6CL, θ_{JA} ..... 122.5℃/W
UTDFN-1.6×1.6-6CL, θ_{JB} ..... 19.9℃/W
UTDFN-1.6×1.6-6CL, θ_{JC} ..... 89.1℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (3) (4)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:
1. All voltage values are with respect to the ground terminal.
2. While switching.
3. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
4. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 2.5V to 5.5V
Output Voltage Range, V_{OUT} ..... 0.6V to V_{IN}
Output Current Range, I_{OUT} ..... 0 to 2A
Sink Current at PG Pin, I_{SINK_PG} ..... < 1mA
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

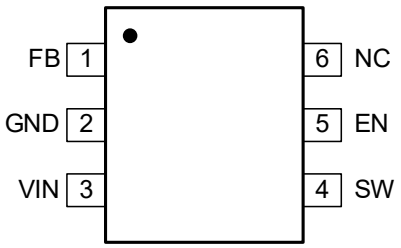
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

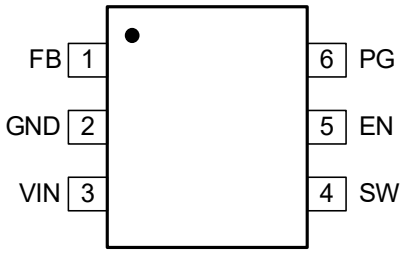
PIN CONFIGURATIONS

SGM61021A/B (TOP VIEW)



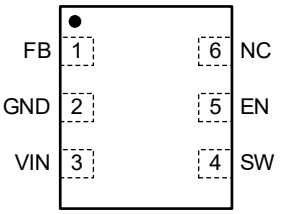
SOT-563-6

SGM61021PA/PB (TOP VIEW)



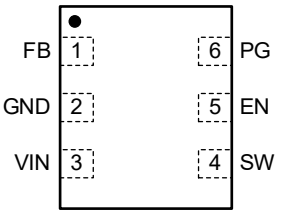
SOT-563-6

SGM61021A (TOP VIEW)



UTDFN-1.6×1.6-6CL

SGM61021PA (TOP VIEW)



UTDFN-1.6×1.6-6CL

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
SGM61021A/B	SGM61021PA/PB			
1	1	FB	I	Feedback Pin for Internal Control Loop. Connect this pin to an external feedback divider.
2	2	GND	G	Ground Pin.
3	3	VIN	P	Power Supply Voltage Input.
4	4	SW	P	Switching Node Output of the Converter. Connect the inductor of the output filter to this pin.
5	5	EN	I	Active High Enable Input. Apply a logic low to shut down the device or pull EN up to VIN to enable it. Do not leave EN floating.
6	—	NC	—	No Connection.
—	6	PG	O	Open-Drain Power Good Output. Pull it up with a resistor to a positive voltage no more than 5.5V. It can be left floating if unused. For the version without power good function, it is disconnection internally.

NOTE: I = input, O = output, P = power, G = ground.

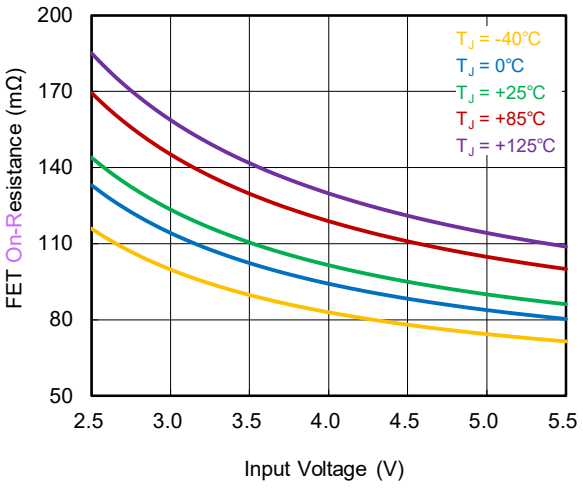
ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_J = -40℃ to +125℃, typical values are at V_{IN} = 5.0V and T_J = +25℃, unless otherwise noted.)

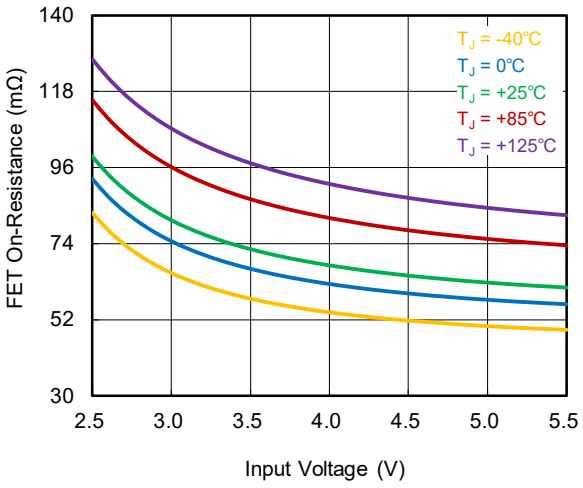
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
Quiescent Current into VIN Pin	I_Q	No switching	SGM61021A/PA		48	82	μA
			SGM61021B/PB		580	750	
Shutdown Current into VIN Pin	I_{SD}	EN = 0V	T_J = +25℃		0.24	0.8	μA
			T_J = -40℃ to +125℃			2.5	
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling		2.14	2.23	2.32	V
Under-Voltage Lockout Hysteresis	V_{HYS}				160		mV
Thermal Shutdown	T_{JSD}	Junction temperature rising			158		℃
		Junction temperature falling			138		
Logic Interface							
High-Level Threshold at EN Pin	V_{IH}			0.7			V
Low-Level Threshold at EN Pin	V_{IL}					0.4	V
Soft Startup Time	t_{SS}	Measure from 10% to 95% × V_{OUT} (set)			970		μs
Output							
Feedback Regulation Voltage	V_{FB}	T_J = +25℃		0.594	0.6	0.606	V
		T_J = -40℃ to +125℃		0.591	0.6	0.609	
High-side FET On-Resistance	R_{DSON}	V_{IN} = 5V, I_{SW} = 500mA			90	135	mΩ
Low-side FET On-Resistance					62	100	mΩ
High-side FET Current Limit	I_{LIM_HS}			2.5	3.7	4.9	A
Switching Frequency	f_{SW}	V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 1A		1.5	2	2.5	MHz
Output Discharge Resistor	R_{DIS}	EN = low, V_{OUT} = 1.8V			52	150	Ω
Low-side FET Sink Current Limit		V_{IN} = 5V, SGM61021B/PB		0.7	1.4	2.1	A
Power Good (SGM61021PA/PB)							
Power Good Threshold	V_{PG}	V_{FB} rising, referenced to V_{FB} nominal			95% × V_{REF}		V
		V_{FB} falling, referenced to V_{FB} nominal			90% × V_{REF}		
Power Good Low-Level Output Voltage	V_{PG_OL}	I_{SINK} = 1mA			0.12	0.3	V
Input Leakage Current into PG Pin	I_{PG_LKG}	V_{PG} = 5.0V			0.01	0.8	μA
Power Good Delay Time	t_{PG_DLY}	V_{FB} falling			46		μs

TYPICAL PERFORMANCE CHARACTERISTICS

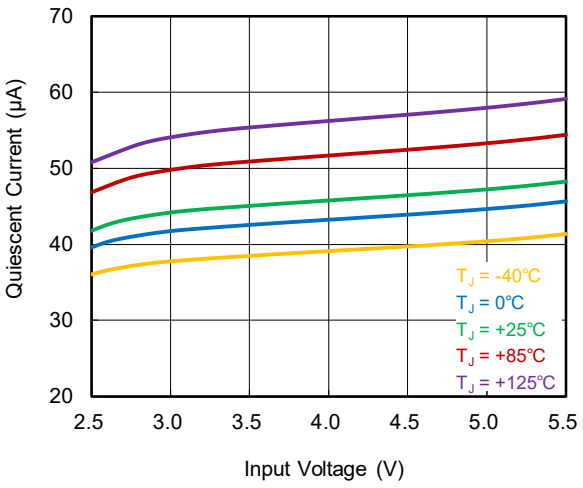
FET On-Resistance vs. Input Voltage (High)



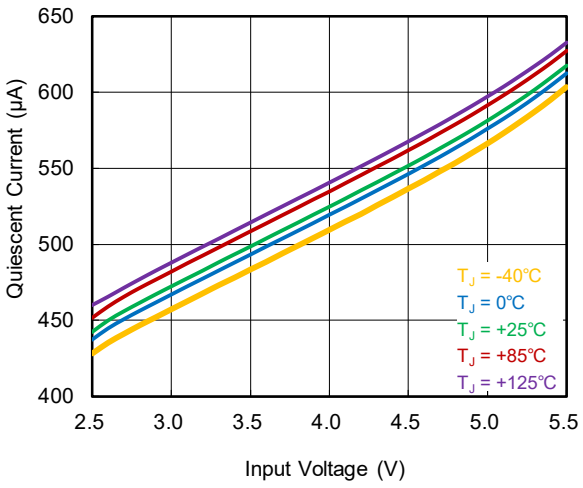
FET On-Resistance vs. Input Voltage (Low)



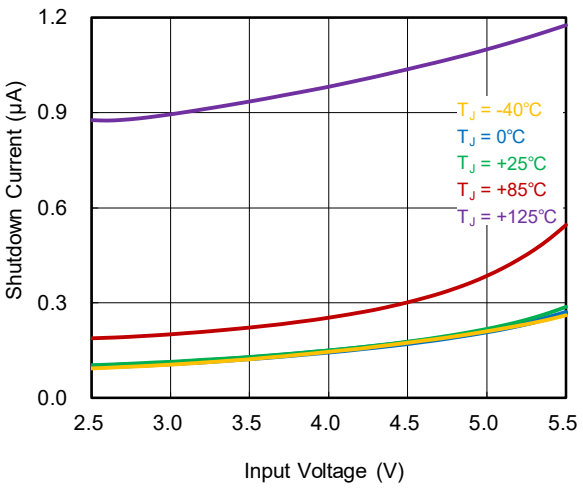
Quiescent Current vs. Input Voltage (SGM61021A/PA)



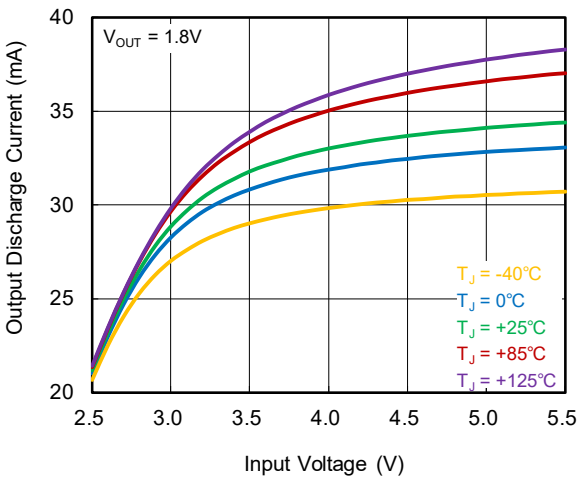
Quiescent Current vs. Input Voltage (SGM61021B/PB)



Shutdown Current vs. Input Voltage



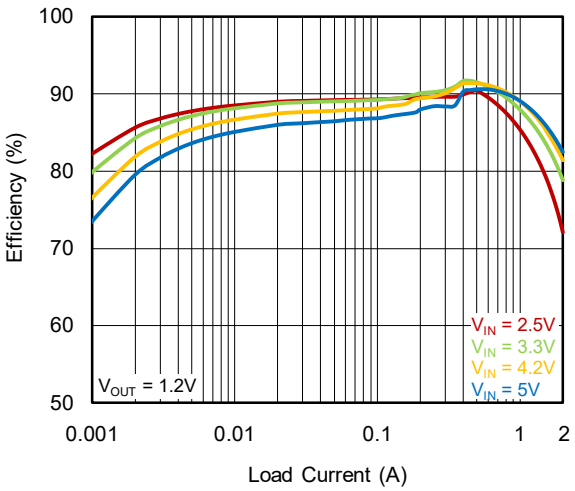
Output Discharge Current vs. Input Voltage



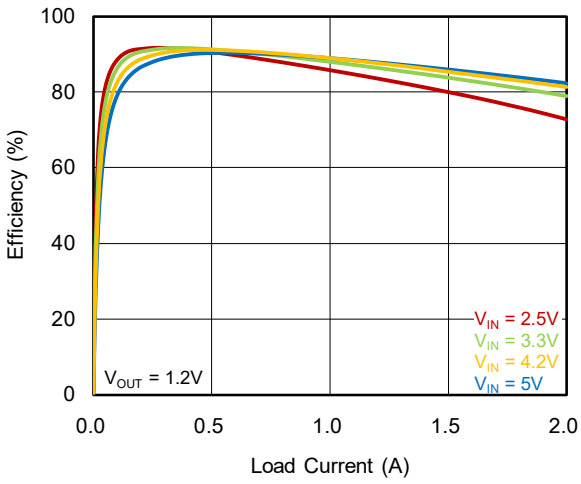
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.2V, L_1 = 1μH (DCR = 13mΩ), and C_{OUT} = 22μF, unless otherwise noted.

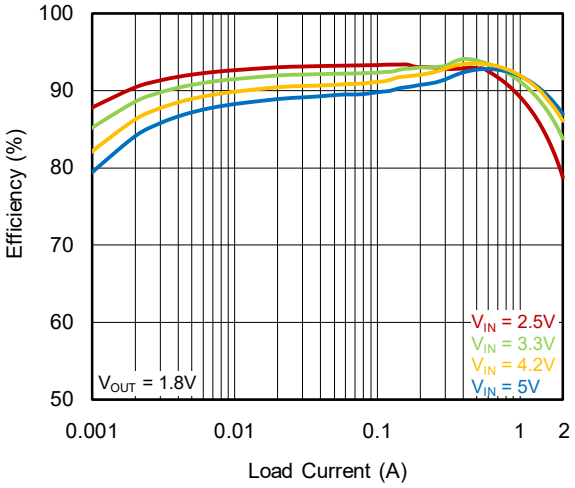
Efficiency vs. Load Current (SGM61021A/PA)



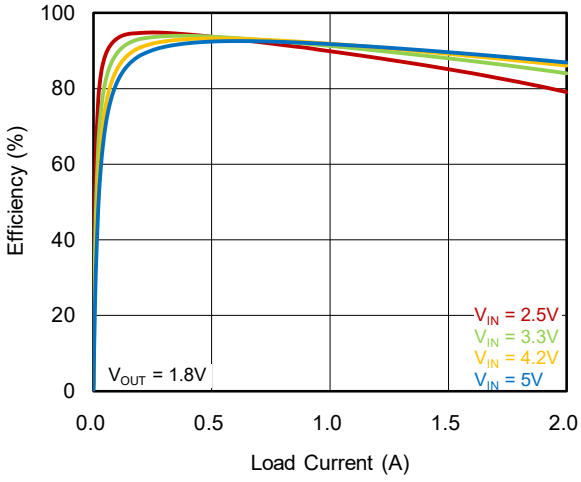
Efficiency vs. Load Current (SGM61021B/PB)



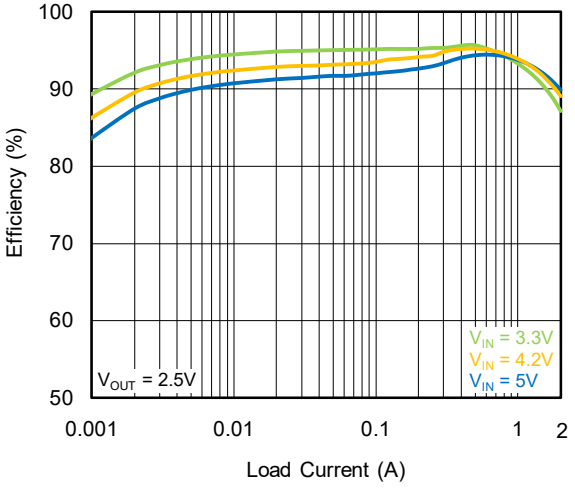
Efficiency vs. Load Current (SGM61021A/PA)



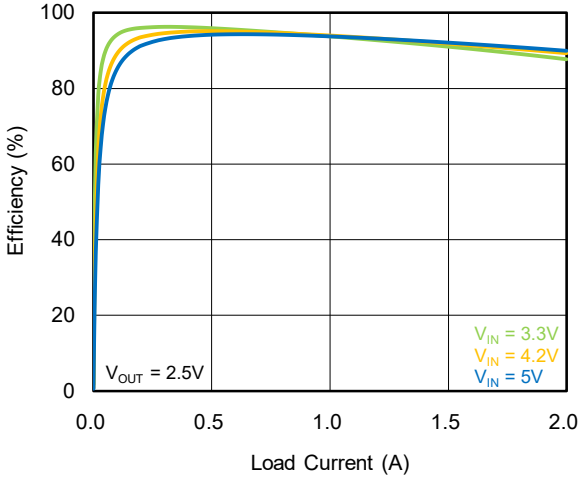
Efficiency vs. Load Current (SGM61021B/PB)



Efficiency vs. Load Current (SGM61021A/PA)



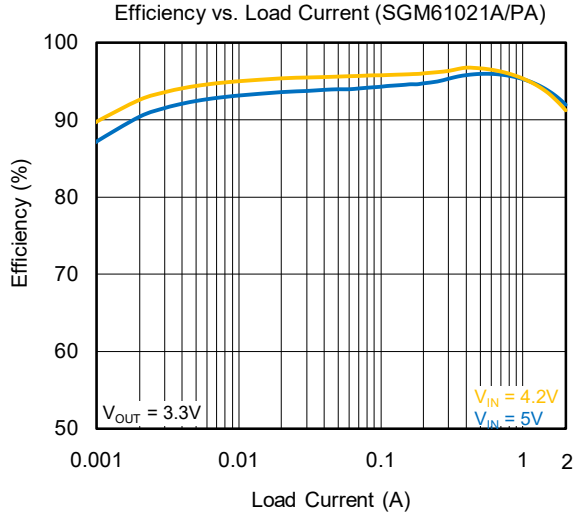
Efficiency vs. Load Current (SGM61021B/PB)



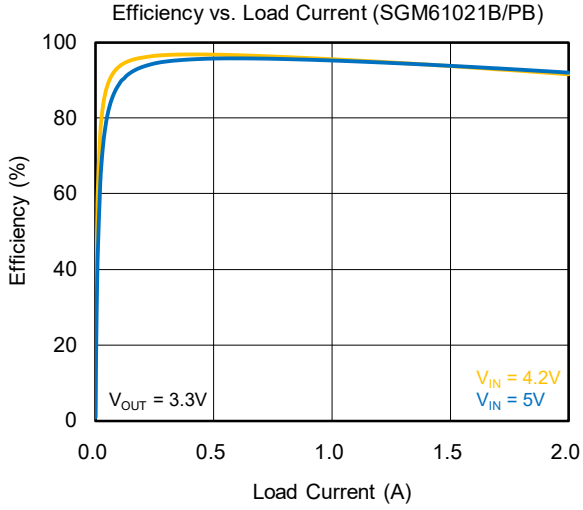
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.2V, L_1 = 1μH (DCR = 13mΩ), and C_{OUT} = 22μF, unless otherwise noted.

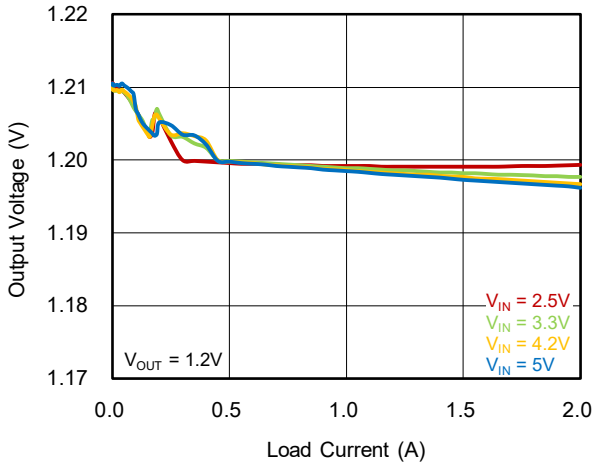
Efficiency vs. Load Current (SGM61021A/PA)



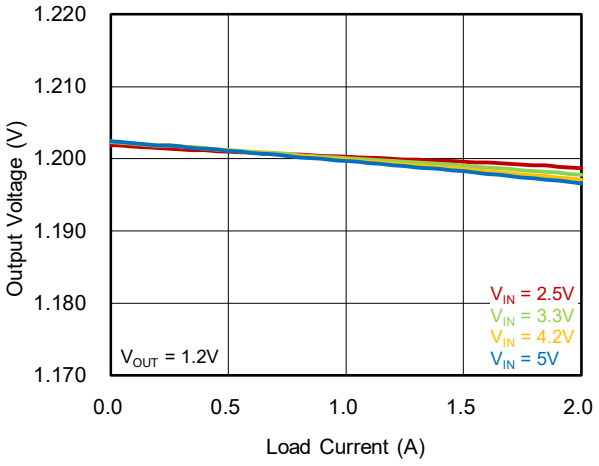
Efficiency vs. Load Current (SGM61021B/PB)



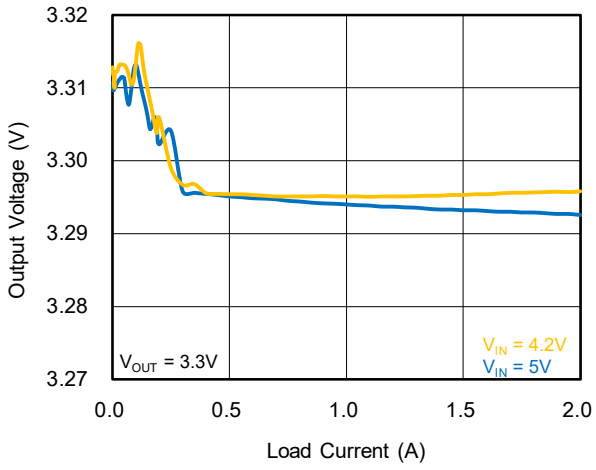
Load Regulation (SGM61021A/PA)



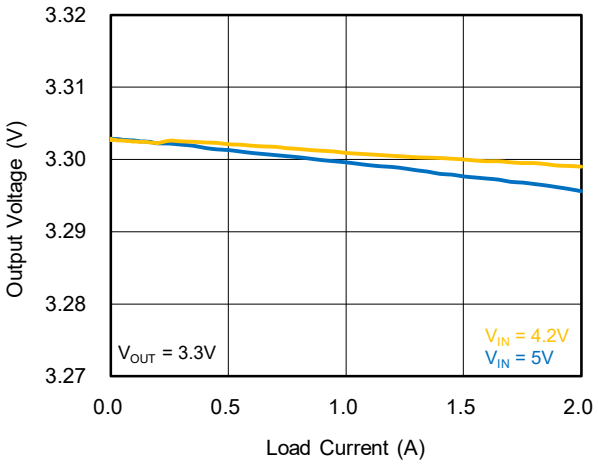
Load Regulation (SGM61021B/PB)



Load Regulation (SGM61021A/PA)



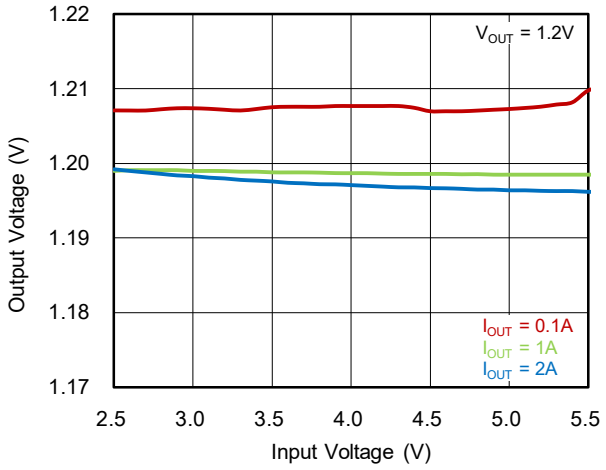
Load Regulation (SGM61021B/PB)



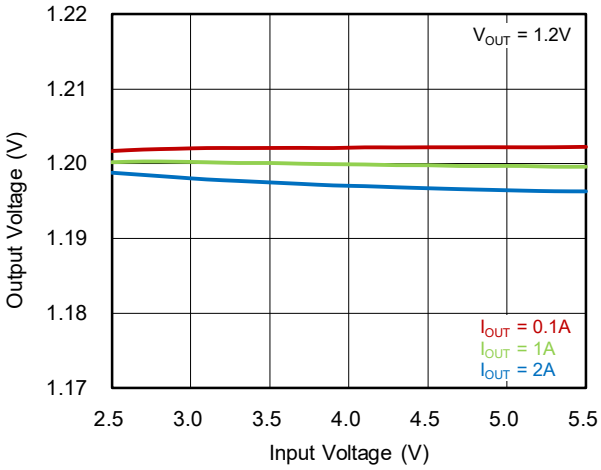
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.2V, L_1 = 1μH (DCR = 13mΩ), and C_{OUT} = 22μF, unless otherwise noted.

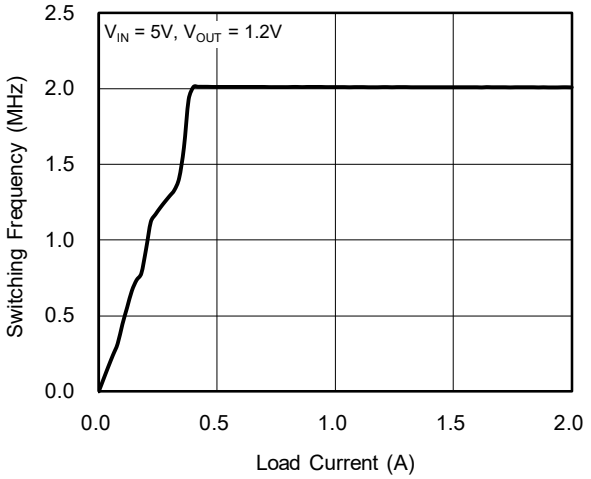
Line Regulation (SGM61021A/PA)



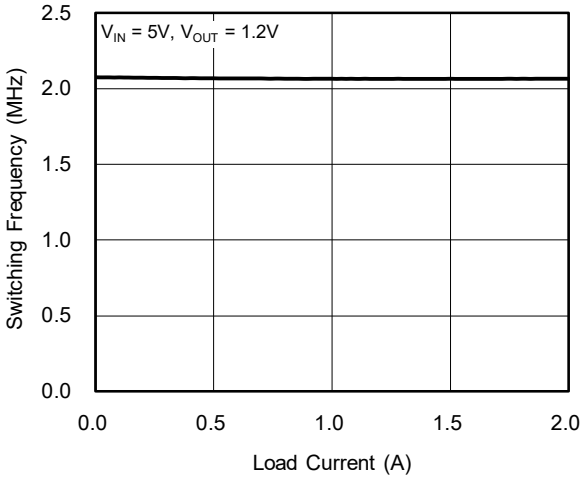
Line Regulation (SGM61021B/PB)



Switching Frequency vs. Load Current (SGM61021A/PA)



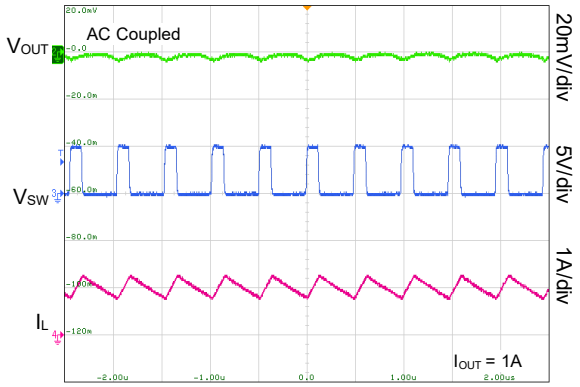
Switching Frequency vs. Load Current (SGM61021B/PB)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

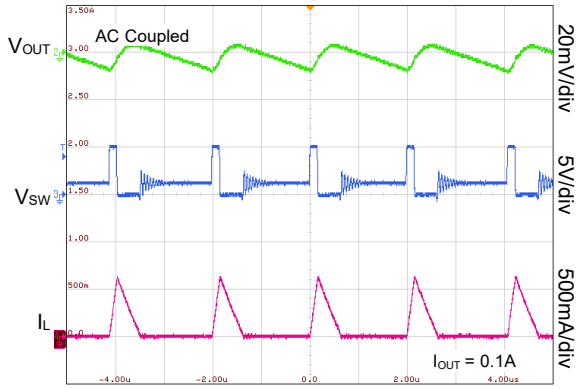
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.2V, L_1 = 1μH (DCR = 13mΩ), and C_{OUT} = 22μF, unless otherwise noted.

PWM Operation (SGM61021A/PA)



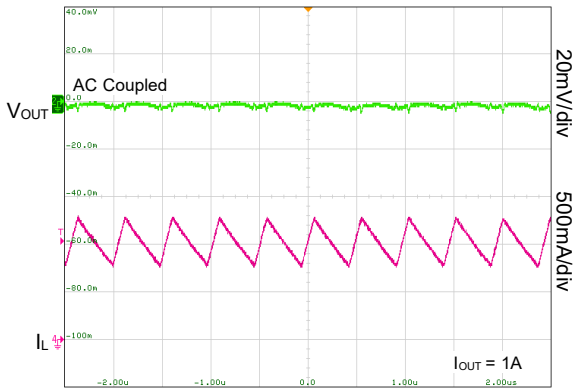
Time (500ns/div)

Power-Save Mode Operation (SGM61021A/PA)



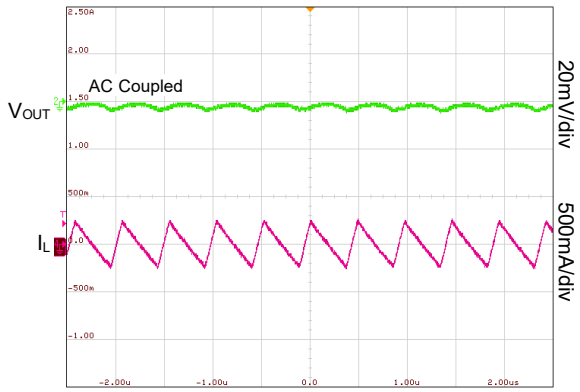
Time (1μs/div)

PWM Operation at FPWM (SGM61021B/PB)



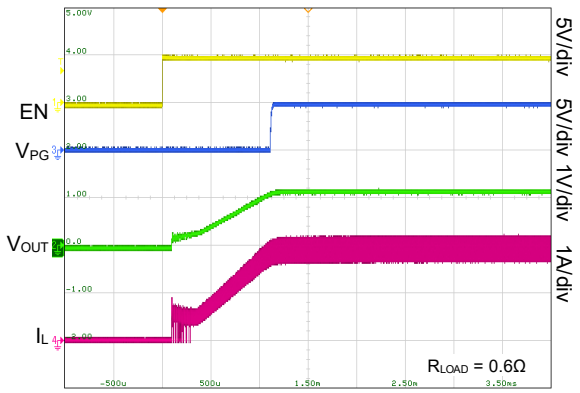
Time (500ns/div)

PWM Operation at FPWM without Load (SGM61021B/PB)



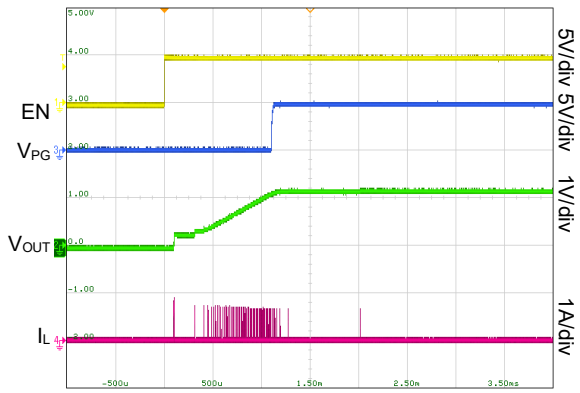
Time (500ns/div)

Startup with Load (SGM61021PA)



Time (500μs/div)

Startup without Load (SGM61021PA)

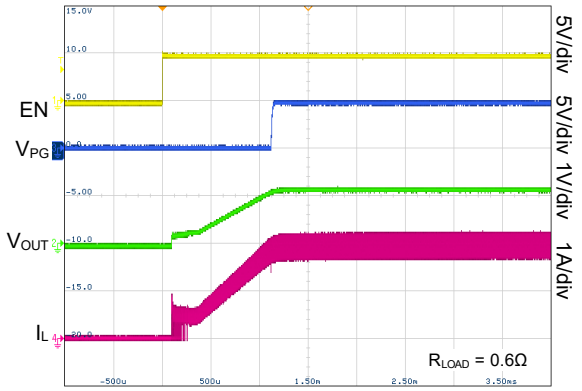


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

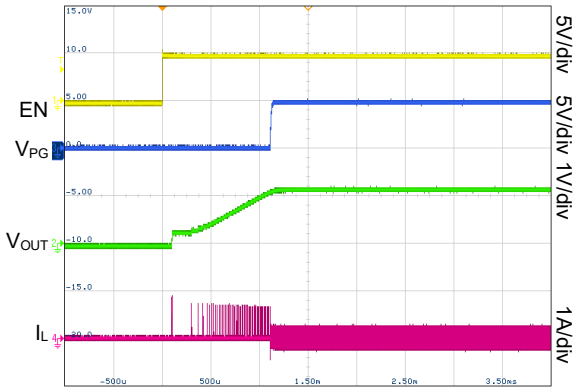
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.2V, L_1 = 1μH (DCR = 13mΩ), and C_{OUT} = 22μF, unless otherwise noted.

Startup with Load (SGM61021PB)



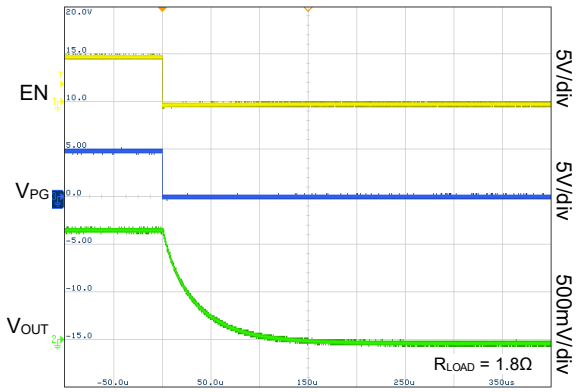
Time (500μs/div)

Startup without Load (SGM61021PB)



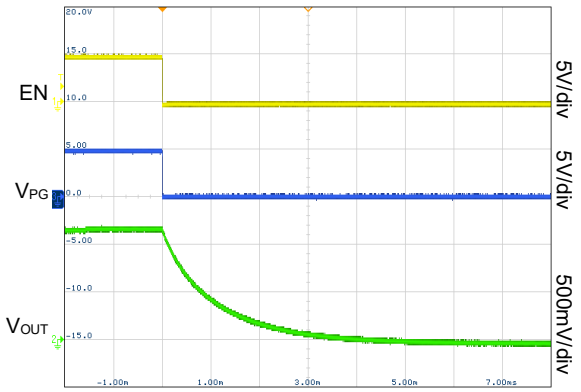
Time (500μs/div)

Disable, Active Output Discharge with Load (SGM61021PA/PB)



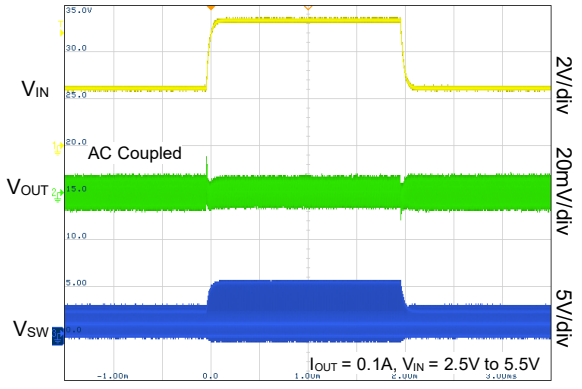
Time (50μs/div)

Disable, Active Output Discharge without Load (SGM61021PA/PB)



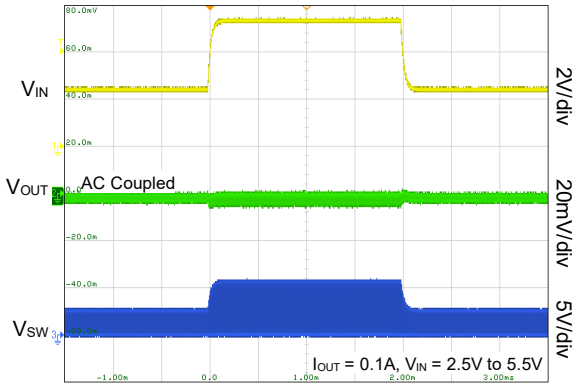
Time (1ms/div)

Line Transient (SGM61021A/PA)



Time (500μs/div)

Line Transient (SGM61021B/PB)

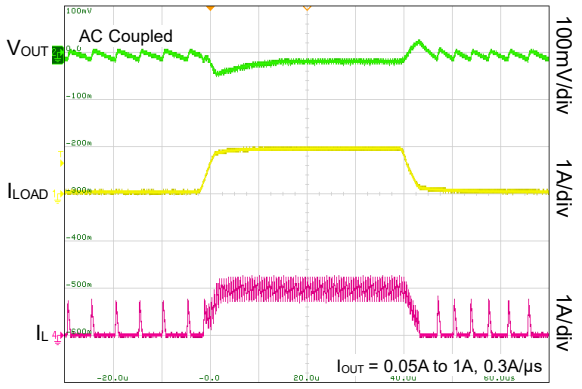


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

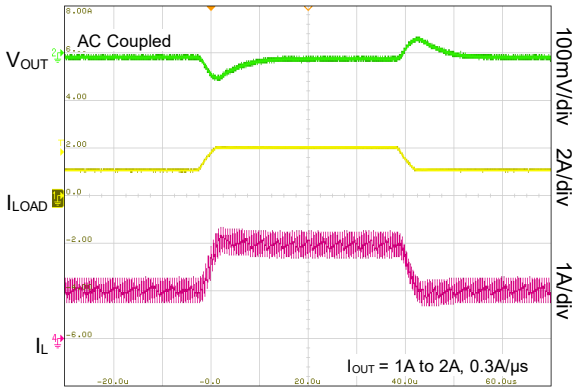
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.2V, L_1 = 1μH (DCR = 13mΩ), and C_{OUT} = 22μF, unless otherwise noted.

Load Transient (SGM61021A/PA)



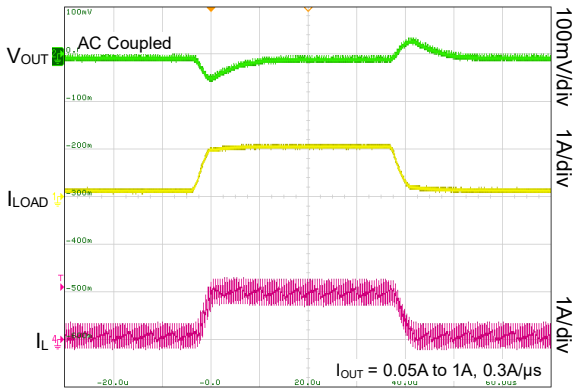
Time (10μs/div)

Load Transient (SGM61021A/PA)



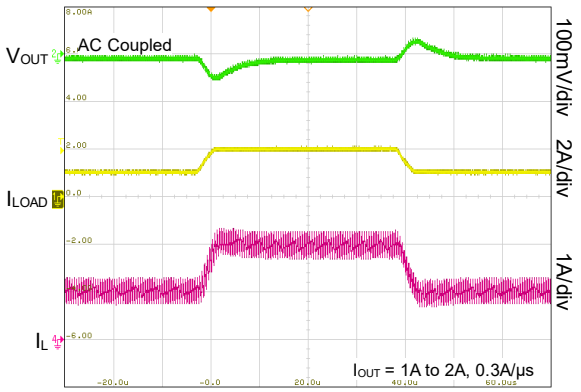
Time (10μs/div)

Load Transient (SGM61021B/PB)



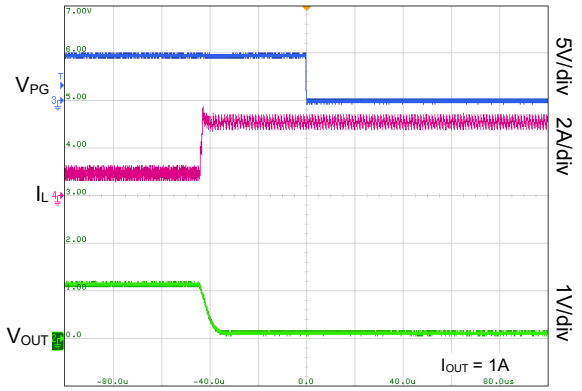
Time (10μs/div)

Load Transient (SGM61021B/PB)



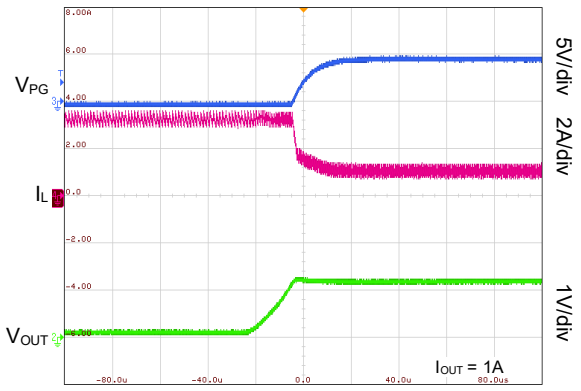
Time (10μs/div)

Short-Circuit Protection (SGM61021PA)



Time (20μs/div)

Short-Circuit Recovery (SGM61021PA)



Time (20μs/div)

FUNCTIONAL BLOCK DIAGRAM

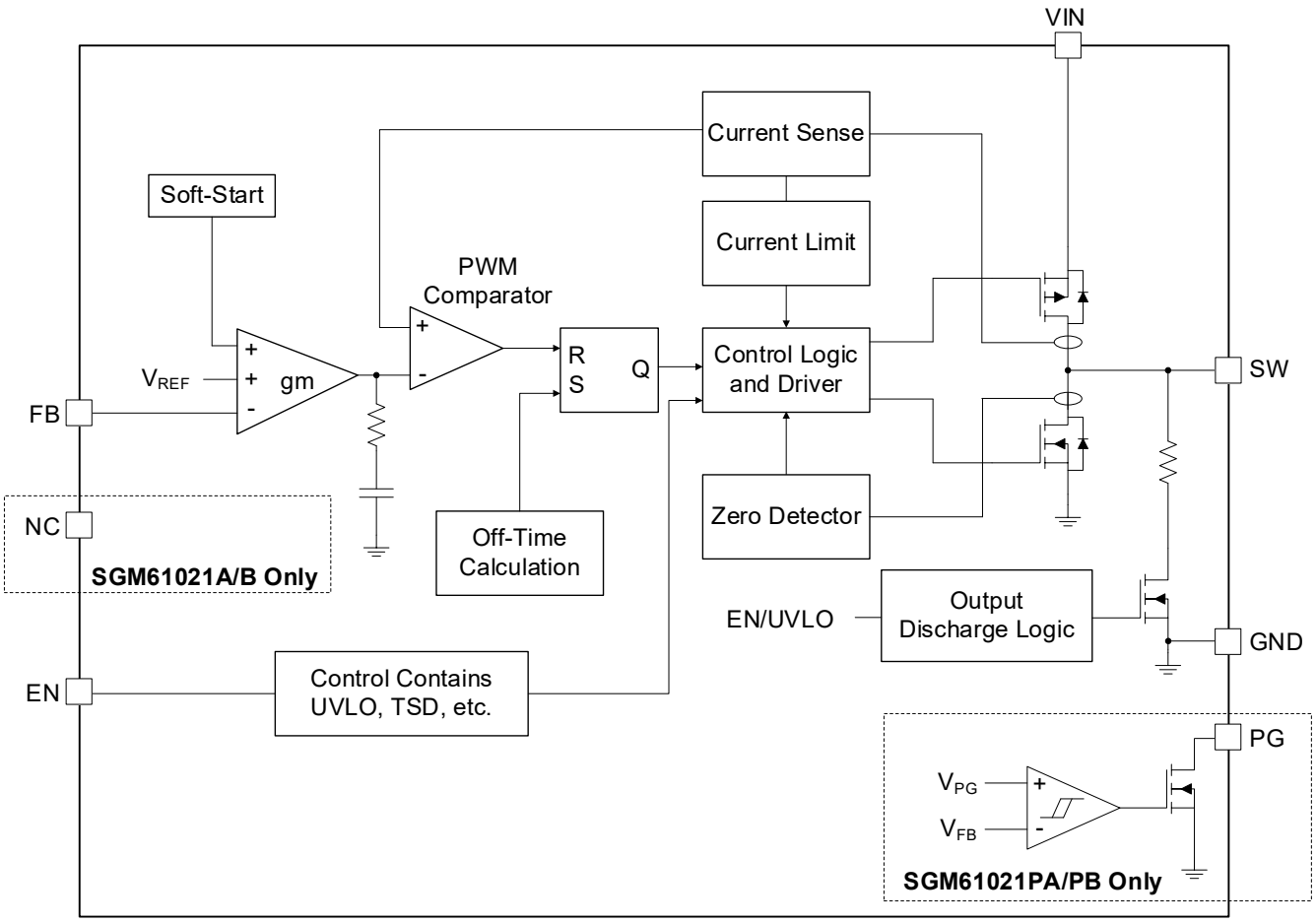


Figure 2. SGM61021 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61021 is a high efficiency Buck switching regulator specifically optimized for handheld battery-powered applications. Utilizing the adaptive off-time peak current control strategy, it operates at a quasi-fixed 2MHz switching frequency for moderate to heavy load conditions. This enables the use of compact inductors and capacitors for space-constrained designs.

At light load condition, this device enters power-save mode (PSM), reducing switching frequency and losses to extend battery life. The PSM quiescent current is typically 48μA while the shutdown current is as low as 0.8μA (MAX).

Under-Voltage Lockout (UVLO)

Operating with insufficient supply voltage can cause device malfunction or failure. The UVLO protection shuts down the device if the input voltage is below the V_{UVLO} threshold. The V_{UVLO} hysteresis is 160mV. When the input voltage exceeds the rising UVLO threshold, the device restarts with a fresh soft startup sequence.

Device Enable and the Output Discharge FET

When the input voltage is valid, pulling the EN input to logic high to enable the device and pulling it low to shut it down. In the shutdown mode, the switches and all control circuits are turned off to reduce the device current to 0.8μA (MAX). During shutdown, an internal FET (52Ω typical on-resistance) is turned on and connects the SW pin to the GND for smooth discharge of the output. This discharge function is also activated when the shutdown is caused by UVLO (V_{IN} < 1.4V, uncertain).

Power Good (SGM61021PA/PB)

The SGM61021 has a power good output (PG). The PG pin is an open-drain output. It should be pulled up with a pull-up resistor (e.g. 499kΩ) to a logic high rail which is no more than 5.5V unless it is not used. It is recommended that the sink current should not exceed 1mA. The PG pin is pulled to high-level immediately once FB voltage reaches 95% of the reference voltage, and is pulled to low-level once FB voltage falls below typically 90% of the reference voltage with a 46μs delay. Table 1 shows how the PG state is changed in different conditions. V_{PG} is the threshold of the PG hysteretic comparator. It has a 5% hysteresis band and goes high when V_{FB} rises above 95% of the V_{REF}.

The PG output is useful for power supply sequencing as well. Usually, the multiple power rails of a system need to be powered in a specific sequence for proper startup. The PG output of the leading power supply is connected to the EN input of the subsequent power supply to implement such sequencing.

Table 1. PG Output State in Different Conditions

Device Conditions		Logic Status	
		Hi-Z	Low
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$1.4V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} \leq 1.4V$	Uncertain	

Soft-Start and Pre-biased Output

A 970μs internal soft-start circuit is included to prevent input inrush current and voltage drops during startup. This circuit slowly ramps up the error amplifier reference voltage (V_{REF} = 0.6V) after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The SGM61021 is also capable of starting with a pre-biased output capacitor when it is powering up or enabled. When the device is turning on, a bias on the output may exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output may not drop during the off-period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device may not be able to start up properly. The output ramp is automatically initiated with the bias voltage and ramps up to the nominal output value.

DETAILED DESCRIPTION (continued)

Power-Save Mode (PSM)

At light load condition, the SGM61021A/PA shift to the PSM mode and operate with pulse skip modulation to reduce the switching frequency and minimize the losses. It also shuts down most of the internal circuits in PSM. In this mode, one or more PWM pulses are sent to charge the output capacitor and then the switches are kept off. The output capacitor voltage gradually drops due to small load current and when it falls below the nominal voltage threshold, the PWM pulses resume. If the load is still low, the output will go slightly higher than normal again and the switches will be turned off. In power-save mode, the output voltage is slightly higher than nominal output voltage. This effect can be mitigated by a larger output capacitor.

Pulse Width Modulation (PWM)

As the load increases, SGM61021A/PA will exit PSM and enter PWM.

The SGM61021B/PB operates in PWM across the all load range. For light load, the inductor current can be negative when the low-side switch is on. However, if the current reaches the low-side sinking current limit (1.4A), the low-side switch will be forced off.

Low Dropout Operation (100% Duty Cycle)

When the input voltage gradually drops to the regulation output voltage, the SGM61021 can operate at 100% duty cycle and keep the high-side MOSFET continuously on for minimal input-to-output voltage difference. The low-side MOSFET is kept off. In this mode, the lowest input voltage for keeping the output regulated is determined by load current and the resistive drops from the input to the output as given in Equation 1:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \quad (1)$$

where:

V_{IN_MIN} is minimum input voltage to maintain output voltage in regulation.

I_{OUT_MAX} is maximum output current.

R_{DSON} is high-side MOSFET on-resistance.

R_L is inductor DC resistance (DCR).

Switch Current Limits and Short-Circuit Protection

The SGM61021 implements current limitation by sensing the current of the high-side switch. At the beginning of each cycle, the high-side switch is turned on. If the converter is overloaded or a short occurs on the output, the inductor current sensed by the high-side switch exceeds the maximum current limit threshold. Under this condition, the high-side switch is turned off to avoid damage. The shortened on-time will result in reduced output voltage.

Note that the measured peak current limit in the closed-loop and open-loop (I_{LIM_HS}) test conditions is slightly different, mainly due to the current comparator propagation delay.

Thermal Shutdown Protection

A thermal shutdown function is implemented to prevent damage caused by excessive heat and power dissipation. Once the junction temperature exceeds +158℃, the device is shut down. The device is released from shutdown automatically when the junction temperature decreases by 20℃.

APPLICATION INFORMATION

In this section, power supply design with the SGM61021 synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

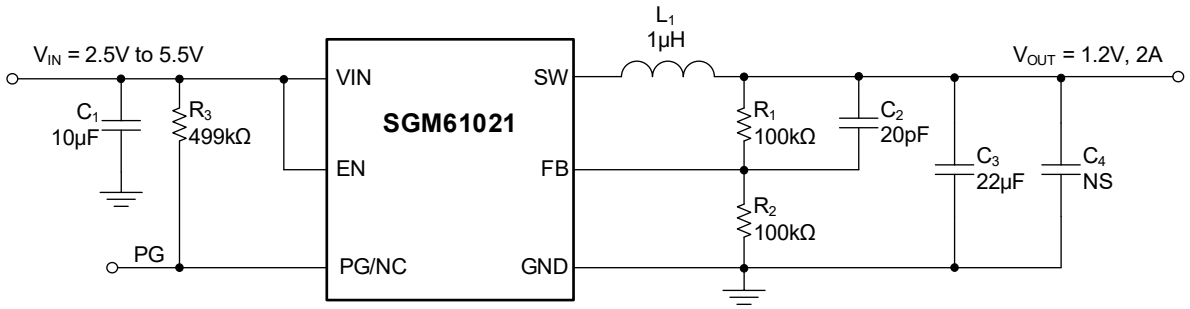


Figure 3. SGM61021 Application Example with 1.2V/2A Output

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 3. The selected components are given in Table 3.

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	2.5V to 5.5V
Output Voltage	1.2V
Output Current	≤ 2A

Table 3. Selected Components for the Design Example

Ref	Description	Manufacturer
C_1	10μF, 10V, X7R, 0603, P/N: GRM188Z71A106KA73	Murata
C_2	20pF, 50V, C0G, 0603	Murata
C_3	22μF, 10V, X5R, 0603, P/N: GRM188R61A226ME15	Murata
L_1	1μH Wire Wound, DCR_{MAX} = 18mΩ, $I_{SAT(30\%)}$ = 5.26A, $I_{RMS(40℃)}$ = 4.15A, SRF = 70MHz, 4mm × 4mm × 3mm, P/N: SWPA4030S1R0MT	Sunlord
R_1	100kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R_2	100kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R_3	499kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard

Input Capacitor Selection

High frequency decoupling input capacitors with low ESR are needed to circulate and absorb the high frequency switching currents of the converter. Place this capacitor right beside the VIN and GND pins. A 10μF ceramic capacitor with X5R or better dielectric and 0805 or smaller size is sufficient in most cases. A larger value can be selected to reduce the input current ripple.

Inductor Selection

The inductor current ripple is determined by the inductance value (L_1). A lower inductance results in higher peak-to-peak current that increases the converter conduction losses. On the other hand, a large inductance results in slower transient response and larger size. I_{SAT} should be higher than I_{L_MAX}, and sufficient margin should be reserved. Generally, the saturation current above high-side current limit is enough. Typically, the peak-to-peak inductor current is selected between 20% and 40% of the maximum output current. Equation 2 can be used to choose the inductance value based on ΔI_L.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$
$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (2)$$

where:

I_{OUT_MAX} is the maximum output DC current.

ΔI_L is the inductor current ripple (peak-to-peak).

f_{SW} is switching frequency (MHz).

L is the inductance value (μH).

APPLICATION INFORMATION (continued)

Output Voltage Adjustment

Use Equation 3 for selecting the feedback resistors (R_1 and R_2) in Figure 3 to set the desired output voltage (V_{OUT}):

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

First choose R_2 value below 100kΩ to avoid high noise sensitivity on the FB pin. Do not choose a very small value for R_2 otherwise the loss will be increased on this resistor that reduces the light load efficiency.

LC Filter

The inductor (L) and the output capacitor (C) form a low-pass filter for removing switching AC components and passing the DC voltage to the output. Note that variations as high as +20% to -30% in the effective inductance due to tolerances. Similarly, for the C_{OUT}, due to tolerances and bias voltage de-rating the effective capacitance can vary by +20% to -50%. For lower ripple at small output voltages (≤ 1.2V), a larger output capacitance is needed (at least 22μF).

A feed-forward capacitor improves transient response to the load steps and reduces the output ripple in PSM. A 20pF capacitor is recommended for the 1.2V output in the typical application.

Thermal Considerations

Especial care must be taken for power dissipation and thermal relief in high power density designs. The SGM61021 is a low-profile and fine-pitch surface-mount package that is typically used in a small area or volume. Thermal coupling, airflow and heat sinking must be considered in the system level and the space between heat generating elements must be managed properly.

To enhance the thermal performance, the PCB itself has a significant role and to help transfer the heat away by using large copper traces/planes that are connected to the device pins (and thermal pads if present). Considering a proper airflow in the system can complete the thermal relief for reliable operation of the power supply.

Layout Guidelines

A critical component of a high frequency switching power supply is the PCB layout. A good layout can improve the overall performance of the system and a poor layout can result in stability issues and EMI problems. The following guidelines are provided for designing a power supply layout with the SGM61021.

• Place the input/output capacitors and the inductor as close as possible to the IC pins and keep the power traces short. Use direct and wide traces for routing power paths to assure low trace parasitic resistance and inductance.

• Connect the ground returns of the input and output capacitors close to the GND pin and at the same point to avoid a ground potential shift and to minimize high frequency current path.

• Keep the output voltage sense trace and FB pin connections away from the high frequency and noisy conductors such as power traces and SW node to avoid magnetic and electric noise coupling.

Layout Example

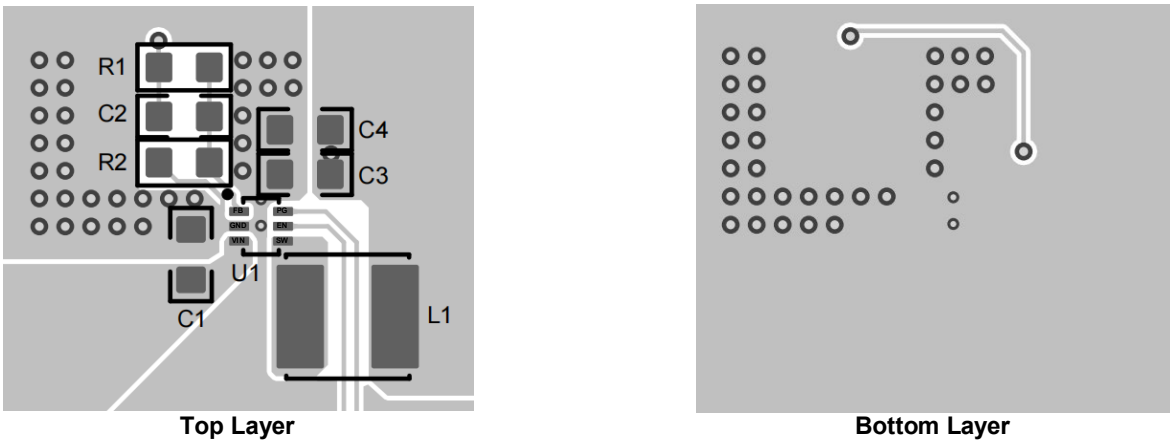


Figure 4. SOT-563-6 PCB Layout

ADDITIONAL TYPICAL APPLICATION CIRCUITS

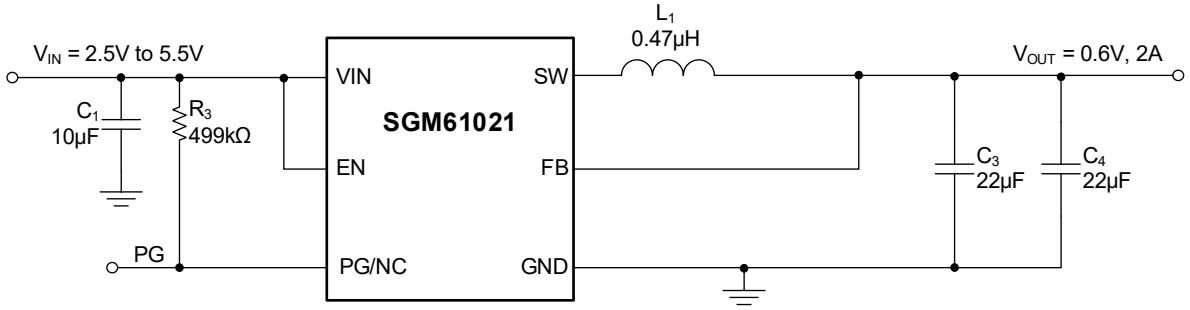


Figure 5. 0.6V Output Voltage Application

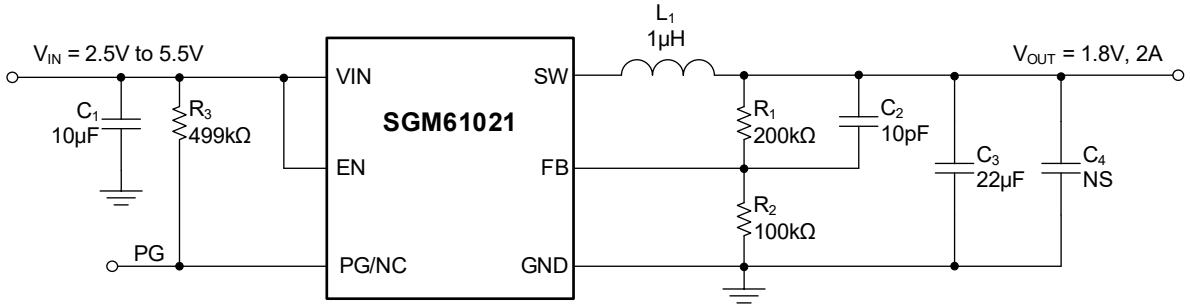


Figure 6. 1.8V Output Voltage Application

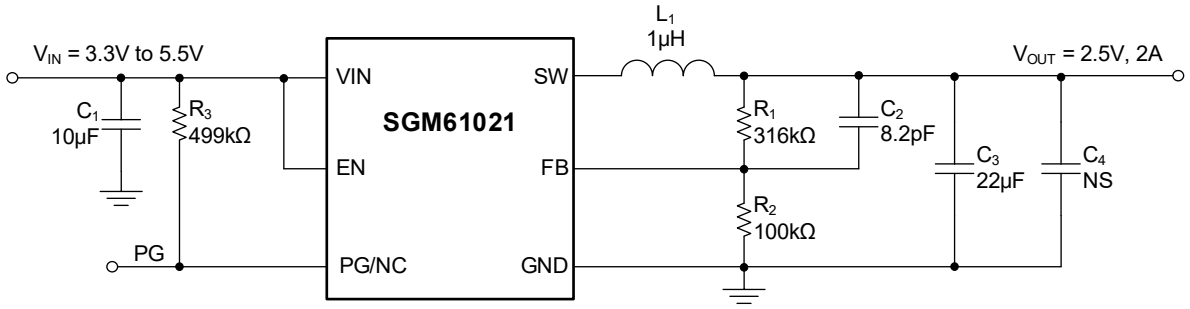


Figure 7. 2.5V Output Voltage Application

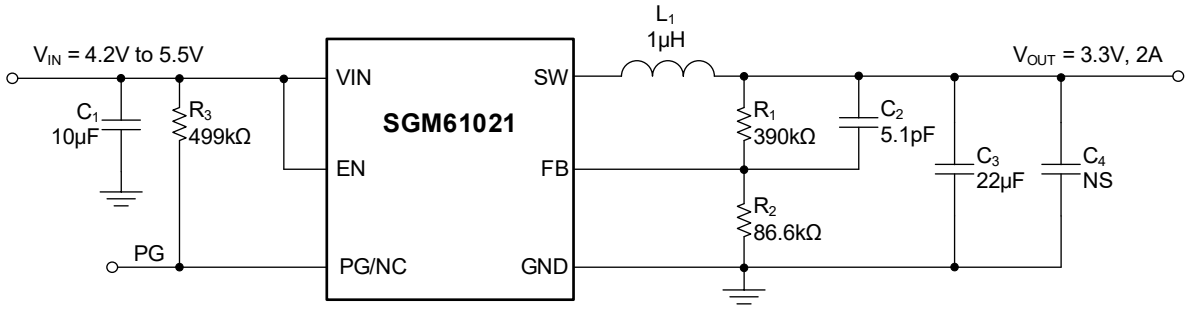


Figure 8. 3.3V Output Voltage Application

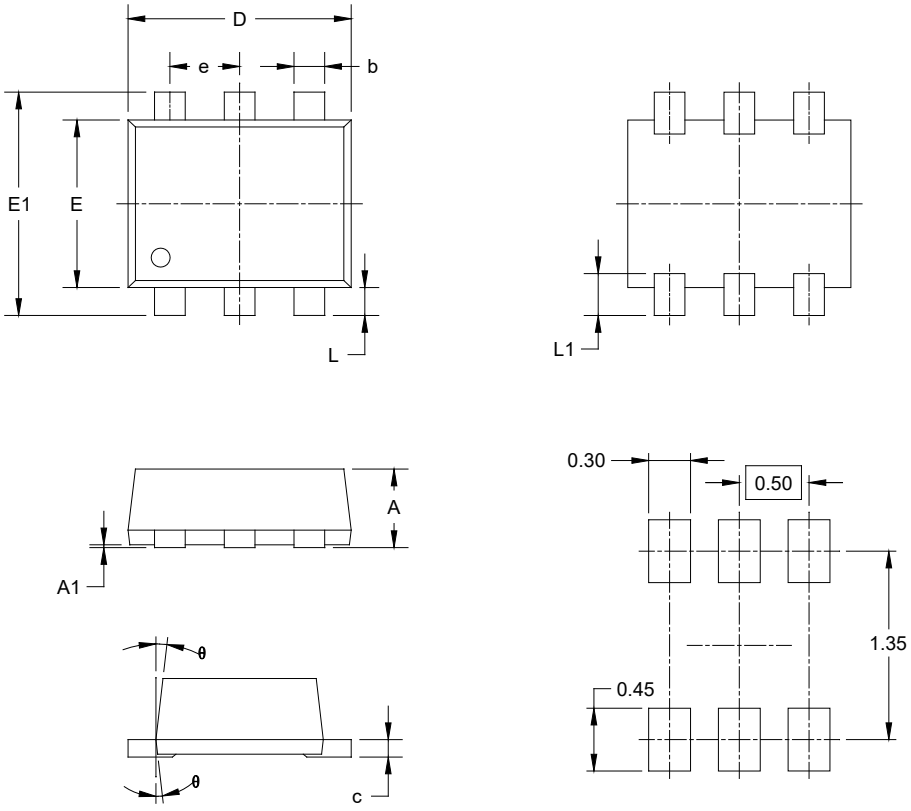
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (APRIL 2025) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

SOT-563-6



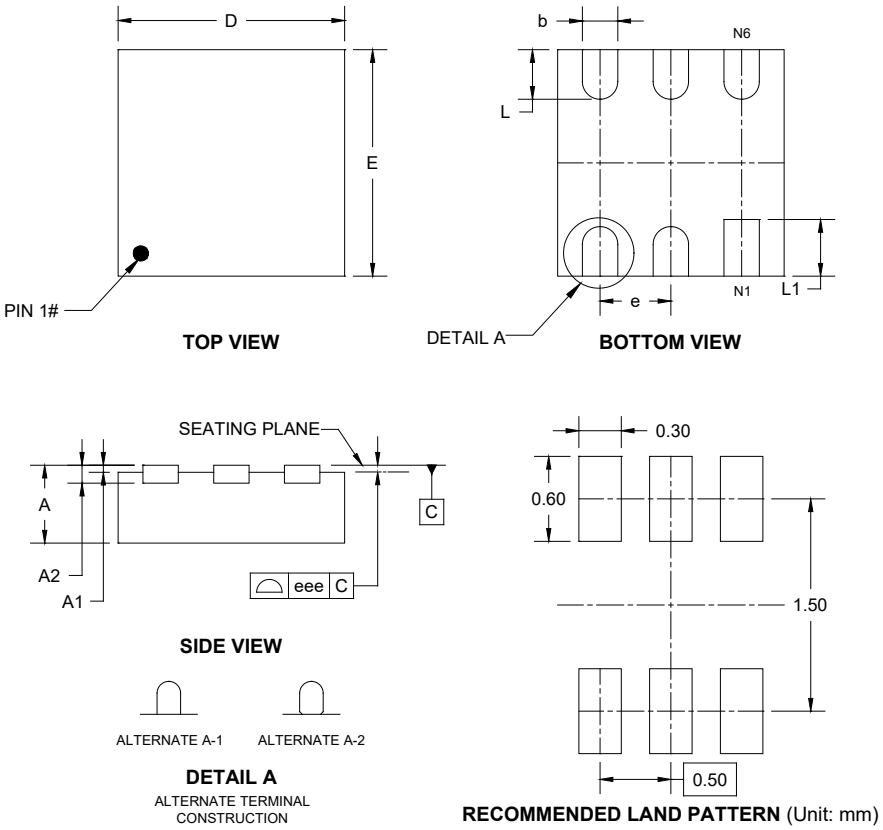
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
b	0.170	0.270	0.007	0.011
c	0.090	0.180	0.004	0.007
D	1.500	1.700	0.059	0.067
E	1.100	1.300	0.043	0.051
E1	1.500	1.700	0.059	0.067
e	0.450	0.550	0.018	0.022
L	0.100	0.300	0.004	0.012
L1	0.200	0.400	0.008	0.016
θ	9° REF		9° REF	

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

UTDFN-1.6×1.6-6CL

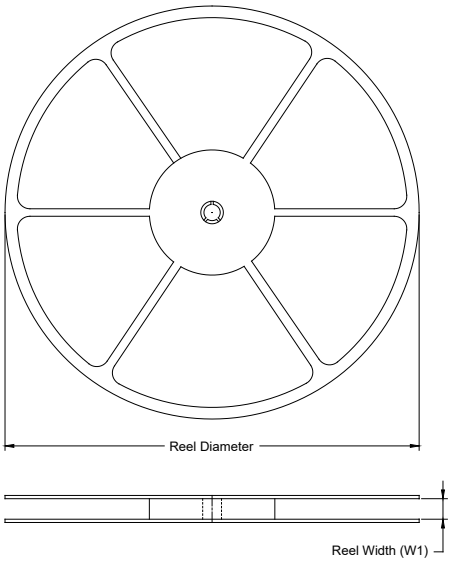


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.500	-	0.600
A1	0.000	-	0.050
A2	0.127 REF		
b	0.200	-	0.300
D	1.500	-	1.700
E	1.500	-	1.700
e	0.500 BSC		
L	0.250	-	0.450
L1	0.300	-	0.500
eee	0.080		

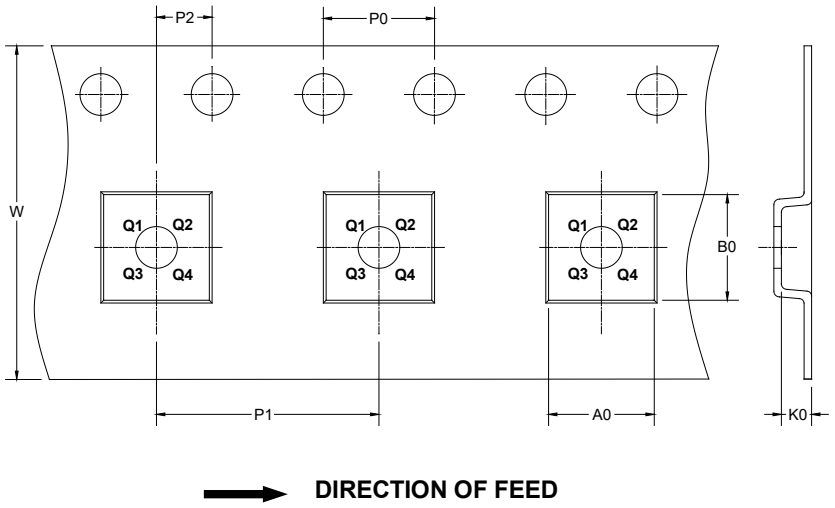
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



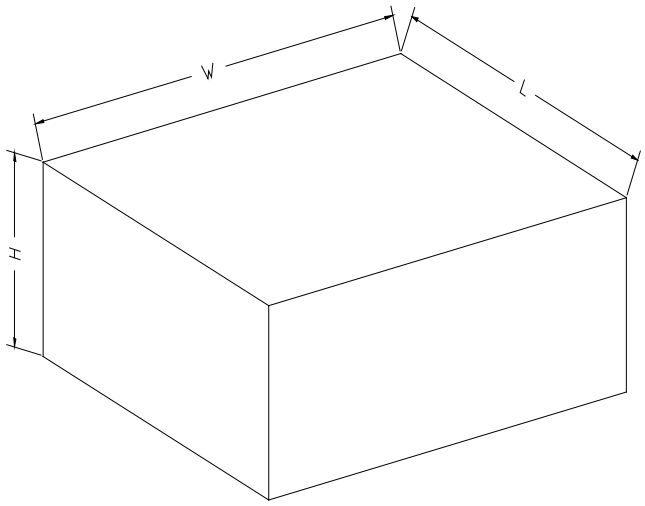
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-563-6	7"	9.5	1.78	1.78	0.69	4.0	4.0	2.0	8.0	Q3
UTDFN-1.6×1.6-6CL	7"	9.5	1.78	1.78	0.69	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002