SGM6625
24V Output, 2A, Non-Synchronous Boost Converter

GENERAL DESCRIPTION

The SGM6625 is a high-voltage non-synchronous Boost converter. The device integrates a 24V power MOSFET and supports an input voltage down to 2.5V. A 1.3MHz switching frequency makes the use of low-profile inductors and low-value ceramic input and output capacitors available. This device is specified for small and low power applications. This device also includes the built-in functions of over-current limit, soft-start, under-voltage lockout (UVLO) and thermal shutdown.

The SGM6625 is available in Green SOT-23-5 and TDFN-2×2-8L packages.

FEATURES

- **Down to 2.5V Low Input Voltage**
- **Up to 24V High Output Voltage**
- **1.3MHz Fixed Switching Frequency**
- **At 5V Input (TYP): 12V at 300mA**
- **Integrated Low-side Power MOSFET**
- **Small Capacitors and Inductors**
- **Internally Compensated**
- **Soft-Start and Current Limit Built-in Functions**
- **Under-Voltage Lockout (UVLO)**
- **Thermal Shutdown**
- **Available in Green SOT-23-5 and TDFN-2×2-8L Packages**

APPLICATIONS

Small LCD Displays and White LED Driver
Flash in Camera or Mobile
Handheld Computers and PDAs
Digital Cameras and Video Cameras
External Modems

TYPICAL APPLICATION

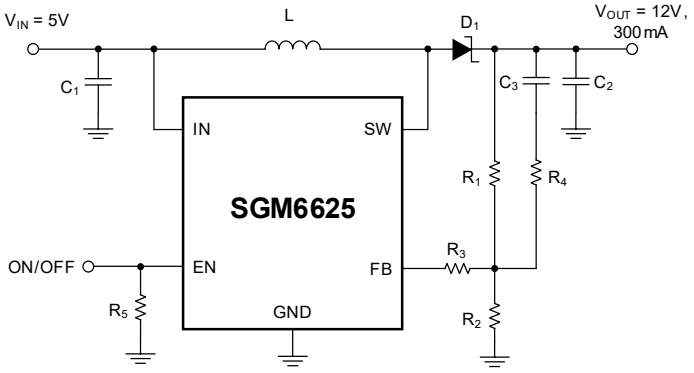
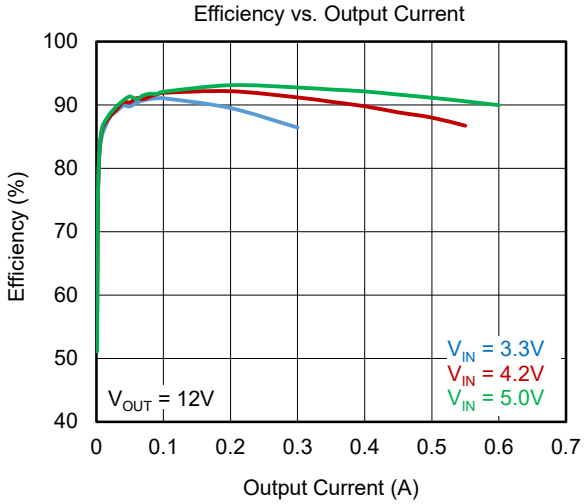


Figure 1. Typical Application Circuit



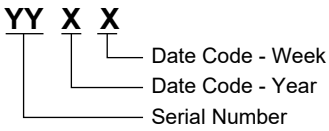
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6625	SOT-23-5	-40℃ to +125℃	SGM6625YN5G/TR	15FXX	Tape and Reel, 3000
	TDFN-2×2-8L	-40℃ to +125℃	SGM6625YTDE8G/TR	6625 XXXX	Tape and Reel, 3000

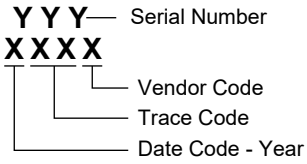
MARKING INFORMATION

NOTE: XX = Date Code. XXXX = Date Code, Trace Code and Vendor Code.

SOT-23-5



TDFN-2×2-8L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

SW Pin ..... -0.3V to 25.5V
All Other Pins ..... -0.3V to 6V
Package Thermal Resistance
SOT-23-5, θ_{JA} ..... 157.1℃/W
SOT-23-5, θ_{JB} ..... 35.7℃/W
SOT-23-5, θ_{JC} ..... 80.9℃/W
TDFN-2×2-8L, θ_{JA} ..... 76.3℃/W
TDFN-2×2-8L, θ_{JB} ..... 41.0℃/W
TDFN-2×2-8L, $\theta_{JC\ (TOP)}$ ..... 88.0℃/W
TDFN-2×2-8L, $\theta_{JC\ (BOT)}$ ..... 12.6℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} ..... 2.5V to 5.5V
Output Voltage, V_{OUT} ..... 3V to 24V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

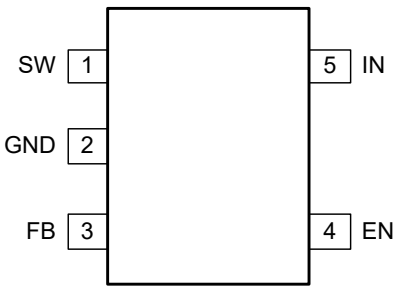
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

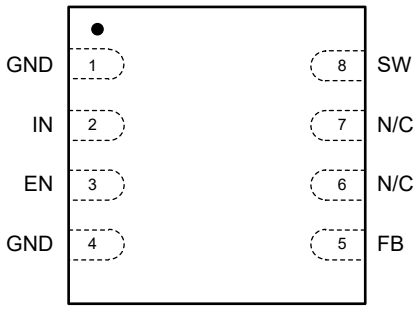
PIN CONFIGURATIONS

(TOP VIEW)



SOT-23-5

(TOP VIEW)



TDFN-2×2-8L

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
SOT-23-5	TDFN-2×2-8L			
2	1, 4	GND	G	Ground Pin of the IC.
5	2	IN	P	Power Supply Input. Must be locally bypassed.
4	3	EN	I	Device Enable Node. Pulling this pin logic high enables the device and pulling it logic low disables the device. When it is not used, connect this pin to the input source for automatic start-up. It cannot be left floating.
3	5	FB	I	Feedback Pin to Program the Output Voltage.
—	6, 7	NC	—	Not Connect. Reserved for factory use.
1	8	SW	I	Switch Node. Drain connection of low-side power MOSFET.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

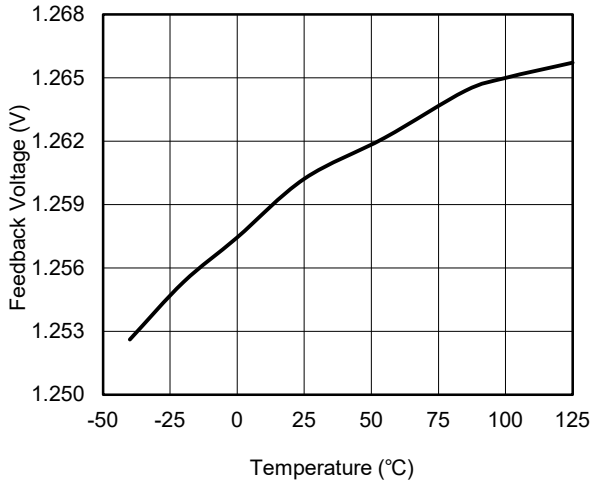
(V_{IN} = 5V, V_{EN} = 5V, T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.5		5.5	V
Under-Voltage Lockout Threshold	V_{UVLO}			2.3	2.45	V
Under-Voltage Lockout Hysteresis	V_{HYS}			100		mV
Shutdown Supply Current	I_{SD}	V_{EN} = 0V		0.02	1	μA
Quiescent Supply Current	I_Q	V_{FB} = 1.4V		249	600	μA
Switching Frequency	f_{SW}		0.9	1.3	1.7	MHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0V	85	93		%
EN Threshold	V_{EN}	V_{EN} Rising			1.2	V
		V_{EN} Falling	0.4			
EN Hysteresis	V_{EN_HYS}			95		mV
EN Input Bias Current		V_{EN} = 0V or 5.5V			1	μA
FB Voltage	V_{FB}		1.21	1.26	1.3	V
FB Input Bias Current		V_{FB} = 1.26V	-200	0.3		nA
SW On-Resistance (1)	R_{DSON}			0.18		Ω
SW Current Limit (1)	I_{LIM_SW}			2		A
SW Leakage Current	I_{SW_LKG}	V_{SW} = 15V			3	μA
Thermal Shutdown (1)	T_{SD}			150		℃

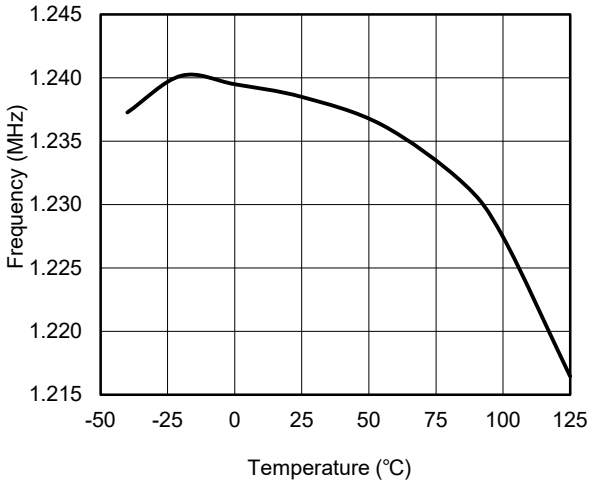
NOTE:
1. Specified by design and characterization, not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

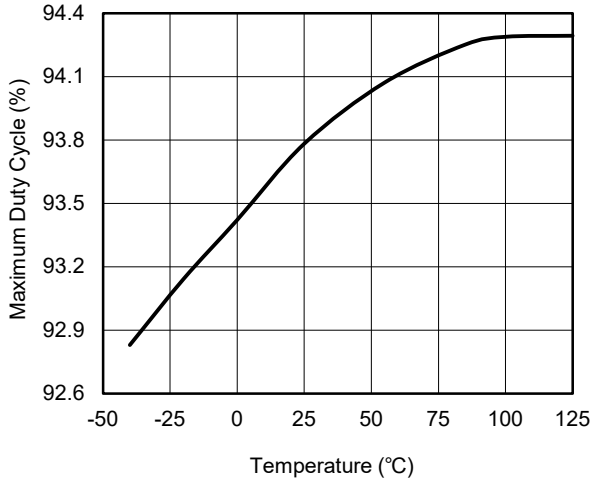
Feedback Voltage vs. Temperature



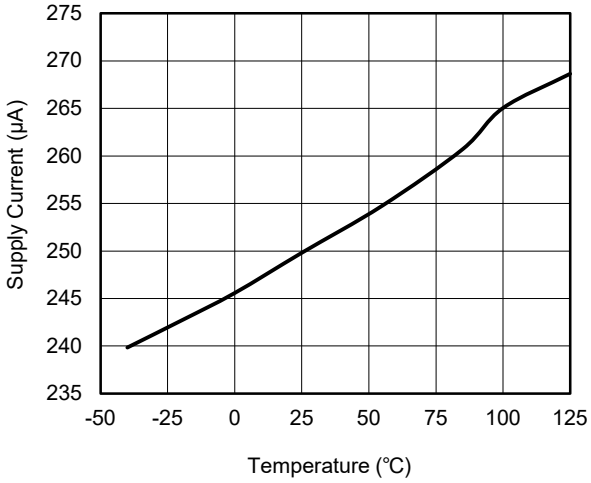
Frequency vs. Temperature



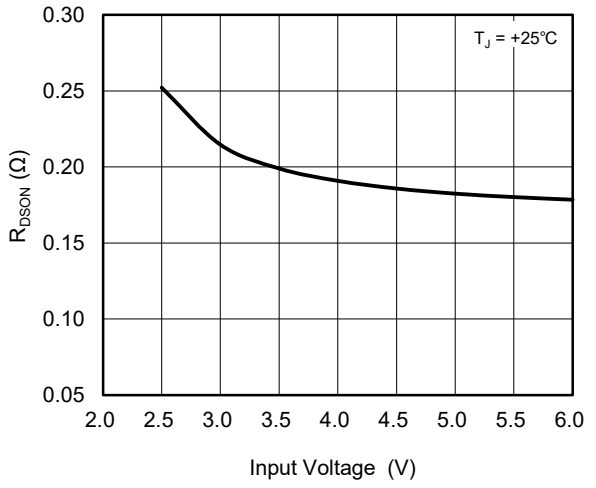
Maximum Duty Cycle vs. Temperature



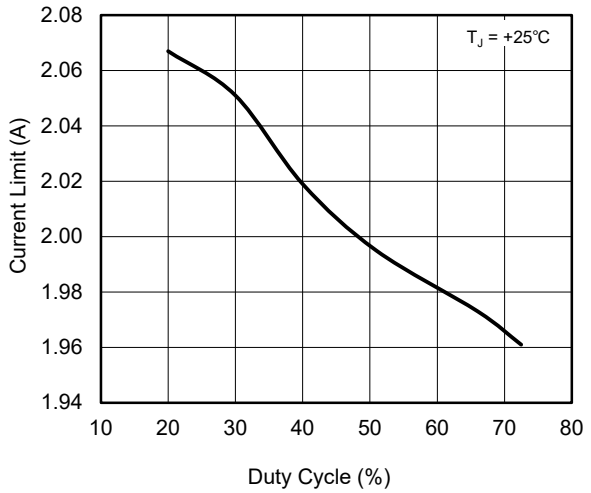
Supply Current vs. Temperature



On-Resistance vs. Input Voltage



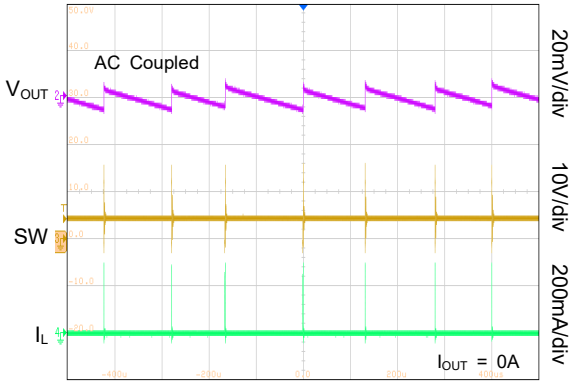
Current Limit vs. Duty Cycle



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

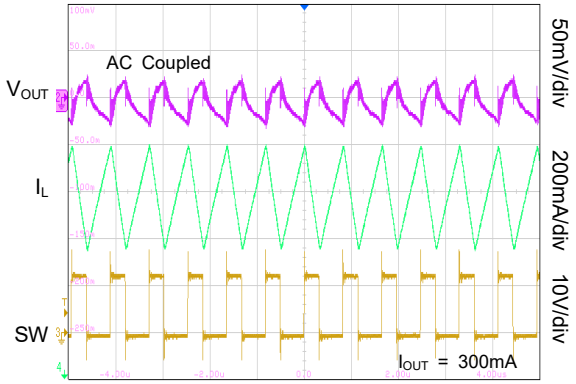
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 12V, unless otherwise noted.

Output Voltage with No Load



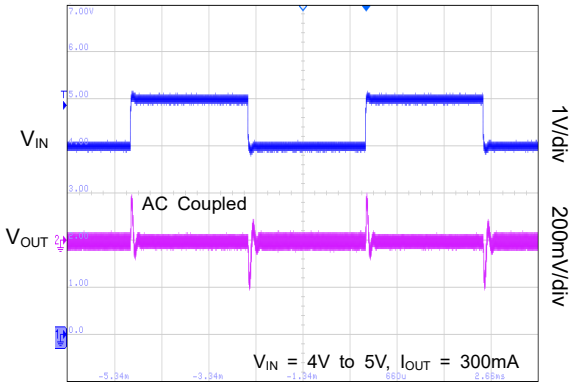
Time (100μs/div)

Output Voltage with Heavy Load



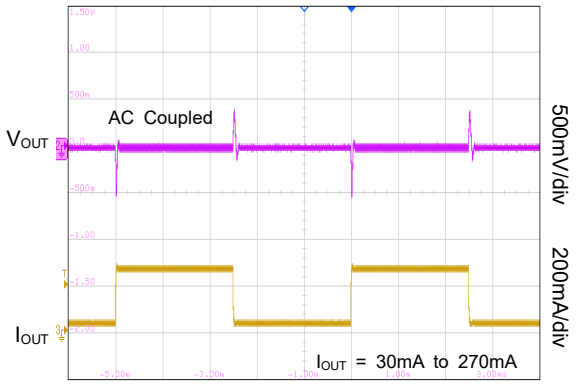
Time (1μs/div)

Line Transient



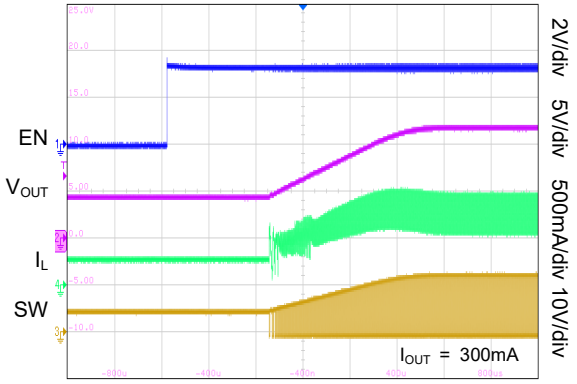
Time (1ms/div)

Load Transient



Time (1ms/div)

Start-up



Time (200μs/div)

FUNCTIONAL BLOCK DIAGRAM

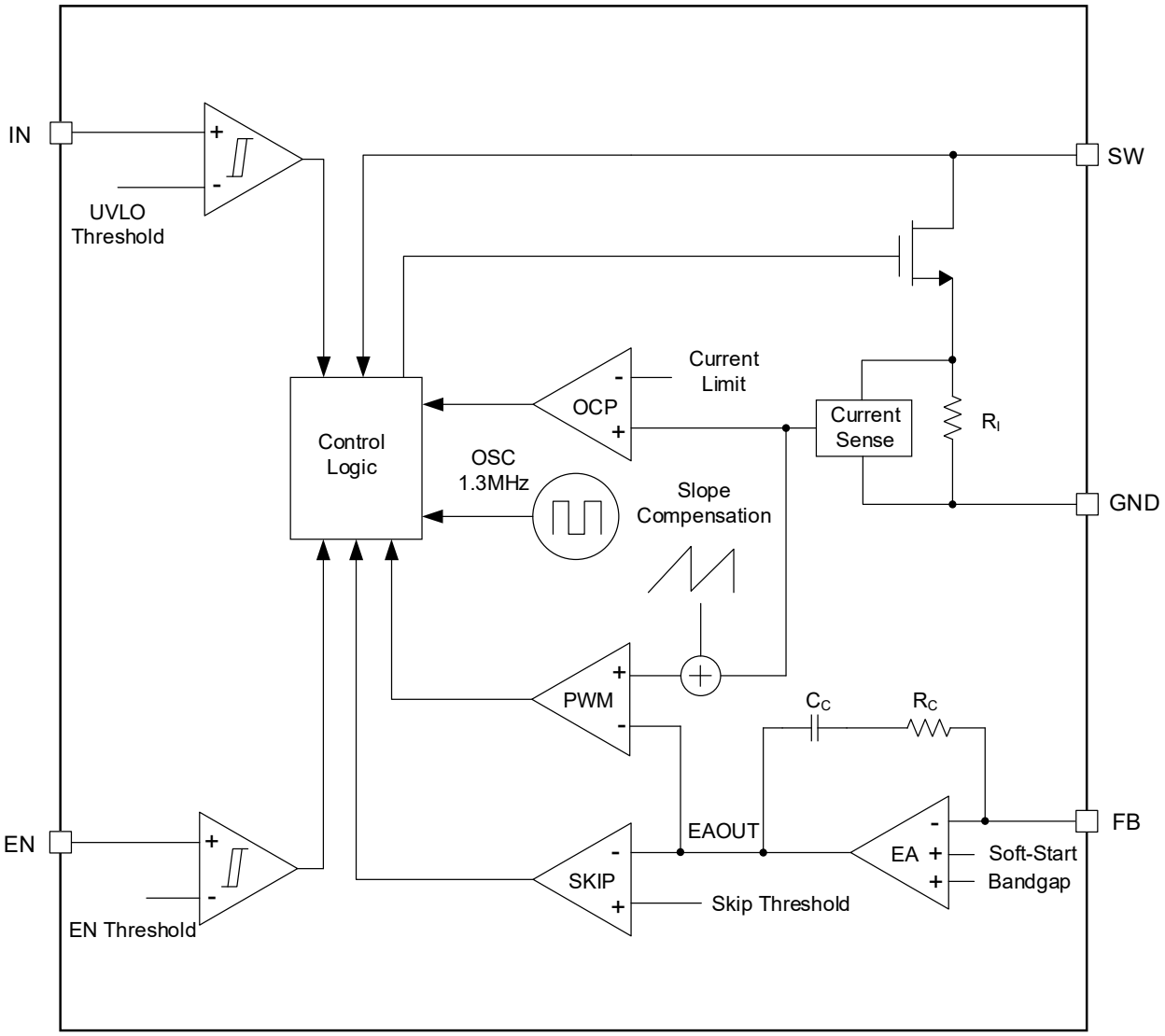


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM6625 is a Boost converter with integrated low-side MOSFET switch, which is capable of delivering up to 24V output voltages. Peak current mode PWM control is used to regulate the output voltage as shown in Figure 4. The device has a fixed switching frequency of 1.3MHz (TYP). A stabilizing ramp is added to the sensed peak current ramp to avoid sub-harmonic oscillation at an operation duty cycle higher than 35%. The error amplifier compares the FB pin voltage with an internal reference signal to provide an error signal for the PWM comparator to adjust the duty cycle which ultimately regulates the output voltage to the desired voltage. At the beginning of each clock cycle, the PWM comparator turns on the low-side MOSFET to ramp up the inductor current. As the inductor current reaches the level set by the error amplifier's output, the low-side MOSFET turns off, which causes the external Schottky diode to be forward biased to ramp down the inductor current that delivers the energy to the load as well as replenishes the output capacitor.

Soft-Start

The SGM6625 implements the internal soft-start feature to reduce the inrush current drawn during start-up. When logic high is applied on the EN pin, the device starts operation and the bandgap (BG) starts to be set up and the reference voltage begins to rise. Once the reference voltage reaches 1.26V (TYP), the device starts switching, and the output voltage ramps up gradually according to the internal soft-start slope. The soft-start time is about 1ms, which effectively reduces the inrush current during start-up.

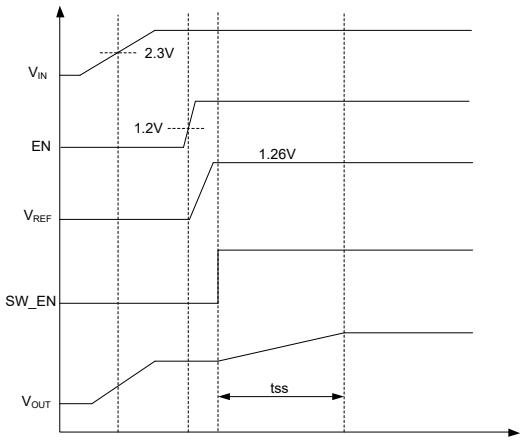


Figure 3. Typical Start-up Waveform

UVLO Protection

Under-voltage lockout protection (UVLO) monitors the V_{IN} power input. When the voltage is lower than UVLO threshold voltage, the device is shut down. This is a non-latched protection.

Over-Current Protection

The SGM6625 provides inherent over-current protection. The low-side MOSFET is turned off when the peak current reaches the current limit threshold of 2A (TYP), and the low-side MOSFET is not turned on again until the next clock cycle.

Thermal Shutdown

The internal thermal shutdown protection turns off the device when the junction temperature exceeds +150℃. The chip will resume operation when the junction temperature drops by at least 15℃ (TYP).

Pulse-Skipping Mode

The SGM6625 integrates a pulse-skipping mode at the light load. When a light load condition occurs, the error amplifier output (EAOUT) voltage naturally decreases and reduces the peak current. When the EAOUT voltage further goes down with the reduced load and reaches the pre-set low threshold, the output of the error amplifier is clamped at this threshold and will not go down any more. If the load is further lowered, the output voltage of SGM6625 exceeds the nominal voltage and the device skips the switching cycles. The pulse-skipping mode reduces the switching losses and improves efficiency at light load condition by reducing the average switching frequency.

APPLICATION INFORMATION

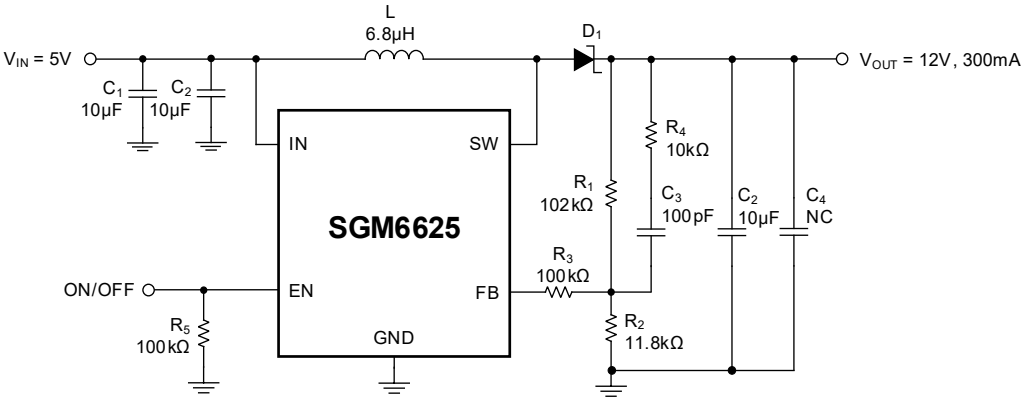


Figure 4. Typical Boost Circuit

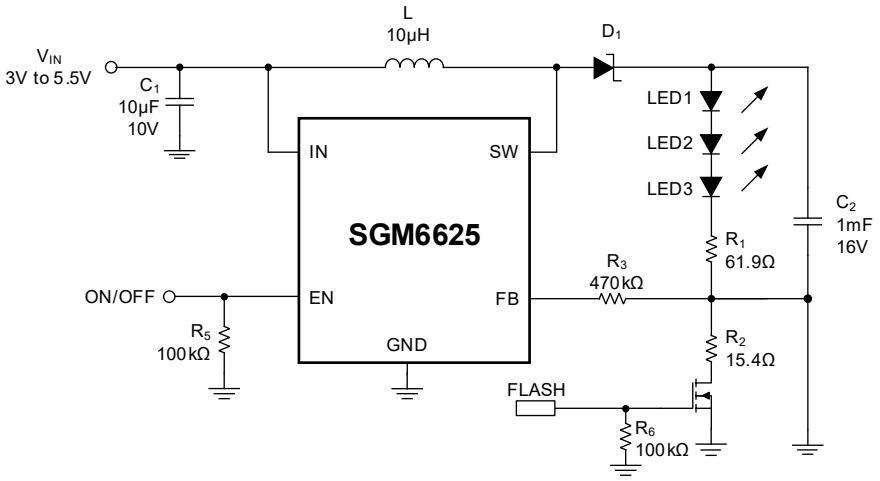


Figure 5. Typical Driving Flashlight LEDs Circuit (20mA Torch Current and 100mA Flash Current)

APPLICATION INFORMATION (continued)

Setting the Output Voltage

The output voltage of SGM6625 is configured via a resistive divider connected to the FB pin. Use Equation 1 to program the output voltage. R_1 is the top feedback resistor and R_2 is the bottom feedback resistor.

$$V_{OUT} = 1.26 \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Due to the leakage current of the resistor divider, the resistance of R_2 should be no less than 10kΩ. Thermally stable resistors with an accuracy of 1% or higher and of the same type are recommended for R_1 and R_2. Put them close to each other for the same thermal variations.

Inductor Selection

Inductor is the most critical component in the design of a Boost converter as SGM6625, because it affects the steady state operation, transient behavior and loop stability (sub-harmonic oscillations). Four parameters of the inductor must be considered in the design: nominal inductance value, DC resistance (DCR), saturation current (or 20% to 30% inductance-drop currents) and maximum RMS current (DC plus AC) for a certain temperature rise.

$$\Delta I_L = \frac{1}{\left[L \times f_{SW} \times \left(\frac{1}{V_{OUT} + V_F - V_{IN}} + \frac{1}{V_{IN}}\right)\right]} \quad (2)$$

where,

ΔI_L = Inductor peak-to-peak ripple current,

L = Inductor value,

V_F = Schottky diode forward voltage,

f_{SW} = Switching frequency.

Inductance and saturation current of an inductor are the two most important criterions for the inductor selection. It is recommended to choose a peak-to-peak ripple current (given by Equation 2) that is in the 30% to 40% range of the maximum DC current of the inductor in the application. Such ripple factor usually gives a good compromise between inductor core and converter conduction losses (due to the AC ripple) and the inductor size. Inductor DC current can be calculated based on input-output power balance as given in Equation 3:

$$I_{IN\_DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (3)$$

Typically, the inductor value can have a ±20% initial tolerance. On top of that, the inductance may drop another 20% to 30% when the inductor current approaches to the maximum saturation or 20% to 30% drops at the maximum current. This drop is usually given by the manufacturer. Note that the powder iron core inductors are not as sharply saturated as ferrite inductors and will show a gradual inductance drop even when the peak current is much higher than its maximum rated currents, which is an important advantage. The manufacturer specifies the 20% to 30% drop current level for them rather than saturation. However, they are usually slightly bigger than the similar ferrite inductor. Finally, the total RMS current of the inductor must be limited to keep the total inductor losses low and prevent excessive temperature rise in the inductor. The DCR of an inductor may increase around 50% if the temperature is increased from +25℃ to +125 ℃ . Such temperature rise needs to be considered in the evaluation of DC losses of the inductor.

Using an inductor with a smaller inductance in a Boost converter will result in extending the discontinuous conduction mode (DCM) range to a higher load current due to the larger ripple. Small inductance can also result in reduced maximum output current, increased input voltage ripple and reduced efficiency. Large inductors with low DCR values can offer better output current and higher conversion efficiency. However, smaller inductance usually provides better load transient response. For these reasons, an inductance with 30% to 40% current ripple (of the peak load current) is recommended.

SGM6625 implements the built-in slope compensation to prevent sub-harmonic oscillation. The use of small inductance might result in insufficient slope compensation, which ultimately results in unstable operation. Therefore, if the inductor is not selected according to the recommended values, the designer must verify the selected inductor for the application with the maximum and minimum margins of the input and output voltages.

APPLICATION INFORMATION (continued)

Input and Output Capacitor Selection

Boost converter's input capacitor has continuous current throughout the entire switching cycle, a 4.7μF to 10μF ceramic capacitor is recommended to place as close as possible between the IN pin and GND pin of the device. For applications where the SGM6625 is located far away from the input source, a capacitor with 47μF or higher capacitance is recommended to damp the wiring harness inductance.

The output capacitors of Boost converter dictate the output voltage ripple and load transient response. Equation 4 is used to estimate the necessary capacitance to achieve desired output voltage ripple, where V_{RIPPLE} is the peak-to-peak output ripple.

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times V_{RIPPLE}} \quad (4)$$

The additional output ripple component caused by ESR can be given by Equation 5:

$$V_{RIPPLE} = \Delta I_L \times ESR \quad (5)$$

For ceramic capacitors, the ESR is usually small and V_{RIPPLE_ESR} can be neglected, but for tantalum or electrolytic capacitors, the capacitive and ESR components of the ripple must be added to estimate the total output voltage ripple.

Schottky Diode Selection

The external rectification diode selection is critical to ensure device performance. A high speed and low forward voltage drop diode is recommended to improve efficiency. The average current rating of the diode should be higher than the peak load. The breakdown voltage of the selected diode should be higher than the maximum output voltage (24V) with margin. To achieve smaller size and less cost, Schottky diodes with lower rated voltages can be used. For example, a 12V output application requires a minimal of 20V breakdown voltage.

Loop Stability

The power loop of SGM6625 requires compensation to achieve better system stability. An internal resistor and capacitor, along with an external resistor, provide the necessary frequency compensation. The control loop stability is ensured by a configuration that includes two poles and one zero. The first pole, f_{P1}, is determined by the internal compensation capacitor (C_C), the gain of the error amplifier, and the resistance observed at the feedback node (R_{EQ}). The second pole, f_{P2}, is defined by the output capacitor and the load resistance.

$$f_{P1} = \frac{1}{2 \times \pi \times (560 \times 10^{-9}) \times R_{EQ}} \quad (6)$$

$$f_{P2} = \frac{1}{\pi \times C_{OUT} \times R_L} \quad (7)$$

$$f_{Z1} = 21kHz \quad (8)$$

$$f_{RHPZ} = \frac{R_L}{2\pi \times L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \quad (9)$$

$$A_V = 54000 \times \frac{V_{IN} \times R_L \times 1.26}{V_{OUT}^2} \quad (10)$$

In addition, a 47kΩ to 100kΩ resistor should be placed in series between the FB pin and the resistor divider, as illustrated in Figure 4. This configuration typically provides sufficient stability for most applications. If a higher phase margin is necessary, a network consisting of a resistor and a capacitor in series can be utilized in parallel with the upper resistor R_1 of the resistor divider. The pole and zero determined by the compensation network can be calculated by the following equations:

$$f_{P3} = \frac{1}{2\pi \times C_5 \times \left(R_4 + \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}\right)} \quad (11)$$

$$f_{Z2} = \frac{1}{2\pi \times C_5 \times (R_1 + R_4)} \quad (12)$$

APPLICATION INFORMATION (continued)

Layout Considerations

For most switching power supplies, especially with high frequency and high current, a good layout is required to prevent EMI failure and device damage as well as good stability of the device. Use wide and short traces for main power traces. Place the input capacitor to the IN and GND pins as close as possible. If possible, choose high capacitance value for C_{IN} for a stable input. Since the SW pin carries high current with fast rising and falling edges, all connections to the SW pin should be kept as short and wide as possible. The output capacitor (C_{OUT}) should be placed close to V_{OUT}. It is also beneficial to have the ground of C_{OUT} close to the GND pin since there is large ground return current flowing between them. Sensitive signals like FB must be placed away from SW trace. Figure 6 shows a reference design for the PCB layout of TDFN package.

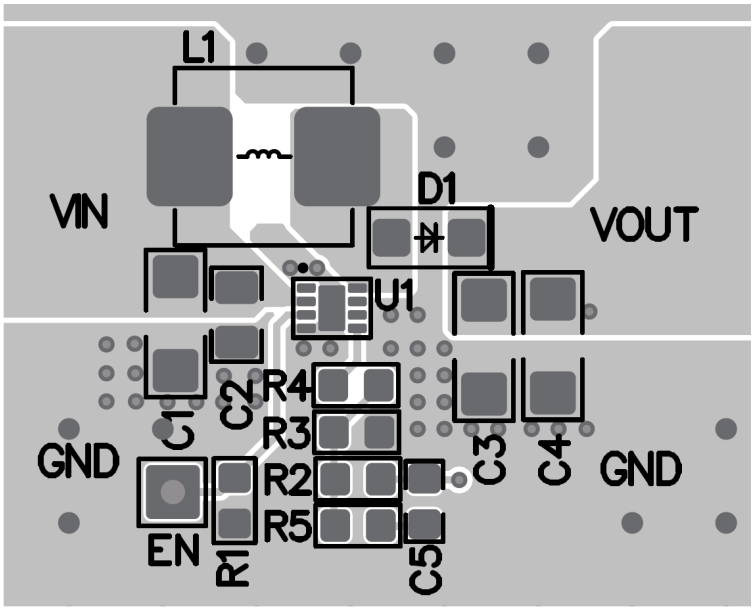


Figure 6. PCB Layout

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

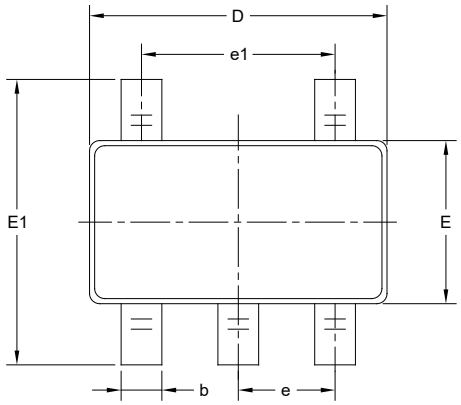
MARCH 2025 – REV.A.1 to REV.A.2	Page
Updated specified temperature range	2
Updated test conditions about temperature in ELECTRICAL CHARACTERISTICS and TYPICAL PERFORMANCE CHARACTERISTICS sections	4, 5, 6

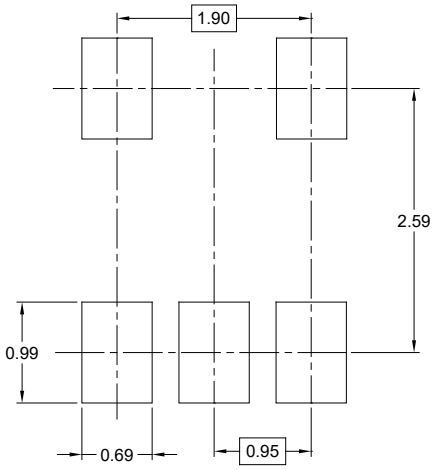
FEBRUARY 2025 – REV.A to REV.A.1	Page
Added SOT-23-5 package	All

Changes from Original (OCTOBER 2024) to REV.A	Page
Changed from product preview to production data	All

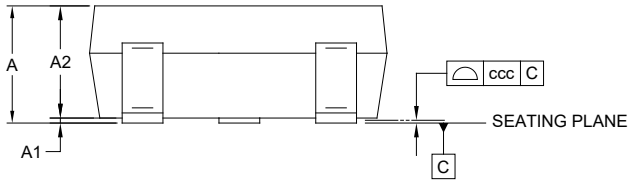
PACKAGE OUTLINE DIMENSIONS

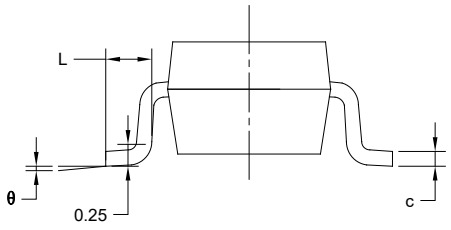
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)



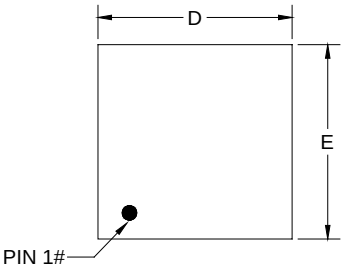


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

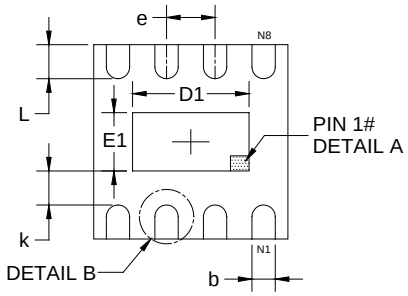
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

PACKAGE OUTLINE DIMENSIONS

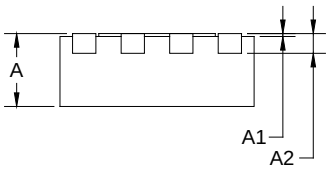
TDFN-2×2-8L



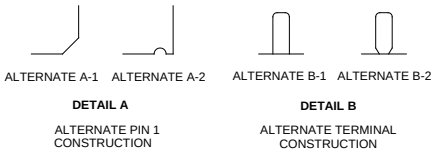
TOP VIEW

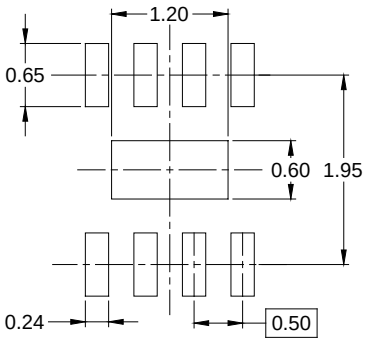


BOTTOM VIEW



SIDE VIEW





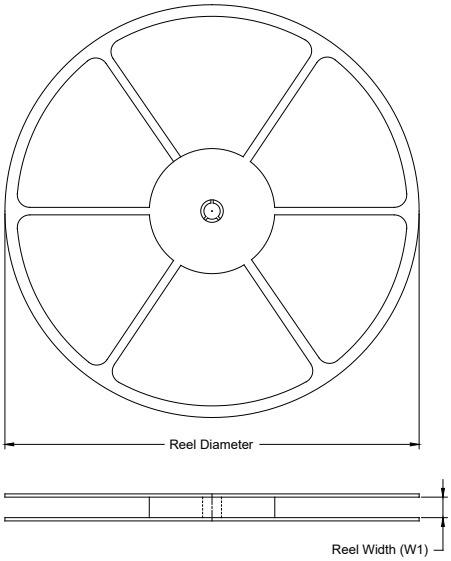
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
D	1.900	2.000	2.100
E	1.900	2.000	2.100
D1	1.100	1.200	1.300
E1	0.500	0.600	0.700
b	0.180	-	0.300
e	0.500 TYP		
k	0.200 MIN		
L	0.250	0.350	0.450

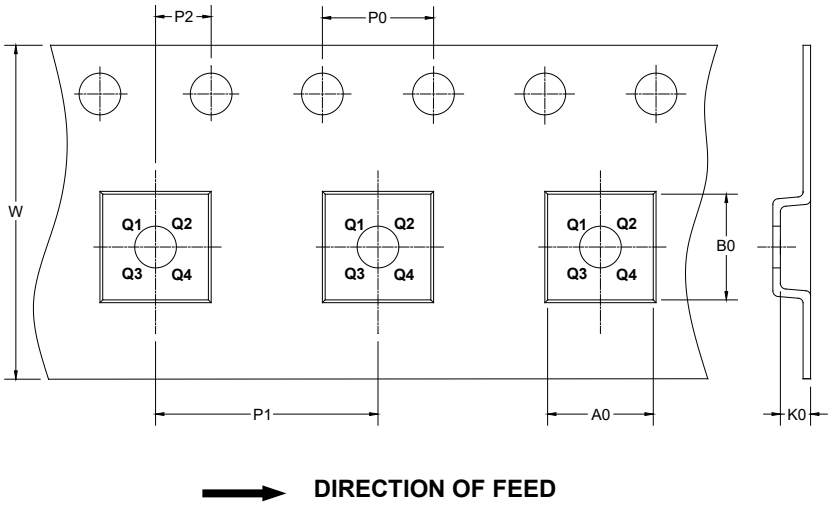
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

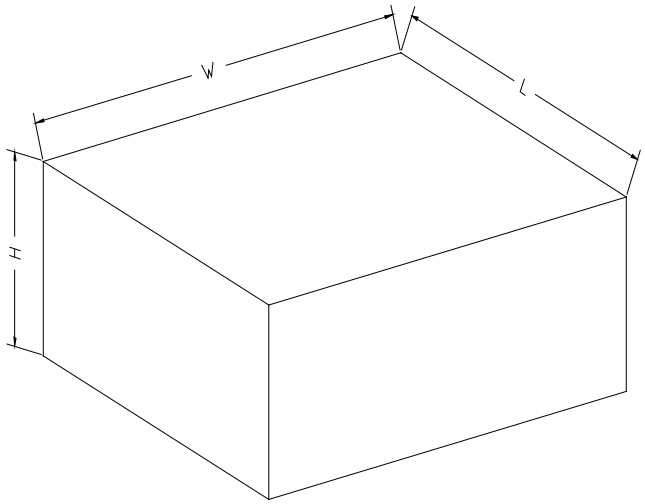
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
TDFN-2×2-8L	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002