SGM62117
High-Efficiency Buck-Boost Converter

GENERAL DESCRIPTION

The SGM62117 is a synchronous 4-switch Buck-Boost converter which is suitable for battery operated applications. The device's programmable light load PFM mode and low quiescent current (18μA, TYP) offer above 90% efficiency in the 10mA to 2A output current range. The output voltage is programmable via external feedback resistor divider.

The SGM62117 can operate in Buck, Boost or a novel 4-cycle Buck-Boost mode when the input voltage is close to or equal to the output voltage. The device implements pre-defined mode transition thresholds to avoid undesired toggling within modes to reduce output voltage ripple.

The SGM62117 offers various protection features to improve device robustness such as over-temperature, input over-voltage and output over-current protections. These features can protect the device against unexpected system failure.

The SGM62117 is available in a small Green TDFN-3×2-10L package. High integration provides a compact solution with only six external components.

TYPICAL APPLICATION

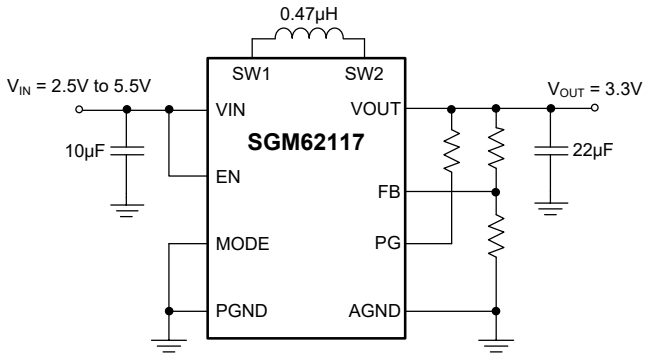


Figure 1. Typical Application Circuit

FEATURES

- **2.2V to 5.5V Input Voltage Range**
- **1.8V to 5.2V Output Voltage Range (Adjustable)**
- **2A Output Current for V_{IN} ≥ 2.5V and V_{OUT} = 3.3V**
- **Above 90% Efficiency for I_{OUT} from 10mA to 2A**
- **High Efficiency over the Entire Load Range**
- **18μA (TYP) Quiescent Current**
- **Programmable Forced PWM Mode and Pulse Frequency Modulation Mode**
- **Real Buck, Boost and Buck-Boost Modes**
- **Power Good**
- **Internal Soft-Start**
- **Forward and Reverse Current Operation and Current Limit**
- **OTP, Input OVP and Output OCP Protections**
- **True Shutdown Function with Load Disconnect**
- **Available in a Green TDFN-3×2-10L Package**

APPLICATIONS

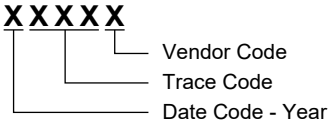
System Pre-Regulator
Point-of-Load Regulation
Thermoelectric Devices
Battery Backup
Voltage Stabilizer and Converter

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM62117	TDFN-3×2-10L	-40℃ to +125℃	SGM62117XTGH10G/TR	01KGH XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltages
VIN, SW1, SW2, EN, MODE, VOUT, FB, PG ..... -0.3V to 6V
SW1, SW2 (AC, less than 10ns) Voltages ..... -0.3V to 8V
Package Thermal Resistance
TDFN-3×2-10L, θ_{JA} ..... 76℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 3000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage, V_{IN} ..... 2.2V (1) to 5.5V
Output Voltage, V_{OUT} ..... 1.8V to 5.2V (2)
Effective Capacitance Connected to V_{IN}, C_{IN} .....
..... 4μF (MIN), 5μF (TYP)
Effective Inductance, L ..... 0.37μH to 0.57μH, 0.47μH (TYP)
Effective Capacitance Connected to V_{OUT}, C_{OUT}
1.8V ≤ V_{OUT} ≤ 2.3V ..... 10μF (MIN)
V_{OUT} > 2.3V ..... 7μF (MIN), 8.2μF (TYP)
Operating Junction Temperature, T_J ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

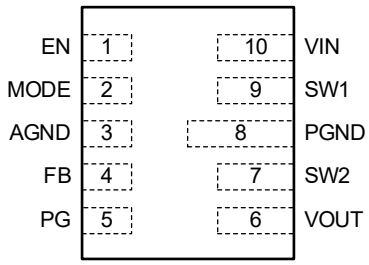
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-3×2-10L

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	EN	I	Active High Logic. Device Enable Input. Do not leave it floating.
2	MODE	I	Logic 0 for PFM Mode and Logic 1 for Forced PWM Mode. Do not leave it floating.
3	AGND	G	Analog Ground. Connect it to the PGND pin under the chip.
4	FB	I	Voltage Feedback Pin. Connect a resistor divider at FB pin to program the output voltage.
5	PG	O	Power Good Indicator. Open-Drain Output. Leave it floating if not used.
6	VOUT	O	Converter Output.
7	SW2	P	Boost Leg Connection for Inductor.
8	PGND	G	Power Ground.
9	SW1	P	Buck Leg Connection for Inductor.
10	VIN	I	Supply Voltage for Power Stage and Control Stage.

NOTE: I = input, O = output, G = ground, P = power.

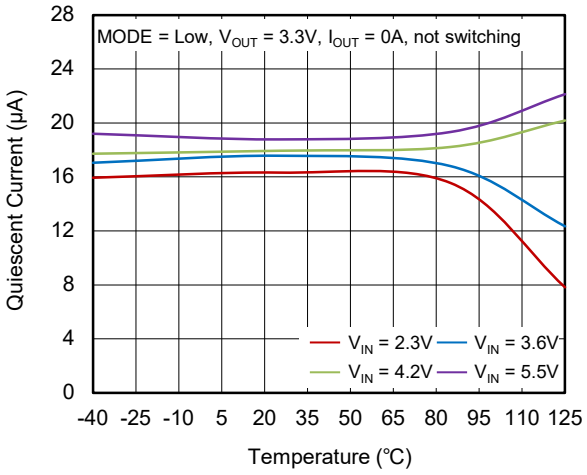
ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.2V to 5.5V, V_{OUT} = 1.8V to 5.2V, T_J = -40℃ to +125℃, typical values are measured at V_{IN} = 3.6V, V_{OUT} = 3.6V and T_J = +25℃, unless otherwise noted.)

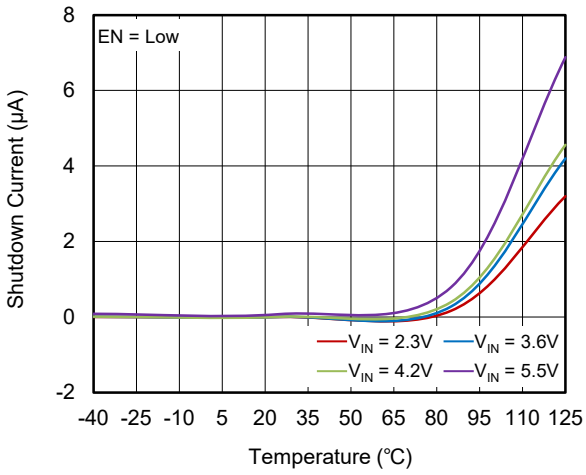
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Minimum Input Voltage for Full Load, Once Started	V_{IN_LOAD}	I_{OUT} = 2A, V_{OUT} = 3.3V		2.5		V
Quiescent Current into VIN	I_{Q_VIN}	EN = V_{IN} = 3.6V, V_{OUT} = 3.6V, not switching		18		μA
Shutdown Current into VIN	I_{SD}	EN = low, V_{IN} = 3.6V, V_{OUT} = 0V, T_J = -40℃ to +85℃		50	500	nA
Under-Voltage Lockout Threshold	UVLO	V_{IN} rising	1.9	2.05	2.2	V
		V_{IN} falling	1.7	1.85	2	
Thermal Shutdown	T_{SD}	Temperature rising		150		℃
Thermal Shutdown Hysteresis	T_{SD_HYST}			20		℃
Soft-Start, Power Good						
Soft-Start, Current Limit Ramp Time	t_{RAMP}	V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 1A, time from first switching to power good		150		μs
Delay from EN-Edge until Rising V_{OUT}	t_{DELAY}	V_{IN} = 3.6V, V_{OUT} = 3.3V, delay from EN-edge until rising first switching		420		μs
Logic Signals EN, MODE						
High-Level Input Voltage	V_{IH}		1.2			V
Low-Level Input Voltage	V_{IL}				0.4	V
Power Good Threshold Voltage	V_{PG_RISING}	V_{OUT} rising, referenced to V_{OUT} nominal		95		%
	$V_{PG\_FALLING}$	V_{OUT} falling, referenced to V_{OUT} nominal		90		%
Power Good Low-Level Output Voltage	V_{PG_LOW}	I_{SINK} = 1mA			0.4	V
Power Good Delay Time	t_{PG_DELAY}	V_{FB} falling		33		μs
Input Leakage Current	I_{LKG}			0.01	1	μA
Output						
Feedback Regulation Voltage	V_{FB}			500		mV
Feedback Voltage accuracy	V_{FB}	T_J= +25℃	-1		1	%
Over-Voltage Protection Threshold		V_{OUT} rising	5.5	5.7	5.9	V
		V_{IN} rising	5.5	5.7	6.0	V
Peak Inductor Current to Enter PFM-Mode	$I_{PWM/PFM}$	V_{IN} = 3.6V, V_{OUT} = 3.3V		1.06		A
Feedback Input Bias Current	I_{FB}	V_{FB} = 500mV		5		nA
Peak Current Limit	I_{PK}			5		A
Peak Current Limit for Reverse Operation	$I_{PK\_REVERSE}$	V_{IN} = 5V, V_{OUT} = 3.3V		-2		A
High-side FET On-Resistance	Buck R_{DSON}	V_{IN} = 5V, V_{OUT} = 3.3V, I_{SW1} = 1A		30		mΩ
Low-side FET On-Resistance				20		
High-side FET On-Resistance	Boost R_{DSON}	V_{IN} = 5V, V_{OUT} = 3.3V, I_{SW2} = 1A		30		mΩ
Low-side FET On-Resistance				15		
Inductor Switching Frequency, Boost Mode	f_{SW}	V_{IN} = 5V, V_{OUT} = 3.3V, no Load		3		MHz
Line Regulation		V_{IN} = 2.5V to 5.5V, V_{OUT} = 3.3V, I_{OUT} = 1.5A		0.3		%
Load Regulation		V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 0A to 2A, forced-PWM mode		0.1		%

TYPICAL PERFORMANCE CHARACTERISTICS

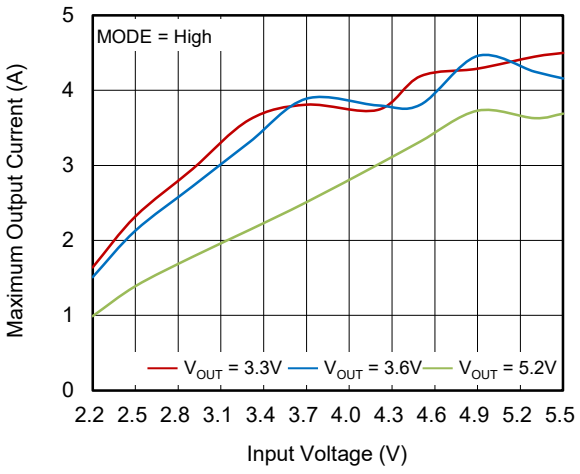
Quiescent Current vs. Temperature



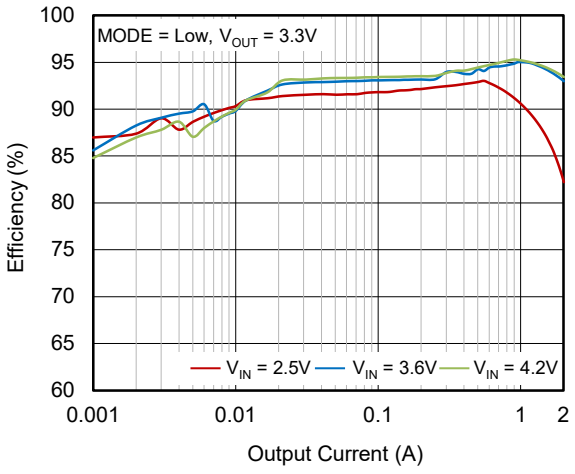
Shutdown Current vs. Temperature



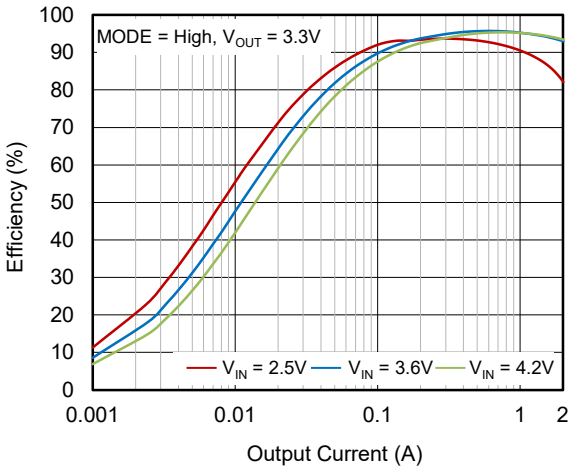
Typical Output Current Capability vs. Input Voltage



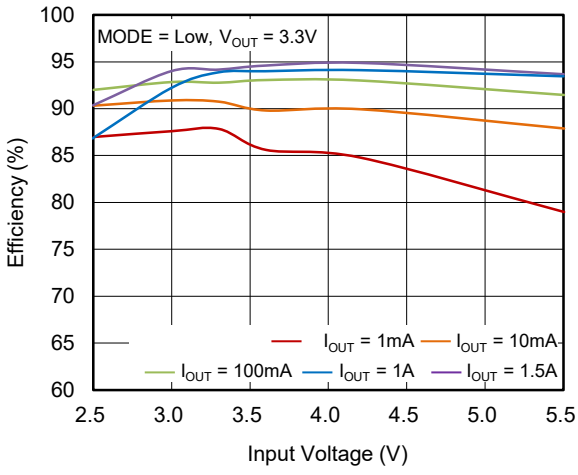
Efficiency vs. Output Current (PFM/PWM)



Efficiency vs. Output Current (PWM)

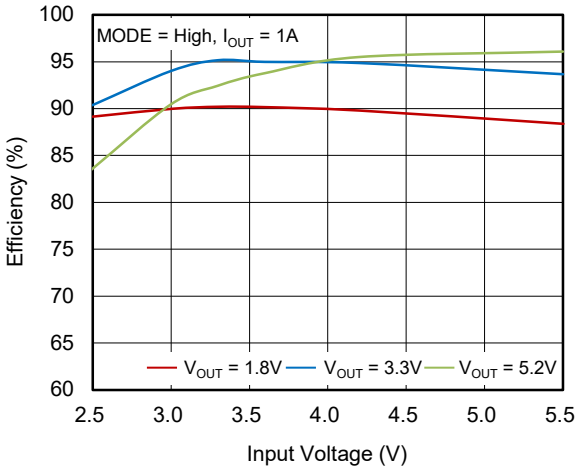


Efficiency vs. Input Voltage (PFM/PWM)

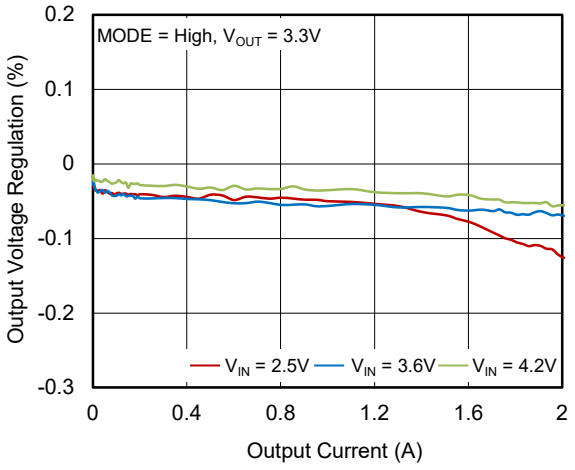


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

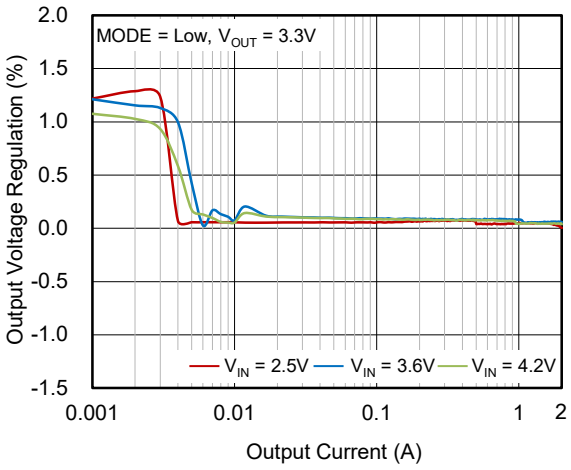
Efficiency vs. Input Voltage (PWM)



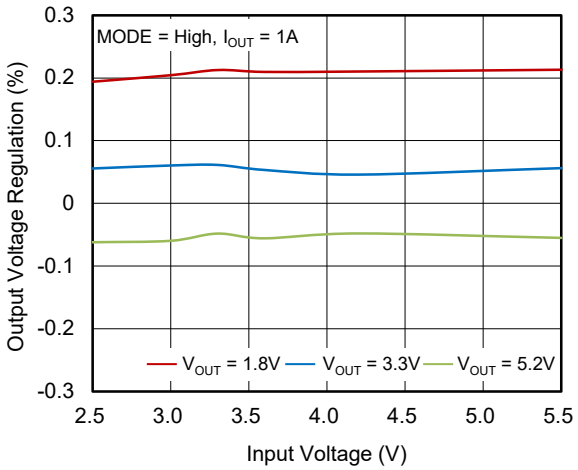
Load Regulation (PWM)



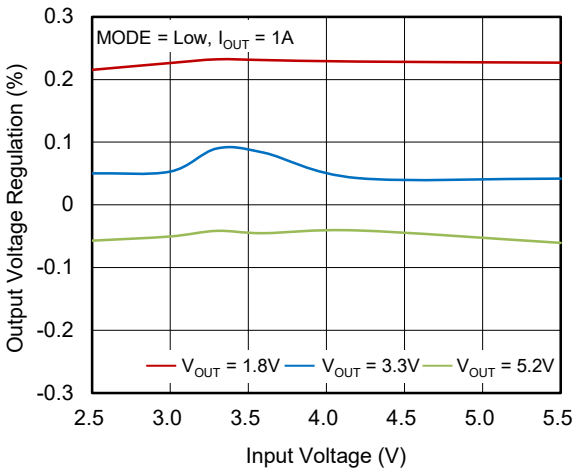
Load Regulation (PFM/PWM)



Line Regulation (PWM)



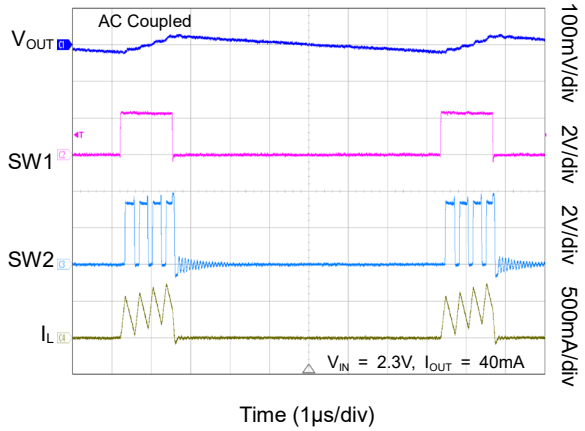
Line Regulation (PFM/PWM)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

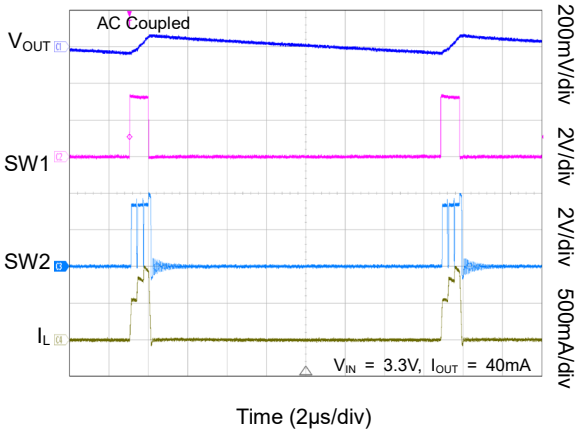
V_{OUT} = 3.3V and MODE = Low, unless otherwise noted.

Switching Waveforms, PFM Boost Operation



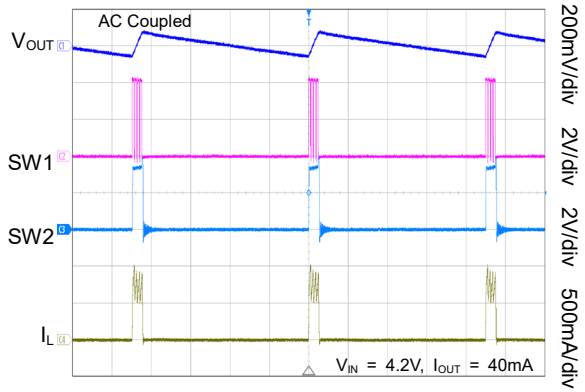
Time (1μs/div)

Switching Waveforms, PFM Buck-Boost Operation



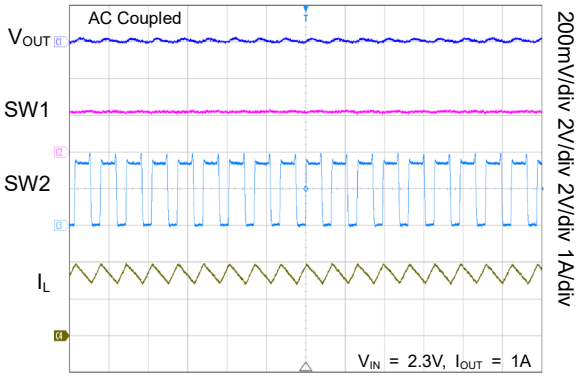
Time (2μs/div)

Switching Waveforms, PFM Buck Operation



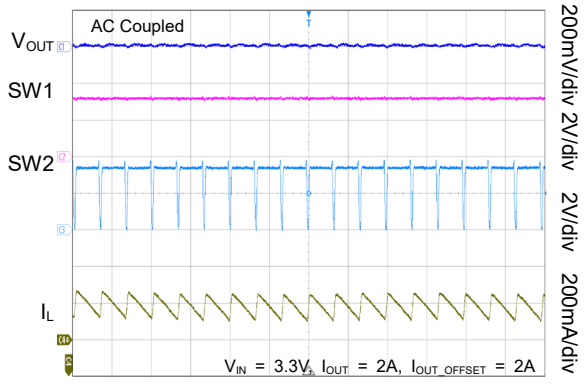
Time (2μs/div)

Switching Waveforms, PWM Boost Operation



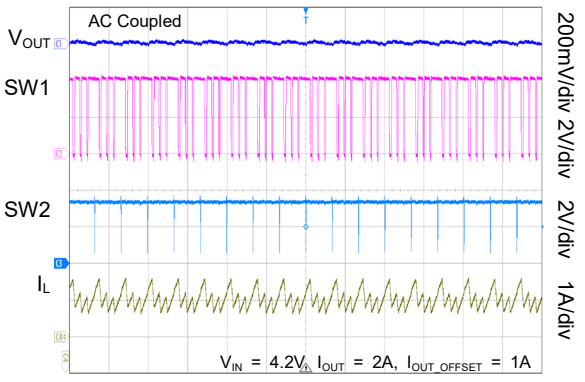
Time (500ns/div)

Switching Waveforms, PWM Buck-Boost Operation



Time (500ns/div)

Switching Waveforms, PWM Buck-Boost Operation

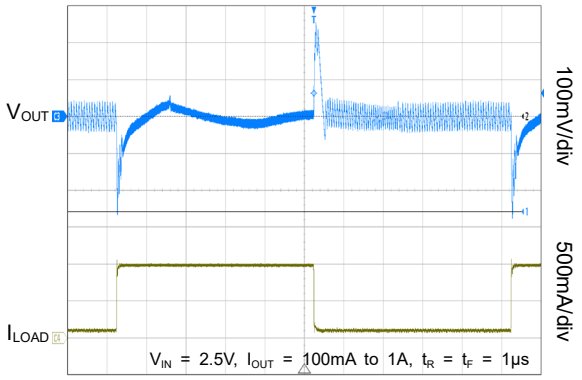


Time (1μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

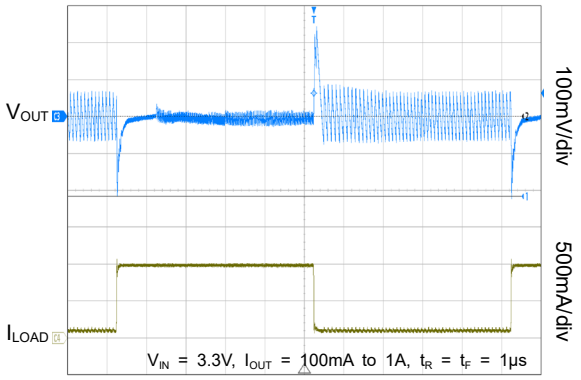
V_{OUT} = 3.3V and MODE = Low, unless otherwise noted.

Load Transient, PFM/PWM Boost Operation



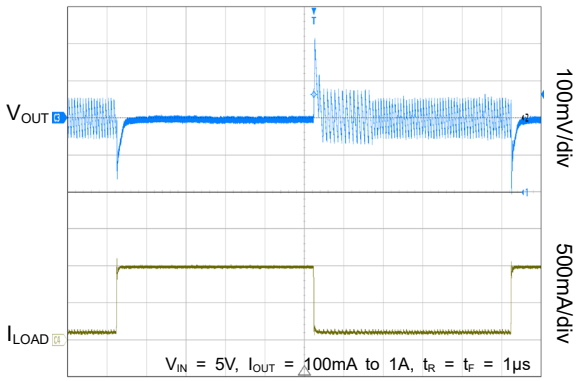
Time (100μs/div)

Load Transient, PFM/PWM Buck-Boost Operation



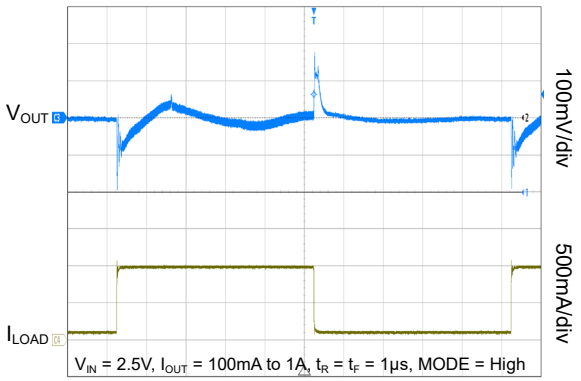
Time (100μs/div)

Load Transient, PFM/PWM Buck Operation



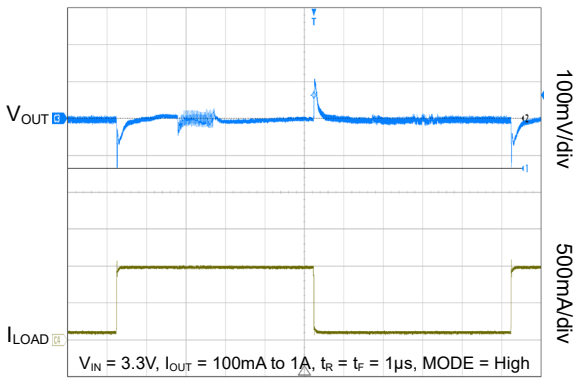
Time (100μs/div)

Load Transient, PWM Boost Operation



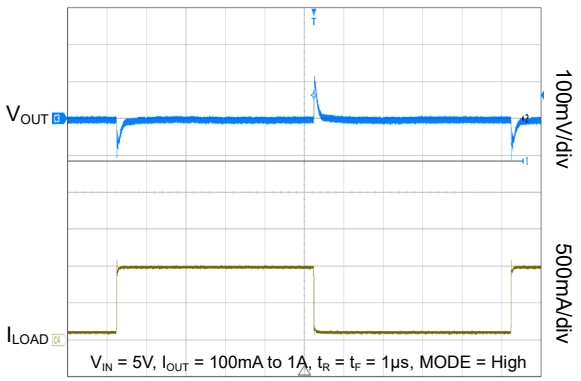
Time (100μs/div)

Load Transient, PWM Buck-Boost Operation



Time (100μs/div)

Load Transient, PWM Buck Operation

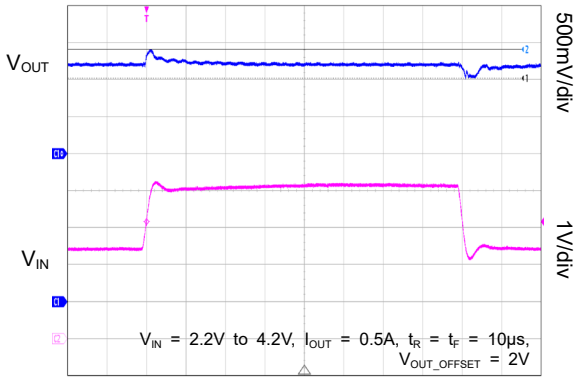


Time (100μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

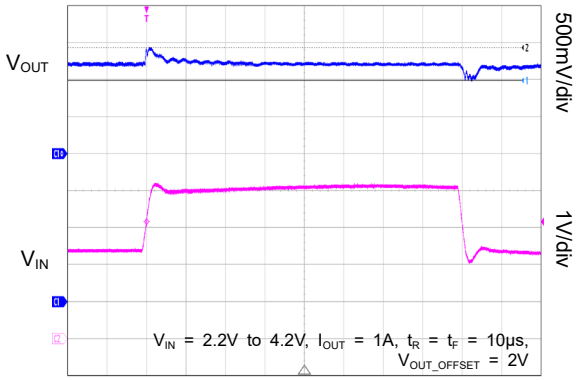
V_{OUT} = 3.3V and MODE = High, unless otherwise noted.

Line Transient, PWM Operation



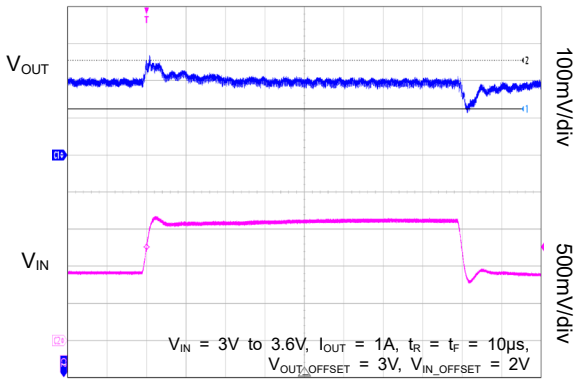
Time (50μs/div)

Line Transient, PWM Operation



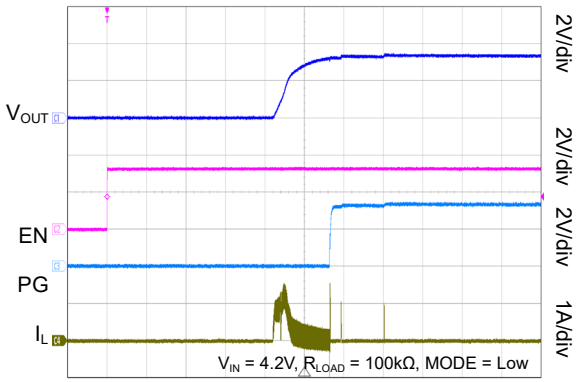
Time (50μs/div)

Line Transient, PWM Operation



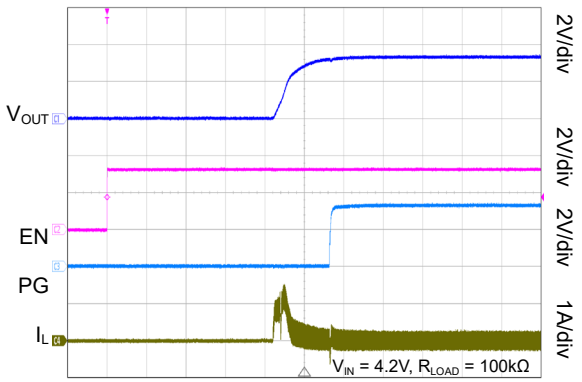
Time (50μs/div)

Startup Behavior from Rising Enable, PFM Operation



Time (100μs/div)

Startup Behavior from Rising Enable, PWM Operation



Time (100μs/div)

FUNCTIONAL BLOCK DIAGRAM

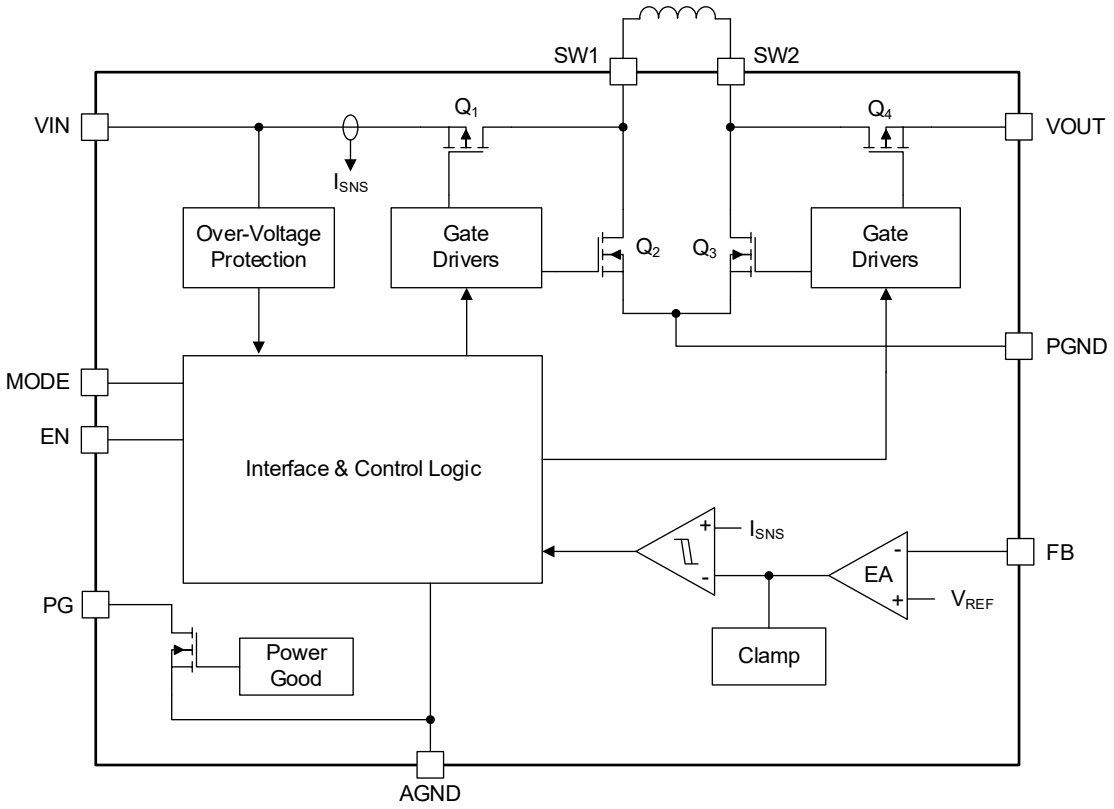


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM62117 is a synchronous Buck-Boost converter with integrated switches that can operate over a wide input voltage and output current range with high efficiency. The device is capable to change mode automatically among Buck, Boost and Buck-Boost depending on the input and output condition. When V_{IN} >> V_{OUT}, the device is in Buck mode, when V_{IN} << V_{OUT}, the device is in Boost mode, and when V_{OUT} ~ V_{IN}, the device is in 4-cycle Buck-Boost mode. In the Buck-Boost mode, the 4-cycle operation controls the four switches to turn on/off alternately to reduce the RMS current in the inductor and output capacitors to maintain low output voltage ripple and achieve high efficiency across entire input voltage range.

Control Loop Description

The SGM62117 adopts the peak current mode control architecture where the peak current of the Buck high-side MOSFET is sensed to provide the current information for the control loop. The sensed current is compared with a voltage loop formed by the FB network and internal reference voltage. The voltage loop outputs the error information between the FB voltage and reference voltage which ultimately determines the proper inductor current level to maintain output voltage regulation.

Figure 3 is a simplified drawing of the internal control loop, which consists of an error amplifier, a type-2 compensation network of the voltage loop and a PFM control block.

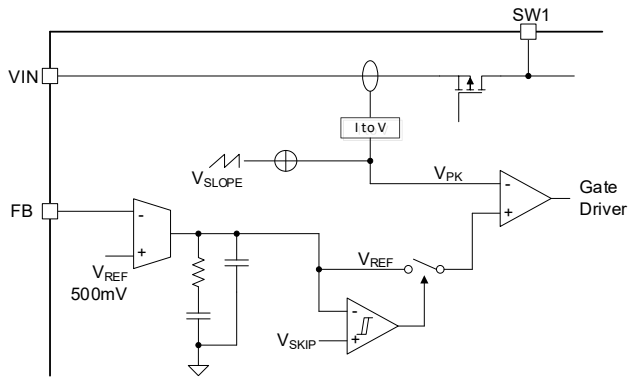


Figure 3. Control Loop Architecture Scheme

Enable

The enable pin is used to enable or disable the device. A logic high turns on the device, while a logic low will disable the device.

PFM/PWM Mode

The SGM62117 allows programmable PFM operation or forced PWM operation at light loads via MODE pin. PFM mode is used to improve efficiency at light loads when MODE pin is logic low. A logic high applied at the MODE pin programs the device in forced PWM operation regardless of the load current. Do not leave this pin floating.

Under-Voltage Lockout (UVLO)

To protect the device from malfunctioning when the input voltage is insufficient, under-voltage lockout (UVLO) protection is included. The device will not operate until the input voltage exceeds UVLO rising threshold, and will lockout if the input voltage falls below the UVLO falling threshold.

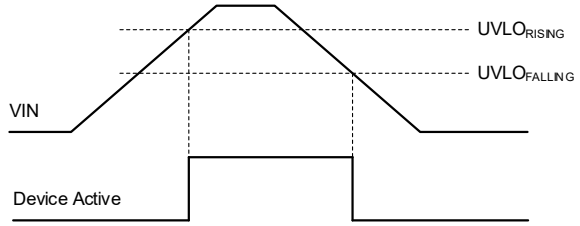


Figure 4. Rising and Falling Under-Voltage Lockout Behavior

Soft-Start

During startup, the built-in soft-start function will minimize the inrush current and limit the output voltage overshoot. When the device is turned on or enabled, the switch current limit is increased gradually to the maximum to prevent large input current at startup. With the gradual increase of the current limit, the inrush current for no-load conditions is minimized while it is still possible to start into heavy loads (as long as the load is within the device current limit).

The output voltage rise time depends on the application and operating condition. It will increase if the output capacitance and load are large or if the device operates in Boost mode. More information can be found in the Application Information section.

DETAILED DESCRIPTION (continued)

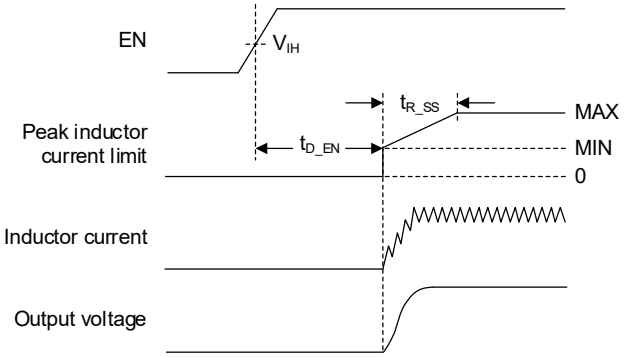


Figure 5. Startup Performance

Output Voltage Adjustment

A resistive divider connected among the VOUT, FB and GND enables output voltage programming. The recommended bottom feedback resistance is within 150kΩ to 200kΩ. The top feedback resistance is calculated based on the output voltage and the selected bottom feedback resistor.

Thermal Shutdown

To protect the device damage from overheating, thermal protection is included in the device. When the junction temperature rises above its threshold, the device will shut down. When the junction temperature drops below the OTP hysteresis, the device resume operation automatically.

Input Over-Voltage Protection (IVP)

The SGM62117 implements negative current operation, where the device is capable to transfer energy from the output back to the input. In such operating condition, if the input is not able to sink the reverse current, the input voltage will increase.

The SGM62117 will provide IVP feature to ensure that the voltage on VIN pin will never exceed 5.7V (TYP) when the MODE pin is set high (Force PWM Mode). Switching is immediately terminated when IVP is triggered and resumes automatically when the condition is removed.

Output Over-Voltage Protection (OVP)

The SGM62117 implements output over-voltage protection when the output voltage exceeds the OVP threshold (5.7V, TYP) during operation. Switching is terminated when OVP is triggered to prevent the device from damage.

Power-Good

The PG pin of the device is an open-drain output. An external pull-up resistor is required for proper operation. When the output voltage reaches above 95% of the programmed output voltage, the PG pin toggles to logic high. When the output voltage falls below 90% of the programmed voltage, the PG pin is pulled low to indicate a power-not-good event has occurred.

Mode Toggle

The SGM62117 automatically selects the operation mode based on the input and output voltages.

Buck Mode

When V_{IN} >> V_{OUT}, the device operates as a Buck converter as shown in Figure 6. Q_1 is the control switch, Q_2 is the synchronous rectifier, Q_3 is off and Q_4 is always on. In Buck mode, each switching cycle has two phases (switch on and off). Note that Q_1 and Q_4 are P-channel MOSFETs, which eliminate the need for external bootstrap capacitors.

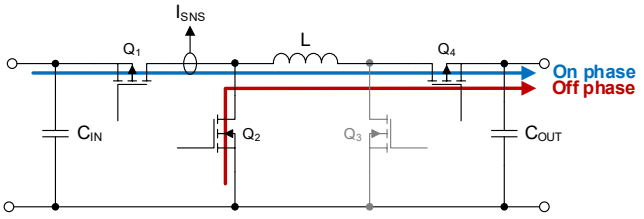


Figure 6. Buck Mode Switching

Boost Mode

If V_{IN} << V_{OUT}, the device operates as a Boost converter (see Figure 7). In the Boost mode, Q_1 is always on, Q_2 is off, Q_3 is the control switch, and Q_4 acts as the synchronous rectifier. Each cycle has two phases (switch on and off).

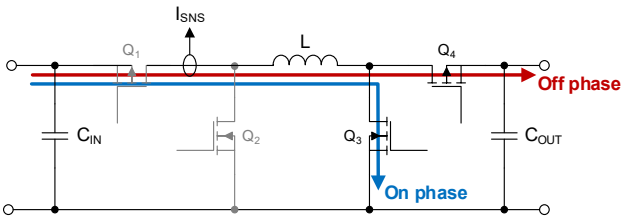


Figure 7. Boost Mode Switching

DETAILED DESCRIPTION (continued)

Buck-Boost Mode

When V_{OUT} ~ V_{IN}, all four switches are controlled in a continuous on manner. The internal control loop controls all 4 switches adaptively based on the load, input voltage and output voltage. The inductor current is regulated to ensure output voltage regulation and load current delivery.

Control Scheme

The SGM62117 employs peak current mode control scheme. The error amplifier (EA) output of the output voltage loop sets the desired current loop threshold for PWM duty cycle control as well as modes of operation. The on phase is terminated and the next phase(s) of the switching cycle starts if the sensed peak inductor current (ILM) reaches the reference signal from the error amplifier.

The off-time is a function of V_{IN} and V_{OUT} and the Buck, Boost or Buck-Boost operating mode of the converter.

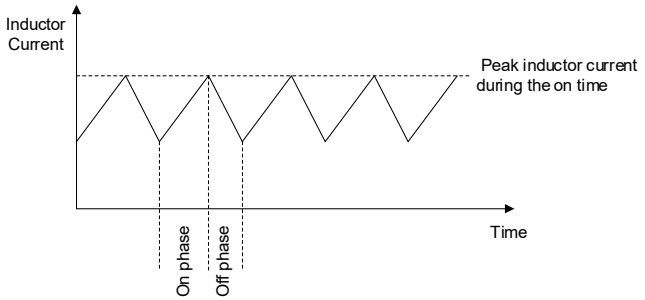


Figure 8. Buck or Boost Modes Peak Current Control

When the forced PWM (FPWM) mode is configured by setting MODE to Logic 1, the SGM62117 remains in continuous conduction mode even if the inductor current is negative, causing the current to flow in the reversed direction. During the negative current phase, the error amplifier will provide a negative current threshold (-2A, TYP) for the inner current loop which causes the average current of the inductor in reversed direction to become more negative. Therefore, as shown in Figure 9, smaller current limit levels must be used for the reverse current.

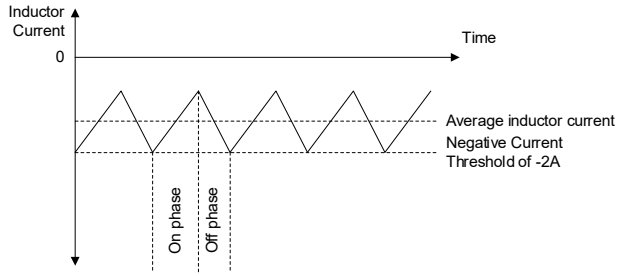


Figure 9. Buck or Boost Mode Reverse Peak Current Control

Pulse Frequency Modulation (PFM)

Pull the MODE pin to logic low, in medium to heavy load condition, the SGM62117 operates in the continuous current mode with constant switching frequency mode. To improve the efficiency at light load condition, the device switches to the pulse frequency modulation (PFM) mode. In the PFM mode, a sequence of burst switching cycles occurs to maintain the output voltage followed by an off period as shown in Figure 10.

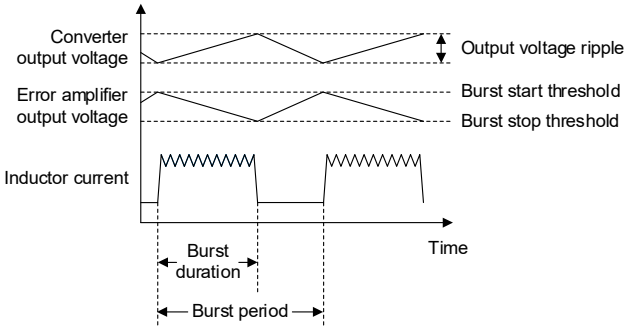


Figure 10. PFM Mode

The burst sequence is issued when the output of the error amplifier exceeds the PFM threshold voltage. The device dynamically adjusts the burst mode switching frequency based on the load to ensure the output voltage regulation accuracy.

In PFM mode, switching loss is reduced due to the reduced switching cycles. Some of the internal blocks are turned off in PFM mode to further improve the light load efficiency. However, output voltage ripple, DC output voltage accuracy and load transient performance are reduced in PFM mode (see Table 1).

DETAILED DESCRIPTION (continued)

Table 1. Comparison of the FPWM and PFM Performances

Parameter	Best Operating Mode
Light Load Efficiency	PFM
DC Output Voltage Accuracy	FPWM
Transient Response	FPWM
Output Voltage Ripple	FPWM

Forced PWM Operation (FPWM)

Force PWM mode is enabled via MODE = High. In the FPWM mode, in light load condition, the synchronous switches are not turned off when the inductor current goes negative to maintain a constant switching frequency. FPWM operation has lower output voltage ripple and better transient response compared to PFM. However, in the lower output currents, FPWM results in higher switching and conduction loss thus lower efficiency.

Current Limit Operation

The SGM62117 implements peak current limit to protect the device from over-current scenarios. Switching is terminated immediately when the peak current sensed from the Buck high-side FET reaches the current limit threshold.

APPLICATION INFORMATION

The SGM62117 is a perfect choice for applications that demand for a power supply with high efficiency over a wide load range. And their input voltage can vary from below, near and above the desired output voltages. The peak current in the internal switch of the device is typically limited to around 5A. The input and output voltage ranges are 2.2V to 5.5V and 1.8V to 5.2V respectively.

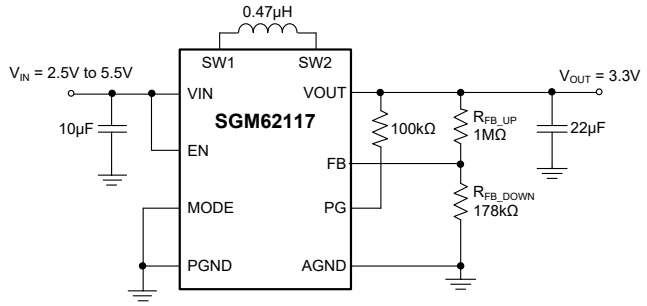


Figure 11. Application Example of 3.3V Output

Design Requirements

Parameters of this design example are shown in Table 2.

Table 2. Design Parameters

Parameter	Symbol	Recommended Value
Input Voltage	V_{IN}	2.5V to 5.5V
Output Voltage	V_{OUT}	3.3V
Output Current	I_{OUT}	2A

Design Procedure

Input Capacitor

The total input capacitance after considering the DC bias de-rating is recommended to be above 5μF. It is recommended to use a 10μF, 6.3V ceramic capacitor in most applications. If the source is far away from the device, it is recommended to use additional bulk capacitance (such as a 47μF electrolytic or tantalum capacitor) for better stability.

Inductor

A 0.47μH inductor is recommended for use with SGM62117. Lower DCR inductors are recommended for better efficiency. The rated saturation current (I_{SAT}) must be at least 20% above the maximum peak current in the worst cases including transients. Usually the worst cases occur in the Boost mode when operating at the lowest input voltage, highest output voltage and with the maximum load. Use Equation 1 to calculate the maximum duty cycle in Boost mode (corresponds to the maximum inductor current).

$$D_{MAX} = \frac{V_{OUT\_MAX} - V_{IN\_MIN}}{V_{OUT\_MAX}} \quad (1)$$

where:

D_{MAX} is the maximum duty cycle in Boost mode.

V_{IN_MIN} is the minimum input voltage.

V_{OUT_MAX} is the maximum output voltage.

In this application:

$$D_{MAX} = \frac{3.3V - 2.5V}{3.3V} \times 100\% = 24\%$$

The maximum inductor current can be calculated by:

$$I_{LM} = \frac{I_{OUT\_MAX}}{\eta(1 - D_{MAX})} + \frac{D_{MAX} \times V_{IN\_MIN}}{2 \times f \times L} \quad (2)$$

where:

I_{LM} is the peak inductor current.

I_{OUT_MAX} is the maximum output current.

η is the converter efficiency (use application curves or choose 90%).

f is the switching frequency (3MHz).

L is the inductance (0.47μH).

$$I_{LM} = \frac{2A}{0.9 \times (1 - 0.24)} + \frac{0.24 \times 2.5V}{2 \times 3MHz \times 0.47\mu H} = 3.1A$$

Choose the I_{SAT} value at least 20% higher than the calculated I_{LM} value. In this example, I_{LM} ≈ 3.1A and the selected inductor saturation current is 3.7A.

Output Voltage

An external resistor divider should be used between VOUT, FB and GND to set the output voltage. Between VOUT and FB is the upper feedback resistor (R_{FB_UP}). Between FB and GND is the lower feedback resistor (R_{FB_DOWN}), and it is recommended not to exceed 200kΩ. V_{OUT} is calculated by Equation 3 below.

$$V_{OUT} = V_{FB} \times \left(\frac{R_{FB\_UP}}{R_{FB\_DOWN}} + 1 \right) \quad (3)$$

where:

V_{FB} is 500mV.

APPLICATION INFORMATION (continued)

Output Capacitor

It is recommended to use at least one 22μF ceramic capacitor for output voltage below 3.6V. For application's output voltage higher than 3.6V, two 22μF, 6.3V ceramic capacitors are recommended. To reduce high frequency noise, a 100nF ceramic capacitor in 0201 or 0402 package is recommended to place as close to the VOUT and GND pins as possible in parallel to the other output capacitors.

There is no upper limit for the SGM62117 output capacitance. However, using large output capacitance will result in slower response to the transients and other issues when the output is discharged.

Application Curves

Table 3 lists the component values and part numbers used for the tests and measurements outlined in the characteristic curves.

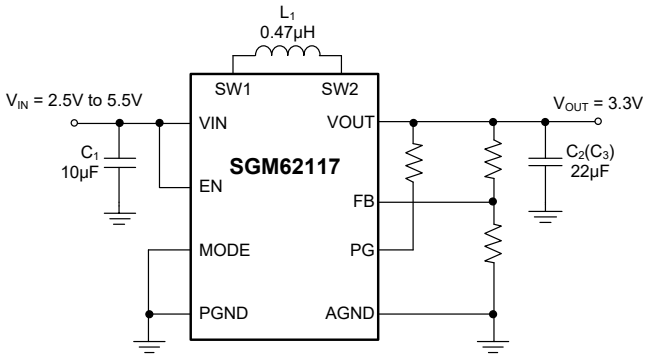


Figure 12. Application Example for Characteristic Curves

Layout

Layout plays a significant role for all switch modes in DC/DC power supplies. Improper layout could result in poor EMI performance, device unstable, and potential device damage. The input capacitor, output capacitor and the inductor should be placed as close as possible to the IC. The SGM62117 implements a power ground and control ground pins to minimize the ground noise effect on sensitive analog circuits. Connect the analog ground trace to the main power ground at a single point.

Figure 13 is an example layout which is also the PCB layout used to collect the data in the Application Curves section.

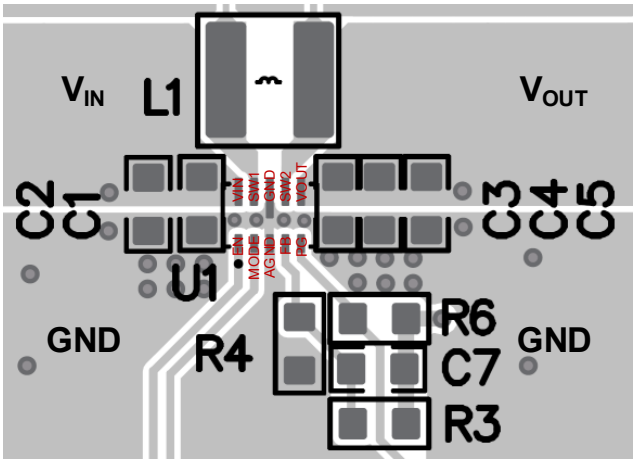


Figure 13. Recommended Top PCB Layout

Table 3. Components used for Characteristic Curves

Reference	Description	Part Number	Manufacturer
C_1	Capacitor, 10μF, 6.3V, 0603, ceramic	GRM155R60J106ME15	Murata
C_2, C_3	Capacitor, 22μF, 6.3V, 0603, ceramic	CL10A226MQ8NRNC	Samsung
L_1	Inductor, 0.47μH	744383560047HT	Wurth
U_1	Integrated circuit	SGM62117	SGMICRO

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

APRIL 2025 – REV.A.2 to REV.A.3	Page
Updated Features section	1

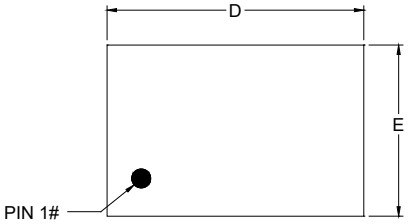
JANUARY 2025 – REV.A.1 to REV.A.2	Page
Updated Figure 1, 11, 12	1, 15, 16

AUGUST 2024 – REV.A to REV.A.1	Page
Added Output Voltage section	15

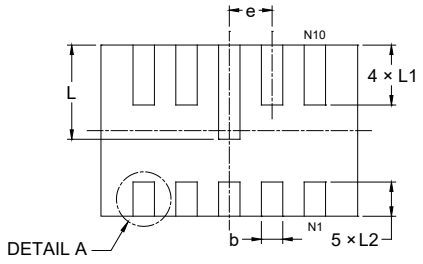
Changes from Original (JANUARY 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

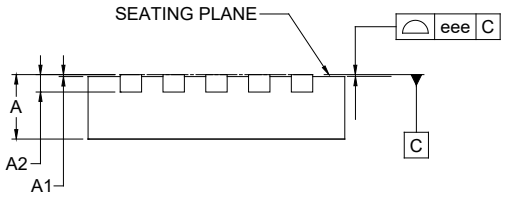
TDFN-3×2-10L



TOP VIEW

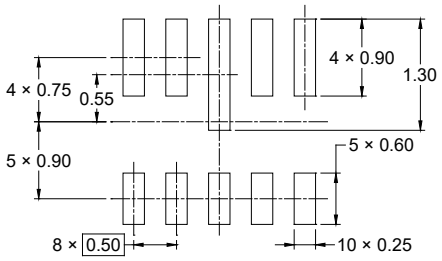


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



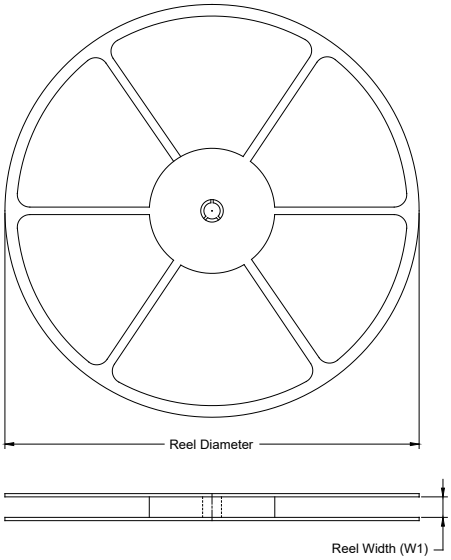
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	2.900	-	3.100
E	1.900	-	2.100
e	0.500 BSC		
L	1.000	-	1.200
L1	0.600	-	0.800
L2	0.300	-	0.500
eee	0.080		

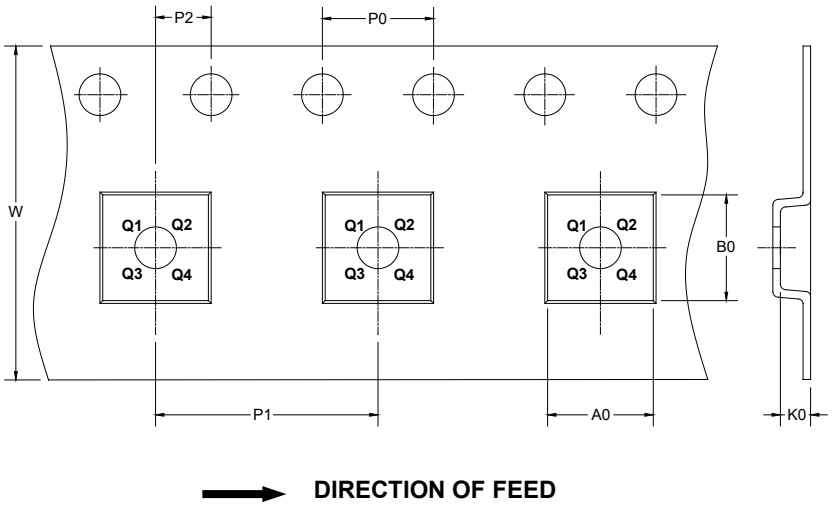
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



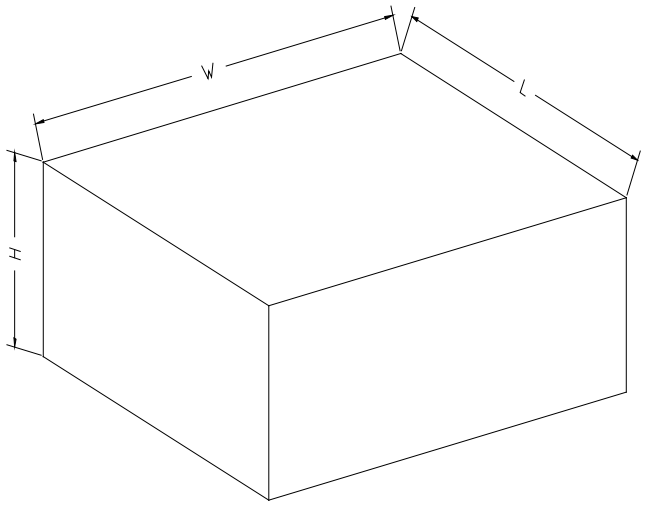
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×2-10L	7"	9.5	2.30	3.30	1.10	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002