SGM41573

I²C NVDC Buck-Boost Charge Controller for 1- to 4-Cell Battery

FEATURES

- 1- to 4-Cell Charging from a Variety of Input Types
  - 3.58V to 24V Input Operating Voltage Range
  - USB 2.0/3.0/3.1 (Type-C)/USB PD Input Current Support
  - Seamless Buck ↔ Buck-Boost ↔ Boost Transitions
  - Input Overload Protection (IDPM and VDPM Regulation)
- CPU Throttling, Power and Current Monitoring
  - Full nPROCHOT Profile
  - Input Current Monitoring
  - Battery Charge/Discharge Current Monitoring
  - System Power Monitoring
- Narrow Voltage DC (NVDC) Power Path Management
  - Instant-On with Depleted or No Battery
  - Battery Supplementation if Adapter is Fully Loaded
  - BATFET Ideal Diode Emulation in Supplement Mode
- Power-Up USB Port from Battery (USB OTG)
  - 3V to 20.56V Adjustable OTG Voltage with 8mV Resolution
  - Up to 6.35A Output Current Limit with 50mA Resolution
- Pass Through Mode (PTM) to Improve Efficiency
- V_{MIN} Active Protection (VAP) Mode
- VAP Supplements Battery from Input Caps for System Power Spikes (Battery-Only Conditions)
- Input Current Optimizer Maximizes Power Extraction
- 800kHz or 1.2MHz Selectable Switching Frequency
- I²C Interface for Flexible System Configuration
- Input Current Limit Setting Pin (without I²C)
- Integrated ADC for Voltage/Current/Power Monitoring
- Low Battery Quiescent Current
- High Accuracy
  - ±0.4% for Charge Voltage Regulation
  - ±2% for Input/Charge Current Regulation
  - ±2% for Input/Charge Current Monitor
  - ±5.8% for Power Monitor
- Safety
  - Thermal Shutdown
  - Input/System/Battery Over-Voltage Protection
  - Input/MOSFET/Inductor Over-Current Protection
- Available in a Green TQFN-4×4-32AL Package

APPLICATIONS

Bluetooth Speakers, Drones, IP Cameras, Detachable Power Supply

Portable Internet Devices and Accessory

Industrial and Medical Equipment

TYPICAL APPLICATION

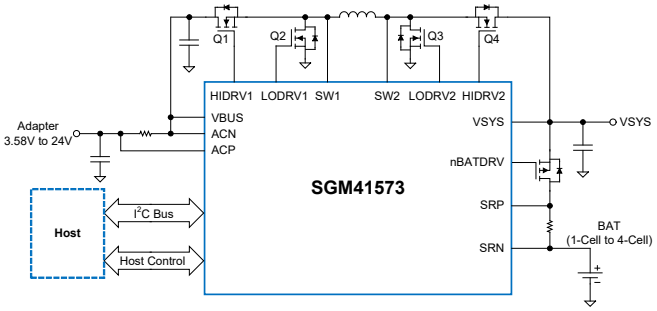


Figure 1. Typical Application Circuit

GENERAL DESCRIPTION

The SGM41573 is a synchronous Buck-Boost battery charge controller with NVDC power path management. It can provide high efficiency and low component count solution for 1-cell to 4-cell batteries charging applications.

The system is regulated slightly to be higher than the battery voltage, but not lower than the programmable system minimum voltage. Therefore, the system power is maintained even if the battery is completely depleted or removed. Dynamic power management (DPM) feature is also included that automatically reduces the charge current if the input current or voltage limit is reached. If the system load continues to increase after reduction of charge current down to zero, the battery enters the supplement mode and both adapter and battery power the system.

A wide range of input sources are supported for SGM41573, including traditional adapters, USB adapter and high voltage USB PD sources. The converter is configured as Buck, Boost or Buck-Boost during power-up, depending on the input source and battery conditions. The charger automatically switches among Buck, Boost and Buck-Boost without host control.

When the input source is absent, the SGM41573 can work in USB On-The-Go (OTG) mode to supply VBUS from battery. The OTG output voltage can be programmed from 3V to 20.56V with 8mV resolution. The slew rate of the output voltage transitions in OTG can be configured (by OTG current setting) to comply with the USB PD 3.0 PPS specifications.

If there is no external load on the USB OTG port and the system is powered by battery-only, the V_{MIN} Active Protection (VAP) feature is supported. In VAP, the VBUS voltage is charged up by the battery and the energy is stored in the input decoupling capacitors. When the system requires peak power spike, the charge stored on the input capacitor discharges to maintain the system voltage at minimum system voltage.

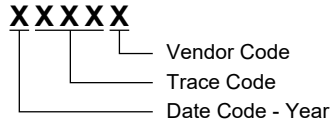
Adapter current, battery current and system power are monitored in SGM41573. When the system power is too high and exceeds available power from adapter and battery together, a flexibly programmed nPROCHOT pulse is asserted to inform CPU for throttle back.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41573	TQFN-4×4-32AL	-40℃ to +125℃	SGM41573XTSE32G/TR	SGM41573 XTSE32 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- SRN, SRP, ACN, ACP, VBUS, VSYS ..... -0.3V to 30V
- SW1, SW2 ..... -2V to 30V
- BTST1, BTST2, HIDRV1, HIDRV2, nBATDRV ... -0.3V to 36V
- LODRV1, LODRV2 (25ns) ..... -4V to 7V
- HIDRV1, HIDRV2 (25ns)..... -4V to 36V
- SW1, SW2 (25ns) ..... -4V to 30V
- SDA, SCL, REGN, CHRG_OK, OTG/VAP, ILIM_HIZ, VDDA, CELL_BATPRESZ, LODRV1, LODRV2, nPROCHOT, CMPIN, CMPOUT ..... -0.3V to 7V
- COMP1, COMP2 ..... -0.3V to 5.5V
- IADPT, IBAT, PSYS..... -0.3V to 3.6V

Differential Voltage Range
- BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2 ..... -0.3V to 7V
- SRP-SRN, ACP-ACN..... -0.5V to 0.5V

Package Thermal Resistance
- TQFN-4×4-32AL, θ_{JA}..... 36℃/W
- TQFN-4×4-32AL, θ_{JB}..... 8.1℃/W
- TQFN-4×4-32AL, $\theta_{JC\ (TOP)}$ ..... 24.1℃/W
- TQFN-4×4-32AL, $\theta_{JC\ (BOT)}$ ..... 1.6℃/W

Junction Temperature.....+150℃

Storage Temperature Range .....-65℃ to +150℃

Lead Temperature (Soldering, 10s).....+260℃

ESD Susceptibility (1) (2)

HBM.....±5000V

CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

RECOMMENDED OPERATING CONDITIONS

Voltage Range (with Respect to GND)
- ACN, ACP, VBUS..... 0V to 24V
- SRN, SRP, VSYS ..... 0V to 19.2V
- SW1, SW2..... -2V to 24V
- BTST1, BTST2, HIDRV1, HIDRV2, nBATDRV..... 0V to 30V
- SDA, SCL, CHRG_OK, COMP1, COMP2, CMPIN, CMPOUT, nPROCHOT ..... 0V to 5.3V
- CELL_BATPRESZ, ILIM_HIZ, LODRV1, LODRV2, VDDA, REGN ..... 0V to 6V
- IADPT, IBAT, PSYS ..... 0V to 3.3V

Differential Voltage Range
- BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2 ..... 0V to 6V
- SRP-SRN, ACP-ACN ..... -0.5V to 0.5V

Operating Junction Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

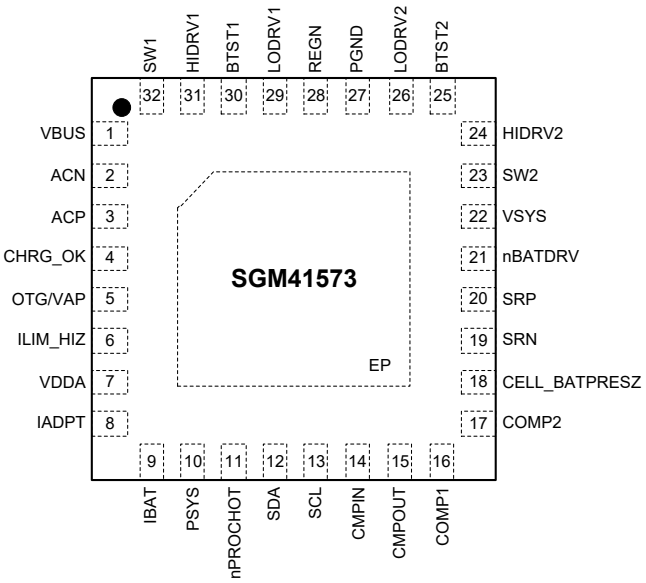
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

PIN CONFIGURATION

(TOP VIEW)



TQFN-4×4-32AL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	VBUS	P	Charger Input. Place an RC low pass filter on this pin (R = 1Ω and C ≥ 0.47μF).
2	ACN	P	Negative Terminal of the Input Current Sense Resistor. Place an RC low pass filter between this pin and the sense resistor.
3	ACP	P	Positive Terminal of the Input Current Sense Resistor. Place an RC low pass filter between this pin and the sense resistor.
4	CHRG_OK	O	Active High Open-Drain Good Power Source Status Output. Place a 10kΩ resistor between this pin and pull-up rail. CHRG_OK goes high with no fault (SYS short latch off, SYSOVP, BATOC, ACOC, force latch off, and thermal shutdown) when VBUS voltage rises above V_{VBUS_CONVEN} or falls below V_{ACOV}. CHRG_OK goes low when VBUS falls below V_{VBUS_CONVEN} or rises above V_{ACOV} or when above fault occurs.
5	OTG/VAP	I	OTG or VAP Modes Enable Input (Active High). OTG mode enable: OTG_VAP_MODE bit = 1, EN_OTG bit = 1 and pull this pin to high. VAP mode enable: OTG_VAP_MODE bit = 0, and pull this pin to high.
6	ILIM_HIZ	I	Input Current Limit Setting Input. Connect this pin to a resistor divider between supply and ground to set the target input current limit I_{DPM} using the following equation: $V_{ILIM\_HIZ} = 1V + 40 \times I_{DPM} \times R_{AC}$ The actual input current limit is the lower setting of ILIM_HIZ pin and IIN_HOST register. The device enters HIZ mode when V_{ILIM_HIZ} < 0.6V, and exits HIZ mode when V_{ILIM_HIZ} > 0.83V.
7	VDDA	P	Internal Reference Bias. Place a 10Ω resistor from REGN to this pin, and place a 1μF ceramic capacitor from this pin to ground.
8	IADPT	O	Adapter Current Monitoring Output. V_{IADPT} = 20 or 40 × (V_{ACP} - V_{ACN}) and 20V/V or 40V/V can be selected in the IADPT_GAIN bit. Place a resistor from this pin to ground according to **Inductance Detection through IADPT Pin** section. The resistor is 137kΩ when L = 2.2μH. Connect a 100pF or less ceramic decoupling capacitor from this pin to ground. IADPT output voltage is clamped below 3.2V.
9	IBAT	O	Battery Current Monitoring Output. The charge current is monitored as V_{IBAT} = 8 or 16 × (V_{SRP} - V_{SRN}), and the discharge current is monitored as V_{IBAT} = 8 or 16 × (V_{SRN} - V_{SRP}). 8V/V or 16V/V can be selected in the IBAT_GAIN bit. Connect a 100pF or less ceramic decoupling capacitor from this pin to ground. IBAT pin can be left floating if not in use and its output voltage is clamped below 3.3V.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
10	PSYS	O	System Power Monitoring Output (Current Mode). The output current of this pin is proportional to the total power from the adapter and the battery refers to **High-Accuracy Power Sense Amplifier (PSYS)** section. The gain can be selected by I²C. Connect a resistor between this pin and ground to generate output voltage. PSYS pin can be left floating if not in use. And its output voltage is clamped below 3.3V.
11	nPROCHOT	O	Active Low Open-Drain Processor Hot Indicator Output. The adapter input current, battery discharge current and system voltage are monitored, and a pulse is asserted if any event in the nPROCHOT profile is triggered. The minimum pulse width is adjustable in PROCHOT_WIDTH[1:0] bits.
12	SDA	I/O	I²C Data Signal. Use a 10kΩ pull-up to the logic high rail.
13	SCL	I	I²C Clock Signal. Use a 10kΩ pull-up to the logic high rail.
14	CMPIN	I	Independent Comparator Input. The voltage sensed on this pin is compared with internal reference by the independent comparator, and the output of comparator is on CMPOUT pin. The internal reference, output polarity and deglitch time are all selectable in the I²C host. When CMP_POL bit = 1, the internal hysteresis is determined by the resistor between CMPIN and CMPOUT. When CMP_POL bit = 0, the internal hysteresis is 110mV. Connect this pin to ground if the independent comparator is not in use.
15	CMPOUT	O	Open-Drain Independent Comparator Output. Place a resistor between this pin and pull-up supply rail.
16	COMP1	I	Buck-Boost Compensation Pin 1. Refer to Figure 2 for the compensation network.
17	COMP2	I	Buck-Boost Compensation Pin 2. Refer to Figure 2 for the compensation network.
18	CELL_BATPRESZ	I	Battery Cell Selection Input. This pin is biased from VDDA, and sets the SYSOVP thresholds (5V for 1-cell, 12V for 2-cell, and 19.4V for 3-cell/4-cell). When the voltage on this pin is pulled below $V_{CELL\_BATPRESZ\_FALL}$, it indicates battery removal. The device exits LEARN mode, the charge current goes back to 0. And the MaxChargeVoltage/MinSystemVoltage register goes to default.
19	SRN	P	Negative Input of the Charge Current Sense Resistor. This pin also senses the battery voltage. Place an optional 0.1μF ceramic capacitor from this pin to GND for common-mode noise filtering. Place a 0.1μF ceramic capacitor from SRP to SRN for differential mode noise filtering.
20	SRP	P	Positive Input of the Charge Current Sense Resistor. Place an optional 0.1μF ceramic capacitor from this pin to GND for common-mode noise filtering. Place a 0.1μF ceramic capacitor from SRP to SRN for differential mode noise filtering.
21	nBATDRV	O	P-Channel BATFET Gate Driver Output. It is shorted to VSYS for turning off the BATFET and goes 11V below VSYS for fully on.
22	VSYS	P	System Voltage Sensing.
23	SW2	P	Boost Mode Switching Node. Connect it to the source of the Boost mode high-side N-channel MOSFET (Q4).
24	HIDRV2	O	Boost Mode High-side N-Channel MOSFET (Q4) Driver. Connect it to the gate of Q4.
25	BTST2	P	Boost Mode High-side N-Channel MOSFET (Q4) Driver Power Supply. Place a 47nF capacitor between SW2 and BTST2. It is internally connected to the boost-strap diode cathode.
26	LODRV2	O	Boost Mode Low-side N-Channel MOSFET (Q3) Driver. Connect it to the gate of Q3.
27	PGND	GND	Power Ground.
28	REGN	P	5.6V LDO Output. It is supplied from VBUS or VSYS and the LDO is active when VBUS voltage is above V_{VBUS_CONVEN}. A 2.2μF or 3.3μF ceramic capacitor is recommended between this pin and PGND.
29	LODRV1	O	Buck Mode Low-side N-Channel MOSFET (Q2) Driver. Connect it to the gate of Q2.
30	BTST1	P	Buck Mode High-side N-Channel MOSFET (Q1) Driver Power Supply. Place a 47nF capacitor between SW1 and BTST1. It is internally connected to the boost-strap diode cathode.
31	HIDRV1	O	Buck Mode High-side N-Channel MOSFET (Q1) Driver. Connect it to the gate of Q1.
32	SW1	P	Buck Mode Switching Node. Connect it to the source of the Buck mode high-side N-channel MOSFET (Q1).
Exposed Pad	EP	–	Thermal Pad. It is the thermal pad to conduct heat from the device. Tie it externally to the PCB power ground plane. Thermal vias under the pad are needed to conduct the heat to the PCB power ground planes.

NOTE: I = input, O = output, I/O = input or output, P = power.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Operating Range	V_{INPUT_OP}			3.58		24	V
Regulation Accuracy							
Max System Voltage Regulation							
System Voltage Regulation	V_{SYSMAX_RNG}	Charge disabled, measured on V_{SYS}		1.024		19.2	V
System Voltage Regulation Accuracy	V_{SYSMAX_ACC}	Charge disabled	MaxChargeVoltage register = 0x41A0 (16.800V)		V_{SRN} + 160mV		V
				-1.5		1.5	%
			MaxChargeVoltage register = 0x3138 (12.600V)		V_{SRN} + 160mV		V
				-1.5		1.5	%
			MaxChargeVoltage register = 0x20D0 (8.400V)		V_{SRN} + 160mV		V
				-2		2	%
			MaxChargeVoltage register = 0x1068 (4.200V)		V_{SRN} + 160mV		V
				-3		3	%
Minimum System Voltage Regulation							
System Voltage Regulation	V_{SYSMIN_RNG}	Measured on V_{SYS}		1.024		16.128	V
Minimum System Voltage Regulation Accuracy	$V_{SYSMIN\_REG\_ACC}$	VBAT below MinSystemVoltage register setting	MinSystemVoltage register = 0x3000		12.288		V
				-2.0		1.0	%
			MinSystemVoltage register = 0x2400		9.216		V
				-2.0		1.0	%
			MinSystemVoltage register = 0x1800		6.144		V
				-2.5		1.5	%
			MinSystemVoltage register = 0x0E00		3.584		V
				-3.5		2.0	%
Charge Voltage Regulation							
Battery Voltage Regulation	V_{BAT_RNG}			1.024		19.2	V
Battery Voltage Regulation Accuracy	$V_{BAT\_REG\_ACC}$	Charge enabled (0℃ to +85℃)	MaxChargeVoltage register = 0x41A0		16.8		V
				-0.6		0.4	%
			MaxChargeVoltage register = 0x3138		12.6		V
				-0.5		0.4	%
			MaxChargeVoltage register = 0x20D0		8.4		V
				-0.7		0.6	%
			MaxChargeVoltage register = 0x1068		4.2		V
				-1.3		1.3	%

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Charge Current Regulation in Fast Charge							
Charge Current Regulation Differential Voltage Range	$V_{IREG\_CHG\_RNG}$	$V_{IREG\_CHG} = V_{SRP} - V_{SRN}$		0		81.28	mV
Charge Current Regulation Initial Accuracy with 10mΩ Sensing Resistor	$I_{CHRG\_REG\_ACC}$	VBAT above MinSystemVoltage register setting (0℃ to +85℃)	ChargeCurrent register = 0x1000		4096		mA
				-3		2	%
			ChargeCurrent register = 0x0800		2048		mA
				-5		4	%
			ChargeCurrent register = 0x0400		1024		mA
				-9		7	%
			ChargeCurrent register = 0x0200		512		mA
				-18		13	%
Charge Current Regulation in LDO Mode							
Pre-Charge Current Clamp	I_{CLAMP}	2-cell to 4-cell			384		mA
		1-cell, V_{SRN} < 3V			384		mA
		1-cell, 3V < V_{SRN} < V_{SYSMIN}			2		A
Pre-Charge Current Regulation Initial Accuracy with 10mΩ SRP/SRN Series Resistor	$I_{PRECHRG\_REG\_ACC}$	VBAT below MinSystemVoltage register setting (0℃ to +85℃)	ChargeCurrent register = 0x0180		384		mA
			1-cell to 4-cell	-17		17	%
			ChargeCurrent register = 0x0100		256		mA
			1-cell to 4-cell	-24		24	%
			ChargeCurrent register = 0x00C0		192		mA
			1-cell to 4-cell	-32		32	%
			ChargeCurrent register = 0x0080		128		mA
SRP, SRN Leakage Current Mismatch	$I_{LEAK\_SRP\_SRN}$	0℃ to +85℃		-13		13	μA
Input Current Regulation							
Input Current Regulation Differential Voltage Range	$V_{IREG\_DPM\_RNG}$	$V_{IREG\_DPM} = V_{ACP} - V_{ACN}$		0.5		63.5	mV
Input Current Regulation Accuracy with 10mΩ ACP/ACN Series Resistor	$I_{DPM\_REG\_ACC}$	IIN_HOST register = 0x5000		3700	3800	3950	mA
		IIN_HOST register = 0x3C00		2740	2850	2990	
		IIN_HOST register = 0x1E00		1300	1425	1550	
		IIN_HOST register = 0x0A00		340	475	590	
ACP, ACN Leakage Current Mismatch	$I_{LEAK\_ACP\_\_ACN}$			-14		10	μA
Voltage Range for Input Current Regulation (ILIM_HIZ Pin)	$V_{IREG\_DPM\_RNG\_ILIM}$			1.15		4	V
Input Current Regulation Accuracy on ILIM_HIZ Pin with 10mΩ ACP/ACN Series Resistor	$I_{DPM\_REG\_ACC\_ILIM}$	V_{ILIM_HIZ} = 1V + 40 × I_{DPM} × R_{AC}	V_{ILIM_HIZ} = 2.6V	3780	4000	4200	mA
			V_{ILIM_HIZ} = 2.2V	2780	3000	3200	
			V_{ILIM_HIZ} = 1.6V	1280	1500	1660	
			V_{ILIM_HIZ} = 1.2V	280	500	660	
ILIM_HIZ Pin Leakage Current	I_{LEAK_ILIM}			-1		1	μA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Regulation						
Input Voltage Regulation Range	$V_{IREG\_DPM\_RNG}$	Voltage on VBUS	3.2		19.52	V
Input Voltage Regulation Accuracy	$V_{DPM\_REG\_ACC}$	InputVoltage register = 0x3C80		18688		mV
			-2		1	%
		InputVoltage register = 0x1E00		10880		mV
			-2.5		1	%
		InputVoltage register = 0x0500		4480		mV
			-3.5		2	%
OTG Current Regulation						
OTG Output Current Regulation Differential Voltage Range	$V_{IOTG\_REG\_RNG}$	$V_{IOTG\_REG} = V_{ACP} - V_{ACN}$	0		63.5	mV
OTG Output Current Regulation Accuracy with 50mA LSB and 10mΩ ACP/ACN Series Resistor	I_{OTG_ACC}	OTGCurrent register = 0x3C00	2800	3000	3160	mA
		OTGCurrent register = 0x1E00	1300	1500	1680	
		OTGCurrent register = 0x0A00	310	500	670	
OTG Voltage Regulation						
OTG Voltage Regulation Range	$V_{OTG\_REG\_RNG}$	Voltage on VBUS	3		20.56	V
OTG Voltage Regulation Accuracy	$V_{OTG\_REG\_ACC}$	OTGVoltage register = 0x2490, OTG_RANGE_LOW = 0		20.000		V
			-1.5		1	%
		OTGVoltage register = 0x1770, OTG_RANGE_LOW = 1		12.000		V
			-1.5		1.5	%
		OTGVoltage register = 0x09C4, OTG_RANGE_LOW = 1		5.000		V
			-2		3.5	%
Reference and Buffer						
REGN Regulator						
REGN Regulator Voltage (0mA to 60mA)	V_{REGN_REG}	V_{VBUS} = 10V	5.36	5.64	5.9	V
REGN Voltage in Drop Out Mode	$V_{DROPOUT}$	V_{VBUS} = 5V, I_{LOAD} = 20mA	4.6	4.8	5	V
REGN Current Limit when Converter is Enabled	$I_{REGN\_LIM\_Charging}$	V_{VBUS} = 10V, force V_{REGN} = 4V	80	100		mA
REGN Output Capacitor Required for Stability	C_{REGN}	I_{LOAD} = 100μA to 50mA	2.2			μF
VDDA Input Capacitor Required for Stability	C_{VDDA}	I_{LOAD} = 100μA to 50mA	1			μF

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current							
System Powered by Battery, BATFET on, I_{SRN} + I_{SRP} + I_{SW2} + I_{BTST2} + I_{SW1} + I_{BTST1} + I_{ACP} + I_{ACN} + I_{VBUS} + I_{VSYS}	$I_{BAT\_BATFET\_ON}$	V_{BAT} = 18V, EN_LWPWR = 1, in low power mode			21	36	μA
		V_{BAT} = 18V, EN_LWPWR = 1, EN_PROCHOT_LPWR = 1, REGN off			180	260	
		V_{BAT} = 18V, EN_LWPWR = 0, EN_PSYS = 0, REGN on, PSYS disabled			1100	1410	
		V_{BAT} = 18V, EN_LWPWR = 0, EN_PSYS = 1, REGN on, PSYS enabled			1200	1510	
Input Current during PSM in Buck Mode, No Load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST1} + I_{SW2} + I_{BTST2}	$I_{AC\_SW\_LIGHT\_Buck}$	V_{IN} = 20V, V_{BAT} = 12.6V, 3-cell, EN_OOA = 0, MOSFET Q_G = 8nC			2.5		mA
Input Current during PSM in Boost Mode, No Load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST1} + I_{SW2} + I_{BTST2}	$I_{AC\_SW\_LIGHT\_Boost}$	V_{IN} = 5V, V_{BAT} = 8.4V, 2-cell, EN_OOA = 0, MOSFET Q_G = 8nC			6.7		mA
Input Current during PSM in Buck-Boost Mode, No Load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST1} + I_{SW2} + I_{BTST2}	$I_{AC\_SW\_LIGHT\_BuckBoost}$	V_{IN} = 12V, V_{BAT} = 12V, EN_OOA = 0, MOSFET Q_G = 8nC			3.3		mA
Quiescent Current during PSM in OTG Mode, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST1} + I_{SW2} + I_{BTST2}	$I_{OTG\_STANDBY}$	V_{BAT} = 8.4V, EN_OOA = 0, 800kHz switching frequency, MOSFET Q_G = 8nC	V_{VBUS} = 5V		3.3		mA
			V_{VBUS} = 12V		3.6		
			V_{VBUS} = 20V		4		
Input Common Mode Range	V_{ACP/N_OP}	Voltage on ACP/ACN		3.8		24	V
IADPT Output Clamp Voltage	V_{IADPT_CLAMP}			3.07	3.2	3.3	V
IADPT Output Current	I_{IADPT}					1	mA
Input Current Sensing Gain	A_{IADPT}	$V_{IADPT}/V_{(ACP-ACN)}$	IADPT_GAIN = 0		20		V/V
			IADPT_GAIN = 1		40		
Input Current Monitor Accuracy	V_{IADPT_ACC}	$V_{(ACP-ACN)}$ = 40.96mV, IADPT_GAIN = 1		-2.5		2.5	%
		$V_{(ACP-ACN)}$ = 20.48mV, IADPT_GAIN = 1		-4		4	
		$V_{(ACP-ACN)}$ = 10.24mV, IADPT_GAIN = 1		-7.5		7.5	
		$V_{(ACP-ACN)}$ = 5.12mV, IADPT_GAIN = 1		-15		15	
Maximum Capacitance on IADPT Pin	C_{IADPT_MAX}					100	pF
Battery Common Mode Range	V_{SRP/N_OP}	Voltage on SRP/SRN		2.5		18	V
IBAT Output Clamp Voltage	V_{IBAT_CLAMP}			2.93	3.27	3.6	V
IBAT Output Current	I_{IBAT}					1	mA
Charge and Discharge Current Sensing Gain on IBAT Pin	A_{IBAT}	$V_{IBAT}/V_{(SRN-SRP)}$	IBAT_GAIN = 0		8		V/V
			IBAT_GAIN = 1		16		
Charge Current Monitor Accuracy on IBAT Pin	$V_{IBAT\_CHG\_ACC}$	$V_{(SRP-SRN)}$ = 40.96mV, IBAT_GAIN = 1		-2		2	%
		$V_{(SRP-SRN)}$ = 20.48mV, IBAT_GAIN = 1		-4		4	
		$V_{(SRP-SRN)}$ = 10.24mV, IBAT_GAIN = 1		-7.3		7.3	
		$V_{(SRP-SRN)}$ = 5.12mV, IBAT_GAIN = 1		-15		15	
Maximum Capacitance on IBAT Pin	C_{IBAT_MAX}					100	pF

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Power Sense Amplifier						
PSYS Output Voltage Range	V_{PSYS}		0		3.3	V
PSYS Output Current	I_{PSYS}		0		160	μA
PSYS System Gain	A_{PSYS}	$V_{PSYS}/(P_{IN}+P_{BAT})$, PSYS_RATIO = 1		1		μA/W
PSYS Gain Accuracy	V_{PSYS_ACC}	Adapter only with system power = 19.5V/45W, PSYS_RATIO = 1, T_J = -40℃ to +85℃	-5.8		7	%
		Battery-only with system power = 11V/44W, PSYS_RATIO = 1, T_J = -40℃ to +85℃	-6.6		6.2	
PSYS Clamp Voltage	V_{PSYS_CLAMP}		3		3.3	V
Comparator						
VBUS Under-Voltage Lockout Comparator						
VBUS Under-Voltage Rising Threshold	V_{VBUS_UVLOZ}	VBUS rising	2.35	2.55	2.75	V
VBUS Under-Voltage Falling Threshold	V_{VBUS_UVLO}	VBUS falling	2.21	2.39	2.57	V
VBUS Under-Voltage Hysteresis	$V_{VBUS\_UVLO\_HYST}$			160		mV
VBUS Converter Enable Rising Threshold	V_{VBUS_CONVEN}	VBUS rising	3.3	3.58	3.9	V
VBUS Converter Enable Falling Threshold	$V_{VBUS\_CONVENZ}$	VBUS falling	2.9	3.2	3.5	V
VBUS Converter Enable Hysteresis	$V_{VBUS\_CONVEN\_HYST}$			380		mV
Battery Under-Voltage Lockout Comparator						
VBAT Under-Voltage Rising Threshold	V_{VBAT_UVLOZ}	V_{SRN} rising, measured on V_{SYS}	2.36	2.56	2.76	V
VBAT Under-Voltage Falling Threshold	V_{VBAT_UVLO}	V_{SRN} falling, measured on V_{SYS}	2.2	2.4	2.6	V
VBAT Under-Voltage Hysteresis	$V_{VBAT\_UVLO\_HYST}$			160		mV
VBAT OTG Enable Rising Threshold	V_{VBAT_OTGEN}	V_{SRN} rising	3.43	3.58	3.73	V
VBAT OTG Enable Falling Threshold	V_{VBAT_OTGENZ}	V_{SRN} falling	2.2	2.35	2.5	V
VBAT OTG Enable Hysteresis	$V_{VBAT\_OTGEN\_HYST}$			1230		mV
VBUS Under-Voltage Comparator (OTG Mode)						
VBUS Under-Voltage Falling Threshold	$V_{VBUS\_OTG\_UV}$	As percentage of OTGVoltage register		85		%
VBUS Time Under-Voltage Deglitch	$t_{VBUS\_OTG\_UV}$			7		ms
VBUS Over-Voltage Comparator (OTG Mode)						
VBUS Over-Voltage Rising Threshold	$V_{VBUS\_OTG\_OV}$	As percentage of OTGVoltage register		110		%
VBUS Time Over-Voltage Deglitch	$t_{VBUS\_OTG\_OV}$			10		ms
Pre-Charge to Fast Charge Transition						
LDO Mode to Fast Charge Mode Threshold	$V_{BAT\_SYSMIN\_RISE}$	As percentage of MinSystemVoltage register; V_{SRN} rising	97.4	100	102.4	%
	$V_{BAT\_SYSMIN\_FALL}$	As percentage of MinSystemVoltage register; V_{SRN} falling		97.5		
Fast Charge Mode to LDO Mode Threshold Hysteresis	$V_{BAT\_SYSMIN\_HYST}$	As percentage of MinSystemVoltage register		2.5		%

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Battery LOWV Comparator (Pre-Charge to Fast Charge Threshold for 1-Cell)							
BATLOWV Falling Threshold	V_{BATLV_FALL}	1-cell			2.78		V
BATLOWV Rising Threshold	V_{BATLV_RISE}				3		V
BATLOWV Hysteresis	V_{BATLV_HYST}				220		mV
Input Over-Voltage Comparator (ACOV)							
VBUS Over-Voltage Rising Threshold	V_{ACOV_RISE}	VBUS rising		25.2	25.7	26.3	V
VBUS Over-Voltage Falling Threshold	V_{ACOV_FALL}	VBUS falling		22.7	23.8	25	V
VBUS Over-Voltage Hysteresis	V_{ACOV_HYST}				1.9		V
VBUS Deglitch Over-Voltage Rising	$t_{ACOV\_RISE\_DEG}$	VBUS converter rising to stop converter			100		μs
VBUS Deglitch Over-Voltage Falling	$t_{ACOV\_FALL\_DEG}$	VBUS converter falling to start converter			1		ms
Input Over-Current Comparator (ACOC)							
ACP to ACN Rising Threshold, w.r.t. ILIM2 in ILIM2_VTH[4:0] Bits	V_{ACOC}	Voltage across input sense resistor rising, ACOC_VTH = 1		1.8	2	2.2	
Measure between ACP and ACN	V_{ACOC_FLOOR}	Set IDPM to minimum		45	50	56	mV
Measure between ACP and ACN	$V_{ACOC\_CEILING}$	Set IDPM to maximum		173	180	186	mV
Rising Deglitch Time	$t_{ACOC\_DEG\_RISE}$	Deglitch time to trigger ACOC			250		μs
Relax Time	t_{ACOC_RELAX}	Relax time before converter starts again			250		ms
System Over-Voltage Comparator (SYSOVP)							
System Over-Voltage Rising Threshold to Turn Off Converter	V_{SYSOVP_RISE}	1-cell		4.82	4.98	5.15	V
		2-cell		11.7	11.93	12.2	
		3-cell, 4-cell		19	19.35	20	
System Over-Voltage Falling Threshold	V_{SYSOVP_FALL}	1-cell			4.76		V
		2-cell			11.4		
		3-cell, 4-cell			18.8		
Discharge Current when SYSOVP Stop Switching is Triggered	I_{SYSOVP}	On VSYS pin			18		mA
BAT Over-Voltage Comparator (BATOVP)							
Over-Voltage Rising Threshold	V_{BATOVP_RISE}	As percentage of V_{BAT_REG} in MaxChargeVoltage register	1-cell, 4.2V	102.4	105.3	108.3	%
			2-cell to 4-cell	102.8	104	106.3	
Over-Voltage Falling Threshold	V_{BATOVP_FALL}	As percentage of V_{BAT_REG} in MaxChargeVoltage register	1-cell	98.8	101.8	104.9	%
			2-cell to 4-cell	100.2	102	103.5	
Over-Voltage Hysteresis	V_{BATOVP_HYST}	As percentage of V_{BAT_REG} in MaxChargeVoltage register	1-cell		3.5		%
			2-cell to 4-cell		3		
Discharge Current during BATOVP	I_{BATOVP}	On VSYS pin			18		mA
Over-Voltage Rising Deglitch to Turn Off BATDRV to Disable Charge	t_{BATOVP_RISE}				20		ms
Converter Over-Current Comparator (Q2)							
Converter Over-Current Limit	$V_{OCP\_limit\_Q2}$	Q2_OCP = 1			150		mV
		Q2_OCP = 0			225		
System Short or SRN < 2.4V	$V_{OCP\_limit\_SYS\ SHORT\_Q2}$	Q2_OCP = 1			45		mV
		Q2_OCP = 0			65		

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Converter Over-Current Comparator (ACX)						
Converter Over-Current Limit	$V_{OCP\_limit\_ACX}$	ACX_OCP = 1		150		mV
		ACX_OCP = 0		280		
System Short or SRN < 2.4V	$V_{OCP\_limit\_SYS\ SHORT\_ACX}$	ACX_OCP = 1		90		mV
		ACX_OCP = 0		150		
Thermal Shutdown Comparator						
Thermal Shutdown Rising Temperature	T_{SHUT_RISE}	Temperature increasing		155		℃
Thermal Shutdown Falling Temperature	T_{SHUT_FALL}	Temperature reducing		135		℃
Thermal Shutdown Hysteresis	T_{SHUT_HYS}			20		℃
Thermal Deglitch Shutdown Rising	T_{SHUT_RDEG}			100		μs
Thermal Deglitch Shutdown Falling	T_{SHUT_FHYS}			12		ms
VSYS PROCHOT Comparator						
VSYS_TH1 Comparator Falling Threshold	V_{SYS_TH1}	VSYS_TH1[3:0] = 0111, 2-cell to 4-cell		6.52		V
		VSYS_TH1[3:0] = 0100, 1-cell		3.55		
VSYS_TH2 Comparator Falling Threshold	V_{SYS_TH2}	VSYS_TH2[1:0] = 10, 2-cell to 4-cell		6.43		V
		VSYS_TH2[1:0] = 10, 1-cell		3.46		
V_{SYS} Falling Deglitch for Throttling	$t_{SYS\_PRO\_falling\_DEG}$			4		μs
ICRIT PROCHOT Comparator						
Input Current Rising Threshold for Throttling as 10% above ILIM2 (ILIM2_VTH[4:0] Bits)	V_{ICRIT_PRO}	Only when ILIM2 setting is higher than 2A	104.5	110	117.5	%
INOM PROCHOT Comparator						
INOM Rising Threshold as 10% above IIN (IIN_HOST Register)	V_{INOM_PRO}		104.5	110	116.5	%
IDCHG PROCHOT Comparator						
IDCHG Threshold for Throttling for IDSCHG of 6A	V_{IDCHG_PRO}	IDCHG_VTH[5:0] = 001100		6144		mA
			95.7		104	%
Independent Comparator						
Independent Comparator Threshold	V_{INDEP_CMP}	CMP_REF = 1, CMPIN falling	1.17	1.19	1.23	V
		CMP_REF = 0, CMPIN falling	2.25	2.28	2.33	
Independent Comparator Hysteresis	$V_{INDEP\_CMP\_HYS}$	CMP_POL = 0, CMPIN falling		110		mV
Power MOSFET Driver						
PWM Oscillator and Ramp						
PWM Switching Frequency	f_{SW}	PWM_FREQ = 0	1020	1200	1320	kHz
		PWM_FREQ = 1	710	800	910	
BATFET Gate Driver (BATDRV)						
Gate Drive Voltage on BATFET	V_{BATDRV_ON}		9.2	10.7	12.2	V
Drain-Source Voltage on BATFET during Ideal Diode Operation	V_{BATDRV_DIODE}			30		mV
Measured by Sourcing 10μA Current to BATDRV	R_{BATDRV_ON}		1.9	4.1	6.4	kΩ
Measured by Sinking 10μA Current from BATDRV	R_{BATDRV_OFF}			1.3	2	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM High-side Driver (HIDRV Q1)						
High-side Driver (HSD) Turn-On Resistance	$R_{DS\_HI\_ON\_Q1}$	V_{BTST1} - V_{SW1} = 5V		5		Ω
High-side Driver Turn-Off Resistance	$R_{DS\_HI\_OFF\_Q1}$	V_{BTST1} - V_{SW1} = 5V		1.1	2	Ω
Bootstrap Refresh Comparator Falling Threshold Voltage	$V_{BTST1\_REFRESH}$	V_{BTST1} - V_{SW1} when low-side refresh pulse is requested	2.7	3.2	3.7	V
PWM High-side Driver (HIDRV Q4)						
High-side Driver (HSD) Turn-On Resistance	$R_{DS\_HI\_ON\_Q4}$	V_{BTST2} - V_{SW2} = 5V		4.85		Ω
High-side Driver Turn-Off Resistance	$R_{DS\_HI\_OFF\_Q4}$	V_{BTST2} - V_{SW2} = 5V		1.2	2.1	Ω
Bootstrap Refresh Comparator Falling Threshold Voltage	$V_{BTST2\_REFRESH}$	V_{BTST2} - V_{SW2} when low-side refresh pulse is requested	2.7	3.2	3.7	V
PWM Low-side Driver (LODRV Q2)						
Low-side Driver (LSD) Turn-On Resistance	$R_{DS\_LO\_ON\_Q2}$	V_{BTST1} - V_{SW1} = 5.5V		4.6		Ω
Low-side Driver Turn-Off Resistance	$R_{DS\_LO\_OFF\_Q2}$	V_{BTST1} - V_{SW1} = 5.5V		1.3	2.3	Ω
PWM Low-side Driver (LODRV Q3)						
Low-side Driver (LSD) Turn-On Resistance	$R_{DS\_LO\_ON\_Q3}$	V_{BTST2} - V_{SW2} = 5.5V		5.1		Ω
Low-side Driver Turn-Off Resistance	$R_{DS\_LO\_OFF\_Q3}$	V_{BTST2} - V_{SW2} = 5.5V		1.25	2.2	Ω
Internal Soft-Start during Charge Enable						
Soft-Start Step Size	SSSTEP_DAC			64		mA
Soft-Start Step Time	t_{SSSTEP_DAC}			10		μs
Integrated BTST Diode (D1)						
Forward Bias Voltage	V_{F_D1}	I_F = 20mA at +25℃, lodrv1 turn on		0.05		V
Reverse Breakdown Voltage	V_{R_D1}	I_R = 2μA at +25℃			20	V
Integrated BTST Diode (D2)						
Forward Bias Voltage	V_{F_D2}	I_F = 20mA at +25℃, lodrv2 turn on		0.05		V
Reverse Breakdown Voltage	V_{R_D2}	I_R = 2μA at +25℃			20	V
Interface						
Logic Input (SDA, SCL, OTG/VAP)						
Input Low Threshold	V_{IN_LO}	I²C			0.4	V
Input High Threshold	V_{IN_HI}	I²C	1.4			V
Logic Output Open-Drain (SDA, CHRG_OK, CMPOUT, PROCHOT)						
Output Saturation Voltage	V_{OUT_LO}	5mA drain current			0.2	V
Leakage Current	I_{OUT_LEAK}	Connected to 7V	-1		1	μA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input (ILIM_HIZ)						
Voltage to Get out of HIZ Mode	V_{HIZ_HIGH}	ILIM_HIZ pin rising	0.83			V
Voltage to Enable HIZ Mode	V_{HIZ_LOW}	ILIM_HIZ pin falling			0.6	V
Analog Input (CELL_BATPRESZ)						
4-Cell Configuration	V_{CELL_4S}	As percentage of REGN	76	80		%
3-Cell Configuration	V_{CELL_3S}	As percentage of REGN	56	60	74	%
2-Cell Configuration	V_{CELL_2S}	As percentage of REGN	41	45	54	%
1-Cell Configuration	V_{CELL_1S}	As percentage of REGN	19.5	30	39	%
Battery is Present	$V_{CELL\_BATPRESZ\_RISE}$	CELL_BATPRESZ rising	19			%
Battery is Removed	$V_{CELL\_BATPRESZ\_FALL}$	CELL_BATPRESZ falling			15	%

TIMING REQUIREMENTS

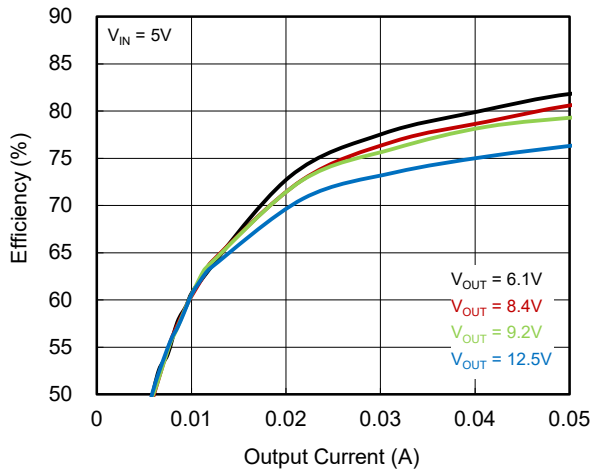
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C Timing Characteristics						
SCLK/SDATA Rise Time	t_R				300	ns
SCLK/SDATA Fall Time	t_F				300	ns
SCLK Pulse Width High	$t_{W(H)}$		0.6		50	μs
SCLK Pulse Width Low	$t_{W(L)}$		1.3			μs
Setup Time for START Condition	$t_{SU(STA)}$		0.6			μs
START Condition Hold Time after which First Clock Pulse is Generated	$t_{H(STA)}$		0.6			μs
Data Setup Time	$t_{SU(DAT)}$		100			ns
Data Hold Time	$t_{H(DAT)}$		300			ns
Setup Time for STOP Condition	$t_{SU(STOP)}$		0.6			μs
Bus Free Time between START and STOP Condition	t_{BUF}		1.3			μs
Clock Frequency	f_{SCL}		10		400	kHz
Host Communication Failure						
I²C Bus Release Timeout (1)	$t_{TIMEOUT}$		25		35	ms
Watchdog Timeout Period	t_{WDI}	WDTMR_ADJ[1:0] = 01	4.0	4.8	5.5	s
		WDTMR_ADJ[1:0] = 10	66	77	84	
		WDTMR_ADJ[1:0] = 11	132	153	167	

NOTE:

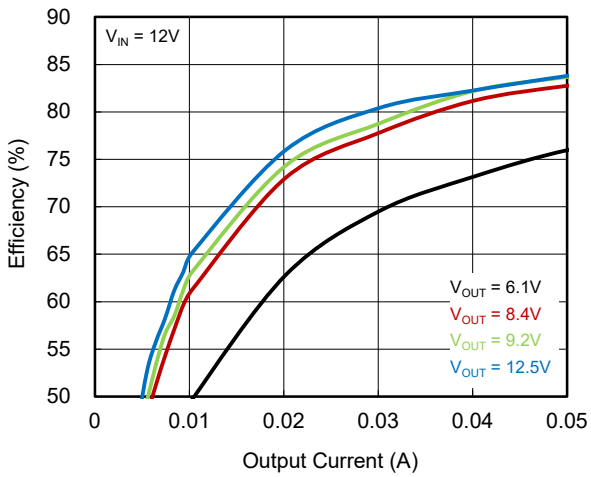
1. A transfer will be timed out for participating devices when any clock low period exceeds the minimum $t_{TIMEOUT}$ (25ms). The communication must be reset within the maximum $t_{TIMEOUT}$ (35ms) if a timeout condition is detected. Both the master and slave must take action within the maximum $t_{TIMEOUT}$ which has incorporated the master cumulative stretch limit (10ms) and slave cumulative stretch limit (25ms).

TYPICAL PERFORMANCE CHARACTERISTICS

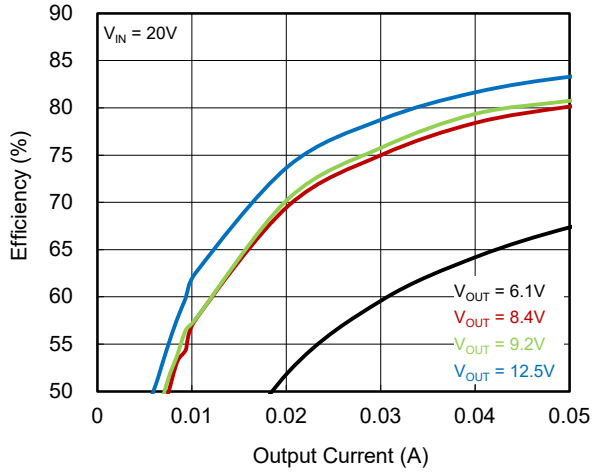
Light Load Efficiency



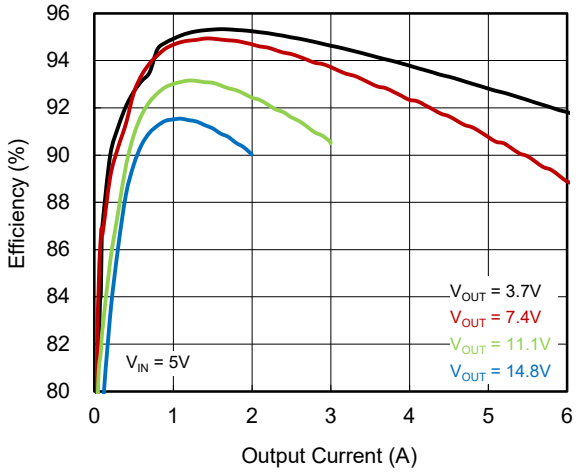
Light Load Efficiency



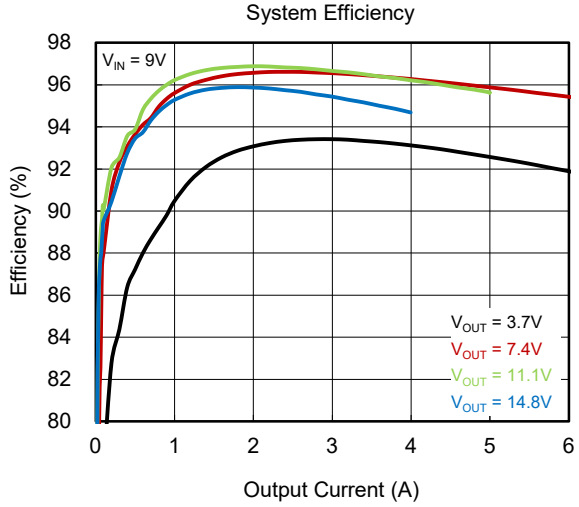
Light Load Efficiency



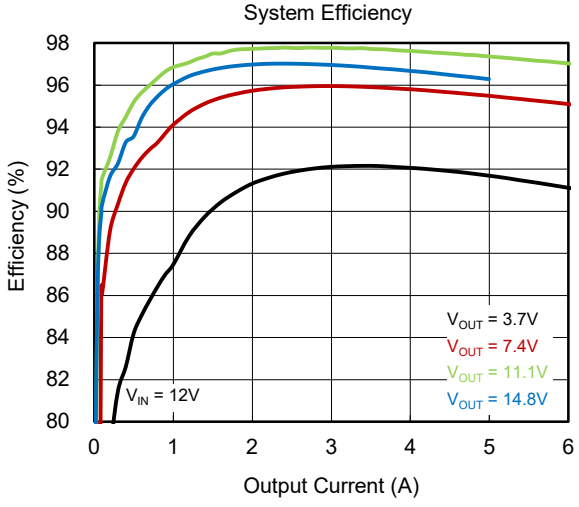
System Efficiency



System Efficiency

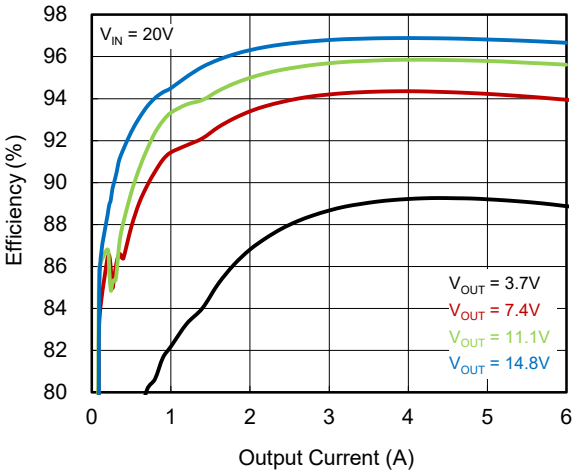


System Efficiency

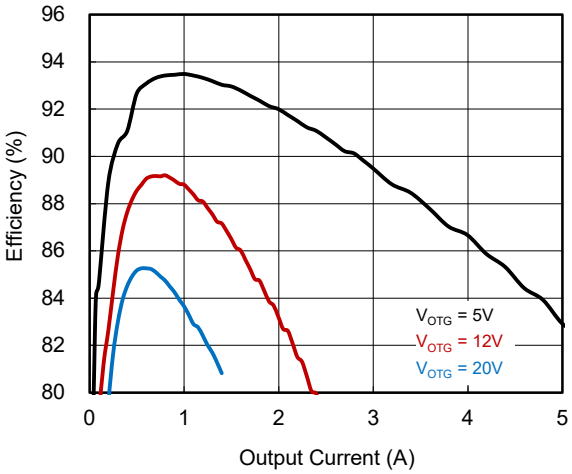


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

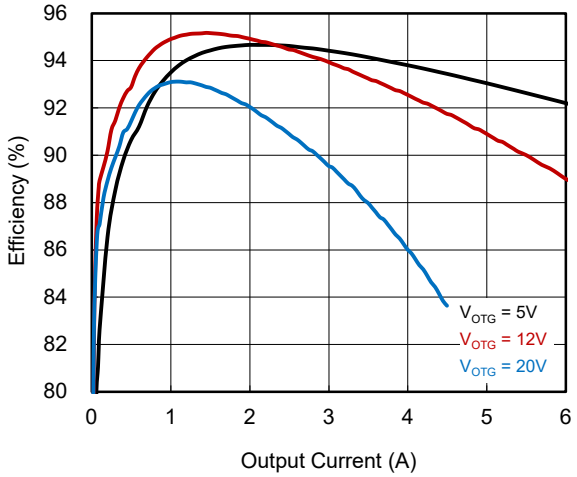
System Efficiency



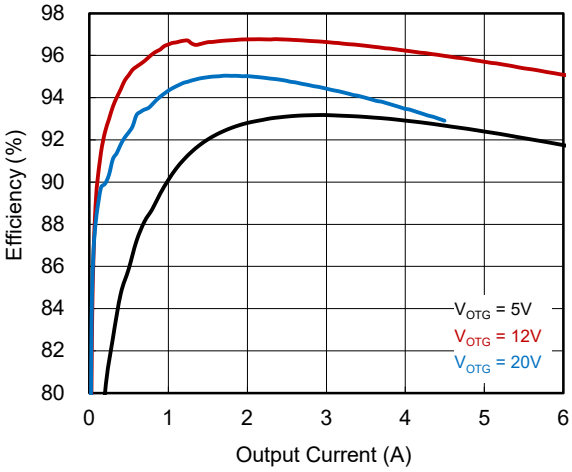
OTG Efficiency with 1-Cell Battery



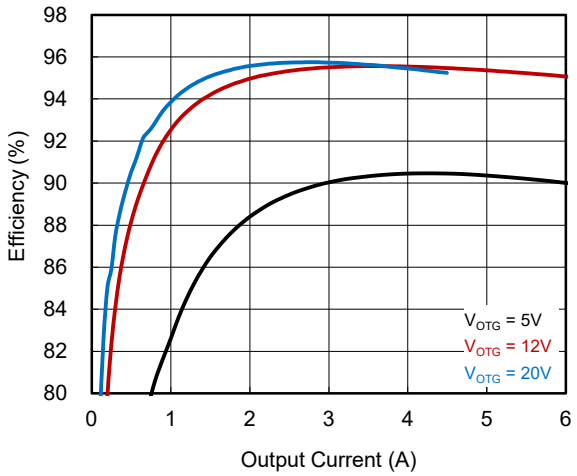
OTG Efficiency with 2-Cell Battery



OTG Efficiency with 3-Cell Battery

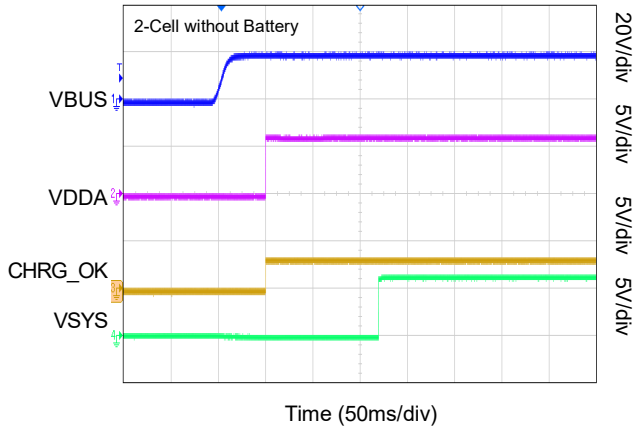


OTG Efficiency with 4-Cell Battery

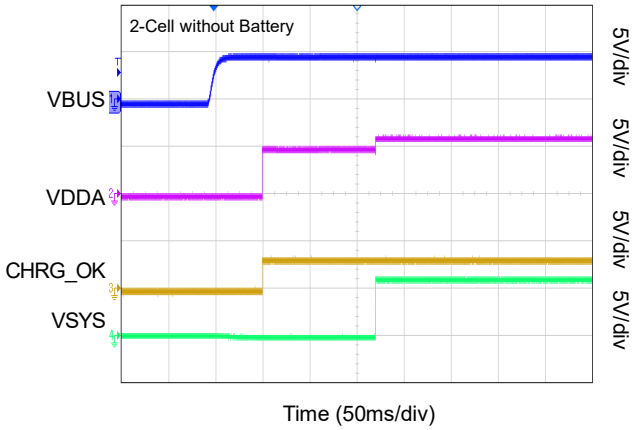


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

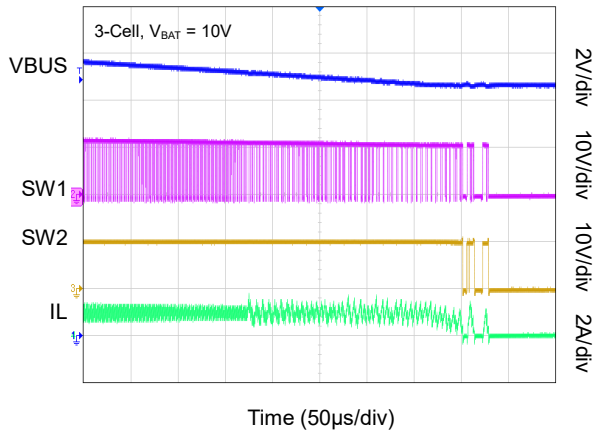
Power-Up from 20V



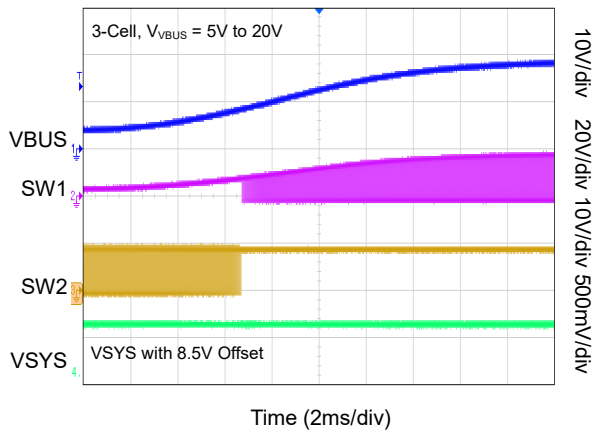
Power-Up from 5V



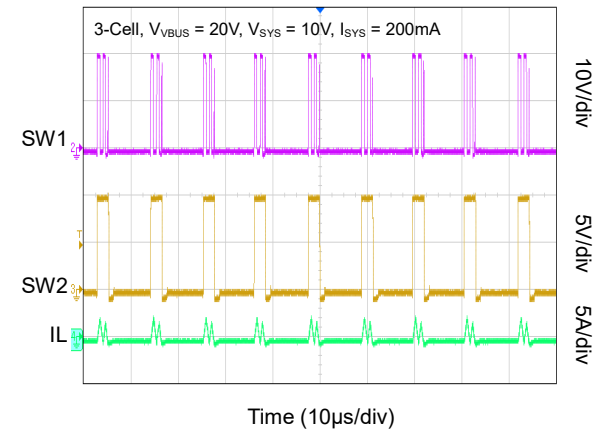
Power-Off from 12V



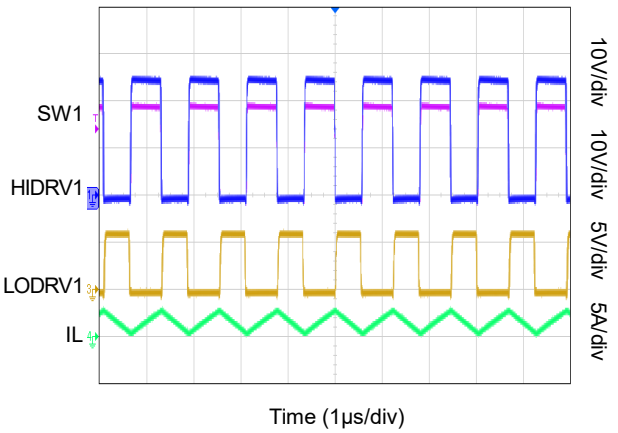
System Regulation



PSM Operation

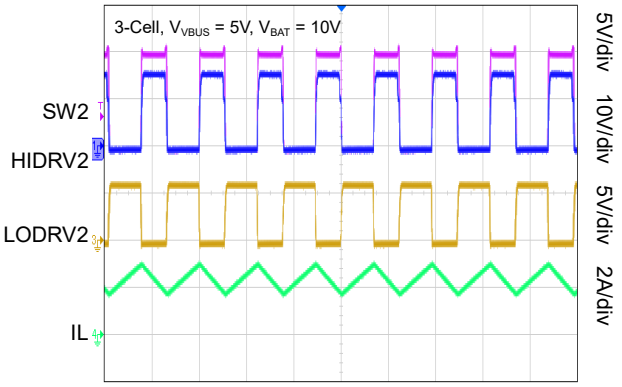


PWM Operation



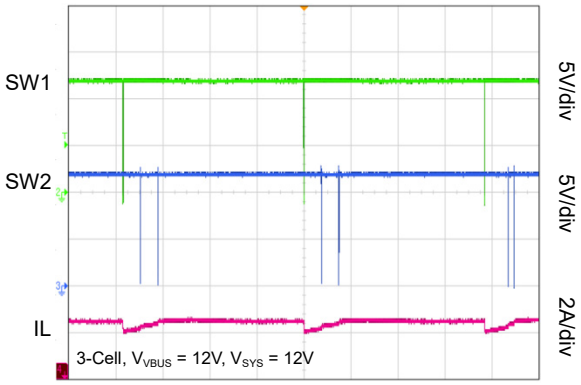
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Switching during Boost Mode



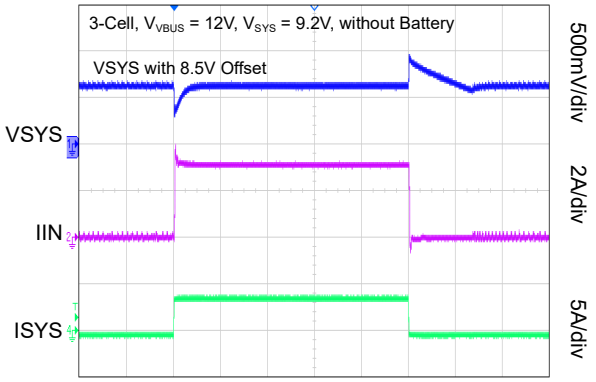
Time (1μs/div)

Switching during Buck-Boost Mode



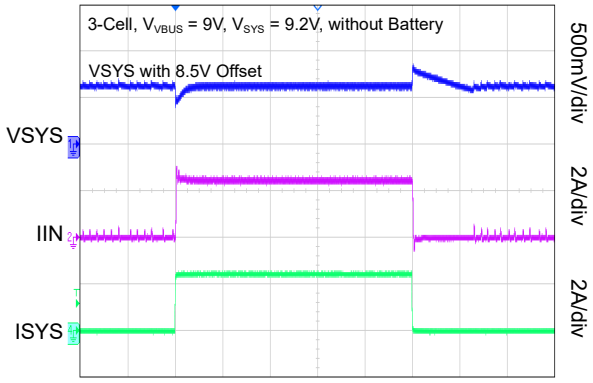
Time (10μs/div)

System Regulation in Buck Mode



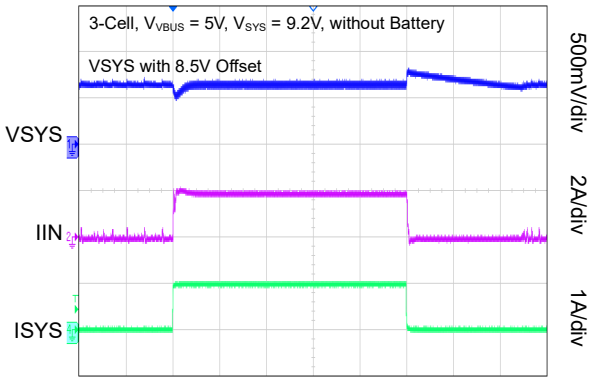
Time (500μs/div)

System Regulation in Buck-Boost Mode



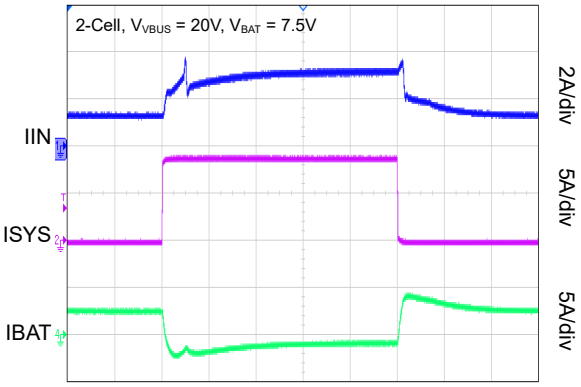
Time (500μs/div)

System Regulation in Boost Mode



Time (500μs/div)

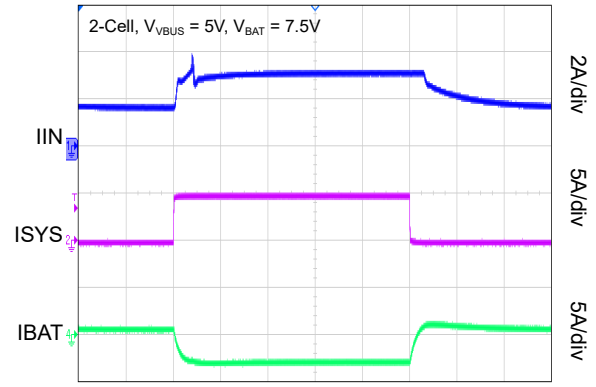
Input Current Regulation in Buck Mode



Time (200μs/div)

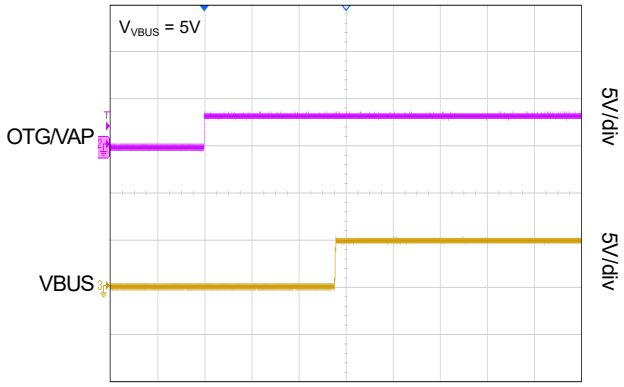
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Input Current in Boost Mode



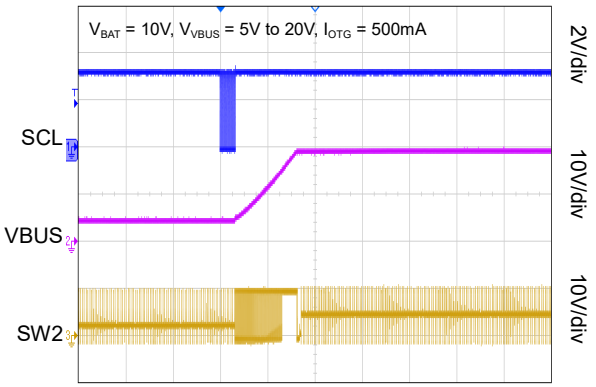
Time (200μs/div)

OTG Power-Up from 8V Battery



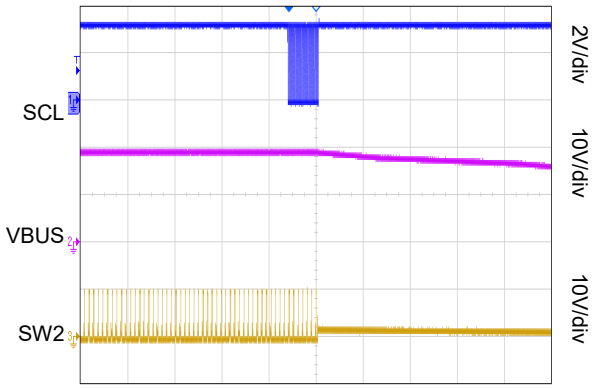
Time (5ms/div)

OTG Voltage Ramp Up



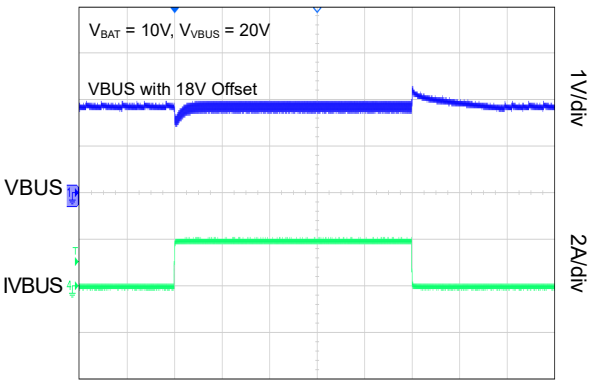
Time (1ms/div)

OTG Power-Off



Time (500μs/div)

OTG Load Transient



Time (500μs/div)

TYPICAL APPLICATION CIRCUIT

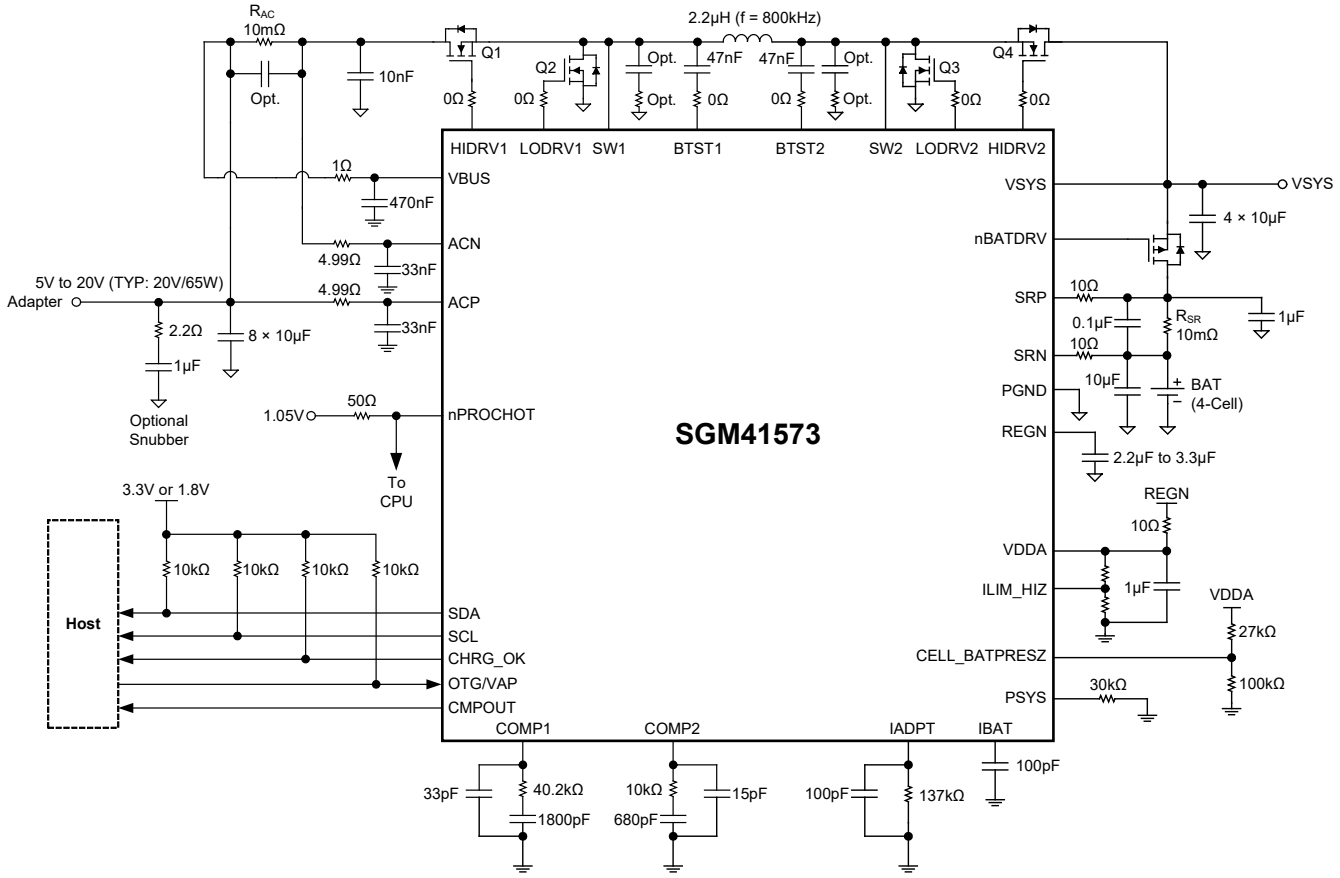


Figure 2. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

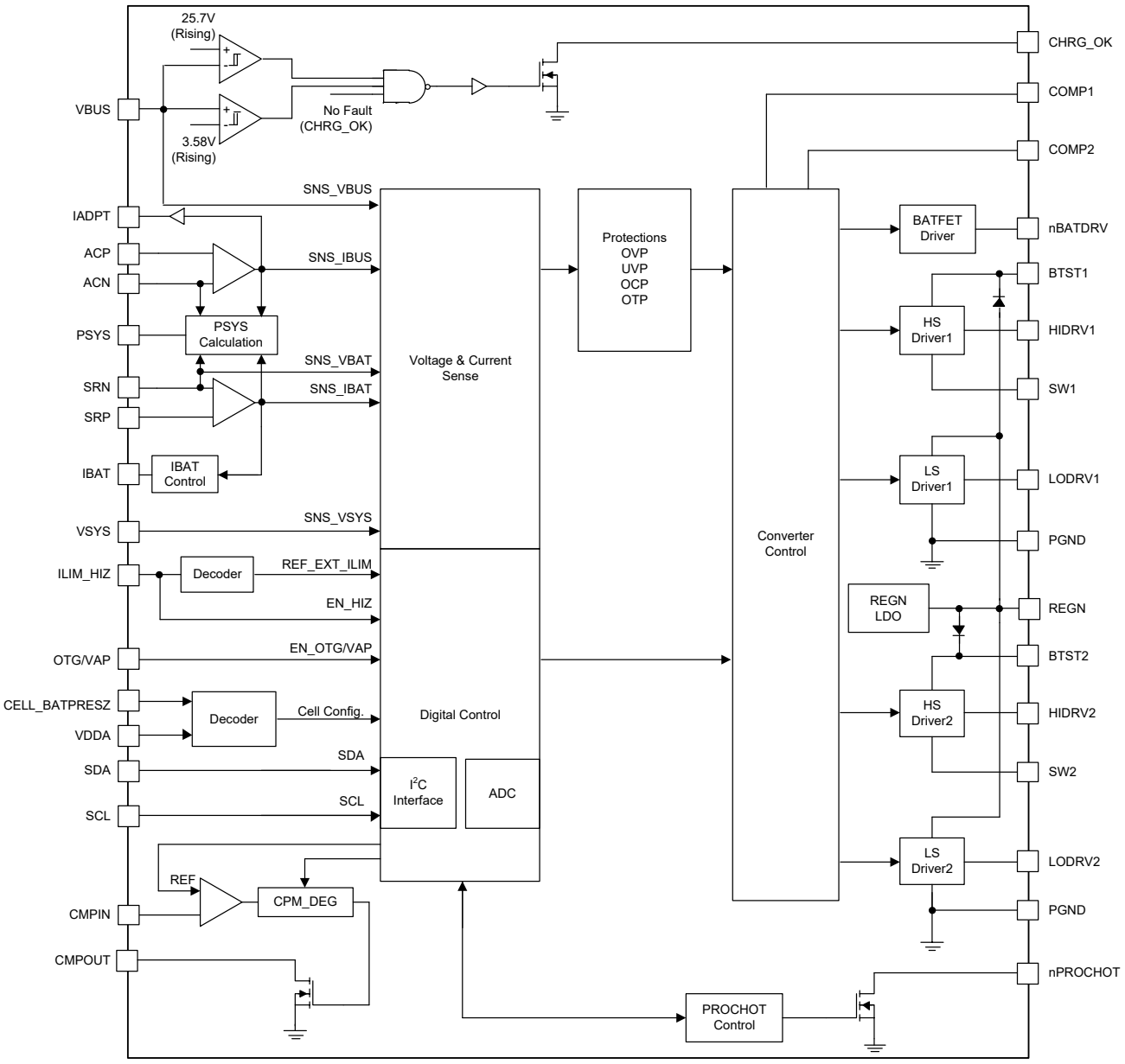


Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM41573 is a charger controller with narrow voltage DC Buck-Boost topology that is suitable for portable applications such as notebooks, tablets and other mobile devices with rechargeable batteries. This device offers high light load efficiency, fast response and it can automatically convert among Buck, Buck-Boost, and Boost operation modes.

A variety of source types, including traditional AC/DC adapters, USB PD and legacy USB ports with 3.58V to 24V voltage range can power the device for charging 1-cell to 4-cell batteries. When there is no adapter, the USB On-The-Go (OTG) function can be enabled to generate adjustable 3V to 20.56V on the USB port with 8mV resolution from a 1-cell to 4-cell batteries. The slew rate of the output voltage transitions in OTG can be configured (by OTG current setting) to comply with the USB PD 3.0 PPS specifications.

When there is only battery and no load connected to the USB OTG port, V_{MIN} Active Protection (VAP) feature is provided to avoid system voltage drops when the load connected to system has rapid changes between light load and heavy load. When the system load is not heavy, the input decoupling capacitors of V_{VBUS} are charged to store energy. During a system power spike, the capacitors are discharged through Buck-Boost converter to keep the system voltage above minimum voltage, because the battery impedance causes the significant system voltage drops during the system load steps. This feature is strongly recommended by Intel for 1-cell or 2-cell battery to smooth the power peaks and improve the system performance when there are the high demands in the system.

The DPM (dynamic power management) feature is provided to avoid the input overload by limiting the input power. With DPM, when the system power increases, the charging current is reduced to keep the input current below the adapter rating. Changing to the supplement mode may be required if the charge current is decreased and reached to zero, but the input is still overloaded. In this case, the charger reduces the system voltage below the battery voltage to allow operation in the supplement mode and provides a portion of system power demand from the battery through the BATFET.

The PSYS function is provided to comply with Intel IMVP8/IMVP9, in which the total input power from the adapter and the battery is monitored. Moreover, the device provides an independent input current buffer (IADPT) and a battery current buffer (IBAT) with the accurate amplifiers.

The input current, charge current and charge voltage registers can be controlled by I²C with high resolution and high accuracy regulation limits. The nPROCHOT timing and threshold profile is also set by I²C to match the system requirements.

Power-Up from Battery without DC Source

If the battery is the only source and $V_{BAT} > V_{VBAT\_UVLOZ}$, it will be connected to the system by turning the BATFET on. By default, the charger starts in low power mode (EN_LWPWR bit = 1) with the lowest quiescent current and keeps the LDO off. The host can change charger operation to the performance mode (EN_LWPWR bit = 0). In this mode, the host can enable IBAT buffer (to monitor discharge current), the PSYS (to monitor total system power), nPROCHOT and the independent comparator through I²C. The REGN (LDO) is kept on in the performance mode to provide an accurate reference for other functions.

V_{MIN} Active Protection (VAP) when Battery-Only Mode

In the V_{MIN} Active Protection (VAP) mode, the VBUS decoupling capacitors are charged to their highest possible voltages (e.g. 20V) by the Buck-Boost converter from the battery. For a system with 2S1P or 1S2P battery configuration, the peak system power may reach 100W if the SoC and system power spike at the same time. Such coincidence is normally rare, but is still possible. At this time, the energy stored in the input decoupling capacitors will be able to supplement the battery through Buck-Boost converter to avoid system voltage drops. With the VAP mode, the higher peak power levels can be set to the SoC to provide much better turbo performance.

The following steps must be followed to enter VAP operation:

1. VBAT should not cause a SYSOVP trip that stops converter switching.
2. VAP output voltage is set by OTGVoltage and OTG_RANGE_LOW registers. If OTG_RANGE_LOW bit = 0, a 1.28V offset is added to the V_{OTG} from digital DAC to achieve the higher ranges from 4.28V to 20.56V. If OTG_RANGE_LOW bit = 1, no offset is added and the V_{OTG} from digital DAC is from 3V to 19.28V.
3. Set the VBUS charge current limit in OTGCurrent register.
4. Set the system voltage regulation point in MinSystemVoltage register. The VSYS_MIN loop regulates VSYS at this point when the input capacitors supplement the battery.

DETAILED DESCRIPTION (continued)

5. Set the PROCHOT_VSYS_TH1 threshold for triggering the VAP discharging VBUS in VSYS_TH1[3:0] register.
6. Set the PROCHOT_VSYS_TH2 threshold to send an nPROCHOT active low signal in VSYS_TH2[1:0] register.
7. Enable VAP by setting OTG_VAP_MODE bit = 0 and pulling the OTG/VAP pin high.

To terminate the VAP mode, either set the OTG_VAP_MODE bit = 1 or pull the OTG/VAP pin low. With any regular charger fault, the VAP mode is automatically terminated by resetting OTG_VAP_MODE bit = 1.

Power-Up from DC Source

After connecting a DC source, the input voltage is checked before turning on the LDO and bias circuits. The input current limit is also set before starting converters.

The power-up sequence from a DC source is:
1. 50ms after V_{VBUS} exceeds V_{VBUS_CONVEN}, the 5.6V LDO is enabled and CHRG_OK is pulled high.
2. Poor source detection.
3. Input voltage and current limits are set.
4. Battery cell configuration (by reading the CELL_BATPRESZ pin voltage).
5. The converter powers up.

CHRG_OK Indicator

The CHRG_OK is an open-drain, active high output, which indicates the normal charger operation. It is activated when the following conditions are met:

- $V_{VBUS} > V_{VBUS\_CONVEN}$.
- $V_{VBUS} < V_{ACOV}$.
- There is no SYS short latch off, SYSOVP, BATOC, ACOC, force latch off, and thermal shutdown.

Setting the Input Voltage and Current Limit

After CHRG_OK is asserted, the default input current limit (3.25A) is set in IIN_HOST register. The actual limit is the lower of IIN_HOST register and the ILIM_HIZ pin settings.

The VBUS measurement is enabled just before enabling the converter (VBUS without any load). The VINDPM threshold is VBUS (without any load on the converter) minus 1.28V (in default). The VINDPM threshold is the input voltage level at which the dynamic power management begins to reduce the charge current to avoid further system voltage drop and gives priority to system load rather than charging.

The charger can be powered up with the proper input current and voltage limits settings. The host can always change these limits after powering up to match with the input source type.

Battery Cell Configuration

A resistor divider between REGN and GND and tapped to CELL_BATPRESZ should be used to define the battery configuration for the charger. The bias voltage on the CELL_BATPRESZ pin is measured by the device to detect the battery configuration after the VDDA LDO is activated. See Table 1 for the cell configuration voltage thresholds and the other affected settings.

Device HIZ State

If the voltage of the ILIM_HIZ pin falls below 0.6V or if EN_HIZ bit is set to 1, the charger will enter the HIZ mode which operates in the low quiescent current mode. And the system is powered from battery even when the input source is present. During this mode, the LDO of REGN is enabled.

Table 1. Battery Cell Configuration

Cell Count	Pin Voltage (With Respect to VDDA)	Battery Voltage (MaxChargeVoltage Register)	SYSOVP
4-Cell	75%	16.8V	19.4V
3-Cell	55%	12.6V	19.4V
2-Cell	40%	8.4V	12V
1-Cell	18.2%	4.2V	5V

DETAILED DESCRIPTION (continued)

Input Current Optimizer (ICO)

The device provides the input current optimizer (ICO) to identify the maximum power point of the input adapter source. To avoid overloading the input adapter source and staying in VINDPM, the ICO algorithm identifies the maximum input current limit of the adapter and updates this input current limit to IIN_DPM register.

The ICO function is disabled by default, and it can be enabled by the host through setting EN_ICO_MODE bit = 1. When the ICO routine is successfully executed, the ICO_DONE bit = 1 notifies ICO done.

When the ICO algorithm is enabled, it runs to dynamically and continuously adjust the input current limit. The operation of ICO algorithm depends on the battery voltage as following:

Case 1: When $V_{BAT} < V_{SYSMIN}$, the device starts ICO algorithm with an initial value that equals to the I_{INDPM}. Where the I_{INDPM} is the maximum input current limit determined by the host.

Case 2: When $V_{BAT} > V_{SYSMIN}$, the device starts ICO algorithm with an initial value of min (500mA, IIN_HOST).

During the optimization, if VINDPM is triggered, the ICO algorithm decreases the input current limit to avoid input source overloading. When the maximum input current limit is detected, the IIN_DPM register reflects the optimal maximum input current limit which does not trigger VINDPM, the ICO_DONE bit = 1 indicates the maximum input current detected.

In above case 1, if both VINDPM and IINDPM are not triggered, the IIN_DPM register keeps the initial value and the ICO_DONE bit = 0 indicates that the ICO optimization is in process. If the load becomes heavy, the VINDPM is still not triggered, but IINDPM is triggered, and the ICO algorithm is also completed. The IIN_DPM register remains the initial value unchanged, and the ICO_DONE bit = 1 indicates the maximum input current detected.

In above case 2, if the VINDPM is not triggered and the converter is under light load condition, the IIN_DPM register gives a little higher input current limit than the actual input current. The ICO_DONE bit = 0 indicates that the ICO optimization is in process. If the load becomes heavy, the ICO algorithm automatically runs to set new IIN_DPM register value.

After the ICO algorithm completes, the host changes the IIN_HOST register or InputVoltage register to force the ICO algorithm to run again.

USB On-The-Go (OTG)

The SGM41573 supports USB OTG operation and can power other portable devices connected to the USB port from the battery. The OTG output voltage and current limit are set in OTGVoltage register and OTGCurrent register. The OTG mode can be enabled if the following conditions are met:

• VBAT should not cause a SYSOVP trip that stops converter switching.
• OTG output voltage is set by OTGVoltage and OTG_RANGE_LOW registers. If OTG_RANGE_LOW bit = 0, a 1.28V offset is added to the V_{OTG} from digital DAC to achieve the higher ranges from 4.28V to 20.56V. If OTG_RANGE_LOW bit = 1, no offset is added and the V_{OTG} from digital DAC is from 3V to 19.28V.
• OTG output current is set in OTGCurrent register.
• OTG/VAP pin is high, EN_OTG bit = 1 and OTG_VAP_MODE bit = 1.
• $V_{VBUS} < V_{VBUS\_CONVEN}$.
• 10ms after having all above conditions valid, the converter starts to generate OTG output from the battery and VBUS ramps up to the target voltage. The CHRG_OK pin goes high only if OTG_ON_CHRGOK bit = 1.

Converter Operation Modes

A synchronous Buck-Boost converter with the external N-channel MOSFET switches is used by this device such that it can charge batteries from a standard 5V or a higher voltage source. It can operate in Buck, Boost or Buck-Boost mode depending on the input/output voltage conditions. The Buck-Boost covers all voltage conditions with smooth transitions between them and continues the operation.

Table 2. MOSFET Operation

Mode	Buck	Buck-Boost	Boost
Q1	Switching	Switching	On
Q2	Switching	Switching	Off
Q3	Off	Switching	Switching
Q4	On	Switching	Switching

DETAILED DESCRIPTION (continued)

Inductance Detection through IADPT Pin

Before powering up the converter, the charger can be informed about the inductance value (L) using an external resistor connected to the IADPT pin. The recommended resistor values for 1μH, 2.2μH and 3.3μH inductances are 93kΩ, 137kΩ and 169kΩ, respectively, refer to Table 3. A ±3% or better chip resistor can be used for inductance identification.

Table 3. Inductor Detection through IADPT Resistor

Inductor in Use	Resistor on IADPT Pin
1μH	93kΩ
2.2μH	137kΩ
3.3μH	169kΩ

Continuous Conduction Mode (CCM)

When the system load or charging current is large enough, the inductor current ripples are always above zero which is defined as CCM. Taking Buck operation as an example, a new switching cycle is started by turning on the high-side switch (HS) each time, and the internal ramp comes up from a pre-biased offset. The HS will turn off and low-side switch (LS) turns on when the ramp exceeds the error amplifier output. When the ramp resets, the LS turns off and a new cycle will begin. A short dead time in which both MOSFETs are off is considered using break-before-make logic to avoid shoot-through during transition. During the dead time, the LS body-diode conducts the inductor current. The LS is turned on when the HS turns off. This keeps the losses low and provides safe charging at high currents.

Pulse Skip Mode

For better light-load efficiency, the converter operates with PSM (pulse skip mode) at light loads. In PSM, the effective switching frequency is reduced as the load decreases. The lowest PSM frequency can be limited to 25kHz by setting the OOA (out-of-audio frequency) bit (EN_OOA bit = 1). The OOA feature is enabled by default.

Current and Power Monitor

High-Accuracy Current Sense Amplifier (IADPT and IBAT)

Accurate current sense amplifiers (CSA) for monitoring the IADPT (input current in forward charging, or the output current during OTG) and IBAT (the battery charge or discharge current) are provided as an industry standard feature. IADPT voltage is 20 or 40 times the ACP to ACN differential voltage, and IBAT voltage is 8 or 16 times the SRP to SRN differential voltage (charging and discharging gains are selectable separately). And if the input or battery voltage is below UVLO level, IADPT output will not be valid.

In summary:

- V_{IADPT} = 20 or 40 × (V_{ACP} - V_{ACN}) in the forward mode.
- V_{IADPT} = 20 or 40 × (V_{ACN} - V_{ACP}) in the reverse OTG mode.
- V_{IBAT} = 8 or 16 × (V_{SRP} - V_{SRN}) in the forward mode when EN_ICHG_IDCHG bit = 1
- V_{IBAT} = 8 or 16 × (V_{SRN} - V_{SRP}) in the supplement mode, or the reverse OTG mode when EN_ICHG_IDCHG bit = 0.

It is recommended that a small decoupling capacitor (100pF MAX) be connected to these outputs to absorb high frequency noise. An additional RC filter can be used carefully if needed. Pay attention that the filter will increase the response delay.

High-Accuracy Power Sense Amplifier (PSYS)

The total system power can also be monitored by the device. In the forward mode, the input adapter powers the system, and in the reverse OTG mode, the battery powers the system and the VBUS output. The PSYS pin output current is proportional to the total system power. The K_{PSYS}, which is the ratio of the PSYS pin output current to the total system power, can be set in PSYS_RATIO register and its default value is 1μA/W. A resistor connects this output to GND to convert the current to an output voltage. The input and battery current sense resistor values (R_{AC} and R_{SR}) are defined for the PSYS calculation in RSNS_RAC register and RSNS_RSR register. Use Equation 1 to calculate the PSYS voltage. When the adapter is connected and the device is in forward charging, I_{IN} > 0 and I_{BAT} < 0. During battery discharge I_{BAT} > 0:

$$V_{PSYS} = R_{PSYS} \times K_{PSYS} (V_{ACP} \times I_{IN} + V_{BAT} \times I_{BAT}) \quad (1)$$

And during OTG mode, there are two selectable modes in PSYS_OTG_IDCHG register. When PSYS_OTG_IDCHG = 0 (default), the PSYS reports the battery discharge power minus OTG output power (for Equation 1, in OTG mode, I_{IN} < 0 and I_{BAT} > 0). When PSYS_OTG_IDCHG = 1, the PSYS reports the battery discharge power only.

R_{AC} and R_{SR} values should be 10mΩ or 20mΩ for proper PSYS function.

The PSYS function is disabled by default to minimize the quiescent current. Set EN_PSYS bit = 1 to enable this function.

DETAILED DESCRIPTION (continued)

Input Source Dynamic Power Manage

For DPM operation, please refer to the **Input Current and Input Voltage Registers for Dynamic Power Management** section.

Two-Level Adapter Current Limit (Peak Power Mode)

An adapter is generally able to provide higher than its rated DC current in a few milliseconds to tens of milliseconds. This overloading capability is used by charger through two-level input current limit (also called peak power mode) to minimize battery usage when the CPU goes in turbo mode. The peak power mode can be enabled in EN_PKPWR_IDPM register and EN_PKPWR_VSYS register. The main current limit (I_{LIM1}) is set equal to the adapter current limit, read from IIN_DPM register. And the overload limit (I_{LIM2}) is set as ratio of I_{LIM1} in ILIM2_VTH[4:0] register.

As shown in Figure 4, a peak power cycle starts when an input current surge/battery discharge is detected by the charger due to a load transient (adapter and battery supply the system together), or by detecting a system voltage drop below 96% V_{SYSMIN}. The charger first applies I_{LIM2} limit for a period of T_{OVLD} (set in PKPWR_TOVLD_DEG[1:0] register) and then applies I_{LIM1} for up to T_{MAX} - T_{OVLD} time (T_{MAX} is set in PKPWR_TMAX[1:0] register). A new peak power cycle will repeat if the overload continues after T_{MAX}. If the T_{OVLD} = T_{MAX}, the peak power mode will be always on.

Processor Hot Indication

In turbo mode, the peak system power may exceed total power available from adapter and battery. Typical indicators of such overload are system voltage drops or reaching the adapter or battery (discharge) maximum currents. These events are observed by the processor hot function in the device that sends an nPROCHOT pulse to CPU, asking for load reduction. The monitored events are:

1. I_{CRIT}: Adapter peak current reaches 110% of I_{LIM2}.
2. I_{NOM}: Adapter average current reaches 110% of input current limit (I_{LIM1}).
3. I_{DCHG}: Battery discharge current reaches its programmed nPROCHOT threshold value. (I_{DCHG} > I_{DCHG_VTH} with t_{IDCHG_DEG} deglitch).
4. V_{SYS}: System voltage on VSYS reaches its programmed nPROCHOT threshold value. (V_{SYS} < V_{SYS_TH2} when EN_CON_VAP bit = 0 or V_{VBUS} < $V_{VBUS\_CONVENZ}$ when EN_CON_VAP bit = 1).
5. Adapter removal: Upon adapter removal that results in CHRG_OK pin to go low when V_{VBUS} < $V_{VBUS\_CONVENZ}$.
6. Battery removal: Upon battery removal that results in CELL_BATPRESZ pin to go low.
7. CMPOUT: Independent comparator output (CMPOUT pin) goes from high to low.
8. VDPM: VBUS falls below 80% or 90% (by PROCHOT_VDPM_80_90 register) or 100% (LOWER_PROCHOT_VDPM register) of the VINDPM threshold.
9. EXIT_VAP: The charger exits VAP mode.

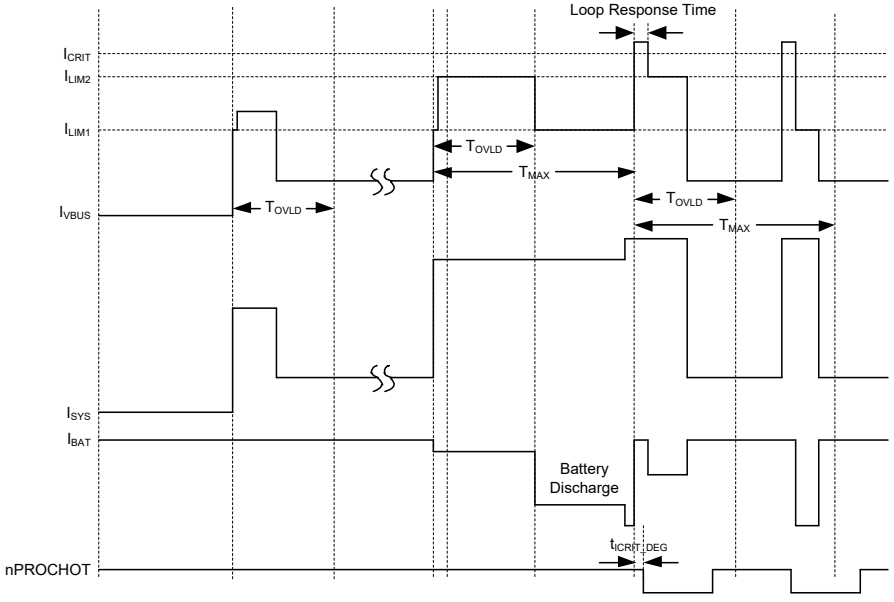


Figure 4. Two-Level Adapter Current Limit Timing Diagram

DETAILED DESCRIPTION (continued)

The thresholds for the I_{DCHG}, I_{CRIT}, V_{SYS}, VDPM events, and the deglitch times of the I_{DCHG}, I_{CRIT}, I_{NOM} or CMPOUT events are I^2C programmable. Triggering by each event is individually enabled or disabled in ProchotOption1[7:0] bits (I^2C address = 0x38) except for the PROCHOT_EXIT_VAP which is always enabled. If any enabled event is triggered, a low pulse with minimum width programmable in PROCHOT_WIDTH[1:0] bits is generated on nPROCHOT. If the event is still active at the end of the pulse, nPROCHOT will still be low until the event is cleared.

By enabling nPROCHOT pulse extension mode (set EN_PROCHOT_EXT bit = 1), the nPROCHOT output remains low until the host writes a 0 to PROCHOT_CLEAR bit even if the triggering event is already cleared. For the STAT_VDPM and STAT_EXIT_VAP events trigged, the nPROCHOT output will be low until the host writes STAT_VDPM or STAT_EXIT_VAP to clear the event, independent of EN_PROCHOT_EXT bit.

nPROCHOT during Low Power Mode

The device provides a low power nPROCHOT function with very low quiescent current consumption if the device is in low power mode (EN_LWPWR bit = 1). In this mode, the independent comparator is used for system voltage monitoring, and sends an nPROCHOT signal to CPU if an overload condition occurs. The independent comparator threshold is always 1.2V. The register settings needed to enable nPROCHOT system voltage monitoring in low power mode are as follows:

- EN_LWPWR bit = 1 (enable charger low power mode).
- ProchotOption1[7:0] bits (I^2C address = 0x38) = 0x40.
- ChargeOption1[6:4] bits (I^2C address = 0x30) = 0b100.
- Independent comparator threshold is always 1.2V.
- When EN_PROCHOT_LPWR bit = 1, the charger can monitor the system voltage by connecting CMPIN pin to a voltage proportional to system. The nPROCHOT will be pulled from high to low when CMPIN voltage (which is proportional to system voltage) falls below 1.2V to indicate an overload condition occurs.

nPROCHOT Status

The event that has triggered nPROCHOT sets the corresponding bit in ProchotStatus[7:0] bits (I^2C address = 0x22) and STAT_EXIT_VAP bit. This status bit (except STAT_VDPM and STAT_EXIT_VAP bits) can be reset to 0 if it is not active anymore after being read by the host. The STAT_VDPM and STAT_EXIT_VAP bits can be reset to 0 after the host writes the corresponding bit to 0.

If an nPROCHOT event occurs while another event is active, both status bits will be 1. The nPROCHOT pulse will be extended if one of the events is still active after the normal nPROCHOT pulse width.

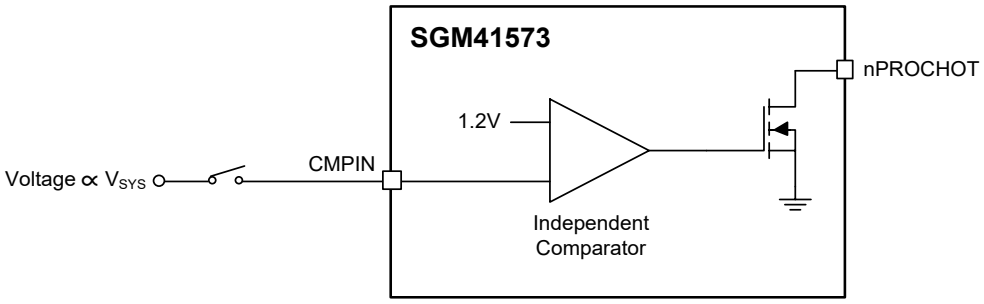


Figure 5. nPROCHOT Low Power Mode Implementation

DETAILED DESCRIPTION (continued)

Device Protection

Watchdog Timer

An internal watchdog timer can terminate the charging if in a 153s window (selectable in WDTMR_ADJ[1:0] bits), a write to MaxChargeVoltage register or ChargeCurrent register does not occur. Except ChargeCurrent register, which is reset to zero and suspends battery charging, the other registers are not changed after watchdog timeout. Therefore, within each watchdog cycle, at least one write to MaxChargeVoltage register or ChargeCurrent register is necessary to reset watchdog timer and continue (or resume) charging if the values are valid. The watchdog timer can be disabled by writing 00 to WDTMR_ADJ[1:0] bits.

Input Over-Voltage Protection (ACOV)

The device has a fixed input over-voltage threshold (the input is conventionally called AC adapter). If V_{VBUS} exceeds ACOV threshold, it is considered as adapter over-voltage. An ACOV event disables the converter and pulls the CHRG_OK low. BATFET will turn on while V_{SYS} drops below V_{BAT}. When V_{VBUS} returns below ACOV (adapter back to normal voltage), the CHRG_OK will be released to go high again and the converter automatically resumes if the other enable conditions are valid.

Input Over-Current Protection (ACOC)

If the input current exceeds the ACOC threshold, the converter stops switching. It will retry switching after 250ms. The ACOC is set by I_{LIM2_VTH} (ILIM2_VTH[4:0] bits) multiplied by 1.33 or 2 (ACOC_VTH register).

System Over-Voltage Protection (SYSOVP)

After the converter starts, the CELL_BATPRESZ pin is read to set the MaxChargeVoltage register. It also sets the SYSOVP threshold to 5V (1-cell battery), or 12V (2-cell battery) or 19.4V (3-cell or 4-cell battery). Before the host writes to MaxChargeVoltage register, the battery configuration is set by CELL pin voltage. If a system over-voltage occurs, the converter will be latched off and SYSOVP_STAT = 1. The latch off can be cleared to restart the converter by writing 0 to this bit or by adapter remove-reconnect.

Battery Over-Voltage Protection (BATOVP)

A battery over-voltage may occur by inserting a wrong battery or due to removal of the battery during charge. Battery over-voltage threshold is 104% (2-4 cells battery) of the regulation voltage (MaxChargeVoltage register). In case of a BATOVP, the Buck-Boost stops switching and the VSYS pin starts to sink current until V_{BAT} falls below 102% of the regulation voltage (MaxChargeVoltage register).

Battery Short

If V_{BAT} drops below V_{SYSMIN} voltage during charging, the maximum current will be limited to 384mA.

System Short Hiccup Mode

The system voltage (V_{SYS}) is constantly monitored and if it falls below 2.4V, it enters SYS short with maximum IINDPM = 500mA. And after a 2ms deglitch time, the charger shuts down for 500ms and then restarts for 10ms. If the V_{SYS} is still below 2.4V, the shutdown will repeat. This hiccup mode will continue until the restarts fail 7 times in 90 second and the charger will latch off if the short is still present. The Fault SYS_SHORT bit will be set to 1 to indicate system short fault. The charger can be re-enabled only by writing 0 to Fault SYS_SHORT bit. The charger system short hiccup mode can be disabled by writing SYS_SHORT_DISABLE bit = 1.

Battery Discharge Over-Current (BATOC)

The battery discharging current (I_{BAT}) is constantly monitored, and if $I_{BAT} > I_{BAT\_OC}$, the BATOC is triggered. After BATOC, the Buck-Boost stops switching and the Fault BATOC bit will be set to 1 to indicate the battery over-current.

During OTG/VAP, whether it exits OTG/VAP after BATOC automatically is described as follows:

1. If it is in OTG mode and $V_{BAT} > V_{SYSMIN}$, OTG doesn't exit, and the BUS_UVP function (refer to BUS UVP in OTG/VAP mode) is disabled. When $I_{BAT} < I_{BAT\_OC}$, it resumes switching, and BUS_UVP function is enabled again.
2. Otherwise, it exits OTG (by setting EN_OTG bit to 0) or VAP (by setting OTG_VAP_MODE = 1) automatically.

The threshold of BATOC is set in BATOC_VTH register as ratio of IDCHG_VTH[5:0] and the minimum value of BATOC is 10A. The BATOC function can be disabled by writing EN_BATOC bit = 0.

DETAILED DESCRIPTION (continued)

Bus Over-Voltage Protection (BUS OVP) in OTG/VAP Mode

During OTG/VAP, when V_{VBUS} > 110% OTGVoltage register, the BUS OVP is triggered. In case of a BUS OVP, the Buck-Boost stops switching and the VBUS pin starts to sink current. Fault_OTG_OVP bit = 1 indicates BUS over-voltage fault. In OTG mode, if VBUS OV exceeds 10ms, it exits OTG (by setting EN_OTG bit to 0) automatically.

Bus Under-Voltage Protection (BUS UVP) in OTG/VAP Mode

During OTG/VAP, OTG output current is limited in OTGCurrent register, when the BUS load is heavier than the current limit, V_{VBUS} voltage decreases. When V_{VBUS} < 85% OTGVoltage register, OTG BUS UVP is triggered. Fault_OTG_UVP bit = 1 indicates BUS under-voltage fault. For OTG mode, if the BUS UV condition lasts for 7ms deglitch (for OTG startup, the BUS UVP deglitch time is 400ms), it exits OTG (by setting EN_OTG bit to 0) automatically. For VAP mode, during VBUS charging, if V_{VBUS} < 2.4V for 7ms, it exits VAP (by setting OTG_VAP_MODE bit = 1) automatically.

Thermal Shutdown (TSHUT)

The device uses a TQFN package with low thermal impedance and excellent junction to ambient thermal conduction. If the junction temperature (T_J) exceeds +155℃, the converter will shut down. The device resumes its normal operation (with soft-start) when T_J returns below +135℃.

Device Functional Modes

Forward Mode

When a qualified input source is connected to VBUS, the device is in the forward mode, regulates the system output and charges the battery.

System Voltage Regulation with Narrow VDC Architecture

The SGM41573 is an NVDC charger and uses the external P-type BATFET transistor to separate the system bus and battery. Using BATFET, the V_{SYS} can be regulated above the minimum system voltage (V_{SYSMIN} is set in MinSystemVoltage register) even if the battery is fully depleted. If V_{BAT} is below V_{SYSMIN}, the BATFET will operate in linear mode (LDO mode) and as V_{BAT} rises, it gradually goes to full-ON state when V_{BAT} reaches V_{SYSMIN}. The BATFET is fully ON in charge and supplement modes so $V_{BAT} \approx V_{SYS}$ (the difference is only the V_{DS} of the BATFET). Normally, the V_{SYS} is regulated to 160mV + V_{BAT} when BATFET is off (not in charging or supplement modes).

Refer to the **System Voltage Regulation** section for more details about system voltage regulation and how it is programmed.

Battery Charging Control

The device can charge 1-cell to 4-cell batteries with constant current (CC) and constant voltage (CV) modes. The CELL_BATPREZ pin voltage setting is read to set the default battery voltage (4.2V/cell) in MaxChargeVoltage register. Depending on the battery capacity, the host should program proper charge current in ChargeCurrent register. If the battery is fully charged or if it is not in proper charge condition, the host can terminate the charge by setting CHRG_INHIBIT bit = 1 or clearing ChargeCurrent register.

USB On-The-Go

The USB OTG function is supported, and the device can send power from the battery to another portable device connected to the USB port (reverse mode). The OTG mode voltage is USB PD compliant and includes 5V, 9V, 15V, and 20V outputs. The output current is also USB type-C compliant and includes 500mA, 1.5A, 3A and 5A currents. Similar to the forward mode, in the OTG mode, the converter can also switches from PWM to pulse skip mode at light loads for efficiency improvement.

Pass Through Mode (PTM)

In the pass through mode, the upper switches of the Buck-Boost are on, and the lower ones are off, connecting the system directly to the source through the upper switches. This mode is used in light load or when the system is in the sleep mode to minimize losses. The switching and inductor core losses are avoided in PTM mode.

The following settings are needed to transfer charger to PTM from normal Buck-Boost operation:

- Set EN_EXTILIM bit = 0, to disable the EN_EXTILIM.
- Set PTM_PINSEL bit = 1.
- Set EN_PTM bit = 1.
- Ground ILIM_HIZ pin.

To leave PTM mode, set EN_PTM bit = 0 or pull ILIM_HIZ high.

The device exits PTM automatically if any of conditions below is triggered:

1. ACOC
2. TSHUT
3. BATOC
4. BATOV
5. VINDPM

DETAILED DESCRIPTION (continued)

Programming

I²C Write-Word or Read-Word charger protocol commands are supported by SGM41573. The charger can be identified by the ManufacturerID and DeviceID. The ManufacturerID always returns 0x07. And the I²C address is 6BH.

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM41573 parameters and get status reports. I²C is well known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM41573 operates as a slave device that address is 0x6B (6BH). It has forty-five 8-bit registers, numbered from REG0x00 to REG0x3C.

Physical Layer

The standard I²C interface of SGM41573 supports standard mode and fast mode communication speeds. The frequency of stand mode is up to 100kbits/s, while the fast mode is up to 400kbits/s. Bus lines are pulled high by weak current source or pull-up resistors and are in logic high state with no clocking when the bus is free. The SDA pin is open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 6. All transactions begin by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is generated by master when SCL is high and a high to low transition on the SDA. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered to be busy.

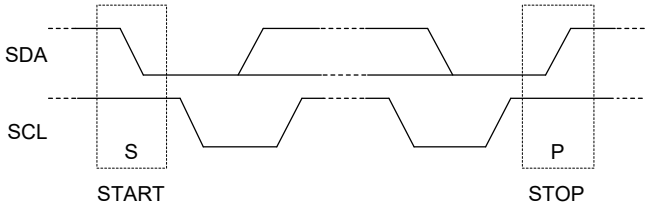


Figure 6. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock HIGH period. The state of SDA only can change when SCL is LOW. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 7.

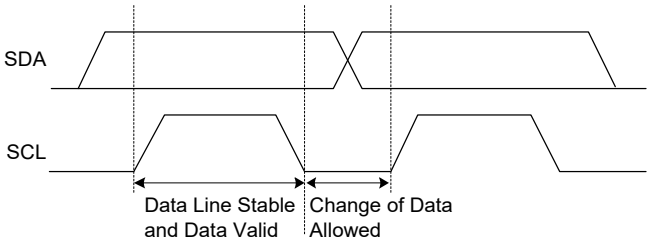


Figure 7. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 8 shows the byte transfer process with I²C interface.

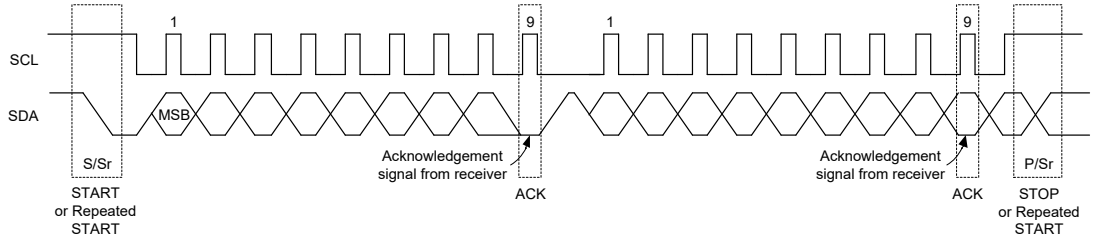


Figure 8. Byte Transfer Process

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and the eighth data-direction bit (R/W). R/W bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be an access in the next byte(s). The data transfer transaction is shown in Figure 9.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 10 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 11), it sends a new START condition along with device address with R/W bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

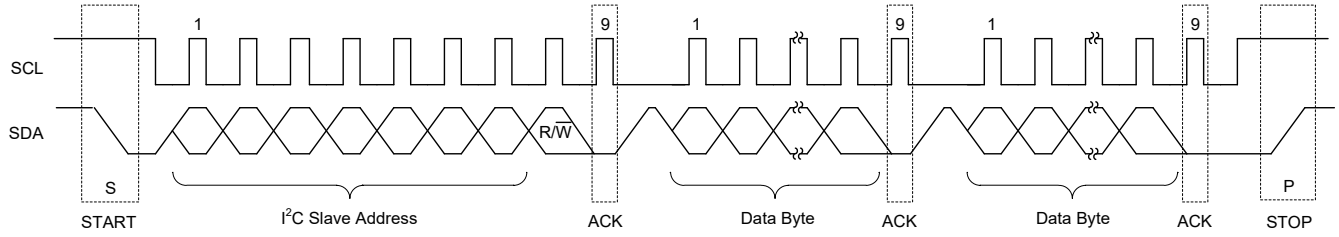


Figure 9. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

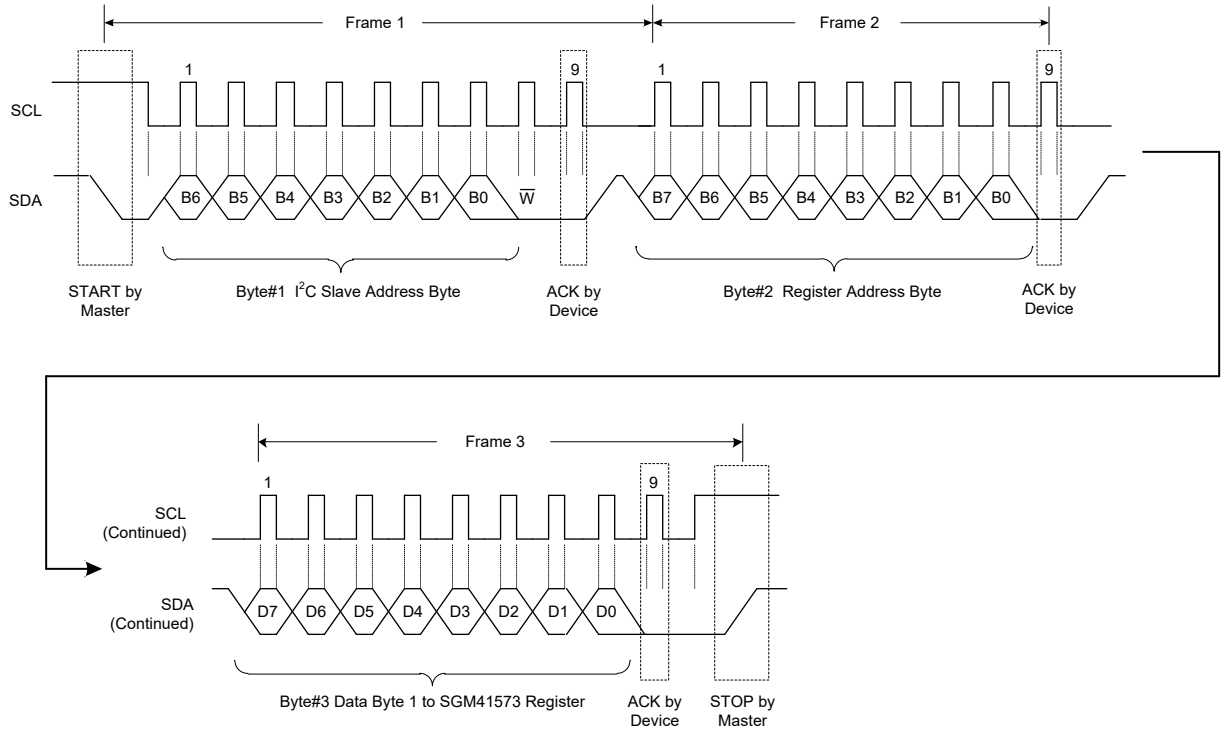


Figure 10. A Single Write Transaction

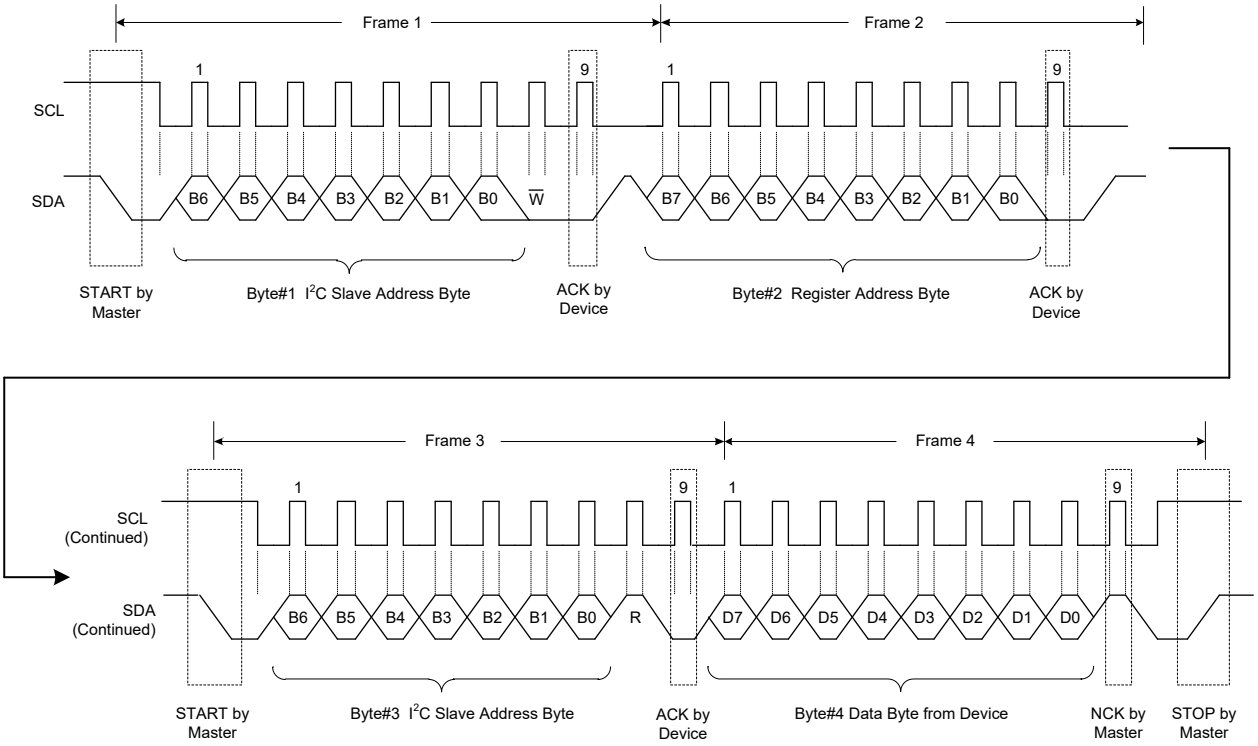


Figure 11. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM41573, as explained in Figure 12 and Figure 13. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave for sending the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

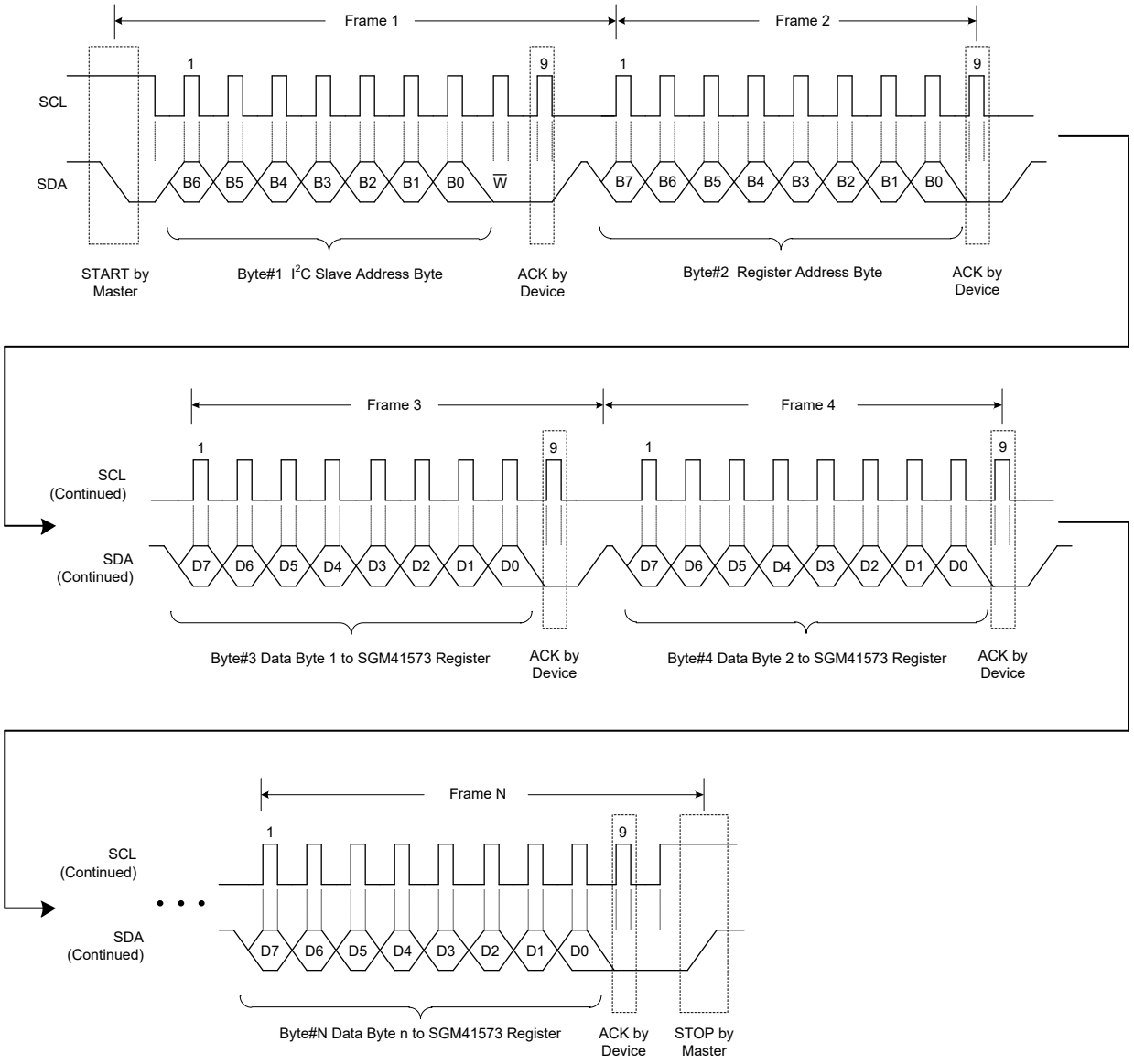


Figure 12. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

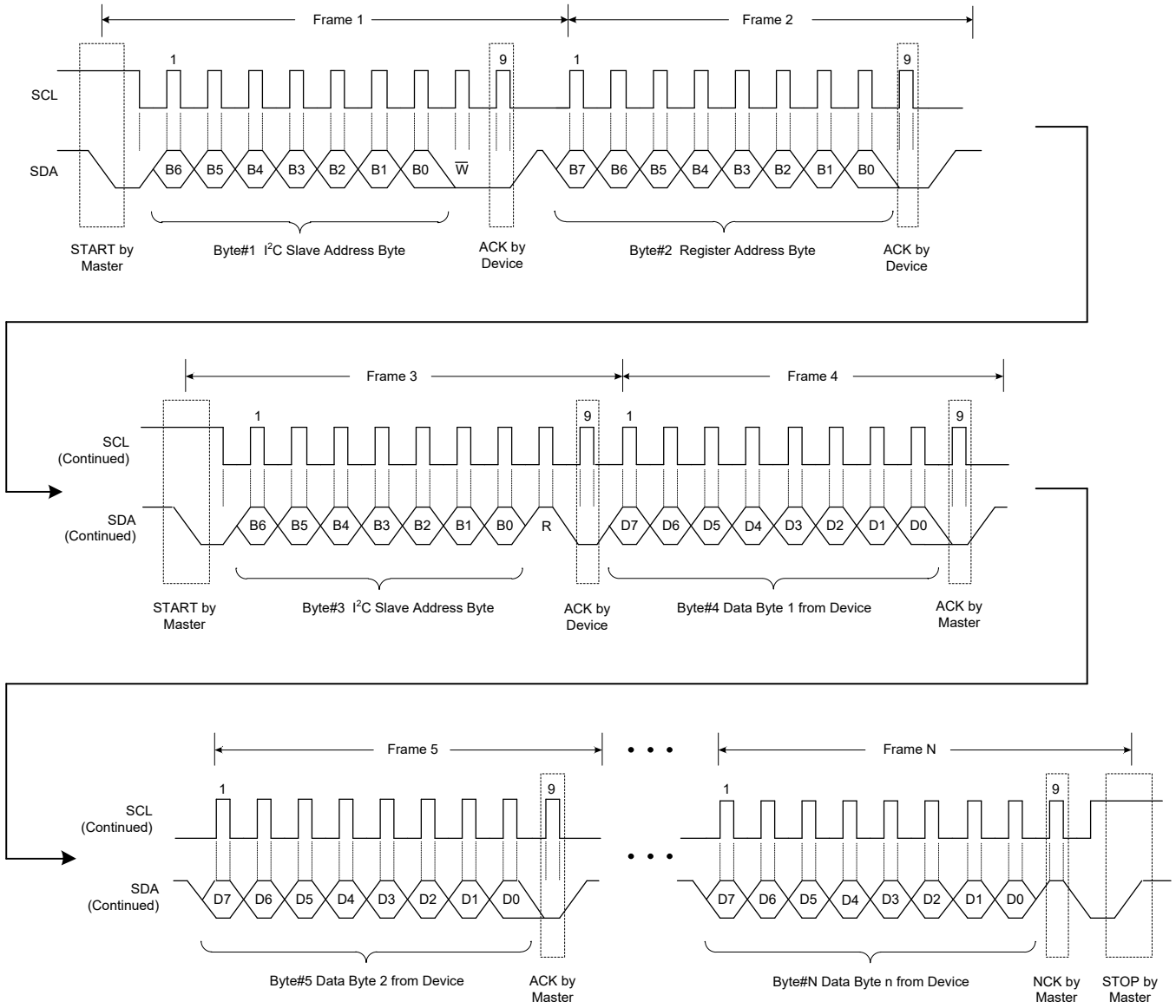


Figure 13. A Multi-Read Transaction

DETAILED DESCRIPTION (continued)

Write 2-Byte I²C Commands

There are some I²C commands combine two 8-bit registers together to form a complete value. These commands include:

- ChargeCurrent()
- MaxChargeVoltage()
- IIN_DPM()
- OTGVoltage()
- InputVoltage()

The host must write the LSB command first and then the MSB command. If the MSB is written first or if the other command (not the MSB) is written after LSB command, this command is ignored. After the LSB command is written, the MSB command must be written within the watchdog time. Otherwise, this command is ignored. Both bytes will be updated simultaneously when the LSB and MSB bytes are properly written.

REGISTER ADDRESS MAPPING

Slave Device Address: 0x6B (0b110 1011 + W/R).

Table 4. Command Register Summary

I²C Address (MSB/LSB)	Register Name	Description	Type	Links
0x01/00	ChargeOption0 Register	Charge Option and Function Enable/Disable	R/W	Go
0x03/02	ChargeCurrent Register	Charge Current Setting	R/W	Go
0x05/04	MaxChargeVoltage Register	Charge Voltage Setting	R/W	Go
0x31/30	ChargeOption1 Register	Charge Option 1	R/W	Go
0x33/32	ChargeOption2 Register	Charge Option 2	R/W	Go
0x35/34	ChargeOption3 Register	Charge Option 3	R/W	Go
0x37/36	ProchotOption0 Register	PROCHOT Option 0	R/W	Go
0x39/38	ProchotOption1 Register	PROCHOT Option 1	R/W	Go
0x3B/3A	ADCOption Register	ADC Option	R/W	Go
0x21/20	ChargerStatus Register	Charger Status	R	Go
0x23/22	ProchotStatus Register	Prochot Status	R	Go
0x25/24	IIN_DPM Register	Actual Input Current Limit Programmed by IIN_HOST or ICO Algorithm	R	Go
0x27/26	ADCVBUS/PSYS Register	Digital Output of Input Voltage and System Power	R	Go
0x29/28	ADCIBAT Register	Digital Output of Battery Charge/Discharge Current	R	Go
0x2B/2A	ADCIINCMPIN Register	Digital Output of Input Current and CMPIN Voltage	R	Go
0x2D/2C	ADCVSYSVBAT Register	Digital Output of System and Battery Voltage	R	Go
0x07/06	OTGVoltage Register	OTG Voltage Setting	R/W	Go
0x09/08	OTGCurrent Register	OTG Output Current Setting	R/W	Go
0x0B/0A	InputVoltage Register	Input Voltage Setting	R/W	Go
0x0D/0C	MinSystemVoltage Register	Minimum System Voltage Setting	R/W	Go
0x0F/0E	IIN_HOST Register	Input Current Limit Set by Host	R/W	Go
0x2E	ManufactureID Register	Manufacture ID - 0x07	R	Go
0x2F	DeviceID Register	Device ID	R	Go
0x3C	ChargeOption4 Register	Charge Option 4	R/W	Go

REGISTER AND DATA

Bit Types:
R/W: Read/Write bit(s)
R: Read only bit(s)
RC: Bit(s) cleared to 0 by being read
PORV: Power-On Reset Value
n: Parameter code formed by the bits as an unsigned binary number.

Setting Charge and nPROCHOT Options

ChargeOption0 Register (I²C Address = 0x01/00) [Reset = 0xE70E]

Table 5. ChargeOption0 Register Details (I²C Address = 0x01)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	EN_LWPWR	Low Power Mode Enable 0 = Disable low power mode. With battery-only, the current/power monitor buffer, nPROCHOT, and comparator follow register setting 1 = Enable low power mode. With battery-only, the device enters low power mode for lowest quiescent current. The LDO of REGN is turned off. IBAT function, PSYS function and ADC are disabled. Independent comparator and nPROCHOT refer to **nPROCHOT during Low Power Mode** section (default)	1	R/W
D[6:5]	WDTMR_ADJ[1:0]	Watchdog Timer Adjust 00 = Disable watchdog timer 01 = 5s 10 = 77s 11 = 153s (default) Set maximum delay between consecutive I²C write of charge voltage or charge current command. If a write on the MaxChargeVoltage register or the ChargeCurrent register is not done within the watchdog period, the watchdog timer expires, and the charger will be suspended (the ChargeCurrent register resets to 0mA). The watchdog timer that is time out will be reset with the first write to ChargeCurrent register, MaxChargeVoltage register or WDTMR_ADJ[1:0]. The charger will resume if the proper values are written.	11	R/W
D[4]	IDPM_AUTO_DISABLE	IDPM Auto Disable 0 = Disable the IDPM auto disable function. CELL_BATPRESZ going low will not disable IDPM (default) 1 = Enable the IDPM auto disable function. CELL_BATPRESZ going low will disable IDPM If CELL_BATPRESZ pin is low, the IDPM function will be disabled automatically by setting EN_IDPM bit = 0. The IDPM function can be enabled later by writing EN_IDPM bit = 1.	0	R/W
D[3]	OTG_ON_CHRGOK	Add OTG to CHRG_OK 0 = Disable (default) 1 = Enable In OTG mode, drive CHRG_OK to high.	0	R/W
D[2]	EN_OOA	Out-of-Audio Enable 0 = No lower limit for PSM burst frequency 1 = Limit PSM burst frequency to above 25kHz for avoiding audio noise (default)	1	R/W
D[1]	PWM_FREQ	Switching Frequency Selection Bit (Choose Based on the Inductor Value) 0 = 1200kHz 1 = 800kHz (default) 800kHz is recommended for 2.2μH or 3.3μH, and 1.2MHz for 1μH.	1	R/W
D[0]	LOW_PTM_RIPPLE	Reduce the Input Voltage and Current Ripple in PTM Mode 0 = Disable 1 = Enable (default)	1	R/W

REGISTER AND DATA (continued)

Table 6. ChargeOption0 Register Details (I²C Address = 0x00)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	Reserved	Reserved.	0	R/W
D[6]	SYS_SHORT_DISABLE	Disable the Hiccup during System Short 0 = Enable hiccup (default) 1 = Disabled hiccup	0	R/W
D[5]	EN_LEARN	In LEARN mode, the battery is allowed to discharge while the adapter is present. Over a complete discharge/charge cycle, the battery gauge is calibrated. When V_{BAT} falls below the battery depletion threshold, the power supply of the system needs to be switched from battery to the input adapter by the host. The device exits LEARN mode and this bit is reset to 0 when CELL_BATPRESZ pin is low. 0 = Disable LEARN mode (default) 1 = Enable LEARN mode	0	R/W
D[4]	IADPT_GAIN	IADPT Amplifier Gain Ratio Selection Bit 0 = 20× (default) 1 = 40× The ratio of IADPT voltage to the sense voltage across ACP and ACN.	0	R/W
D[3]	IBAT_GAIN	IBAT Amplifier Gain Ratio Selection Bit 0 = 8× 1 = 16× (default) The ratio of IBAT voltage to the sense voltage across SRP and SRN.	1	R/W
D[2]	EN_LDO	LDO Mode Enable 0 = Disable LDO mode. BATFET is fully on and charge current follows the ChargeCurrent register setting even when battery voltage is below the programmed minimum system voltage setting in MinSystemVoltage register 1 = Enable LDO mode. BATFET is in LDO mode and pre-charge current follows the ChargeCurrent register setting and is clamped below 384mA (2-cell to 4-cell). The system is regulated at the minimum system voltage (default)	1	R/W
D[1]	EN_IDPM	IDPM Enable 0 = Disable IDPM 1 = Enable IDPM (default)	1	R/W
D[0]	CHRG_INHIBIT	Charge Inhibit 0 = Enable charge (default) 1 = Inhibit charge The device starts charging battery depending on the valid charge current and charge voltage programmed in registers if this bit is 0.	0	R/W

REGISTER AND DATA (continued)

ChargeOption1 Register (I²C Address = 0x31/30) [Reset = 0x0211]

Table 7. ChargeOption1 Register Details (I²C Address = 0x31)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	EN_IBAT	IBAT Output Buffer Enable 0 = Disable IBAT buffer to minimize I_Q (default) 1 = Enable IBAT buffer IBAT buffer is disabled even this bit is 1 if EN_LWPWR bit = 1.	0	R/W
D[6]	Reserved	Reserved.	0	R/W
D[5]	EN_PROCHOT_LPWR	Enable nPROCHOT during Battery-Only Low Power Mode 0 = Disable low power nPROCHOT (default) 1 = Enable VSYS monitor low power nPROCHOT With battery-only, enable VSYS monitor in nPROCHOT with low power consumption, refer to **nPROCHOT during Low Power Mode** section. When adapter is present, this function should be disabled.	0	R/W
D[4]	EN_PSYS	PSYS Sense Circuit and Output Buffer Enable 0 = Disable PSYS buffer to minimize I_Q (default) 1 = Enable PSYS buffer PSYS sense circuit and output buffer are disabled even this bit is 1 if EN_LWPWR bit = 1.	0	R/W
D[3]	RSNS_RAC	Input Sense Resistor R_{AC} 0 = 10mΩ (default) 1 = 20mΩ	0	R/W
D[2]	RSNS_RSR	Charge Sense Resistor R_{SR} 0 = 10mΩ (default) 1 = 20mΩ	0	R/W
D[1]	PSYS_RATIO	PSYS Gain Ratio 0 = 0.25μA/W 1 = 1μA/W (default) The ratio of PSYS output current to the total power of input and battery.	1	R/W
D[0]	PTM_PINSEL	ILIM_HIZ Pin Function Selection Bit 0 = Enter HIZ mode when pull ILIM_HIZ pin to low (default) 1 = Enter PTM mode when pull ILIM_HIZ pin to low	0	R/W

REGISTER AND DATA (continued)

Table 8. ChargeOption1 Register Details (I²C Address = 0x30)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	CMP_REF	Internal Reference Voltage of Independent Comparator 0 = 2.3V (default) 1 = 1.2V	0	R/W
D[6]	CMP_POL	Output Polarity of Independent Comparator 0 = Negative. CMPOUT is low when CMPIN is above internal reference threshold (internal hysteresis) (default) 1 = Positive. CMPOUT is low when CMPIN is below internal reference threshold (external hysteresis)	0	R/W
D[5:4]	CMP_DEG[1:0]	Deglitch Time of Independent Comparator 00 = Disable the independent comparator 01 = Enable independent comparator with 1μs output deglitch time (default) 10 = Enable independent comparator with 2ms output deglitch time 11 = Enable independent comparator with 5s output deglitch time Only applied to the CMPOUT falling edge (HIGH → LOW).	01	R/W
D[3]	FORCE_LATCHOFF	Force Power Path Off 0 = Disable this function (default) 1 = Enable this function When independent comparator is enabled and triggered, Q1 and Q4 are turned off, system is disconnected from the input source, and CHRG_OK signal goes to low. The user must unplug the adapter to clear the LATCHOFF condition to enable the converter again.	0	R/W
D[2]	EN_PTM	PTM Enable 0 = Disable PTM (default) 1 = Enable PTM	0	R/W
D[1]	EN_SHIP_DCHG	Discharge Battery for Shipping Mode 0 = Disable shipping mode (default) 1 = Enable shipping mode When set to 1, discharge battery with 20mA discharge current in 140ms. After the 140ms period, this bit is reset to 0.	0	R/W
D[0]	AUTO_WAKEUP_EN	Auto Wakeup Enable 0 = Disable 1 = Enable (default) When set to 1, if battery voltage is below the minimum system voltage programmed in MinSystemVoltage register, wake-up charge with 128mA charge current for 30mins is automatically enabled. When VBAT exceeds the minimum system voltage, this bit is reset to 0 and the wake-up charge is terminated. Writing a non-zero charge current in ChargeCurrent register also resets this bit to 0.	1	R/W

REGISTER AND DATA (continued)

ChargeOption2 Register (I²C Address = 0x33/32) [Reset = 0x02B7]

Table 9. ChargeOption2 Register Details (I²C Address = 0x33)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:6]	PKPWR_TOVLD_DEG[1:0]	Input Overload Time in Peak Power Mode 00 = 1ms (default) 01 = 2ms 10 = 10ms 11 = 20ms	00	R/W
D[5]	EN_PKPWR_IDPM	Enable Input Current Overshoot to Trigger Peak Power Mode 0 = Disable input current overshoot to trigger peak power mode (default) 1 = Enable input current overshoot to trigger peak power mode If both EN_PKPWR_IDPM and EN_PKPWR_VSYS are 0, the peak power mode is disabled. These bits are both reset to 0 when adapter removal.	0	R/W
D[4]	EN_PKPWR_VSYS	Enable System Voltage Under-Shoot to Trigger Peak Power Mode 0 = Disable system voltage under-shoot to trigger peak power mode (default) 1 = Enable system voltage under-shoot to trigger peak power mode If both EN_PKPWR_IDPM and EN_PKPWR_VSYS are 0, the peak power mode is disabled. These bits are both reset to 0 when adapter removal.	0	R/W
D[3]	PKPWR_OVLD_STAT	Status bit indicates that it is in overload cycle. Write 0 to this bit to exit the overload cycle. 0 = Not in overload cycle (default) 1 = In overload cycle	0	R/W
D[2]	PKPWR_RELAX_STAT	Status bit indicates that it is in relax cycle. Write 0 to this bit to exit the relax cycle. 0 = Not in relax cycle (default) 1 = In relax cycle	0	R/W
D[1:0]	PKPWR_TMAX[1:0]	Peak Power Mode Overload and Relax Cycle Time 00 = 5ms 01 = 10ms 10 = 20ms (default) 11 = 40ms When PKPWR_TMAX[1:0] is shorter than PKPWR_TOVLD_DEG[1:0], the device work in overload stat all the time.	10	R/W

Table 10. ChargeOption2 Register Details (I²C Address = 0x32)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	EN_EXTILIM	Enable ILIM_HIZ Pin to Set External Input Current Limit 0 = Disable ILIM_HIZ pin to set external input current limit 1 = Enable ILIM_HIZ pin to set external input current limit. The actual input current limit is set by the lower value of external input current limit, IIN_DPM and IIN_HOST registers (default)	1	R/W
D[6]	EN_ICHG_IDCHG	0 = IBAT pin output represents discharge current (default) 1 = IBAT pin output represents charge current	0	R/W
D[5]	Q2_OCP	Q2 OCP Threshold Sensed by Q2 V_{DS} Voltage 0 = 225mV 1 = 150mV (default) It is the valley current for Q2.	1	R/W
D[4]	ACX_OCP	Input Current OCP Threshold Sensed by the Voltage across ACP and ACN 0 = 280mV 1 = 150mV (default) It is the peak current limit for Q1.	1	R/W
D[3]	EN_ACOC	ACOC Enable 0 = Disable ACOC (default) 1 = Enable ACOC If ACOC is detected, the converter is disabled.	0	R/W
D[2]	ACOC_VTH	ACOC Limit (Adapter Average Current as Percentage of ILIM2) 0 = 133% 1 = 200% (default)	1	R/W
D[1]	EN_BATOC	Battery Discharge Over-Current (BATOC) Enable 0 = Disable BATOC 1 = Enable BATOC (default) If BATOC is detected, the converter is disabled.	1	R/W
D[0]	BATOC_VTH	Battery Discharge Over-Current Threshold Sensed by the Voltage across SRN and SRP (As Percentage of IDCHG_VTH[5:0]) 0 = 133% 1 = 200% (default)	1	R/W

REGISTER AND DATA (continued)

ChargeOption3 Register (I²C Address = 0x35/34) [Reset = 0x0030]

Table 11. ChargeOption3 Register Details (I²C Address = 0x35)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	EN_HIZ	HIZ Mode Enable 0 = Disable HIZ mode (default) 1 = Enable HIZ mode In HIZ mode, the device operates with the low quiescent current. And the system is powered from battery when the input source is present. During this mode, the LDO of REGN is enabled.	0	R/W
D[6]	RESET_REG	Reset Registers All the registers are reset to default except VINDPM register. 0 = Idle (default) 1 = Reset the registers to default. This bit is reset to 0 after reset Using this bit to reset the registers to default is not recommended when the battery voltage is below minimal system voltage or in battery removal.	0	R/W
D[5]	RESET_VINDPM	Reset VINDPM Threshold 0 = Idle (default) 1 = Temporary disable the converter to measure VINDPM threshold. After the measurement is done, this bit is reset to 0 and converter restarts	0	R/W
D[4]	EN_OTG	OTG Enable 0 = Disable OTG (default) 1 = Enable OTG	0	R/W
D[3]	EN_ICO_MODE	Enable ICO 0 = Disable ICO (default) 1 = Enable ICO	0	R/W
D[2:0]	Reserved	Reserved.	000	R/W

Table 12. ChargeOption3 Register Details (I²C Address = 0x34)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	Reserved	Reserved.	0	R/W
D[6]	EN_CON_VAP	Enable the Conservative VAP Mode 0 = Disabled. When V_{SYS} < V_{SYS_TH2}, generate an nPROCHOT pulse if PROCHOT_PROFILE_VSYS bit = 1 (default) 1 = Enabled. When V_{VBUS} < $V_{VBUS\_CONVENZ}$, generate an nPROCHOT pulse if PROCHOT_PROFILE_VSYS bit = 1	0	R/W
D[5]	OTG_VAP_MODE	OTG/VAP Pin Control Selection 0 = The OTG/VAP pin controls the enable/disable of VAP 1 = The OTG/VAP pin controls the enable/disable of OTG (default)	1	R/W
D[4:3]	IL_AVG[1:0]	Inductor Average Current Clamp Selection 00 = 6A 01 = 10A 10 = 15A (default) 11 = Disabled	10	R/W
D[2]	OTG_RANGE_LOW	OTG Output Voltage Range Selection 0 = High range 4.28V to 20.56V (default) 1 = Low range 3V to 19.28V	0	R/W
D[1]	BATFETOFF_HIZ	BATFET On/Off during HIZ Mode 0 = On (default) 1 = Off	0	R/W
D[0]	PSYS_OTG_IDCHG	PSYS Function during OTG Mode 0 = PSYS reports the battery discharge power minus OTG output power (default) 1 = PSYS reports the battery discharge power only	0	R/W

REGISTER AND DATA (continued)

ProchotOption0 Register (I²C Address = 0x37/36) [Reset = 0x4A65]

Table 13. ProchotOption0 Register Details (I²C Address = 0x37)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:3]	ILIM2_VTH[4:0]	I_{LIM2} Threshold Sensed by the Voltage between ACP and ACN (As Percentage of the Value Setting in IIN_HOST Register) 00001 - 11001 = 110% - 230%, step 5% 11010 - 11110 = 250% - 450%, step 50% 11111 = Out of range (ignored) Default: 150%, or 01001	0 1001	R/W
D[2:1]	ICRIT_DEG[1:0]	ICRIT Deglitch Time to Trigger nPROCHOT I_{CRIT} is 110% of I_{LIM2}. 00 = 15μs 01 = 100μs (default) 10 = 400μs (500μs MAX) 11 = 800μs (1ms MAX)	01	R/W
D[0]	PROCHOT_ VDPM_80_90	Lower Threshold of the PROCHOT_VDPM Comparator (As Percentage of VINDPM Threshold) 0 = 80% (default) 1 = 90% The threshold of the PROCHOT_VDPM comparator is determined by this bit if LOWER_PROCHOT_VDPM bit = 1.	0	R/W

Table 14. ProchotOption0 Register Details (I²C Address = 0x36)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:4]	VSYS_TH1[3:0]	VSYS Threshold to Discharge VBUS in VAP Mode In VAP mode, when the VSYS pin voltage is below this threshold with fixed 5μs deglitch time, VBUS starts to discharge. For 2-cell to 4-cell batteries: 0000 - 1111 = 5.9V - 7.4V with 0.1V step Default: 0b0110, V_{SYS_TH1} = 6.5V For 1-cell battery: 0000 - 0111 = 3.1V - 3.8V with 0.1V step 1000 - 1111 = 3.1V - 3.8V with 0.1V step Default: 0b0110, V_{SYS_TH1} = 3.7V	0110	R/W
D[3:2]	VSYS_TH2[1:0]	VSYS Threshold to Assert PROCHOT_VSYS When the VSYS pin voltage is below this threshold with fixed 5μs deglitch time, assert the PROCHOT_VSYS. For 2-cell to 4-cell batteries: 00 = 5.9V 01 = 6.2V (default) 10 = 6.4V 11 = 6.8V For 1-cell battery: 00 = 3.1V 01 = 3.3V (default) 10 = 3.5V 11 = 3.7V	01	R/W
D[1]	INOM_DEG	INOM Deglitch Time 0 = 1ms (MAX) (default) 1 = 50ms (MAX 65ms) INOM is 110% of the input current limit setting in IIN_HOST register. When the current sensed by voltage across ACP and ACN is above INOM with this deglitch time, INOM is triggered.	0	R/W
D[0]	LOWER_PROCHOT _VDPM	Lower Threshold of the PROCHOT_VDPM Comparator Enable 0 = Disable. The PROCHOT_VDPM comparator threshold follows the InputVoltage register setting 1 = Enable. The PROCHOT_VDPM comparator threshold is lower and determined by PROCHOT_VDPM_80_90 bit setting (default)	1	R/W

REGISTER AND DATA (continued)

ProchotOption1 Register (I²C Address = 0x39/38) [Reset = 0x81A0]

When the bit in REG0x38 is set to 0, the nPROCHOT pin will not be pulled low when the associated event happens, and the event will not be reported in ProchotStatus[7:0] register (I²C address = 0x22).

Table 15. ProchotOption1 Register Details (I²C Address = 0x39)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:2]	IDCHG_VTH[5:0]	IDCHG Threshold IDCHG is measured by the sensed voltage between SRN and SRP. IDCHG is triggered when the discharge current is above this threshold. Range from 0A to 32256mA with 512mA step. If the value is programmed to 000000b, IDCHG threshold is 128mA. Default: 100000b for16384mA	10 0000	R/W
D[1:0]	IDCHG_DEG[1:0]	IDCHG Deglitch Time 00 = 1.6ms 01 = 100μs (default) 10 = 6ms 11 = 12ms	01	R/W

Table 16. ProchotOption1 Register Details (I²C Address = 0x38)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	PROCHOT _PROFILE_VDPM	Enable PROCHOT_PROFILE_VDPM 0 = Disable 1 = Enable (default) This bit detects the VBUS voltage.	1	R/W
D[6]	PROCHOT _PROFILE_COMP	Enable PROCHOT_PROFILE_COMP 0 = Disable (default) 1 = Enable	0	R/W
D[5]	PROCHOT _PROFILE_ICRIT	Enable PROCHOT_PROFILE_ICRIT 0 = Disable 1 = Enable (default)	1	R/W
D[4]	PROCHOT _PROFILE_INOM	Enable PROCHOT_PROFILE_INOM 0 = Disable (default) 1 = Enable	0	R/W
D[3]	PROCHOT _PROFILE_IDCHG	Enable PROCHOT_PROFILE_IDCHG 0 = Disable (default) 1 = Enable	0	R/W
D[2]	PROCHOT _PROFILE_VSYS	Enable PROCHOT_PROFILE_VSYS 0 = Disable (default) 1 = Enable (one-shot trigger) When the device enters the VAP mode, PROCHOT_PROFILE_VSYS bit will be automatically set to 1.	0	R/W
D[1]	PROCHOT _PROFILE_BATPRES	Enable PROCHOT_PROFILE_BATPRES 0 = Disable (default) 1 = Enable (one-shot falling edge triggered) If PROCHOT_PROFILE_BATPRES is enabled in nPROCHOT after the battery removal, one-shot nPROCHOT pulse will be send immediately.	0	R/W
D[0]	PROCHOT _PROFILE_ACOK	Enable PROCHOT_PROFILE_ACOK 0 = Disable (default) 1 = Enable (one-shot trigger) This bit detects adapter removal.	0	R/W

REGISTER AND DATA (continued)

ADCOption Register (I²C Address = 0x3B/3A) [Reset = 0x2000]

The ADC registers reading order: VBAT, VSYS, ICHG, IDCHG, IIN, PSYS, VBUS, and CMPIN. In low power mode, ADC is disabled.

Table 17. ADCOption Register Details (I²C Address = 0x3B)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	ADC_CONV	ADC Conversion Update Mode Selection 0 = One-shot update. Update the registers of ADCVBUS/PSYS, ADCIBAT, ADCIINCMPIN and ADCVSYSVBAT once after ADC_START = 1 (default) 1 = Continuous update. Update the registers of ADCVBUS/PSYS, ADCIBAT, ADCIINCMPIN and ADCVSYSVBAT every 1 second The typical time of ADC conversion is 10ms.	0	R/W
D[6]	ADC_START	0 = No ADC conversion (default) 1 = Start ADC conversion This bit automatically resets to 0 when the one-shot update is completed.	0	R/W
D[5]	ADC_FULLSCALE	ADC Input Voltage Range 0 = 2.04V (recommended when input voltage is below 5V or 1-cell battery) 1 = 3.06V (default)	1	R/W
D[4:0]	Reserved	Reserved.	0 0000	R/W

Table 18. ADCOption Register Details (I²C Address = 0x3A)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	EN_ADC_CMPIN	0 = Disable (default) 1 = Enable	0	R/W
D[6]	EN_ADC_VBUS	0 = Disable (default) 1 = Enable	0	R/W
D[5]	EN_ADC_PSYS	0 = Disable (default) 1 = Enable	0	R/W
D[4]	EN_ADC_IIN	0 = Disable (default) 1 = Enable	0	R/W
D[3]	EN_ADC_IDCHG	0 = Disable (default) 1 = Enable	0	R/W
D[2]	EN_ADC_ICHG	0 = Disable (default) 1 = Enable	0	R/W
D[1]	EN_ADC_VSYS	0 = Disable (default) 1 = Enable	0	R/W
D[0]	EN_ADC_VBAT	0 = Disable (default) 1 = Enable	0	R/W

REGISTER AND DATA (continued)

Charge and nPROCHOT Status

ChargerStatus Register (I²C Address = 0x21/20) [Reset = 0x0000]

Table 19. ChargerStatus Register Details (I²C Address = 0x21)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	AC_STAT	0 = Input is not present (default) 1 = Input is present	0	R
D[6]	ICO_DONE	The bit is set to 1 when the ICO routine is successfully executed. 0 = ICO is not complete (default) 1 = ICO is complete	0	R
D[5]	IN_VAP	0 = Not in VAP mode (default) 1 = In VAP mode	0	R
D[4]	IN_VINDPM	0 = Not in VINDPM during the forward mode, or not in voltage regulation during OTG mode (default) 1 = In VINDPM during the forward mode, or in voltage regulation during OTG mode	0	R
D[3]	IN_IINDPM	0 = Not in IINDPM (default) 1 = In IINDPM	0	R
D[2]	IN_FCHRG	0 = Not in fast charge (default) 1 = In fast charger	0	R
D[1]	IN_PCHRG	0 = Not in pre-charge (default) 1 = In pre-charge	0	R
D[0]	IN_OTG	0 = Not in OTG (default) 1 = In OTG	0	R

Table 20. ChargerStatus Register Details (I²C Address = 0x20)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	Fault ACOV	0 = No fault (default) 1 = ACOV fault has occurred. After the ACOV fault disappears, host reads this bit to reset it to 0	0	RC
D[6]	Fault BATOC	0 = No fault (default) 1 = BATOC fault has occurred. After the BATOC fault disappears, host reads this bit to reset it to 0	0	RC
D[5]	Fault ACOC	0 = No fault (default) 1 = ACOC fault has occurred. After the ACOC fault disappears, host reads this bit to reset it to 0	0	RC
D[4]	SYSOVP_STAT	SYSOVP Status and Clear Bit 0 = Not in SYSOVP (default) 1 = SYSOVP has occurred. During SYSOVP, the converter is disabled. To clear SYSOVP condition and re-enable the converter (after OVP cleared), the adapter must be unplugged or this bit must be reset to 0 by the host.	0	R/W
D[3]	Fault SYS_SHORT	0 = No fault (default) 1 = In hiccup mode (SYS_SHORT_DISABLE = 0), SYS_SHORT 7 times restarts fail fault has occurred. Host writes this bit to 0 to clear the SYS_SHORT latch	0	R/W
D[2]	Fault Latchoff	0 = No fault (default) 1 = Latch off (FORCE_LATCHOFF bit) fault has occurred. After the latch off fault disappears, host reads this bit to reset it to 0	0	RC
D[1]	Fault_OTG_OVP	0 = No fault (default) 1 = OTG OVP fault has occurred. After the OTG OVP fault disappears, host reads this bit to reset it to 0	0	RC
D[0]	Fault_OTG_UVP	0 = No fault (default) 1 = OTG UVP fault has occurred. After the OTG UVP fault disappears, host reads this bit to reset it to 0	0	RC

REGISTER AND DATA (continued)

ProchotStatus Register (I²C Address = 0x23/22) [Reset = 0xA800]

Table 21. ProchotStatus Register Details (I²C Address = 0x23)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	Reserved	Reserved.	1	R
D[6]	EN_PROCHOT_EXT	nPROCHOT Pulse Extension Enable 0 = Disable (default) 1 = Enable When it is enabled, the nPROCHOT pin voltage keeps low until PROCHOT_CLEAR bit = 0 is written.	0	R/W
D[5:4]	PROCHOT_WIDTH[1:0]	Minimum nPROCHOT Pulse Width when EN_PROCHOT_EXT Bit = 0 00 = 100μs 01 = 1ms 10 = 10ms (default) 11 = 5s	10	R/W
D[3]	PROCHOT_CLEAR	nPROCHOT Pulse Clear when EN_PROCHOT_EXT Bit = 1 0 = Clear nPROCHOT pulse and drive nPROCHOT pin high 1 = Idle (default)	1	R/W
D[2]	TSHUT	TDIE Thermal Shutdown Fault Status Bit 0 = No TDIE thermal shutdown fault (default) 1 = Device in TDIE thermal shutdown fault status After the TSHUT fault disappears, the host reads this bit to reset it to 0.	0	RC
D[1]	STAT_VAP_FAIL	The failure that charging VBUS for 7 consecutive times in VAP mode shows either VBAT is too low to enter VAP mode, or the VAP load current is set too high. 0 = Not in VAP failure (default) 1 = In VAP failure, charger exits VAP mode automatically (OTG_VAP_MODE bit = 1), and latches off until the host resets this bit to 0	0	R/W
D[0]	STAT_EXIT_VAP	In VAP mode, the charger can exit VAP mode by either being disabled through host, or any charger faults occurs. 0 = STAT_EXIT_VAP is not active (default) 1 = STAT_EXIT_VAP is active. nPROCHOT pin keeps low until host writes 0 to this bit	0	R/W

Table 22. ProchotStatus Register Details (I²C Address = 0x22)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	STAT_VDPM	0 = Not triggered (default) 1 = Triggered. nPROCHOT pin keeps low until host writes 0 to this bit when PROCHOT_PROFILE_VDPM bit = 1	0	R/W
D[6]	STAT_COMP	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse when PROCHOT_PROFILE_COMP bit = 1. After CMPOUT pin goes high, host reads this bit to reset it to 0	0	RC
D[5]	STAT_ICRIT	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse when PROCHOT_PROFILE_ICRIT bit = 1. After adapter peak current falls below 110% of I_{LIM2}, host reads this bit to reset it to 0	0	RC
D[4]	STAT_INOM	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse when PROCHOT_PROFILE_INOM bit = 1. After adapter average current falls below 110% of IINDPM, host reads this bit to reset it to 0	0	RC
D[3]	STAT_IDCHG	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse when PROCHOT_PROFILE_IDCHG bit = 1. After battery discharge current falls below IDCHG_VTH, host reads this bit to reset it to 0	0	RC
D[2]	STAT_VSYS	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse (one shot trigger, not extend with the fault condition) when PROCHOT_PROFILE_VSYS bit = 1. Host reads this bit to reset it to 0	0	RC
D[1]	STAT_Battery_Removal	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse (one shot trigger, not extend with the fault condition) when PROCHOT_PROFILE_BATPRES bit = 1. Host reads this bit to reset it to 0	0	RC
D[0]	STAT_Adapter_Removal	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse (one shot trigger, not extend with the fault condition) when PROCHOT_PROFILE_ACOK bit = 1. After V_{VBUS} > 3.58V and CHRG_OK pin goes high, host reads this bit to reset it to 0	0	RC

REGISTER AND DATA (continued)

ChargeCurrent Register

Charge current is set in ChargeCurrent register (REG0x03/02). When a 10mΩ sense resistor is used, the charge current range is 64mA to 8.128A with 64mA resolution.

The ChargeCurrent register will be set to 0A when:

1. Auto wakeup is not active after POR.
2. The CELL_BATPRESZ goes low.
3. Write MaxChargeVoltage register to 0.
4. Adapter plugs out.
5. Watchdog timer out.

The default current sense resistor R_{SR} between SRP and SRN is 10mΩ, other value resistor can also be used. Larger sense resistor will increase the regulation accuracy but increase the conduction loss at the same time, thus values above 20mΩ are not recommended.

Battery Pre-Charge Current Clamp

In pre-charge, BATFET operates in linear (LDO) mode when EN_LDO bit = 1. For 2-cell/3-cell/4-cell battery, VSYS voltage is regulated at minimum system voltage and the maximum pre-charge current is 384mA. For 1-cell battery, the pre-charge current is clamped at 384mA. When VBAT is above 3V but below minimum system voltage, the BATFET operates in LDO mode and the charge current is clamped at 2A.

ChargeCurrent Register with 10mΩ Sense Resistor (I²C Address = 0x03/02) [Reset = 0x0000]

Table 23. ChargeCurrent Register with 10mΩ Sense Resistor Details (I²C Address = 0x03)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:5]	Reserved	Reserved.	000	R/W
D[4]	Charge Current, Bit 6	0 = Add 0mA of charger current (default) 1 = Add 4096mA of charger current	0	R/W
D[3]	Charge Current, Bit 5	0 = Add 0mA of charger current (default) 1 = Add 2048mA of charger current	0	R/W
D[2]	Charge Current, Bit 4	0 = Add 0mA of charger current (default) 1 = Add 1024mA of charger current	0	R/W
D[1]	Charge Current, Bit 3	0 = Add 0mA of charger current (default) 1 = Add 512mA of charger current	0	R/W
D[0]	Charge Current, Bit 2	0 = Add 0mA of charger current (default) 1 = Add 256mA of charger current	0	R/W

Table 24. ChargeCurrent Register with 10mΩ Sense Resistor Details (I²C Address = 0x02)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	Charge Current, Bit 1	0 = Add 0mA of charger current (default) 1 = Add 128mA of charger current	0	R/W
D[6]	Charge Current, Bit 0	0 = Add 0mA of charger current (default) 1 = Add 64mA of charger current	0	R/W
D[5:0]	Reserved	Reserved.	00 0000	R/W

REGISTER AND DATA (continued)

MaxChargeVoltage Register (I²C Address = 0x05/04) [Reset Value Based on CELL_ BATPRESZ Pin Setting]

Charge voltage is set in MaxChargeVoltage register (REG0x05/04). The charge voltage range is 1.024V to 19.200V with 8mV resolution.

The MaxChargeVoltage register is set to 4200mV for 1-cell, 8400mV for 2-cell, 12600mV for 3-cell or 16800mV for 4-cell by default. After CHRG_OK goes high, the charge will start depending on the charge current setting in ChargeCurrent register and the charge voltage setting in MaxChargeVoltage register. MaxChargeVoltage register needs to be set before ChargeCurrent register for correct battery voltage setting if battery voltage is different from 4.2V/cell. Writing MaxChargeVoltage register to 0 will set MaxChargeVoltage register to the corresponding value depending on CELL_BATPRESZ pin (refer to Battery Cell Configuration section).

The battery voltage is sensed on SRN pin for regulation, and the battery should be placed as close to SRN pin as possible.

Table 25. MaxChargeVoltage Register Details (I²C Address = 0x05)

BITS	BIT NAME	DESCRIPTION		PORV	TYPE
D[7]	Reserved	Reserved.		0	R/W
D[6]	Max Charge Voltage, Bit 11	0 = Add 0mV of charger voltage (default) 1 = Add 16384mV of charger voltage	n_2 = D[6:0] $n = n_1$ (1) + 32×n_2 MaxChargeVoltage Value = 8×n (mV) (n ≥ 128)	0	R/W
D[5]	Max Charge Voltage, Bit 10	0 = Add 0mV of charger voltage (default) 1 = Add 8192mV of charger voltage		0	R/W
D[4]	Max Charge Voltage, Bit 9	0 = Add 0mV of charger voltage (default) 1 = Add 4096mV of charger voltage		0	R/W
D[3]	Max Charge Voltage, Bit 8	0 = Add 0mV of charger voltage (default) 1 = Add 2048mV of charger voltage		0	R/W
D[2]	Max Charge Voltage, Bit 7	0 = Add 0mV of charger voltage (default) 1 = Add 1024mV of charger voltage		0	R/W
D[1]	Max Charge Voltage, Bit 6	0 = Add 0mV of charger voltage (default) 1 = Add 512mV of charger voltage		0	R/W
D[0]	Max Charge Voltage, Bit 5	0 = Add 0mV of charger voltage (default) 1 = Add 256mV of charger voltage		0	R/W

NOTE:

1. For details of n_1, see Table 26.

Table 26. MaxChargeVoltage Register Details (I²C Address = 0x04)

BITS	BIT NAME	DESCRIPTION		PORV	TYPE
D[7]	Max Charge Voltage, Bit 4	0 = Add 0mV of charger voltage (default) 1 = Add 128mV of charger voltage	n_1 = D[7:3] $n = n_1 + 32×n_2$ (1) MaxChargeVoltage Value = 8×n (mV) (n ≥ 128)	0	R/W
D[6]	Max Charge Voltage, Bit 3	0 = Add 0mV of charger voltage (default) 1 = Add 64mV of charger voltage		0	R/W
D[5]	Max Charge Voltage, Bit 2	0 = Add 0mV of charger voltage (default) 1 = Add 32mV of charger voltage		0	R/W
D[4]	Max Charge Voltage, Bit 1	0 = Add 0mV of charger voltage (default) 1 = Add 16mV of charger voltage		0	R/W
D[3]	Max Charge Voltage, Bit 0	0 = Add 0mV of charger voltage (default) 1 = Add 8mV of charger voltage		0	R/W
D[2:0]	Reserved	Reserved.		000	R/W

NOTE:

1. For details of n_2, see Table 25.

REGISTER AND DATA (continued)

MinSystemVoltage Register

The minimum system voltage is set in MinSystemVoltage register (REG0x0D/0C). The minimum system voltage range is 1.024V to 16.128V with 256mV resolution. Any out-of-range write is ignored. The MinSystemVoltage register is set to 3.584V for 1-cell, 6.144V for 2-cell, 9.216V for 3-cell, and 12.288V for 4-cell by default. Writing MinSystemVoltage register to 0 will set MinSystemVoltage register to the corresponding value depending on CELL_BATPRESZ pin (refer to Battery Cell Configuration section).

System Voltage Regulation

The system is separated from battery by BATFET, and the system is regulated above the minimum system voltage setting in MinSystemVoltage register even if the battery is completely depleted or removed.

The BATFET is in LDO mode and the system is regulated above V_{SYSMIN} when the battery voltage is below V_{SYSMIN}.

When the battery voltage is above V_{SYSMIN}, the BATFET is fully on (during charge or in the supplement mode) and the system voltage is regulated at battery voltage plus the V_{DS} of BATFET. The BATFET is off and the system voltage is regulated at battery voltage plus about 180mV when the charge is disabled or no supplement mode.

VSYS is shorted to SRP if BATFET is removed. At this condition, LDO mode must be disabled before starting converter. Follow the sequence below to configure charger.

1. Before the adapter is plugged in, set the charger into HIZ mode by pulling ILIM_HIZ pin to ground or setting EN_HIZ bit to 1.
2. Disable LDO mode by setting EN_LDO bit to 0.
3. Disable auto-wakeup mode by setting AUTO_WAKEUP_EN bit to 0.
4. Make sure the battery voltage is set properly in MaxChargeVoltage register.
5. Set pre-charge/charge current in ChargeCurrent register.
6. Exit HIZ mode by releasing ILIM_HIZ from ground and set EN_HIZ bit to 0.

When exiting HIZ mode, the low input current limit (a few hundred milliamps) should be set to avoid accidental SW mistakes.

MinSystemVoltage Register (I²C Address = 0x0D/0C) [Reset Value Based on CELL_BATPRESZ Pin Setting]

Table 27. MinSystemVoltage Register Details (I²C Address = 0x0D)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:6]	Reserved	Reserved.	00	R/W
D[5]	Minimum System Voltage, Bit 5	n = D[5:0] Minimum System Voltage Value = 256×n (mV) (n ≥ 4) Range: 1024mV (00 0100) - 16128mV (11 1111)	0	R/W
D[4]	Minimum System Voltage, Bit 4		0	R/W
D[3]	Minimum System Voltage, Bit 3		1	R/W
D[2]	Minimum System Voltage, Bit 2		1	R/W
D[1]	Minimum System Voltage, Bit 1		1	R/W
D[0]	Minimum System Voltage, Bit 0		0	R/W

Table 28. MinSystemVoltage Register Details (I²C Address = 0x0C)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:0]	Reserved	Reserved.	0000 0000	R/W

REGISTER AND DATA (continued)

Input Current and Input Voltage Registers for Dynamic Power Management

The SGM41573 features dynamic power management (DPM). When the input current tries to exceed the input current limits or the input voltage tends to fall below the input voltage limit, the device gives priority to provide system load by reducing the battery charge current adequately to avoid the input parameter (voltage or current) exceeding the limit.

If the charge current is decreased and reached to zero, but the input is still overloaded, the system voltage starts to drop with the system load rising. When the system voltage drops below the battery voltage, the device operates in the supplement mode and the battery provides a portion of system power demand through BATFET.

Input Current Limit Registers

The input current limit is set in IIN_HOST register (REG0x0F/0E). With a 10mΩ sense resistor, the input current limit range is 50mA to 6350mA with 50mA resolution. The default input current limit is 3.25A. The input current limit is reset to the default value when the adapter is removed, and the input current limit is 50mA when the IIN_HOST register code is set to 0.

The default current sense resistor R_{AC} between ACP and ACN is 10mΩ, the other value resistor such as 20mΩ can also be used. Larger sense resistor will increase the regulation accuracy, but will increase the conduction loss at the same time.

External input current limit can be set by ILIM_HIZ pin voltage using the following equation, in which I_{DPM} is the target input current limit.

$$V_{ILIM\_HIZ} = 1V + 40 \times (V_{ACP} - V_{ACN}) = 1+ 40 \times I_{DPM} \times R_{AC} \quad (2)$$

Writing EN_EXTILIM bit to 0 or pulling ILIM_HIZ pin above 4.0V can disable ILIM_HIZ pin.

IIN_HOST Register with 10mΩ Sense Resistor (I²C Address = 0x0F/0E) [Reset = 0x4100]

Table 29. IIN_HOST Register with 10mΩ Sense Resistor Details (I²C Address = 0x0F)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	Reserved	Reserved.	0	R/W
D[6]	Input Current set by Host, Bit 6	n = D[6:0] IIN_HOST Value = 50×n (mA) (n ≠ 0) Range: 50mA (000 0001) - 6350mA (111 1111)	1	R/W
D[5]	Input Current set by Host, Bit 5		0	R/W
D[4]	Input Current set by Host, Bit 4		0	R/W
D[3]	Input Current set by Host, Bit 3		0	R/W
D[2]	Input Current set by Host, Bit 2		0	R/W
D[1]	Input Current set by Host, Bit 1		0	R/W
D[0]	Input Current set by Host, Bit 0		1	R/W

NOTE: The low clamp value is 0b0000001.

Table 30. IIN_HOST Register with 10mΩ Sense Resistor Details (I²C Address = 0x0E)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:0]	Reserved	Reserved.	0000 0000	R

REGISTER AND DATA (continued)

IIN_DPM Register with 10mΩ Sense Resistor (I²C Address = 0x25/24) [Reset = 0x4100]

IIN_DPM register reports the actual input current limit programmed by IIN_HOST or ICO algorithm. ICO algorithm may change the input current limit and the value in IIN_DPM register. The input current limit read-back value is 50mA when IIN_DPM register code is 0. Refer to Table 31 and Table 32.

InputVoltage Register (I²C Address = 0x0B/0A) [Reset = VBUS - 1.28V]

The input voltage limit is set in InputVoltage register (REG0x0B/0A). When the input voltage drops below the value programmed in InputVoltage register, the charger enters VINDPM. The default value of input voltage limit is 1.28V below the no-load VBUS voltage, and the value is 3.2V when the InputVoltage register code is set to 0. Refer to Table 33 and Table 34.

Table 31. IIN_DPM Register with 10mΩ Sense Resistor Details (I²C Address = 0x25)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	Reserved	Reserved.	0	R
D[6]	Input Current in DPM, Bit 6	n = D[6:0] Input Current Limit Read-Back Value = 50 (mA) (n = 0) Input Current Limit Read-Back Value = 50×n (mA) (n ≠ 0) Range: 50mA (000 0000) - 6350mA (111 1111)	1	R
D[5]	Input Current in DPM, Bit 5		0	R
D[4]	Input Current in DPM, Bit 4		0	R
D[3]	Input Current in DPM, Bit 3		0	R
D[2]	Input Current in DPM, Bit 2		0	R
D[1]	Input Current in DPM, Bit 1		0	R
D[0]	Input Current in DPM, Bit 0		1	R

Table 32. IIN_DPM Register with 10mΩ Sense Resistor Details (I²C Address = 0x24)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:0]	Reserved	Reserved.	0000 0000	R

Table 33. InputVoltage Register Details (I²C Address = 0x0B)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:6]	Reserved	Reserved.	00	R/W
D[5]	Input Voltage, Bit 7	0 = Add 0mV of input voltage (default) 1 = Add 8192mV of input voltage	0	R/W
D[4]	Input Voltage, Bit 6	0 = Add 0mV of input voltage (default) 1 = Add 4096mV of input voltage	0	R/W
D[3]	Input Voltage, Bit 5	0 = Add 0mV of input voltage (default) 1 = Add 2048mV of input voltage	0	R/W
D[2]	Input Voltage, Bit 4	0 = Add 0mV of input voltage (default) 1 = Add 1024mV of input voltage	0	R/W
D[1]	Input Voltage, Bit 3	0 = Add 0mV of input voltage (default) 1 = Add 512mV of input voltage	0	R/W
D[0]	Input Voltage, Bit 2	0 = Add 0mV of input voltage (default) 1 = Add 256mV of input voltage	0	R/W

Table 34. InputVoltage Register Details (I²C Address = 0x0A)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	Input Voltage, Bit 1	0 = Add 0mV of input voltage (default) 1 = Add 128mV of input voltage	0	R/W
D[6]	Input Voltage, Bit 0	0 = Add 0mV of input voltage (default) 1 = Add 64mV of input voltage	0	R/W
D[5:0]	Reserved	Reserved.	00 0000	R/W

REGISTER AND DATA (continued)

OTGVoltage Register (I²C Address = 0x07/06) [Reset = 0x0000]

The OTG output voltage limit is set in OTGVoltage register (REG0x07/06). The range of OTG output voltage limit is 3V to 20.56V. Although it is possible to successfully write the registers with a value below the minimum or above the maximum, the actual OTG output voltage is limited. The DAC offset is 1.28V when OTG_RANGE_LOW bit = 0, and there is no offset when OTG_RANGE_LOW bit = 1.

Table 35. OTGVoltage Register Details (I²C Address = 0x07)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:6]	Reserved	Reserved.	00	R/W
D[5]	OTG Voltage, Bit 11	0 = Add 0mV of OTG voltage (default) 1 = Add 16384mV of OTG voltage	0	R/W
D[4]	OTG Voltage, Bit 10	0 = Add 0mV of OTG voltage (default) 1 = Add 8192mV of OTG voltage	0	R/W
D[3]	OTG Voltage, Bit 9	0 = Add 0mV of OTG voltage (default) 1 = Add 4096mV of OTG voltage	0	R/W
D[2]	OTG Voltage, Bit 8	0 = Add 0mV of OTG voltage (default) 1 = Add 2048mV of OTG voltage	0	R/W
D[1]	OTG Voltage, Bit 7	0 = Add 0mV of OTG voltage (default) 1 = Add 1024mV of OTG voltage	0	R/W
D[0]	OTG Voltage, Bit 6	0 = Add 0mV of OTG voltage (default) 1 = Add 512mV of OTG voltage	0	R/W

Table 36. OTGVoltage Register Details (I²C Address = 0x06)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	OTG Voltage, Bit 5	0 = Add 0mV of OTG voltage (default) 1 = Add 256mV of OTG voltage	0	R/W
D[6]	OTG Voltage, Bit 4	0 = Add 0mV of OTG voltage (default) 1 = Add 128mV of OTG voltage	0	R/W
D[5]	OTG Voltage, Bit 3	0 = Add 0mV of OTG voltage (default) 1 = Add 64mV of OTG voltage	0	R/W
D[4]	OTG Voltage, Bit 2	0 = Add 0mV of OTG voltage (default) 1 = Add 32mV of OTG voltage	0	R/W
D[3]	OTG Voltage, Bit 1	0 = Add 0mV of OTG voltage (default) 1 = Add 16mV of OTG voltage	0	R/W
D[2]	OTG Voltage, Bit 0	0 = Add 0mV of OTG voltage (default) 1 = Add 8mV of OTG voltage	0	R/W
D[1:0]	Reserved	Reserved.	00	R/W

REGISTER AND DATA (continued)

OTGCurrent Register (I²C Address = 0x09/08) [Reset = 0x0000]

The OTG output current limit is set in OTGCurrent register (REG0x09/08).

Table 37. OTGCurrent Register Details (I²C Address = 0x09)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	Reserved	Reserved.	0	R/W
D[6]	OTG Current Set by Host, Bit 6	n = D[6:0] OTG Output Current Limit Value = 50×n (mA) Range: 0mA (000 0000) - 6350mA (111 1111)	0	R/W
D[5]	OTG Current Set by Host, Bit 5		0	R/W
D[4]	OTG Current Set by Host, Bit 4		0	R/W
D[3]	OTG Current Set by Host, Bit 3		0	R/W
D[2]	OTG Current Set by Host, Bit 2		0	R/W
D[1]	OTG Current Set by Host, Bit 1		0	R/W
D[0]	OTG Current Set by Host, Bit 0		0	R/W

Table 38. OTG Current Register Details (I²C Address = 0x08)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:0]	Reserved	Reserved.	0000 0000	R/W

ADCVBUS/PSYS Register (I²C Address = 0x27/26)

- VBUS: Range from 3200mV to 19520mV with 64mV LSB
- PSYS: Range from 0V to 3.06V with 12mV LSB

Table 39. ADCVBUS/PSYS Register Details (I²C Address = 0x27)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:0]		8-Bit Digital Output of Input Voltage	0000 0000	R

Table 40. ADCVBUS/PSYS Register Details (I²C Address = 0x26)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:0]		8-Bit Digital Output of System Power	0000 0000	R

ADCIBAT Register (I²C Address = 0x29/28)

- ICHG: Range from 0A to 8.128A with 64mA LSB
- IDCHG: Range from 0A to 32.512A with 256mA LSB

Table 41. ADCIBAT Register Details (I²C Address = 0x29)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	Reserved	Reserved.	0	R
D[6:0]		7-Bit Digital Output of Battery Charge Current	000 0000	R

Table 42. ADCIBAT Register Details (I²C Address = 0x28)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	Reserved	Reserved.	0	R
D[6:0]		7-Bit Digital Output of Battery Discharge Current	000 0000	R

REGISTER AND DATA (continued)

ADCIINCMPIN Register (I²C Address = 0x2B/2A)

• IIN: Range from 0A to 12.75A with 50mA LSB

• CMPIN: Range from 0V to 3.06V with 12mV LSB

Table 43. ADCIINCMPIN Register Details (I²C Address = 0x2B)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:0]		8-Bit Digital Output of Input Current	0000 0000	R

Table 44. ADCIINCMPIN Register Details (I²C Address = 0x2A)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:0]		8-Bit Digital Output of CMPIN voltage	0000 0000	R

ADCVSYSVBAT Register (I²C Address = 0x2D/2C)

• VSYS: Range from 2.88V to 19.2V with 64mV LSB

• VBAT: Range from 2.88V to 19.2V with 64mV LSB

Table 45. ADCVSYSVBAT Register Details (I²C Address = 0x2D)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:0]		8-Bit Digital Output of System Voltage	0000 0000	R

Table 46. ADCVSYSVBAT Register Details (I²C Address = 0x2C)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:0]		8-Bit Digital Output of Battery Voltage	0000 0000	R

ID Registers

ManufactureID Register (I²C Address = 0x2E) [Reset = 0x07]

Table 47. ManufactureID Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:0]	MANUFACTURE_ID	0x07, read only.	0000 0111	R

DeviceID (DeviceAddress) Register (I²C Address = 0x2F) [Reset = 0x88]

Table 48. DeviceID (DeviceAddress) Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:0]	DEVICE_ID	I²C, read only. 0x88 = SGM41573	1000 1000	R

Setting Other Charge Options

ChargeOption4 Register (I²C Address = 0x3C) [Reset = 0x00]

Table 49. ChargeOption4 Register Details (I²C Address = 0x3C)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7:2]	Reserved	Reserved.	00 0000	R/W
D[1:0]	PKPWR_TMAX2[1:0]	Peak Power Mode Overload and Relax Cycle Time 00 = The time follows the same PKPWR_TMAX[1:0] bits setting in ChargeOption2 register (I²C address = 0x33) (default) 01 = 100ms 10 = 500ms 11 = 1000ms	00	R/W

APPLICATION INFORMATION

The SGM41573 is a synchronous Buck-Boost battery charge controller with NVDC power path management. It is typically used as a charger controller with portable applications such as notebooks, tablets and other mobile devices with rechargeable batteries.

Design Requirements

Table 50 provides a list of requirements for a typical application design. Input voltage and current are specified based on the adapter specifications and minimum system voltage. Battery charge voltage and charge current are determined based on the battery specifications.

Table 50. Design Requirements for a 2-Cell Battery Application

Design Parameter	Example Values (for a 2-Cell Battery)
Input Voltage	3.5V < Adapter Voltage < 24V
Input Current Limit	3.2A (for a 65W Adapter)
Battery Charge Voltage	8400mV
Battery Charge Current	3072mA
Minimum System Voltage	6144mV

Detailed Design Procedure

Many parameters such as charging current and voltage can be configured by the software. Figure 2 shows a simplified application circuit. Inductor, capacitor, and MOSFET are essential for the converter.

ACP-ACN Input Filter

Because the SGM41573 uses average current mode control, proper sensing of the input current is critical to recover the inductor current ripple. This current is sensed by the differential voltage between ACP and ACN across R_{AC} resistor. Parasitic inductances over the shunt and PCB connections must be avoided because they cause high frequency ringing on ACP-ACN and deteriorate the sensed current. Large parasitic inductance can also cause current loop instability. The filter suggested in Figure 14 can be used to remove such parasitic noises. Insignificant delays would not deteriorate the loop stability.

Inductor Selection

Two fixed switching frequencies (f_S) can be selected. Choose the higher one to reduce the inductor and capacitors values. Select the inductor saturation current larger than maximum charging current (I_{CHG}, plus system current if there is any system load) plus half the peak-to-peak ripple current (I_{RIPPLE_BUCK}) for the Buck mode:

$$I_{SAT} \geq I_{CHG} + (1/2)\ I_{RIPPLE\_BUCK} \quad (3)$$

Select the inductor saturation current which is larger than the maximum input current plus half the peak-to-peak ripple current (I_{RIPPLE_BOOST}) for the Boost mode:

$$I_{SAT} \geq I_{IN} + (1/2)\ I_{RIPPLE\_BOOST} \quad (4)$$

In Buck CCM mode ($D = V_{BAT}/V_{IN}$), the inductor ripple current is determined by:

$$I_{RIPPLE\_BUCK} = \frac{V_{IN} \times D \times (1-D)}{f_S \times L} \quad (5)$$

And in Boost CCM mode ($D = 1 - V_{IN}/V_{BAT}$), the inductor ripple current is determined by:

$$I_{RIPPLE\_BOOST} = (V_{IN} \times D)/(f_S \times L)$$

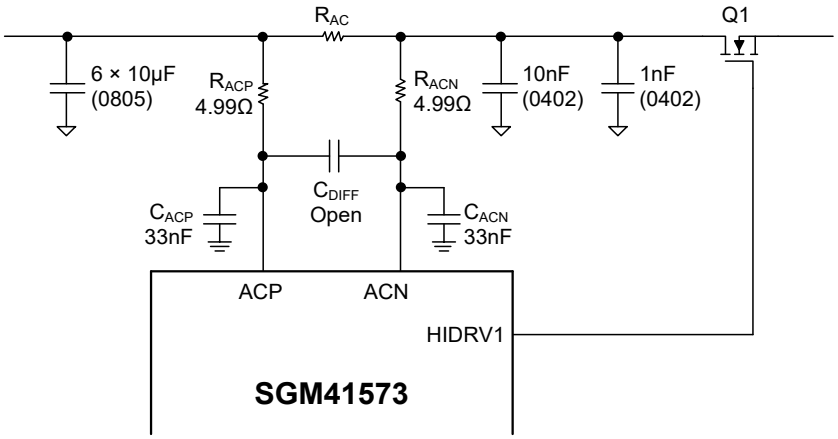


Figure 14. ACN-ACP Input Filter

APPLICATION INFORMATION (continued)

In Buck mode, the maximum ripple current occurs around D = 0.5. For example, for a 3-cell battery, the charging voltage range is 9V to 12.6V and if a 20V adapter voltage is applied, the inductor current ripple is maximum when the battery voltage is around 10V. For a 4-cell battery (12V to 16.8V voltage range), when battery voltage is 12V, the inductor ripple current is at its maximum.

Typically the inductance is selected such that the ripple is within 20% to 40% of the maximum charging current for a tradeoff between the inductor losses and its dimensions.

Input Capacitor

The input capacitor must tolerate the inductor ripple current. With a pulse current duty cycle of D and the DC charging current of I_{CHG} (plus system current if there is any system load), the RMS current can be estimated of the Buck mode by Equation 6:

$$I_{CIN\_BUCK} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (6)$$

Note that around D = 0.5 the RMS current in the capacitor is maximum.

The RMS current can be estimated of Boost mode by Equation 7:

$$I_{CIN\_BOOST} = \frac{I_{RIPPLE\_BOOST}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE\_BOOST} \quad (7)$$

Use low ESR ceramic capacitor (X7R or X5R etc.) for input decoupling and place them before current sense resistor and as close as possible to the power stage. The capacitance between the R_{AC} (current sense resistor) and the power stage should not be too large. Otherwise, the ripple information of the inductor current will be distorted. Consider ceramic capacitor (MLCC) DC bias voltage derating (which may leads significant capacitance drop) of the capacitors for choosing their rated voltage. Tantalum capacitors (POSCAP) can avoid DC bias effect and temperature variation effect which is recommended for higher power application.

In addition, the input capacitor of the system in OTG mode is changed to the output capacitance of OTG. It should also be considered that the input capacitance can affect the output voltage ripple and transient response in OTG mode.

Output Capacitor

The output capacitor (on the system) must have enough RMS current rating to carry the inductor switching ripple and provides enough energy for system transient current demands. For the Buck mode, I_{COUT} (C_{OUT} RMS current) can be calculated by:

$$I_{COUT\_BUCK} = \frac{I_{RIPPLE\_BUCK}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE\_BUCK} \quad (8)$$

The output voltage ripple can be calculated by:

$$\Delta V_{O\_BUCK} = \frac{V_{OUT}}{8 L C_{OUT} f_S^{\,2}} \left(1 - \frac{V_{OUT}}{V_{VBUS}}\right) \quad (9)$$

For the Boost mode, I_{COUT} (C_{OUT} RMS current) can be calculated by:

$$I_{COUT\_BOOST} = I_{IN} \times \sqrt{D \times (1-D)} \quad (10)$$

The output voltage ripple can be calculated by:

$$\Delta V_{O\_BOOST} = \frac{I_{CHG} \times D}{f_{SW} \times C_{OUT}} \quad (11)$$

For the best stability, place at least a 10μF/0805 capacitor after the charge current sense resistor (R_{SR}).

Power MOSFETs Selection

Four N-channel MOSFETs are needed for the charger's synchronous switching converter along with one P-channel MOSFET for BATFET. The internal gate drivers provide 5.6V drive voltage.

To tradeoff between conduction and switching losses, the figure-of-merit (FOM) is a common parameter used for switch comparison. The FOM is defined as the product of the MOSFETs $R_{DS(ON)}$ to its gate-to-drain charge, and Q_{GD} is for top-side switches. The $R_{DS(ON)}$ times total gate charge, and Q_G is for the bottom-side switches.

$$FOM_{TOP} = R_{DS(ON)} \times Q_{GD};\ FOM_{BOTTOM} = R_{DS(ON)} \times Q_G \quad (12)$$

A lower FOM value shows smaller total loss. Switches with lower $R_{DS(ON)}$ in the same package are usually more expensive. 30V or higher voltage rating MOSFETs are preferred, the C_{ISS} of N-channel MOSFET should be chosen less than 1nF.

The top-side MOSFET loss can be calculated as (Buck mode):

$$P_{TOP} = D \times I_{CHG}^{\,2} \times R_{DS(ON)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times (t_{ON} + t_{OFF}) \times f_S \quad (13)$$

APPLICATION INFORMATION (continued)

The first and second terms represents the conduction and switching losses respectively. t_{ON} and t_{OFF} are switch turn on and turn off times which are given by:

$$t_{ON} = \frac{Q_{SW}}{I_{ON}}, t_{OFF} = \frac{Q_{SW}}{I_{OFF}} \quad (14)$$

Where I_{ON} and I_{OFF} are gate drive currents. Q_{SW} is the switching charge. It can also be estimated by the following equation if it is not given:

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \quad (15)$$

The gate driving/sinking currents can be estimated from (16) in which the V_{REGN} is the REGN voltage, V_{PLT} is the MOSFET plateau voltage, R_{ON} is the total turn-on gate resistance, and R_{OFF} is the total driver turn-off gate resistance:

$$I_{ON} = \frac{V_{REGN} - V_{PLT}}{R_{ON}}, I_{OFF} = \frac{V_{PLT}}{R_{OFF}} \quad (16)$$

For the bottom switches, the conduction loss in synchronous continuous conduction mode is given by:

$$P_{BOTTOM} = (1 - D) \times I_{CHG}^2 \times R_{DS(ON)} \quad (17)$$

MOSFET Gate Drive

In some applications, it may be necessary to slow down the dV/dt of MOSFETs to optimize EMI noise. It is recommended to use a series resistor on the bootstrap capacitor side or add an RC snubber instead of adding a series gate drive resistor.

Power Supply Recommendations

An adapter with 3.58V to 24V voltage which is capable to provide at least 500mA can be used with this device. CHRG_OK = HIGH shows that adapter is powering the system through the charger. If the adapter is removed, the system will connect to the battery through BATFET. Usually, the battery depletion threshold is larger than the minimum system voltage setting such that full battery capacity can be utilized.

Layout Guidelines

A good layout is critical for proper performance of a switching charger. To reduce the switching losses, the hard switching rise and fall times of the switching nodes should be minimized. Also, to reduce electric and magnetic couplings and noise radiation from the high frequency path, the loop area and conductor surfaces must be minimized.

A list of PCB layout guidelines is given below. It is important to prioritize these guidelines in the as ordered in this list.

1. Place the input capacitor right on the supply and ground connection points of switching legs and on the same layer with the switches. Avoid vias in the high frequency current paths if possible.
2. Keep the device close to the switch gate pins to minimize gate drive trace lengths. The device can be placed on the opposite side of the PCB. Connect the gates with some parallel vias to minimize gate connection impedance.
3. Place the inductor pins as close as possible to the switching nodes. Keep the switching node connections short and wide with minimal copper area to minimize capacitive coupling noise and radiation. Do not use multiple traces in parallel layers. Try to minimize parasitic capacitance from this area to any other trace or plane, especially the sensitive analog signal traces.
4. Place the charge current sense resistor right next to the inductor output. Use kelvin contact to connect the sense traces across the shunt resistor and keep both traces on the same layer, close to each other and away from high current paths. Place a decoupling capacitor between sense lines just before reaching the device.
5. Place one of the output capacitors next to the battery sensing resistor and ground.
6. Connect the ground returns of the input and output capacitors together and then connect them to the system ground to minimize high frequency current loop areas and path length.
7. Connect the charger power and analog grounds only at one point just beneath the device (thermal pad). Pour analog ground copper planes but keep them away from power pins to minimize inductive and capacitive noise coupling.
8. Use separate routes for analog and power grounds. Connect analog and power grounds at one point on the thermal pad or use a 0Ω resistor as connection to separate analog and power ground nets in the layout. In this case, tie the thermal pad to the analog ground if possible.
9. Always place the decoupling capacitors right next to the device pins with the shortest possible traces.
10. It is important to solder the device thermal pad and use proper thermal vias to conduct the heat to the backside ground plane of the board for cooling.
11. Choose proper size and quantity of vias in each current path.

APPLICATION INFORMATION (continued)

Recommended PCB layout

The layout example of top layer (including all the key power components) is shown below based on the above layout guidelines.

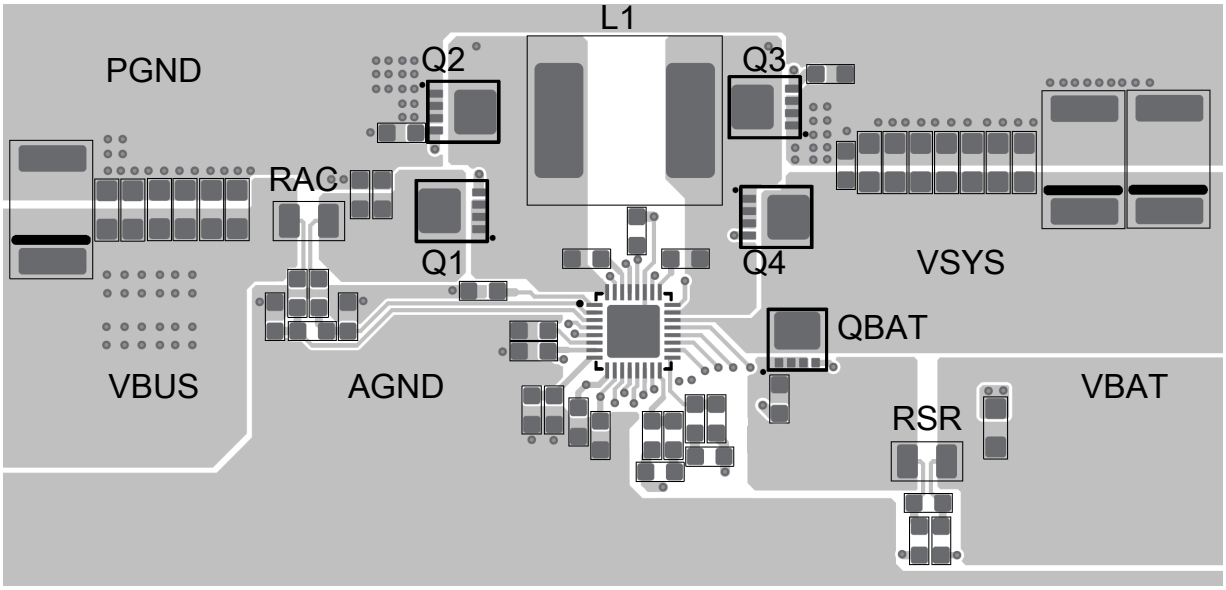


Figure 15. PCB Layout Example

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

APRIL 2025 – REV.A.4 to REV.B	Page
Updated Typical Application Circuit section	20
Updated Application Information section	57, 58

OCTOBER 2024 – REV.A.3 to REV.A.4	Page
Updated Absolute Maximum Ratings section	3
Updated Application Information section	57

SEPTEMBER 2024 – REV.A.2 to REV.A.3	Page
Updated Electrical Characteristics section	14
Updated Typical Application Circuit section	20
Updated Detailed Description section	30

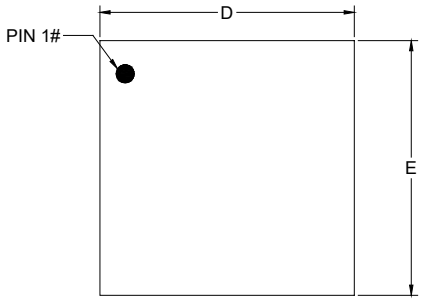
APRIL 2024 – REV.A.1 to REV.A.2	Page
Updated Typical Application Circuit section	20

OCTOBER 2023 – REV.A to REV.A.1	Page
Updated Register and Data section	49

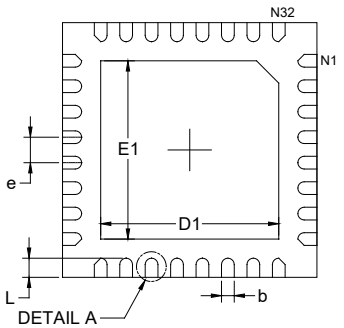
Changes from Original (AUGUST 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

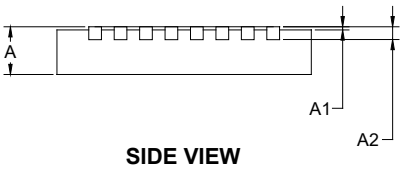
TQFN-4×4-32AL



TOP VIEW



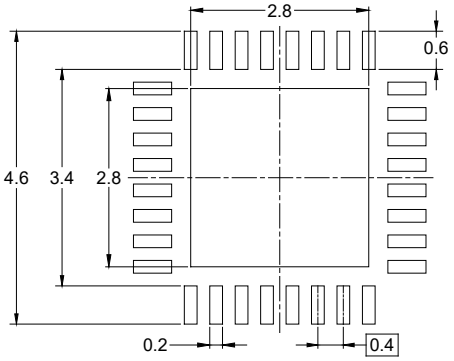
BOTTOM VIEW



SIDE VIEW

DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



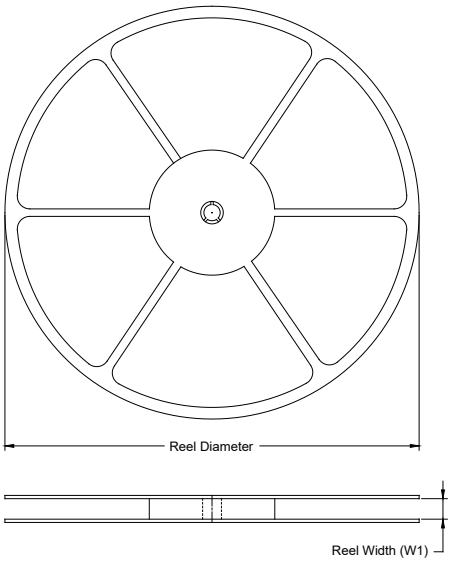
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.200 REF		
D	3.900	4.000	4.100
E	3.900	4.000	4.100
D1	2.700	2.800	2.900
E1	2.700	2.800	2.900
b	0.150	0.200	0.250
e	0.400 BSC		
L	0.250	0.300	0.350

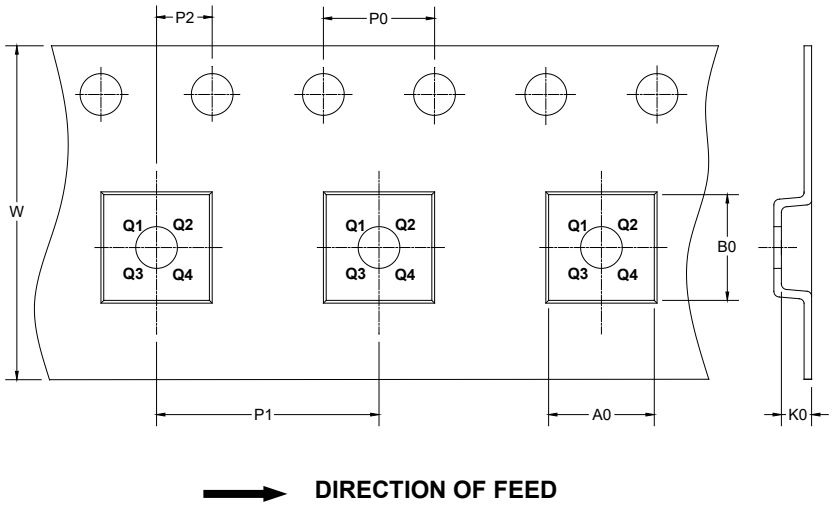
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



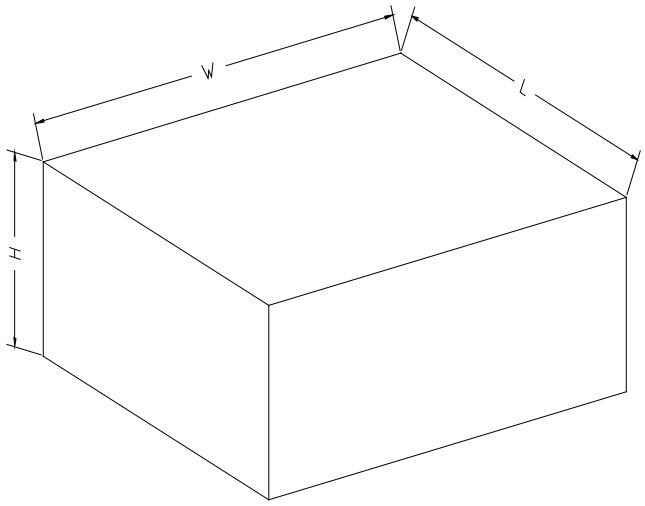
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-32AL	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002