SGM42537
Low-Voltage H-Bridge Driver

GENERAL DESCRIPTION

The SGM42537 is a low voltage integrated motor driver that can be used in battery or non-battery powered applications. The N-MOSFET H-bridge output can drive brushed DC motors for motion control or other loads such as solenoids and relays. A separate supply pin (VM) is provided for the power stage that can deliver up to 3A peak current to the load from a second source. The VM voltage range is 0V to 12V while the device itself can be supplied from a low-current (< 2mA) 2V to 5.5V source (V_{CC}). An internal charge pump provides the gate driving voltage for the high-side switches.

The standard input interface for the SGM42537 is PWM (IN1/IN2). The device uses a dedicated nSLEEP input for sleep mode.

The SGM42537 is available in a Green TDFN-2×2-8AL package.

SIMPLIFIED SCHEMATIC

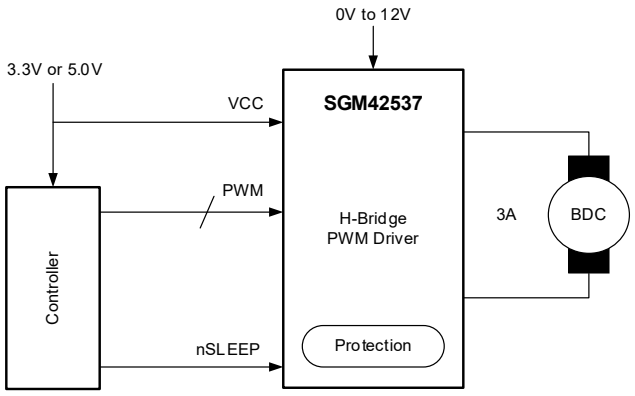


Figure 1. Simplified Schematic

FEATURES

- **N-Channel H-Bridge Motor (Load) Driver**
- **180mΩ HS + LS MOSFET On-Resistances**
- **Bidirectional BDC Motor Driving**
- **Up to 3A Output Current**
- **0kHz to 250kHz Switching Frequency**
- **Separate Load (Motor) and Logic Supplies**
- **0V to 12V Load Supply Voltage Range (VM)**
- **2V to 5.5V VCC Logic Supply (needs less than 2mA)**
- **VCC Can be Supplied from a GPIO for Shutdown**
- **Ultra Low-Power Sleep Mode**
- **PWM Bridge-Control Interface**
- **IN1/IN2 (PWM)**
- **Auto-sleep Mode**
- **nSLEEP Input**
- **Protection Features with Auto Recovery:**
  - **VCC Under-Voltage Lockout (UVLO)**
  - **Over-Current Protection (OCP)**
  - **Thermal Shutdown (TSD)**
- **Available in a Green TDFN-2×2-8AL Package**

APPLICATIONS

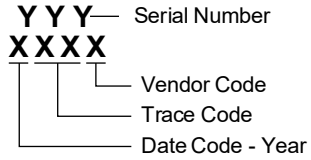
Brushed DC Motor, Solenoid, and Relay Driving
Cameras
DSLR Lenses
Consumer Products
Toys
Robotics
Medical Devices

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42537	TDFN-2×2-8AL	-40℃ to +125℃	SGM42537XTDE8G/TR	1Z7 XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Motor Power Supply Voltage, V_M ..... -0.3V to 13.2V
Logic Power Supply Voltage, V_{CC} ..... -0.3V to 6V
Digital Input Pin Voltage ..... -0.5V to V_{CC} +0.5V
Output Pin Voltage, OUTx ..... -0.7V to V_M + 0.7V
Peak Drive Current, OUT1, OUT2 ..... Internally limited
Package Thermal Resistance
TDFN-2×2-8AL, θ_{JA} ..... 52.6℃/W
TDFN-2×2-8AL, θ_{JB} ..... 18.5℃/W
TDFN-2×2-8AL, $\theta_{JC\ (TOP)}$ ..... 69.5℃/W
TDFN-2×2-8AL, $\theta_{JC\ (BOT)}$ ..... 2.2℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±2000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Motor Power Supply Voltage, V_M ..... 0V to 12V
Logic Power Supply Voltage, V_{CC} ..... 2V to 5.5V
Logic Level Input Voltage, V_{IN} ..... 0V to V_{CC}
Peak Output Current, I_{OUT} ..... 0A to 3A
Externally Applied PWM Frequency, f_{PWM} ..... 0kHz to 250kHz
Operating Ambient Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

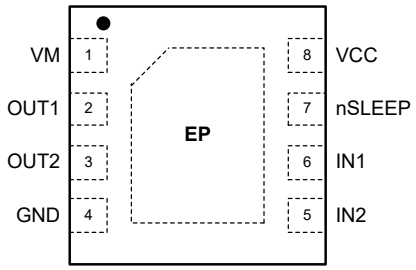
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM42537 (TOP VIEW)



TDFN-2×2-8AL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	VM	P	Motor (Load) Power Supply. Bypass this pin to the GND with a high frequency 0.1μF ceramic capacitor rated for VM voltage.
2	OUT1	O	Load Connection Outputs. Connect these pins to the load (e.g. brushed DC motor) terminals.
3	OUT2	O	
4	GND	P	Device Ground and Returns for VM and VCC and Reference for Logic Inputs. This pin must be connected to the PCB ground.
5	IN2	I	H-Bridge IN2 PWM Control Input.
6	IN1	I	H-Bridge IN1 PWM Control Input.
7	nSLEEP	I	Sleep Mode Control Input. If it is pulled low or left open, the device enters low-power sleep mode. Normal operation is allowed when this pin is pulled high. The nSLEEP has an internal pull-down resistor to GND.
8	VCC	P	Device Logic Power Supply. Bypass this pin to the GND pin using a high frequency 0.1μF ceramic capacitor with sufficient voltage rating.
Exposed Pad	GND	G	Exposed Pad. This pad helps cooling the device and is internally connected to GND, however it is not an electrical connection point for GND currents. Connect it to the large ground planes for better thermal performance. Thermal vias connected to the ground planes on the other layers also can improve thermal performance.

NOTE: I = input, O = output, P = power, G = ground.

TYPICAL APPLICATION

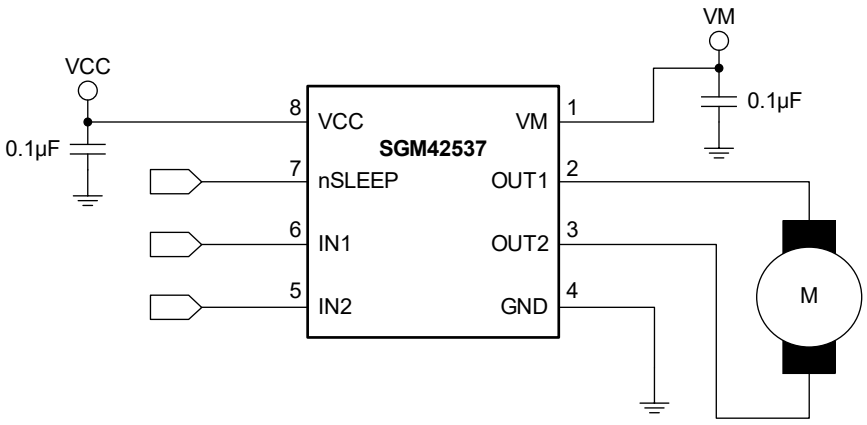


Figure 2. Schematic of SGM42537 Application

ELECTRICAL CHARACTERISTICS

(V_M = 5V, V_{CC} = 3V, and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
VM Operating Supply Current	I_{VM}	No PWM, no load			100	130	μA
		50kHz PWM, no load			175	210	
VM Sleep Mode Supply Current	I_{VMQ}	V_{CC} = 0V, all inputs 0V	V_M = 2V		10	70	nA
			V_M = 5V		20	70	
VCC Operating Supply Current	I_{VCC}				700	1050	μA
VCC Under-Voltage Lockout Voltage	V_{UVLO}	V_{CC} rising threshold		1.65	1.8	2	V
		V_{CC} falling threshold		1.55	1.7	1.85	
Logic-Level Inputs							
Input Low Voltage	V_{IL}					0.3 × V_{CC}	V
Input High Voltage	V_{IH}			0.5 × V_{CC}			V
Input Low Current	I_{IL}	V_{IN} = 0V		-200		200	nA
Input High Current	I_{IH}	V_{IN} = 3.3V		15	23	30	μA
Pull-Down Resistance	R_{PD}				140		kΩ
H-Bridge FETs							
HS + LS FET On-Resistance	R_{DSON}	I_O = 800mA, T_J = +25℃	V_{CC} = 3V, V_M = 3V		195	240	mΩ
			V_{CC} = 5V, V_M = 5V		165	210	
OFF-State Leakage Current	I_{OFF}			-500		500	nA
Protection Circuits							
Over-Current Protection Trip Level (1)	I_{OCP}			3.1	5.0	7.0	A
Over-Current Protection Retry Time (1)	t_{OCR}				5		ms
Over-Current De-Glitch Time	t_{DEG}				1.4		μs
Output Dead Time	t_{DEAD}				100		ns
Thermal Shutdown Temperature (2)	T_{SD}	Die temperature		150	165	180	℃
Thermal Shutdown Hysteresis (2)	T_{HYS}				30		℃

NOTES:

1. When V_M ≥ 3.5V and V_{CC} ≤ 2.9V, I_{OCP} and t_{OCR} will cut off 50%.
2. Not production tested.

TIMING REQUIREMENTS

(V_M = 5V, V_{CC} = 3V, T_A = +25℃, and R_L = 20Ω, unless otherwise noted.)

SYMBOL	CONDITIONS		MIN	MAX	UNITS
t_1	Output enable time.	See Figure 3.		160	ns
t_2	Output disable time.			300	ns
t_3	Delay time, INx high to OUTx high.			300	ns
t_4	Delay time, INx low to OUTx low.			300	ns
t_5	Output rise time.		10	70	ns
t_6	Output fall time.		10	110	ns

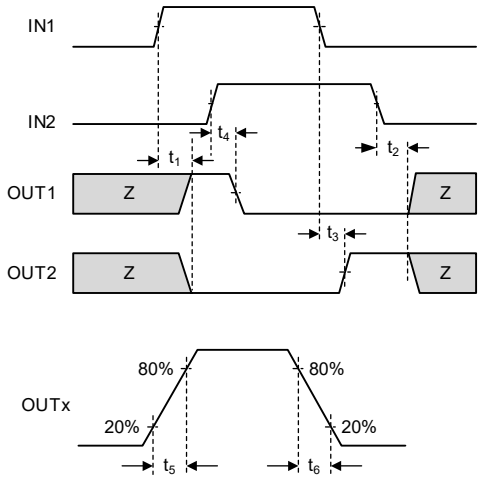
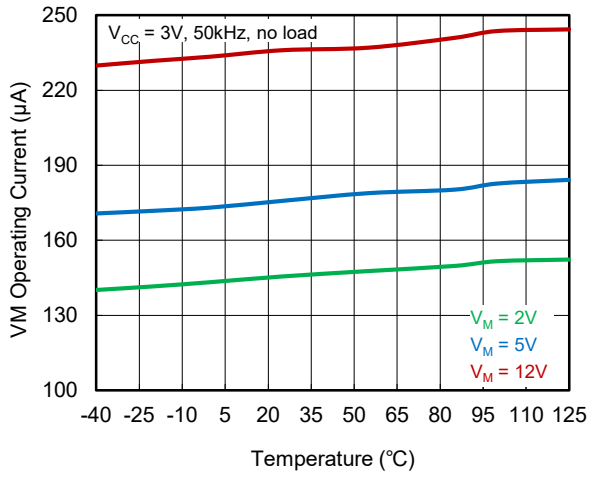


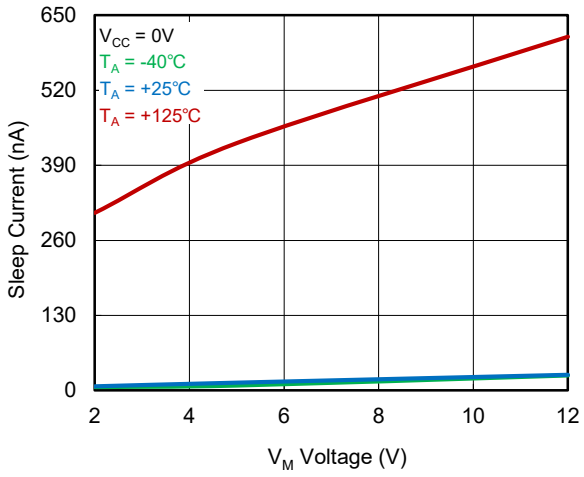
Figure 3. Input and Output Timing for SGM42537

TYPICAL PERFORMANCE CHARACTERISTICS

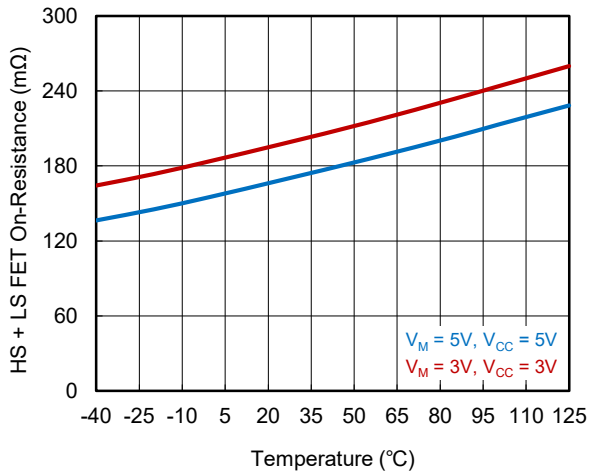
VM Operating Current vs. Temperature



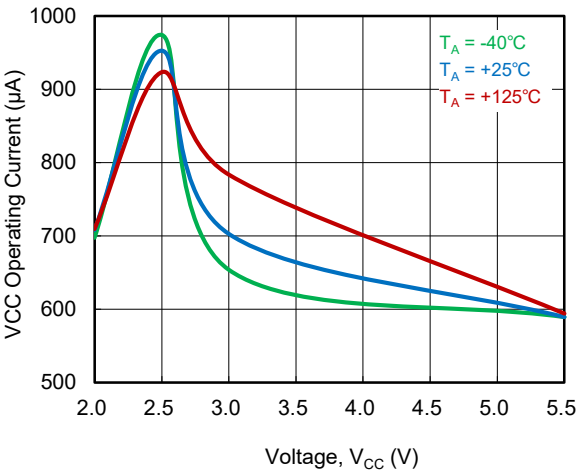
Sleep Current vs. V_M Voltage



HS + LS FET On-Resistance vs. Temperature



VCC Operating Current vs. V_{CC} Voltage



FUNCTIONAL BLOCK DIAGRAM

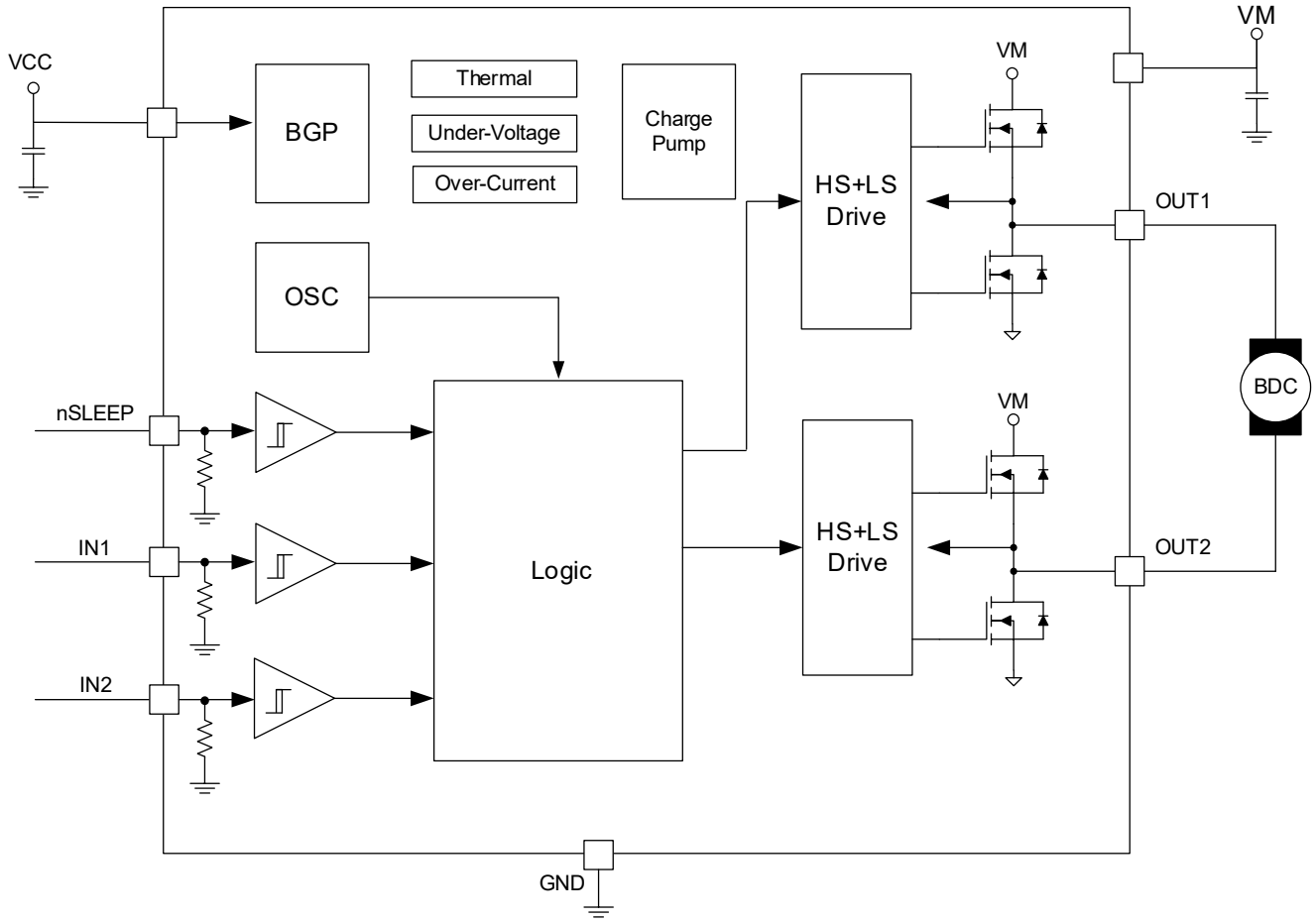


Figure 4. Block Diagram

DETAILED DESCRIPTION

The SGM42537 supports PWM (IN1/IN2) interface. Sleep mode is available in the SGM42537 using a dedicated nSLEEP input pin to enter (nSLEEP = 0) or exit (nSLEEP = 1) the low-power sleep mode.

The device is a good choice for compact motor drive solutions with minimal external components. The device provides under-voltage lockout, over-current, and thermal shutdown protections that are not typically available in a traditional discrete solution.

Please refer to Table 1 for the H-bridge control logic.

Table 1. The SGM42537 Control Logic (PWM)

nSLEEP	IN1	IN2	OUT1	OUT2	Function (DC Motor or Load Voltage)
0	X	X	Hi-Z	Hi-Z	Sleep mode/Coast
1	0	0	Hi-Z	Hi-Z	Sleep mode/Coast
1	1	0	H	L	Forward ($V_L = V_M$)
1	0	1	L	H	Reverse ($V_L = -V_M$)
1	1	1	L	L	Brake ($V_L = 0$)

Sleep Mode

The nSLEEP pin in the SGM42537 can be pulled low to enter the low-power sleep mode in which most of the internal circuitry is powered down to minimize supply current.

Power and Input Pin Considerations

There is no special power up sequence requirement for this device. If removing VCC, the device enters low-power mode and current from VM supply will be very small. If the VM supply voltage is between 2V to 5.5V, the VCC and VM pins can be tied together.

The VM voltage has no UVLO protection and can go down to 0V. All input pins are weakly pull-down to ground by 140kΩ (approximate) internal pull-down resistors.

Protection Features

The device is fully protected against outputs over-current, junction over-temperature and VCC under-voltage faults.

VCC Under-Voltage Lockout (UVLO)

If at any time the VCC voltage drops below its UVLO falling threshold (V_{UVLO}), all bridge MOSFETs, charge pump and logic circuit are disabled. Normal operation resumes when VCC exceeds the UVLO rising threshold.

Output Over-Current Protection (OCP)

Current in each MOSFET is limited by an analog circuit that kills its gate signal when it reaches the limit (5A TYP). This protection is effective in hard short-circuit events besides the load over-current events. If the current across a FET exceeds the OCP level and lasts for longer than a deglitch time (t_{DEG}), all bridge MOSFETs will be disabled. The OCP is a hiccup type and device operation resumes automatically after t_{RETRY} and may repeats if the OC condition is still present. The OCP is detected for OUTx shorts to VM, GND or between OUT1 and OUT2.

Overheating Protection (Thermal Shutdown, TSD)

To protect the device against overheating damage all H-bridge switches are disabled if the die temperature (T_J) exceeds the temperature shutdown rising threshold limit (T_{SD}). The device resumes its normal operation automatically when the die cools and T_J drops below the thermal shutdown falling threshold (T_{SD} - T_{HYS}).

Table 2. Summary of the SGM42537 Faults and Protection Behavior

Fault	Condition	H-Bridge	Recovery
VCC Under-Voltage Lockout (UVLO)	$V_{CC} < V_{UVLO}$ (falling)	Disabled	Re-enable when $V_{CC} > V_{UVLO}$ (rising)
Over-Current Protection (OCP)	$I_{OUT} > I_{OCP}$	Disabled (Retries Automatically)	Re-enable after t_{RETRY}
Thermal Shutdown (TSD)	$T_J > T_{SD}$	Disabled (Retries Automatically)	Re-enable when $T_J < T_{SD} - T_{HYS}$

DETAILED DESCRIPTION (continued)

Functional Modes

The SGM42537 has three different modes of operation depending on the inputs and conditions.

Active Mode

In active mode, all internal circuits including the H-bridge, charge pump, and internal logic are active and the device drives the load normally. The device leaves active mode if entering sleep mode or fault mode. If supplying the VCC by MCU GPIO, to protect the microcontroller GPIO pin from excess current due to the decoupling capacitor charging current, a resistor may be needed to be added between the GPIO and the decoupling capacitor on the VCC pin.

Sleep Mode

The device would enter sleep mode if nSLEEP input is pulled low. In this mode, he H-bridge switches are disabled and remain in Hi-Z state. For normal active mode operation, the nSLEEP pin must be set to logic high state.

To ensure lowest supply current, SGMICRO recommends setting all input pins to logic low to eliminate current draw through the pull-down resistors in sleep mode.

Fault Mode

The device enters fault mode when encountering a fault,for example, OCP or thermal protection. The device would automatically return to active mode if the recovery conditions are met. (Refer to Table 2).

Table 3. Summary of the SGM42537 Operating Modes

Mode	Condition	H-Bridge Status
Active Mode	nSLEEP Pin = 1	Outputs follow the control Inputs as defined in truth table.
Sleep Mode	nSLEEP Pin = 0	Disabled (Hi-Z)
Fault Mode	A Fault Occurs	Disabled (Hi-Z), automatically returns to active mode if the recovery conditions are met

APPLICATION INFORMATION

The SGM42537 is H-bridge driver typically suitable for driving brushed DC motors or solenoid loads. The design process to configure these devices is explained in the following section.

Design Requirements

Table 4. SGM42537 Typical Design Requirements

Parameter	Reference	Example Value
Motor Supply Voltage	V_M	9V
Logic Supply Voltage	V_{CC}	3.3V
Target RMS Current	I_{OUT}	0.8A

Detailed Design Procedure

VM Supply Voltage

Usually the load voltage rating determines the required VM voltage (motor, solenoid, relay, etc.). For a brushed DC motor, lowering the supply voltage reduces the speed (RPM) of the motor at the same PWM duty ratio. Also note that, the load current is typically increased if a higher VM is selected. Higher VM values increase the current rate of change (di/dt slope) during switching in inductive loads such as motor windings, solenoid, or relay.

Bulk Capacitance

It is important to have sufficient bulk capacitance on the supply lines to avoid instability. Too much bulk capacitance increases the size and cost of the design and may have adverse effects on the system stability as well. System-level testing is highly recommended to verify and determine the proper size of the bulk capacitors. The required local capacitance can be selected by considering many factors including:

- The peak current of the load or motor system.
- The power supply current sourcing capability and installed capacitance. Note that in case of regenerative motor braking, motor current is injected back to the VM line and if this kinetic energy is not properly absorbed in the capacitors, it can cause large over-voltages.
- The parasitic line inductance between the source and load location.
- The system acceptable line voltage ripple.
- The motor braking/reversal method (kinetic energy recycled to the line capacitors or dissipated in the motor/bridge).

The supply line parasitic inductance limits the current change rate supplied from the source. If the load (like motor) has fast current changes, the deficit/excess current during transitions must be supplied/absorbed by the local line capacitors. Therefore, if the total bulk capacitance near the load is too small, the excessive currents can result in large voltage variations. So, sufficient bulk capacitance must be used to keep the VM voltage stable.

The bulk capacitor voltage rating should be selected with a sufficient margin above the peak operating voltage to safely absorb motor energy during braking. It also helps to prolong the capacitor's lifetime.

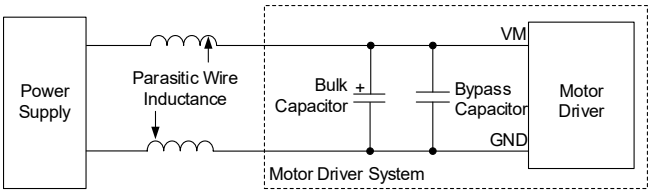


Figure 5. Example Setup of Motor Drive System with External Power Supply

Power Supply and Inputs

The VCC and VM sources may be applied and removed in any order. By removing VCC, a low-power sleep state is initiated and VM current drops to very small levels. All input pins are weakly pulled down to GND with approximately 100kΩ resistors, so to minimize supply currents in the sleep mode, the inputs should be kept at GND level.

As long as V_{CC} is above 1.8V, the device remains active. There is no UVLO limit for the VM and it can go down to 0V, however, the load may not function properly at low VM voltage levels.

PCB Layout Considerations

Use 0.1μF low ESR ceramic capacitor (rated for VCC voltage or higher) near the VCC and GND pins to decouple VCC voltage. Choose thick traces for connection of this capacitor to minimize parasitic resistance and inductance. Using ground plane connection for capacitor return to the device GND is preferred. A bulk capacitor (e.g. electrolytic) is also needed between VCC and GND near the device to stabilize supply voltage.

APPLICATION INFORMATION (continued)

Thermal Considerations

The device thermal shutdown (TSD) occurs when the die temperature exceeds approximately +160℃. This fault disables the device until the temperature falls to the safe level. To avoid unwanted thermal shutdowns, proper heatsinking of the device should be considered in the layout. Use the exposed pad under the device for heatsinking and connect it to the large copper planes. Preferably use thermal vias connected to the planes on all other layers and especially the layer in the back of the PCB, to improve heat removal and device cooling. Note that this pad is internally connected to GND, but it is not an electrical connection point for GND currents.

Natural air circulation should also be considered to keep low ambient temperature around the device.

Power Losses

The active mode power loss in these devices is mainly due to the output MOSFET On-resistances (R_{DSON}). The approximate power loss in the H-bridge can be estimated from Equation 1:

$$P_{TOT} = 2 \times R_{DSON} \times (I_{OUT\_RMS})^2 \quad (1)$$

where,

P_{TOT} is the power dissipation in the device, and I_{OUT_RMS} is the RMS output current in the load or motor winding.

The maximum amount of power dissipated in the device is dependent on ambient temperature and heat sinking performance as well.

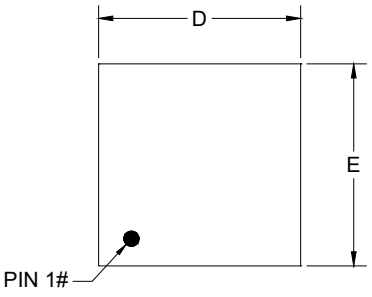
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

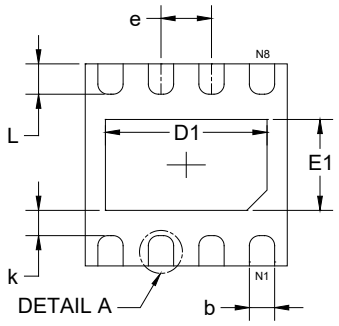
Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

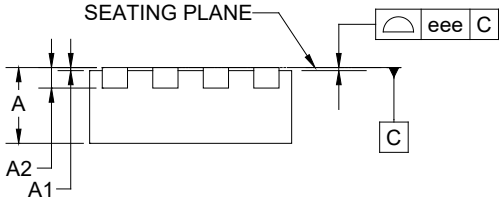
TDFN-2×2-8AL



TOP VIEW

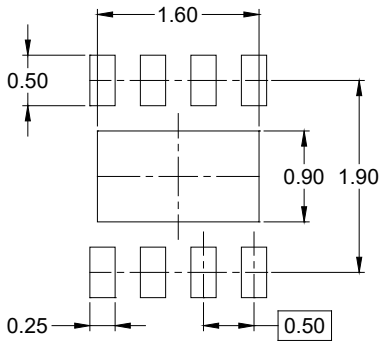


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



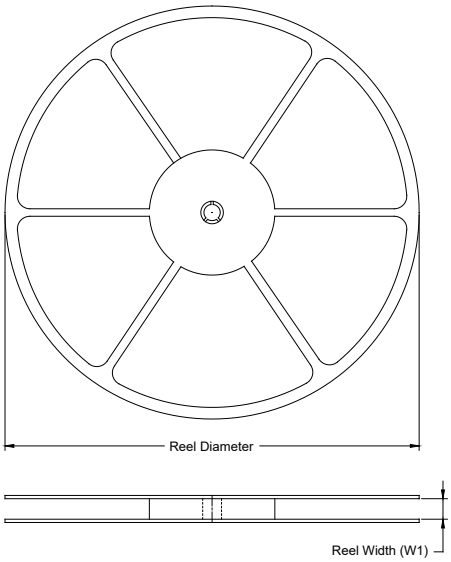
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	1.900	-	2.100
D1	1.450	-	1.700
E	1.900	-	2.100
E1	0.750	-	1.000
k	0.200	-	-
e	0.500 BSC		
L	0.200	-	0.400
eee	0.080		

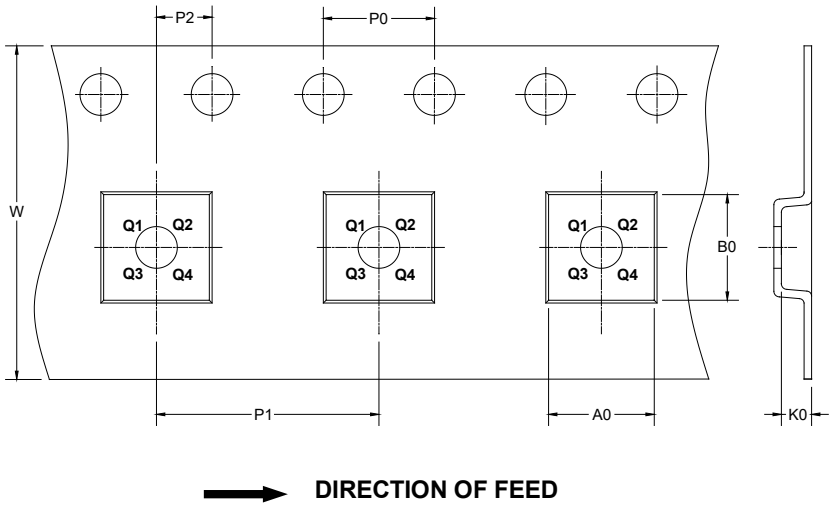
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



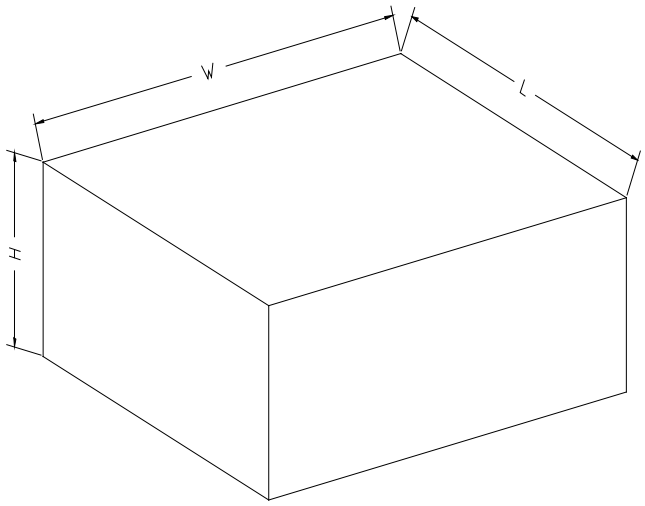
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8AL	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

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