SGM61431
4.5V to 36V Input, 3A, Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61431 is an internally compensated, synchronous Buck converter with a wide 4.5V to 36V input voltage range and 3A output current capability. The device can be easily used in various industrial applications powered from unregulated sources. Easy compensation and cycle-by-cycle current limit are obtained by peak current mode control. With ultra-low 0.6μA (TYP) shutdown current, it is well suited for battery powered systems to prolong battery life. Internal compensation allows quick and low component count design.

The SGM61431 can operate at fixed frequency with moderate or heavy load condition. In light load condition, the SGM61431 works in the forced pulse width modulation (FPWM) mode to achieve low output ripple and good regulation.

The EN/SYNC employs an enable divider to establish a precision threshold that simplifies UVLO adjustment, device on/off control and power sequencing. Thermal shutdown and output short-circuit protection (hiccup mode) are also provided.

The SGM61431 is available in a Green SOIC-8 (Exposed Pad) package and can operate over -40℃ to +125℃ ambient temperature range.

FEATURES

- **Wide 4.5V to 36V Input Voltage Range**
- **Up to 3A Continuous Output Current**
- **0.8V to 24V Output Voltage Range**
- **FPWM at Light Load Condition**
- **390kHz Switching Frequency (Normal Operation)**
- **SYNC Input for External Switching Clock**
- **Integrated R_{DSON} Switches: 115mΩ/90mΩ (TYP)**
- **High Efficiency at Light Load Condition**
- **Ultra-Low Shutdown Current: 0.6μA (TYP)**
- **Peak Current Mode Control**
- **Precision Enable Threshold with UVLO Setting**
- **Cycle-by-Cycle Current Limit**
- **1.5ms (TYP) Internal Soft-Start Time**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SOIC-8 (Exposed Pad) Package**

APPLICATIONS

Industrial Power Supplies
Telecom and Datacom Systems
General Purpose Wide V_{IN} Regulation

TYPICAL APPLICATION

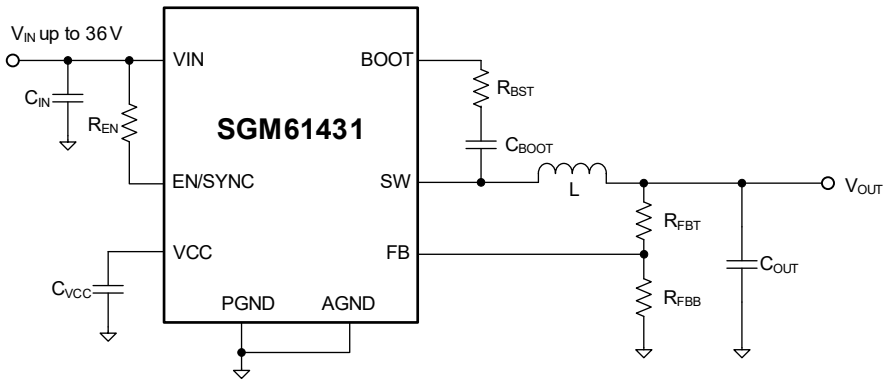


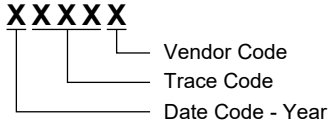
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61431	SOIC-8 (Exposed Pad)	-40℃ to +125℃	SGM61431XPS8G/TR	SGM 61431XPS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltages:
- VIN to PGND ..... -0.3V to 42V
- EN to AGND ..... -5.5V to V_{IN} + 0.3V
- FB to AGND ..... -0.3V to 4.5V
- AGND to PGND ..... -0.3V to 0.3V

Output Voltages:
- SW to PGND ..... -0.3V to V_{IN} + 0.3V
- SW to PGND (Less than 10ns Transients) ..... -5V to 42V
- BOOT to SW ..... -0.3V to 5.5V
- VCC to AGND ..... -0.3V to 5.5V

Package Thermal Resistance
- SOIC-8 (Exposed Pad), θ_{JA} ..... 36.7℃/W
- SOIC-8 (Exposed Pad), θ_{JB} ..... 13.3℃/W
- SOIC-8 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 53.1℃/W
- SOIC-8 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 3.4℃/W

Package Thermal Characterization Parameter
- SOIC-8 (Exposed Pad), ψ_{JT} ..... 4.5℃/W
- SOIC-8 (Exposed Pad), ψ_{JB} ..... 12.9℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltages:
- VIN to PGND ..... 4.5V to 36V
- EN to AGND ..... -5V to 36V
- FB to AGND ..... -0.3V to 1.2V

Output Voltage Range ..... 0.8V to 24V
Output Current Range ..... 0A to 3A
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

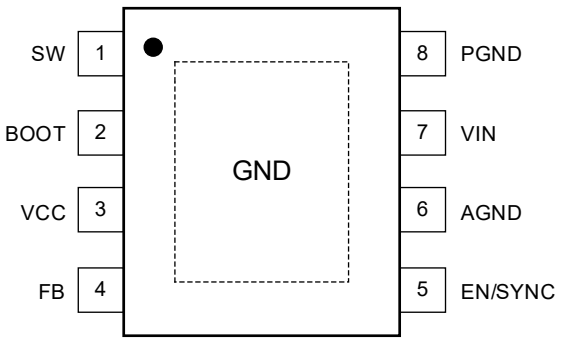
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



SOIC-8 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
1	SW	P	Switching Node Output. Switching node of the internal synchronous Buck converter with N-MOSFET switches. Connect to the output inductor and bootstrap capacitor.
2	BOOT	P	Bootstrap Input. Bootstrap supply for high-side driver. Connect a 470nF ceramic capacitor between BOOT and SW pins.
3	VCC	P	LDO (Internal Bias) Output. This pin is provided for bypassing to AGND only. Never load VCC.
4	FB	A	Feedback Input. Connect the midpoint of the feedback resistor divider.
5	EN/SYNC	A	Active High Enable and Synchronous Input. Do not float. EN: This pin can be connected to VIN pin via a resistor if the shutdown feature is not required or to a resistor divider to adjust UVLO threshold. SYNC: An external clock with positive pulses can be coupled to this pin by a small capacitor for synchronizing the internal switching oscillator.
6	AGND	G	Analog Ground. Reference for internal analog signals and logic. Connect it to system ground.
7	VIN	P	Power Supply Input Pin. Connect C_{IN} as close as possible between this pin and PGND pin.
8	PGND	G	Power Ground. It is internally connected to converter return. Returns of the C_{IN} and C_{OUT} capacitors should be connected close to this pin. Connect to system ground, exposed pad and AGND together.
Exposed Pad	GND	G	Thermal Exposed Pad. Must be connected to ground plane on PCB. It is the main thermal relief path for the die.

NOTE: 1. A = analog, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
Input Voltage Range	V_{IN}			4.5		36	V
Input UVLO Rising Threshold	V_{IN_UVLO}	Rising threshold, T_J = -40℃ to +125℃		4.1	4.3	4.5	V
Input UVLO Hysteresis	V_{UVLO_HYS}	Falling hysteresis			290		mV
Shutdown Current into VIN	I_{SHDN}	V_{IN} = 6V to 36V, V_{EN} = 0V, T_J = -40℃ to +125℃			0.6	1.8	μA
Enable							
Enable Rising Threshold	V_{EN_H}	T_J = -40℃ to +125℃		1.35	1.50	1.65	V
Enable Hysteresis	V_{EN_HYS}				430		mV
Input Leakage Current at EN Pin	I_{EN}	V_{IN} = 4.5V to 36V, V_{EN} = 2V, T_J = -40℃ to +125℃			10	500	nA
		V_{IN} = V_{EN} = 36V				1	μA
Voltage Reference							
Reference Voltage	V_{REF}	V_{IN} = 6V to 36V	T_J = +25℃	0.782	0.804	0.824	V
			T_J = -40℃ to +125℃	0.780	0.804	0.826	
Input Leakage Current at FB Pin	I_{LKG_FB}	V_{FB} = 0.8V			10		nA
Internal LDO							
Internal LDO Output Voltage	V_{CC}	V_{IN} = 6V to 36V, T_J = -40℃ to +125℃		4.6	5.0	5.3	V
Current Limit							
Peak Inductor Current Limit	I_{HS_LIMIT}	T_J = +25℃		5.0	5.9	6.8	A
Valley Inductor Current Limit	I_{LS_LIMIT}	T_J = +25℃		2.2	2.9	3.5	A
Negative Current Limit (FPWM)	I_{L_NEG}				-2.0		A
Integrated MOSFETs							
High-side MOSFET On-Resistance	R_{DSON_HS}	V_{IN} = 12V, I_{OUT} = 0.5A			115		mΩ
Low-side MOSFET On-Resistance	R_{DSON_LS}	V_{IN} = 12V, I_{OUT} = 0.5A			90		mΩ
Thermal Shutdown							
Thermal Shutdown Threshold	T_{SHDN}				175		℃
Thermal Shutdown Hysteresis	T_{HYS}				20		℃

TIMING REQUIREMENTS

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hiccup Mode						
Number of Cycles that LS Current Limit is Tripped to Enter Hiccup Mode	N_{OC} (1)			128		Cycles
Hiccup Retry Delay Time	t_{OC}			30		ms
Soft-Start						
Internal Soft-Start Time	t_{SS}	The time of internal reference to increase from 0V to 0.8V.		1.5		ms

NOTE: 1. Guaranteed by design.

SWITCHING CHARACTERISTICS

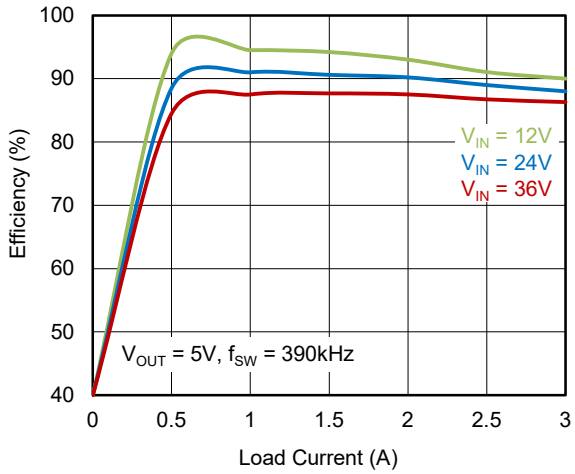
(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SW (SW Pin)						
Default Switching Frequency	f_{SW}	T_J = -40℃ to +125℃	310	390	470	kHz
Minimum Turn-On Time	t_{ON_MIN}			110		ns
Minimum Turn-Off Time	t_{OFF_MIN}			80		ns
SYNC (EN/SYNC Pin)						
SYNC Frequency Range	f_{SYNC}		200		2200	kHz
Amplitude of SYNC Clock AC Signal (Measured at SYNC Pin)	V_{SYNC}		2.8		5.5	V
Minimum SYNC Clock On/Off Time	t_{SYNC_MIN}			100		ns

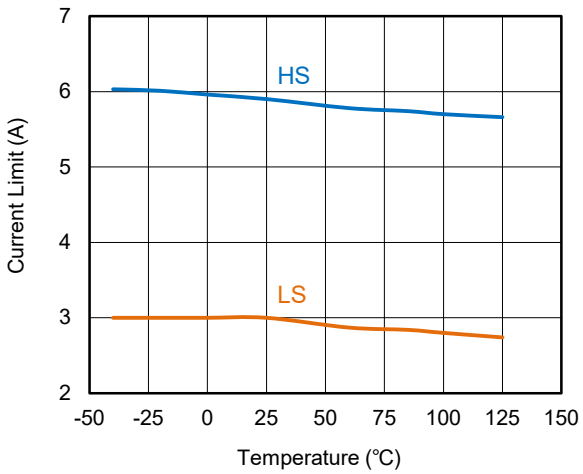
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, f_{SW} = 390kHz, L = 10μH and C_{OUT} = 100μF, unless otherwise noted.

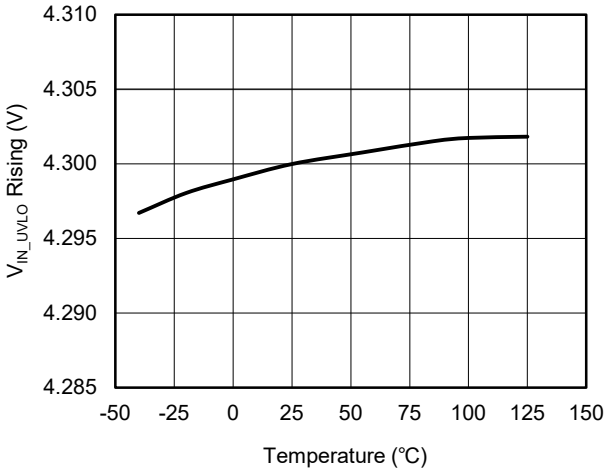
Efficiency vs. Load Current



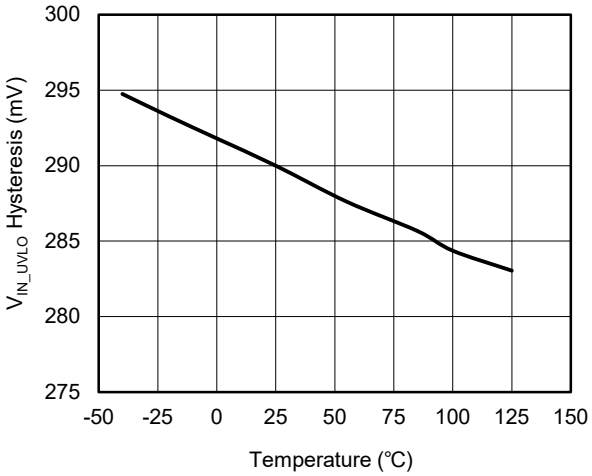
Current Limit vs. Junction Temperature



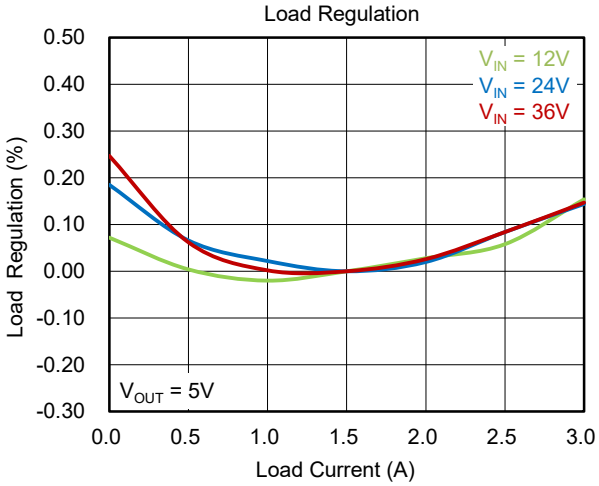
V_{IN_UVLO} Rising vs. Junction Temperature



V_{IN_UVLO} Hysteresis vs. Junction Temperature



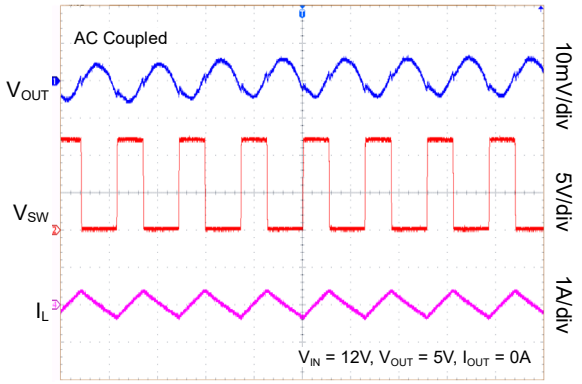
Load Regulation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

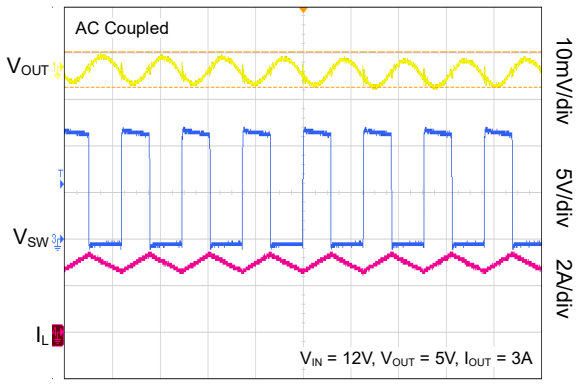
T_A = +25℃, V_{IN} = 12V, f_{SW} = 390kHz, L = 10μH and C_{OUT} = 100μF, unless otherwise noted.

Steady State



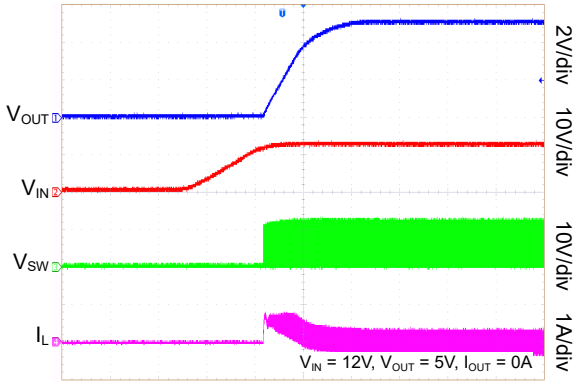
Time (2μs/div)

Steady State



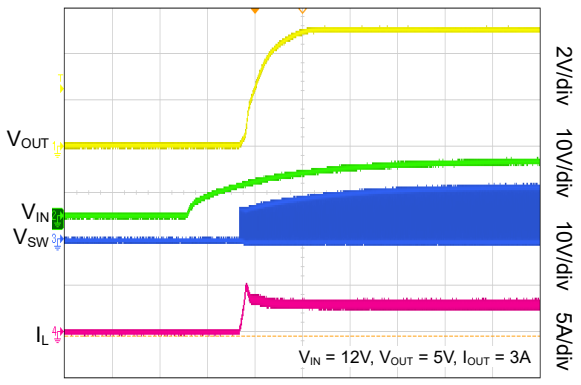
Time (2μs/div)

Start-Up by V_{IN}



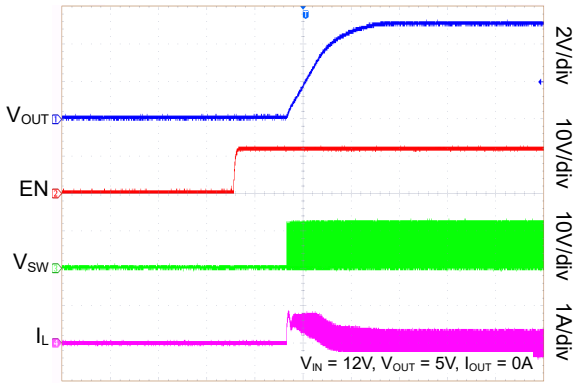
Time (800μs/div)

Start-Up by V_{IN}



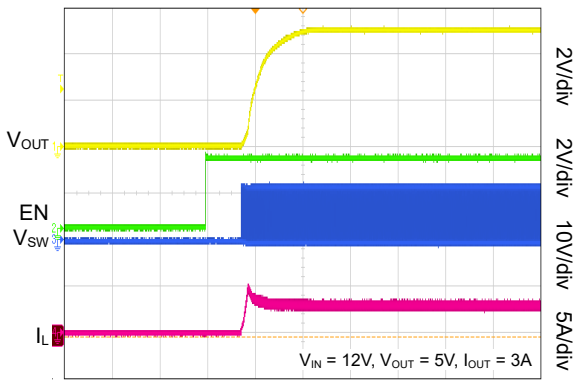
Time (1ms/div)

Start Up by EN



Time (800μs/div)

Start-Up by EN

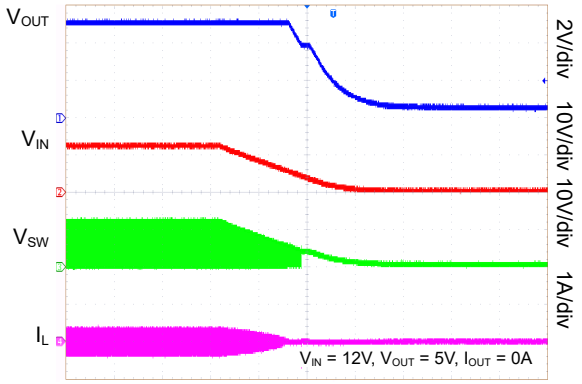


Time (1ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

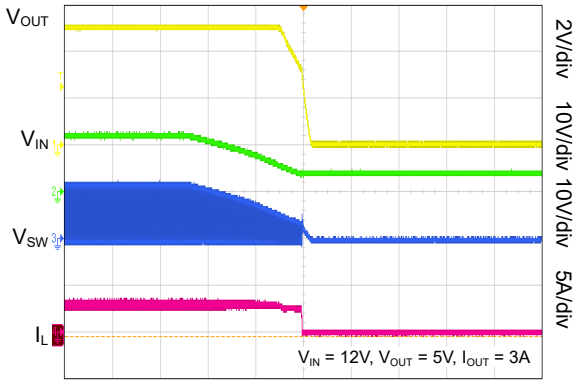
T_A = +25℃, V_{IN} = 12V, f_{SW} = 390kHz, L = 10μH and C_{OUT} = 100μF, unless otherwise noted.

Shutdown by V_{IN}



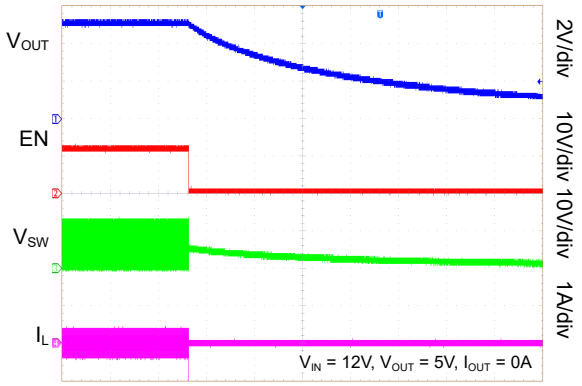
Time (10ms/div)

Shutdown by V_{IN}



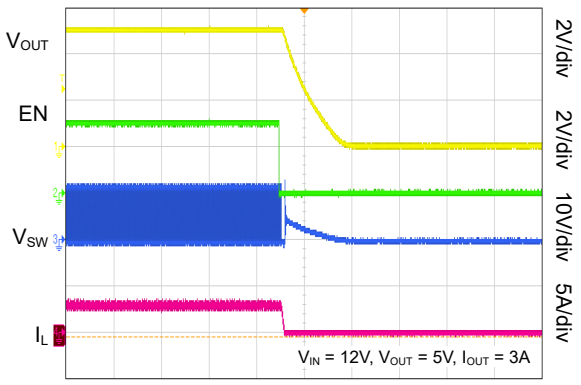
Time (500μs/div)

Shutdown by EN



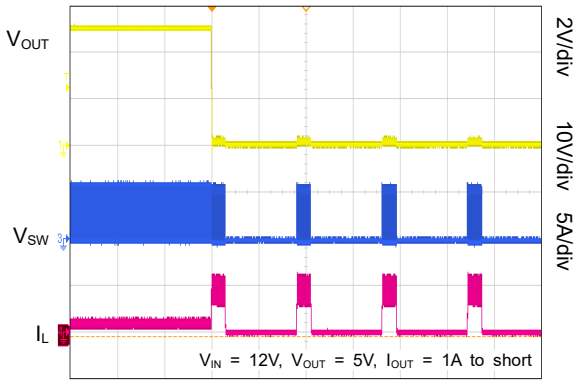
Time (1s/div)

Shutdown by EN



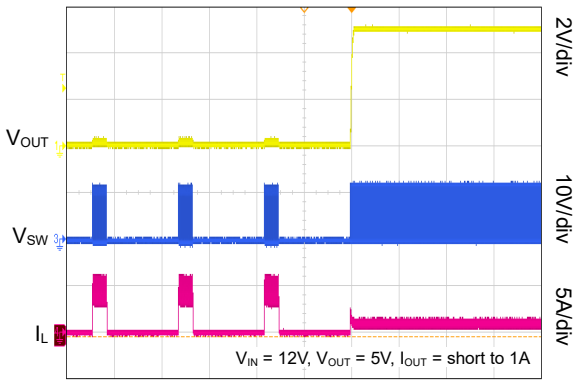
Time (100μs/div)

Short Protection



Time (20ms/div)

Short Recovery

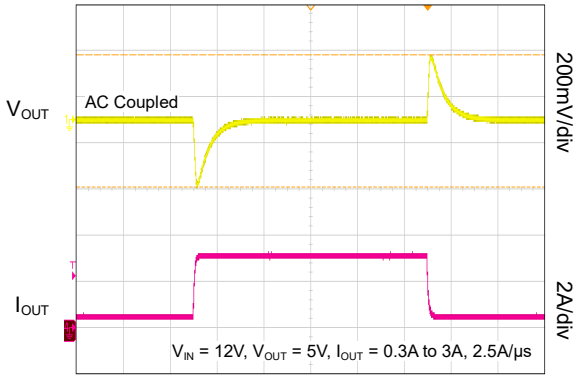


Time (20ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, f_{SW} = 390kHz, L = 10μH and C_{OUT} = 100μF, unless otherwise noted.

Load Transient



Time (200μs/div)

FUNCTIONAL BLOCK DIAGRAM

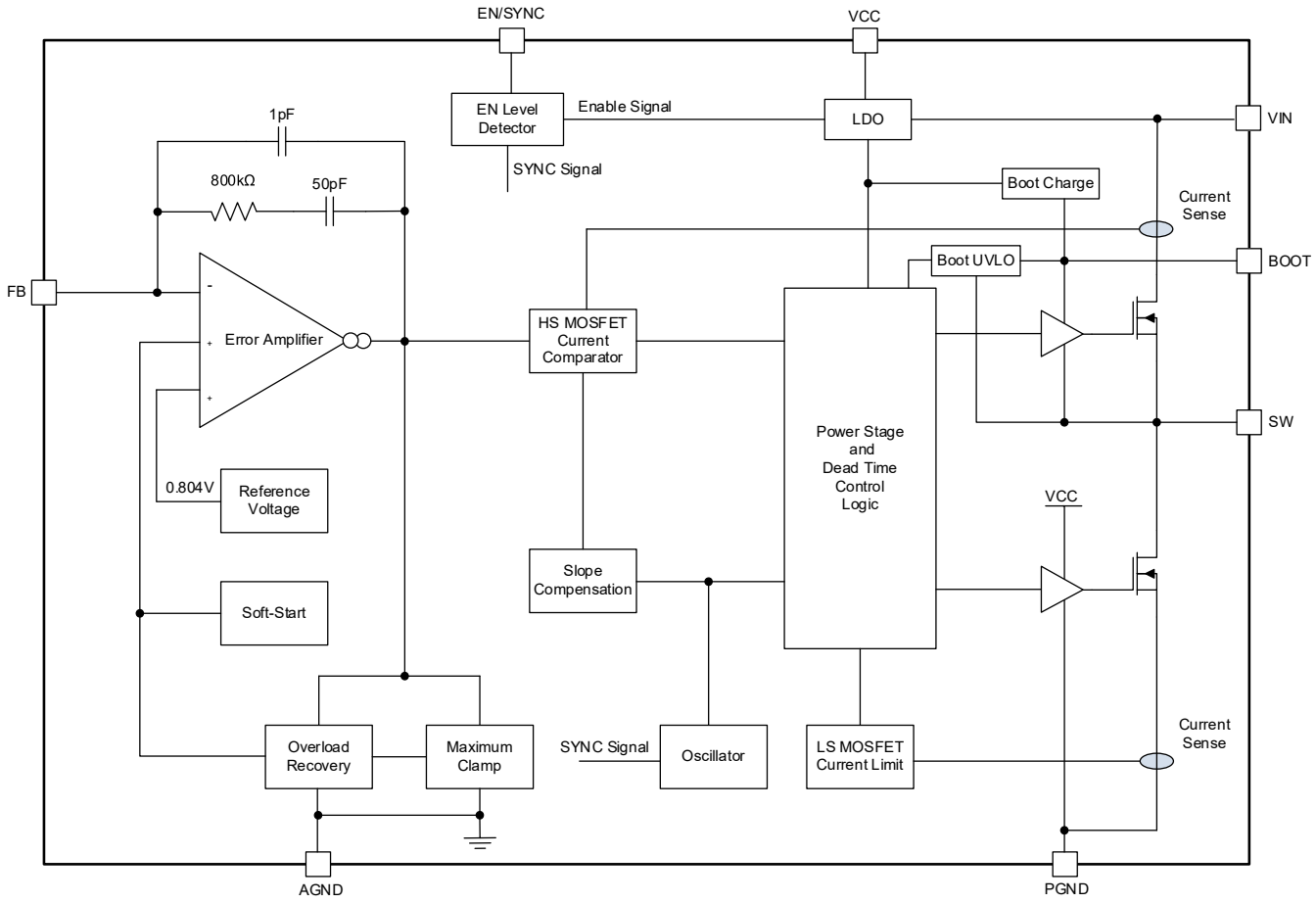


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61431 is a 3A output synchronous Buck converter with internal compensation and peak current mode control. It can operate from an input voltage range of 4.5V to 36V. The device needs a few external components and provides an easy and small size power supply solution for industrial applications with good thermal performance. With 0.6μA (TYP) shutdown current, it is also well suited for battery powered applications.

The device normally operates at fixed 390kHz frequency. At light load condition, the SGM61431 maintains FPWM mode to keep low output ripple and tight voltage regulation at light loads. The normal frequency can be synchronized to an external clock between 200kHz and 2.2MHz.

Accurate EN input threshold and internal soft-start time (1.5ms TYP) add more design flexibility to the device.

Additional features such as thermal shutdown, input under-voltage lockout, cycle-by-cycle current limit, and short-circuit protection (hiccup mode) are also provided.

Switching Frequency and Current Mode Control

The Functional Block Diagram and basic waveforms of this Buck synchronous converter are shown in Figure 2 and Figure 3. The N-MOSFETs are used for high-side (HS) and low-side (LS) (synchronous rectifier) switches. The HS duty cycle ($D = t_{ON}/t_{SW}$) is controlled in closed loop to regulate and maintain the output voltage at a constant level. The switching period is $t_{SW} = 1/f_{SW}$, and the HS on-time is t_{ON}. When HS is turned on, the SW node voltage sharply rises towards V_{IN}, and the inductor current (I_L) starts ramping up with (V_{IN} - V_{OUT})/L slope. When HS is turned off, the LS is turned on after a very short dead time to avoid shoot-through, and I_L ramps down with -V_{OUT}/L slope. When the inductor current is continuous, the output voltage is proportional to the input voltage and duty cycle ($V_{OUT} = D \times V_{IN}$) if component parasitics are ignored.

The output voltage is sensed by a resistor divider through FB pin and is regulated by feedback loop. This voltage is compared to an accurate reference and the voltage error signal is used as set point for an inner current loop that adjusts the peak inductor current. The input to the current loop is clamped to a fixed level to limit the maximum peak current and is compared to the actual peak current, sensed by the voltage drop across the HS switch to control the HS switch on-time. The loop internal compensation allows easy and stable design of the power supply with a few external elements for almost any output capacitor arrangement.

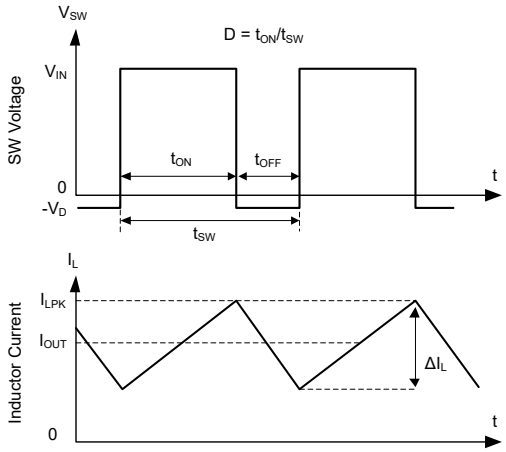


Figure 3. Converter Switching Waveforms in CCM

Output Voltage Setting

The output voltage can be stepped down to as low as the 0.804V reference voltage (V_{REF}). An external feedback resistor divider along with the internal reference is used to set the output voltage (V_{OUT}) as shown in Figure 4. The V_{REF} is compared to the V_{FB} voltage and the control loop adjusts the duty cycle to null the V_{REF} - V_{FB}.

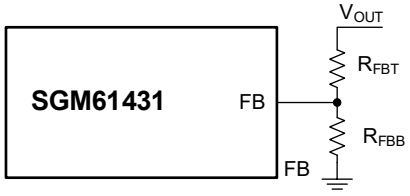


Figure 4. Output Voltage Setting

Use Equation 1 to calculate the output voltage:

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (1)$$

DETAILED DESCRIPTION (continued)

Use 1% or higher quality resistors with low thermal tolerance for an accurate and thermally stable output voltage. The low-side resistor R_{FBB} is selected based on the desired current in the divider. Typically, a 10kΩ to 100kΩ resistor is selected for R_{FBB}.

Large R_{FBT} values (>1MΩ) are not recommended because the feedback path impedance will be too high and more noise sensitive. If a large R_{FBT} value is necessary, the PCB layout design will be more critical because the feedback path must be short and away from noise sources such as SW node or inductor body.

EN/SYNC Input

The EN/SYNC pin is an input and must not be left open. The simplest way to enable the device is to connect this pin to VIN pin via a resistor. This allows for self-startup of the SGM61431 when $V_{IN} > V_{IN_UVLO}$. This pin can also be used to turn the device on or off with logic or analog signals. If V_{EN} < 1.07V (TYP), the device will shut down. Only if V_{EN} > 1.50V (TYP) the device will start operation.

The system UVLO level can be increased accurately with a resistor divider (see Figure 5). This feature can be used for power supply sequencing which is required for proper power up of the system voltage rails. It can also be used as protection, such as preventing supply battery from depletion. Control of the enable input by logic signals may also be used for sequencing or protection.

The EN/SYNC pin can also be used to synchronize the internal oscillator to an AC coupled external clock (see Figure 6). The SW cycles synchronize to the rising edges of the clock. Synchronization range is from 200kHz to 2.2MHz. The clock signal peak-to-peak voltage must exceed 2.8V to override the internal oscillator but must be kept below 5.5V. Also the on and off pulse widths of the clock must be at least 100ns (TYP). 3.3V clock amplitude and C_{SYNC} = 1nF (coupling capacitor) should be sufficient for most designs. Keep the $R_{ENT}||R_{ENB}$ near 100kΩ range for stable syncing. The R_{ENT} is necessary for external syncing but the R_{ENB} is only needed for UVLO adjustment.

The SGM61431 switching action can be synchronized to an external clock from 200kHz to 2.2MHz. Figure 6 shows the device synchronized to an external system clock.

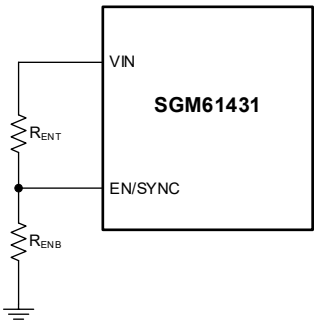


Figure 5. Changing the System UVLO

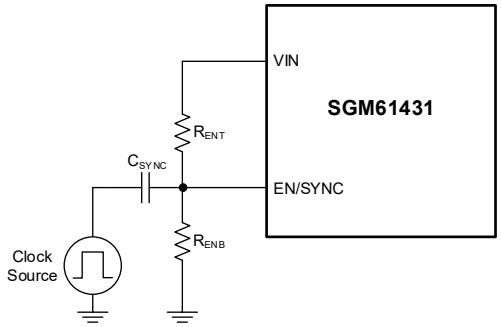


Figure 6. Synchronization to External Clock

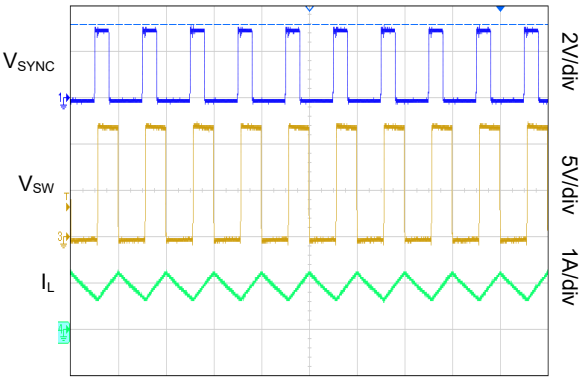


Figure 7. Synchronizing in PWM Mode

DETAILED DESCRIPTION (continued)

BOOT (Bootstrap Voltage)

The gate driver of the HS N-MOSFET switch requires a voltage higher than V_{IN} that is present on its drain. A bootstrap voltage regulator is integrated to provide this voltage which is powered by bootstrapping through a small ceramic capacitor placed between the BOOT and SW pins. C_{BOOT} is charged in each cycle when the LS switch is turned on (V_{SW} ≈ 0V) and discharges to the boot regulator when the HS switch is turned on (V_{SW} ≈ V_{IN}). A 0.47μF ceramic capacitor with 16V or higher rated voltage is recommended.

VCC Decoupling

The VCC pin is connected to the output of an LDO that is integrated in the device and provides a 5V supply (nominal) for the internal circuitry and MOSFET drivers. It is intended for bypassing LDO output to ground and should not be loaded. A 2.2μF to 10μF stable ceramic capacitor rated for $16V_{DC}$ or higher must be placed as close as possible to VCC pin and grounded to the exposed pad and ground pins. The device may be damaged if VCC pin is shorted to ground during operation.

Minimum On-Time and Off-Time

The shortest duration for the HS switch on-time (t_{ON_MIN}) is 110ns (TYP). For the off-time (t_{OFF_MIN}) the minimum value is 80ns (TYP). The duty cycle (or equivalently the V_{OUT}/V_{IN} ratio) range in CCM operation is limited by t_{ON_MIN} and t_{OFF_MIN} depending on the switching frequency. The minimum and maximum allowed duty cycles are given by Equations 2 and 3:

$$D_{MIN} = t_{ON_MIN} \times f_{SW} \quad (2)$$

and

$$D_{MAX} = 1 - t_{OFF_MIN} \times f_{SW} \quad (3)$$

Note that the duty cycle has a more limited range at higher frequencies. D_{MAX} limits the lowest V_{IN} voltage for a given V_{OUT}.

For any given output voltage, the switching frequency is an important factor to maximize efficiency and input voltage range and minimize solution size. The highest input voltage can be calculated from:

$$V_{IN_MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON_MIN}} \quad (4)$$

Due to losses in heavy load conditions there is a small increase in duty cycle and the actual V_{IN_MAX} is higher than Equation 4 prediction.

The minimum V_{IN} is estimated by:

$$V_{IN_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF_MIN}} \quad (5)$$

Compensation and Feed-Forward Capacitor (C_{FF})

The SGM61431 is internally compensated (see Figure 2) and is stable over the entire f_{SW} and V_{OUT} operating range. However, the phase margin can be low for some ranges of V_{OUT} when low ESR ceramic capacitors are used in the output. In such cases, it is recommended to use a feed-forward capacitor (C_{FF}) in parallel with the R_{FBT} to improve the transient response as shown in Figure 8.

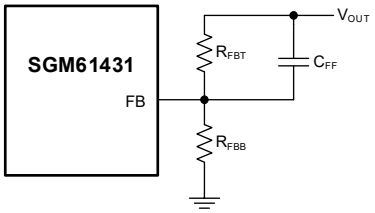


Figure 8. Improving Loop Compensation by Feed-Forward Capacitor

The C_{FF} in parallel with R_{FBT} places an additional zero before the loop cross over frequency and boosts the phase margin. The zero will be located at:

$$f_{Z_CFF} = \frac{1}{2\pi \times C_{FF} \times R_{FBT}} \quad (6)$$

Refer to Table 1 for a list of suitable C_{OUT}, C_{FF} and R_{FBT} combinations. If for similar C_{OUT} values, other R_{FBT} values are used, adjust the C_{FF} such that (C_{FF} × R_{FBT}) is unchanged. C_{FF} must also be modified if C_{OUT} is changed. For C_{OUT} capacitors with lower ESR, larger C_{FF} values are needed. For example, with electrolytic capacitors (large ESR), the location of ESR zero, (Equation 7), is typically low enough for phase boost at crossover and C_{FF} is not needed.

$$f_{Z_ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR} \quad (7)$$

DETAILED DESCRIPTION (continued)

Note that C_{FF} increases the feedback of the output ripple and the coupled noise to the FB node. A large C_{FF} value can deteriorate the V_{OUT} regulation. If significant derating for the C_{FF} value at cold operating temperatures is expected, it is better to use larger C_{OUT} capacitance rather than increasing the nominal C_{FF} value.

Thermal Shutdown (TSD)

If the junction temperature exceeds +175℃ (TYP), the device will shut down. It will recover automatically with a normal power up sequence and soft-start when the temperature falls below +155℃ (TYP).

Functional Modes

Shutdown Mode

The EN input controls the device on/off condition. If V_{EN} < 1.07V (TYP), the device will shut down. The device will also turn off if either V_{IN} or V_{CC} falls below its UVLO threshold.

Active Mode

If V_{EN} is above its precision threshold, and V_{IN} and V_{CC} are above their UVLO levels, the device will be activated. EN pin can be connected to VIN to allow self-startup when V_{IN} voltage is in the 4.5V to 36V operating range. VCC, UVLO and EN/SYNC settings in active mode are explained in the previous sections.

These operating modes are possible depending on the load current: (ΔI_L = inductor peak-to-peak current ripple)

1. **CCM**: Fixed frequency continuous conduction mode: it can operate in CCM when $I_{OUT} > \Delta I_L/2$.

2. **FPWM**: Forced pulse width modulation mode: it operates with fixed frequency at light load operation.

Continuous Conduction Mode (CCM)

In CCM, the frequency is fixed and the output voltage ripple will be minimal. The maximum output current of 3A is supplied in CCM.

Light Load Operation with FPWM

For FPWM option, SGM61431 is locked in PWM mode from full load to no load. Negative inductor currents are allowed at light load to continue PWM operation. It is a tradeoff that sacrifices light load efficiency for lower output ripple, better output regulation and keeping switching frequency fixed. To avoid fatal negative current in the LS switch, this current is limited at I_{L_NEG}. Synchronization is available over the full load range in the FPWM mode.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

Cycle-by-cycle current limit for both peak and valley currents (upper and lower switches peak currents) are included in the SGM61431. If the OCP or SCP persists, it will enter hiccup mode to avoid thermal shutdown.

The HS switch over-current protection is natural in peak current mode control. In each cycle the HS current sensing starts a short time (blanking time) after it is turned on. The slope compensation ramp is deducted from the EA (Error Amplifier) output to avoid sub harmonic oscillations and the result is compared to the HS current to determine the HS turn-off time (on-time). See Figure 2 for details. Before comparison, the EA output is clamped to a fixed maximum threshold (I_{HS_LIMIT}) to limit the current. So, the peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

When the LS switch turns on the inductor current starts falling. The LS current is sensed while it is on and the switch will not turn off at the end of cycle if this current is still higher than its limit (I_{LS_LIMIT}) and keeps conducting until the current falls below I_{LS_LIMIT}. During OCP or SCP, the LS current limit is not effective until the HS current limit is triggered.

A short dead time is considered after the LS switch is turned off, in which both switches are kept off and then a new cycle starts by turning the HS switch on.

If the LS switch over-current detection continues for 128 successive cycles, hiccup current protection will be started in which the regulator remains off for 30ms (TYP) before restarting the converter. If OCP or SCP is still detected after this restart, a new hiccup cycle will be repeated. Hiccup mode is considered to protect the device from overheating and damage in severe over-current conditions.

In the FPWM option, the inductor current can go negative at light load or during transients. For this device, the LS switch current is limited by negative current (I_{L_NEG}) and if the magnitude of the negative current exceeds this limit, the LS switch will turn off until the next cycle to protect the switch from large currents.

APPLICATION INFORMATION

The design method and component selection for the SGM61431 Buck converter are explained in this section. Schematic of a basic design is shown in Figure 9. Only a few external components are needed to provide a constant output voltage from a wide input voltage range.

The external components are designed based on the application requirements and device stability. Some suitable output filters (L and C_{OUT}) along with C_{FF} and R_{FBT} values are provided in Table 1 to simplify component selection. Consider the following notes when using this table.

1. Choose the inductance for V_{IN} = 36V.
2. C_{OUT} values in the table are actual derated values. Use higher nominal values for ceramic capacitors.
3. Use R_{FBT} = 0Ω to set V_{OUT} = 0.804V. Use R_{FBB} = 14.3kΩ for any other V_{OUT} setting.
4. If any other R_{FBT} value is designed, resize C_{FF} to keep (C_{FF} × R_{FBT}) unchanged.
5. If the selected output capacitance has high ESR, the C_{FF} is not necessary for extra phase boost.

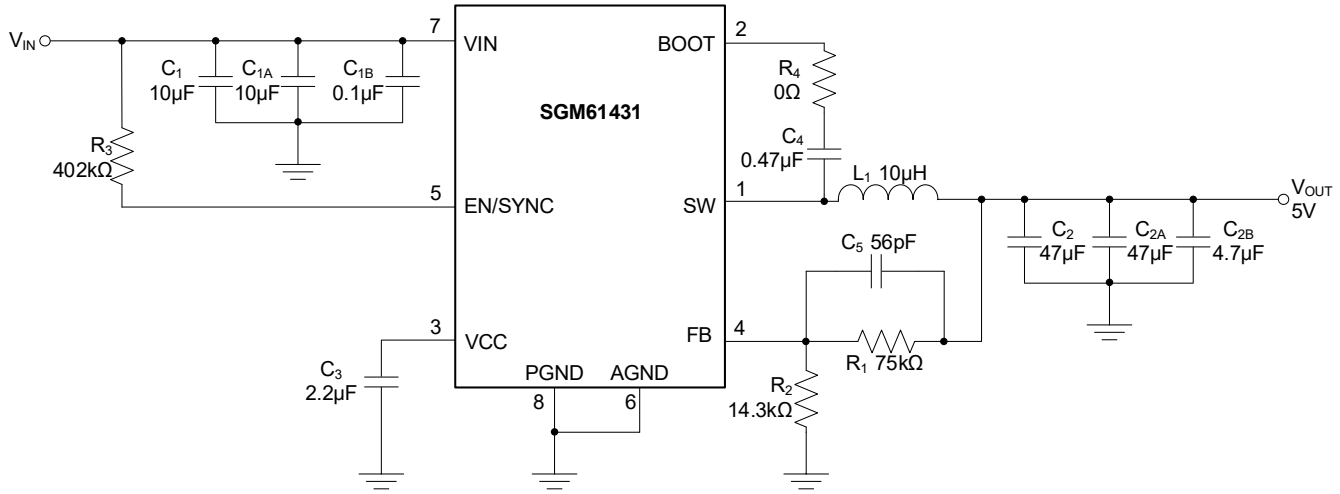


Figure 9. SGM61431 Basic Application Schematic

Table 1. Some Typical L, C_{OUT} and C_{FF} Values for Stable Operation

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	C_{FF} (pF)	R_{FBB} (kΩ)	R_{FBT} (kΩ)
390	3.3	6.8	150	75	14.3	44.2
390	5	10	100	56	14.3	75
390	12	15	68	-	14.3	200
390	24	15	47	-	14.3	412

Design Requirements

The design process will be explained by an example with the required input parameters listed in Table 2.

Table 2. Design Example Parameters

PARAMETER	SGM61431
Input Voltage (V_{IN})	12V (TYP), variation range is from 8V to 28V
Output Voltage (V_{OUT})	5V
Maximum Output Current (DC) (I_{OUT_MAX})	3A
Transient Response (0.3A to/from 3A)	5% (V_{OUT} drop/rise)
Output Voltage Ripple	50mV
Input Voltage Ripple	400mV
Switching Frequency (f_{SW})	390kHz

APPLICATION INFORMATION (continued)

Input Capacitor

High frequency decoupling on the input supply pins is necessary for the device. A bulk capacitor may also be needed in some applications. Typically, 10μF to 22μF high quality ceramic capacitor (X5R, X7R or better) with voltage rating twice the maximum input voltage is recommended for decoupling capacitor. If the source is away from the device (> 5cm) some bulk capacitance is also needed to damp the voltage spikes caused by the wiring or PCB trace parasitic inductances. In this example, 2×10μF/50V/X7R capacitors and a 0.1μF ceramic capacitor placed right beside the device VIN and GND pins for very high-frequency filtering are used.

Output Capacitor

The main factors for designing C_{OUT} are output voltage ripple, control loop stability and the magnitude of output voltage overshoot/undershoot after a load transients.

The output voltage ripple has two main components. One is due to the ac current (ΔI_L) going through the capacitor ESR:

$$\Delta V_{OUT_ESR} = \Delta I_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (8)$$

and the other one is caused by the charge and discharge of capacitor by the ac current (ΔI_L):

$$\Delta V_{OUT_C} = \frac{\Delta I_L}{\left(8 \times f_{SW} \times C_{OUT}\right)} = \frac{K_{IND} \times I_{OUT}}{\left(8 \times f_{SW} \times C_{OUT}\right)} \quad (9)$$

These AC components are not in phase and the total peak-to-peak ripple is less than $\Delta V_{OUT_ESR} + \Delta V_{OUT_C}$.

In many applications, tight regulation in response to large and fast load transients is required. This can be a more severe condition on designing C_{OUT} value. Typically the control loop recovers the output voltage after four or five cycles and C_{OUT} should be large enough to provide the difference between current received from inductor and the current delivered to the load during this period. The minimum capacitance needed to limit the undershoot to V_{US} when the load steps up from I_{OL} to I_{OH} is given in Equation 10. Similarly, when the load steps from I_{OH} down to I_{OL}, C_{OUT} should be large enough to absorb the extra energy coming from the inductor without a large voltage overshoot (V_{OS}) as calculated in Equation 11:

$$C_{OUT} > \frac{4 \times \left(I_{OH} - I_{OL}\right)}{f_{SW} \times V_{US}} \quad (10)$$

$$C_{OUT} > \frac{I_{OH}^2 - I_{OL}^2}{\left(V_{OUT} + V_{OS}\right)^2 - V_{OUT}^2} \times L \quad (11)$$

In this example, maximum acceptable ripple is 50mV. Assuming $\Delta V_{OUT_ESR} = \Delta V_{OUT_C} = 50mV$ and $K_{IND} = 0.4$. Equation 8 results in ESR < 41.7mΩ and Equation 9 leads to C_{OUT} > 7.5μF. If the overshoot/undershoot transient requirement is 5% then $V_{US} = V_{OS} = 5\% \times V_{OUT}$ = 250mV. Equations 10 and 11, I_{OH} = 2.5A, I_{OL} = 0.2A, lead to C_{OUT} > 94μF and C_{OUT} > 24μF respectively. Now considering all conditions and including voltage derating of the ceramic capacitors, C_{OUT} is composed of a 47μF/16V ceramic capacitor parallel with a 100μF/10V capacitor with 5mΩ ESR.

Output Voltage Setting

An external resistor divider is used to set the output voltage as shown in Figure 8. Use Equation 12 to set V_{OUT}:

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (12)$$

where V_{REF} = 0.804V is the internal reference. For example, by choosing R_{FBB} = 14.3kΩ, the R_{FBT} value for 5V output will be calculated as 75kΩ.

Switching Frequency

The SGM61431 switching frequency is 390kHz (TYP). However, it can be modified by synchronizing to an external clock in the 200kHz to 2.2MHz range.

Inductor

Three main inductor parameters that need to be designed are inductance, saturation current and rated current. The DCR is also an important factor for efficiency. Physical dimensions, form factor and shielded or non-shielded structure are other important factors that are selected based on the application. The inductance is designed by selecting the peak-to-peak current ripple (ΔI_L) that is given by Equation 13. ΔI_L is increase at higher input voltages, so V_{IN_MAX} is used in the equation. The minimum required inductance (L_{MIN}) is calculated from Equation 14. K_{IND} represents the ratio of inductor ripple current to the maximum output current

APPLICATION INFORMATION (continued)

(K_{IND} =$\Delta I_L/I_{OUT_MAX}$). It is typically chosen between 20% to 40%.

$$\Delta I_L = \frac{V_{OUT} \times \left(V_{IN_MAX} - V_{OUT}\right)}{V_{IN_MAX} \times L \times f_{SW}} \quad (13)$$

$$L_{MIN} = \frac{V_{IN_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \quad (14)$$

During a short or over current, either RMS or peak inductor current can increase significantly. The inductor rated RMS and saturation current ratings should be higher than those peaks respectively. It is generally desired to choose an smaller inductance value to have faster transient response, smaller size, and lower DCR. However, reducing the inductance increases the current ripple that may result in over current detection and triggering OCP before reaching full load current. Moreover, higher current ripple increases core, conduction, and capacitor losses. Output voltage ripple will also be higher with the same output capacitance. In general, choosing a too small inductance is not recommended for peak current mode control. On the other hand, too large inductance is also not recommended, because the reduced current ripple degrades the comparator signal to noise ratio.

Selecting K_{IND} = 0.4 results in L_{MIN} = 8.78μH. A 10μH ferrite inductor with 5A RMS rating and 7.6A saturation current is selected as the closest standard value.

Designing Feed-Forward Capacitor

Even though the SGM61431 is internally compensated, with low ESR ceramic capacitors, the phase margin can be low depending on the V_{OUT} and f_{SW} values. By adding an external feed-forward capacitor (C_{FF}) in parallel with the R_{FBT}, the phase margin can be improved (phase boost around crossover frequency). Without C_{FF}, and if ESR is very small, the crossover frequency (f_X) can be estimated from Equation 15, in which C_{OUT} is the actual derated value:

$$f_X = \frac{8.32}{V_{OUT} \times C_{OUT}} \quad (15)$$

Then C_{FF} value can be estimated from:

$$C_{FF} = \frac{1}{4\pi \times f_X \times R_{FBT}} \quad (16)$$

For slightly larger ESR values, choose a C_{FF} value that is less than Equation 16 estimate. For larger ESR values, C_{FF} is not needed. Table 1 gives a quick starting point. In this example, a 56pF/50V/COG is selected for C_{FF}.

Bootstrap Capacitor

The bootstrap capacitor powers the floating power MOSFET driver. It is recommended to use 0.47μF/16V/X5R ceramic capacitor.

The value of BST resistor generally is recommended to be in the range from 0 to 10Ω. BST resistor determines the turning on speed of the high side MOSFET. For the design where the critical path layout could not be optimized and follow the recommended layout, the 10Ω BST resistor is recommended to be used to in series with the Bootstrap capacitor.

VCC Decoupling Capacitor (LDO Output)

Use a 2.2μF/16V/X7R capacitor for decoupling VCC to assure stability of the device. It must be placed with minimum distance between VCC and GND pins.

V_{IN} UVLO Adjustment

The system UVLO threshold can be increase using two external resistors R_{ENT} and R_{ENB} (see Figure 5) to form a voltage divider between VIN and EN pins. The UVLO comparator provides a rising threshold (power-up) and a falling threshold (power-down) for V_{IN}. Use Equation 17 to set the UVLO rising threshold.

$$V_{IN_RISING} = V_{EN_H} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (17)$$

V_{EN_H} is the EN rising threshold (1.50V TYP). Choose a large value for R_{ENB} (e.g., 287kΩ), to minimize supply drain. The R_{ENT} value is given by:

$$R_{ENT} = \left(\frac{V_{IN_RISING}}{V_{EN_H}} - 1\right) \times R_{ENB} \quad (18)$$

The resulting falling threshold can be calculated from:

$$V_{IN_FALLING} = \left(V_{EN_H} - V_{EN_HYS}\right) \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (19)$$

In which the V_{EN_HYS} is 0.43V (TYP).

In this example, V_{IN_RISING} = 6.0V is needed that results in R_{ENT} = 853kΩ and a UVLO falling threshold of 4.29V.

APPLICATION INFORMATION (continued)

Layout

Consider the following layout design guidelines for a high-quality power supply with good thermal and EMI performances.

1. Place C_{INx} as close as possible to the VIN and PGND pins. C_{INx} and C_{OUTx} returns should be close together and connected on the top layer PGND pin/plane and PAD.

2. Place C_{VCC} bypass capacitor right beside the VCC and ground pins on the top layer.

3. Minimize FB trace length and keep both feedback resistors close to the FB pin. Bring the V_{OUT} sense trace from the point where V_{OUT} accuracy is important and keep it away from the noisy nodes (SW), preferably through another layer that is on the other side of a shield layer. Place C_{FF} right beside R_{FBT}.

4. Use one of the mid-layers as ground plane for noise shielding and extra path for heat dissipation.

5. Connect the ground layer to only one ground point on the top layer. The feedback and enable circuit returns must be routed separately through the ground plane to avoid large load currents or high di/dt switching currents to flow in these sensitive analog ground traces. Bad grounding results in poor regulation and erratic output ripple.

6. Choose wide traces for V_{IN}, V_{OUT} and ground to minimize voltage drops and maximize efficiency.

7. Use an array of thermal vias (e.g., 8 filled vias) under the exposed pad and connect them to the ground planes on mid-layers and the bottom layer. Maximize the heat sinking copper areas and solidify them with metal coatings such that the die temperature remains below +125℃ in all operating conditions.

Layout Example

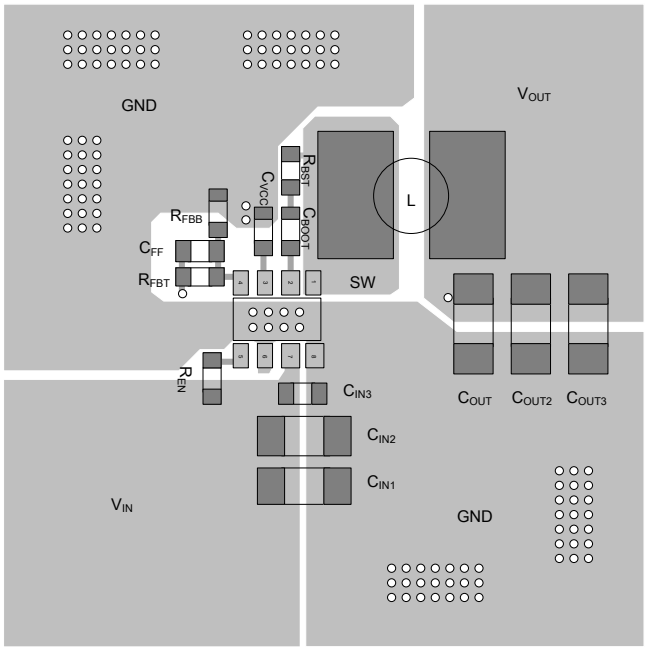


Figure 10. Top Layer

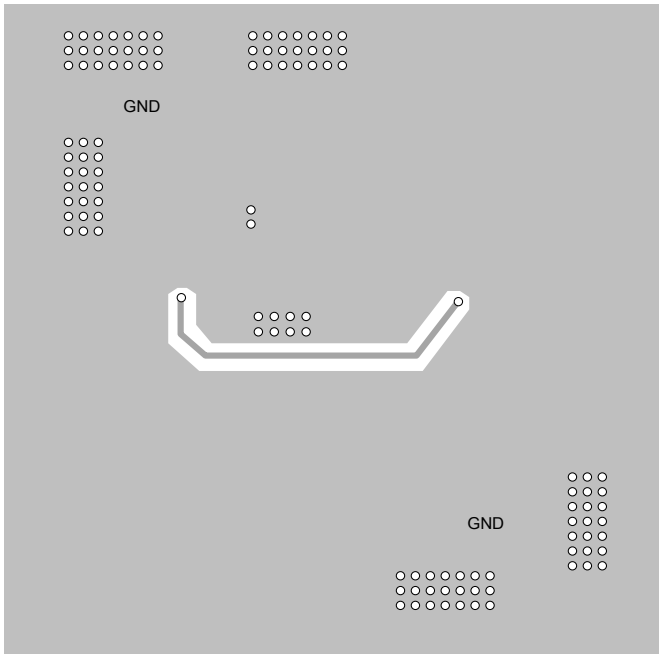


Figure 11. Bottom Layer

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JANUARY 2025 – REV.A.3 to REV.A.4	Page
Removed SGM61430	All
Updated Package Thermal Resistance	2
Updated Block Diagram	10

JANUARY 2023 – REV.A.2 to REV.A.3	Page
Changed Detailed Description	16

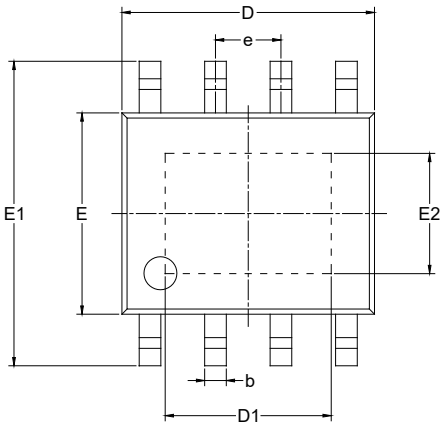
JULY 2022 – REV.A.1 to REV.A.2	Page
Added thermal information	2

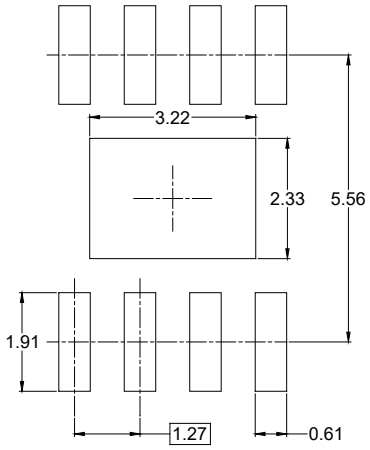
JANUARY 2022 – REV.A to REV.A.1	Page
Added SGM61431 part	All

Changes from Original (SEPTEMBER 2021) to REV.A	Page
Changed from product preview to production data	All

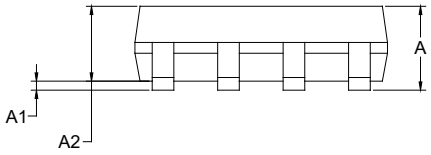
PACKAGE OUTLINE DIMENSIONS

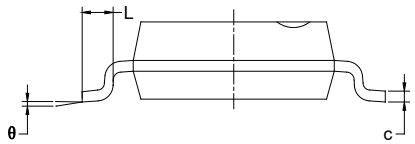
SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)





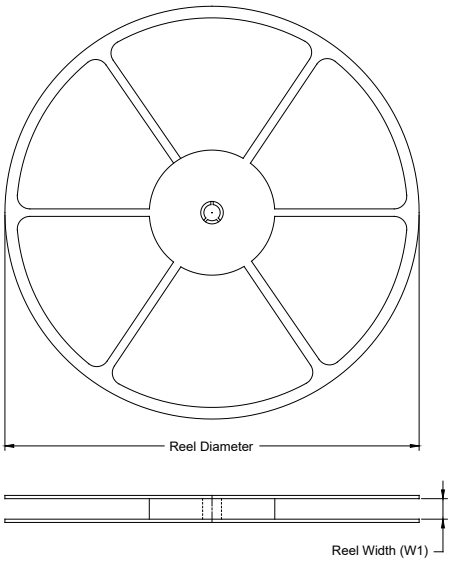
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°

NOTES:

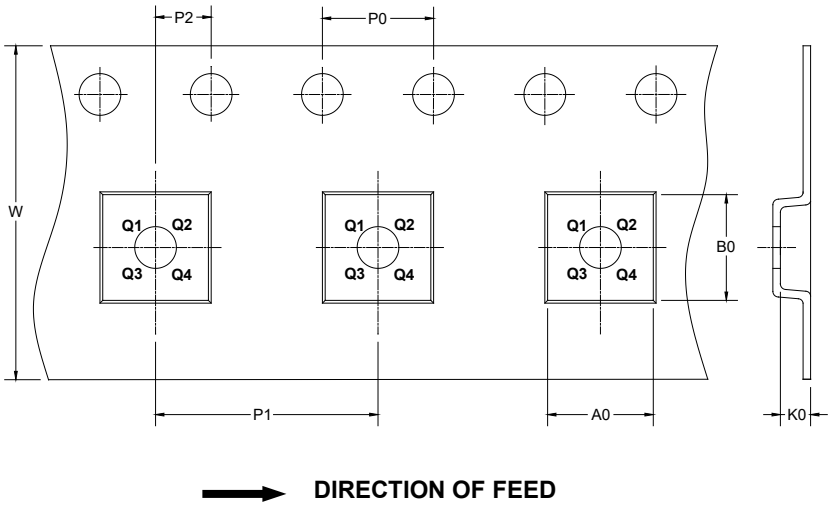
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



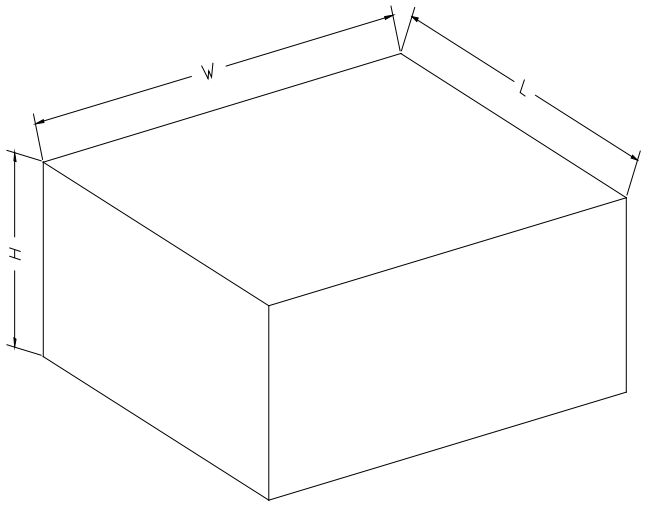
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002