# SGM48523C/SGM48524C
# Dual 5A, High-Speed, Low-Side Gate Drivers with Negative Input Voltage Capability

## GENERAL DESCRIPTION

The SGM48523C and SGM48524C are dual high-speed low-side gate drivers for power switches. They have rail-to-rail driving capability and can sink or source up to 5A peak current with capacitive loads. The propagation delays are very short and well matched between the two channels that make the device well suited for applications that need accurate dual gate driving such as synchronous rectifiers. The matched propagation delays also allow for paralleling the two channels when higher driving current is required for example for paralleled switches. The input voltage thresholds are fixed, independent of supply voltage ($V_{DD}$), and compatible with low voltage TTL and CMOS logic. Noise immunity is excellent due to the wide hysteresis window between the input low and high thresholds. The devices have internal pull-up/pull-down resistors on the input pins to ensure low state on the driver output when the input is floating.

The dual inverting SGM48523C and the dual non-inverting SGM48524C are both available in Green SOIC-8, TDFN-3×3-8L and MSOP-8 (Exposed Pad) packages.

## FEATURES

- **Two Independent Gate Drive Channels**
- **5A Source and 5A Sink Peak Currents**
- **Wide Supply Voltage Range: 8.5V to 18V**
- **TTL and CMOS Compatible Logic Threshold**
- **Logic Levels Independent of Supply Voltage**
- **Hysteretic Input Logic for High Noise Immunity**
- **Outputs Held Low when Inputs are Floating**
- **Fast Propagation Delays**
- **Fast Rise Time: 7ns (TYP)**
- **Fast Fall Time: 7ns (TYP)**
- **Ringing Suppression**
- **Negative Voltage Capability on INx Pins: -10V when ($V_{DD}$ - $V_{INx}$) ≤ 20V**
- **Negative Voltage Capability on ENx Pins: -10V when ($V_{DD}$ - $V_{ENx}$) ≤ 20V**
- **Negative Voltage Capability on OUTx Pin: -2V (Pulse < 200ns)**
- **Protection Features**
  - **Thermal Shutdown Protection**
  - **Under-Voltage Lockout**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-8, MSOP-8 (Exposed Pad) and TDFN-3×3-8L Packages**

## APPLICATIONS

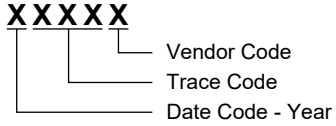
DC/DC Converters
Solar Power, Motor Drivers
Switched-Mode Power Supplies
Gate Drive for Emerging Wide Bandgap Devices

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM48523C | SOIC-8 | -40℃ to +125℃ | SGM48523CXS8G/TR | SGM<br>48523CXS8<br>XXXXX | Tape and Reel, 4000 |
| | MSOP-8 (Exposed Pad) | -40℃ to +125℃ | SGM48523CXPMS8G/TR | SGM03G<br>XPMS8<br>XXXXX | Tape and Reel, 4000 |
| | TDFN-3×3-8L | -40℃ to +125℃ | SGM48523CXTDB8G/TR | SGM<br>03DDB<br>XXXXX | Tape and Reel, 4000 |
| SGM48524C | SOIC-8 | -40℃ to +125℃ | SGM48524CXS8G/TR | SGM<br>48524CXS8<br>XXXXX | Tape and Reel, 4000 |
| | MSOP-8 (Exposed Pad) | -40℃ to +125℃ | SGM48524CXPMS8G/TR | SGM03E<br>XPMS8<br>XXXXX | Tape and Reel, 4000 |
| | TDFN-3×3-8L | -40℃ to +125℃ | SGM48524CXTDB8G/TR | SGM<br>03BDB<br>XXXXX | Tape and Reel, 4000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

VDD ..... -0.3V to 20V
Continuous INA, INB when ($V_{DD}$ - $V_{INx}$) ≤ 20V
.....-10V to $V_{DD}$ + 0.3V
Continuous ENA, ENB when ($V_{DD}$ - $V_{ENx}$) ≤ 20V
.....-10V to $V_{DD}$ + 0.3V
Continuous OUTA, OUTB (DC) .....-0.3V to $V_{DD}$ + 0.3V
Pulse OUTA, OUTB (Pulse < 200ns).....-2V to $V_{DD}$ + 0.3V
Package Thermal Resistance
SOIC-8, $\theta_{JA}$ ..... 121℃/W
MSOP-8 (Exposed Pad), $\theta_{JA}$..... 55℃/W
TDFN-3×3-8L, $\theta_{JA}$ ..... 70℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility
HBM.....7000V
CDM .....1000V

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range .....8.5V to 18V
Operating Junction Temperature Range.....-40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

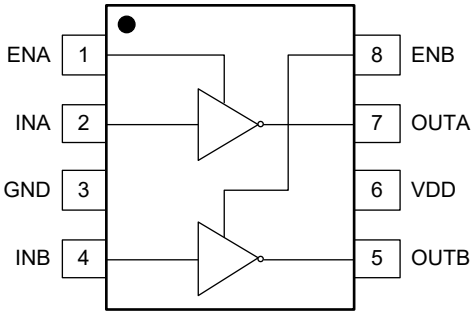
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

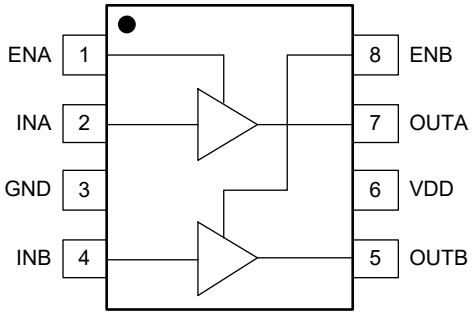
## PIN CONFIGURATIONS

SGM48523C (TOP VIEW)



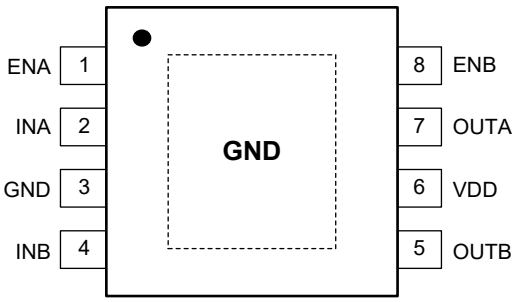

SOIC-8

SGM48524C (TOP VIEW)



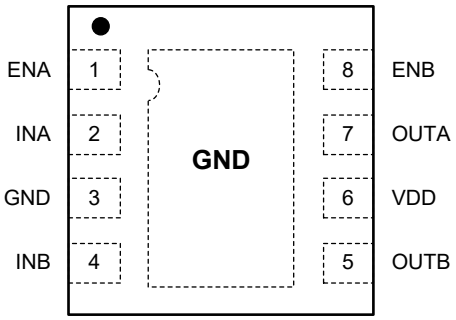

SOIC-8

SGM48523C/SGM48524C (TOP VIEW)




MSOP-8 (Exposed Pad)

SGM48523C/SGM48524C (TOP VIEW)




TDFN-3×3-8L

## PIN DESCRIPTION

| PIN | NAME | I/O | FUNCTION |
|---|---|---|---|
| 1 | ENA | I | Channel A Enable Input. Pull ENA high or leave it floating to enable OUTA output. Pull ENA low to disable OUTA output, ignoring INA state. |
| 2 | INA | I | Input for Channel A. Inverting input in SGM48523C and non-inverting input in SGM48524C. OUTA is held low if INA is unbiased or left floating. |
| 3 | GND | — | Ground. Reference pin for all signals. |
| 4 | INB | I | Input for Channel B. Inverting input in SGM48523C and non-inverting input in SGM48524C. OUTB is held low if INB is unbiased or left floating. |
| 5 | OUTB | O | Channel B Output. |
| 6 | VDD | I | Power Supply Input. |
| 7 | OUTA | O | Channel A Output. |
| 8 | ENB | I | Channel B Enable Input. Pull ENB high or leave it floating to enable OUTB output. Pull ENB low to disable OUTB output, ignoring INB state. |
| Exposed Pad | GND | — | Exposed Pad. It is internally connected to GND. Connect it to a large ground plane to maximize thermal performance; not intended as an electrical connection point. |

NOTE: I: input, O: output.

## FUNCTION TABLE

| SGM48523C/SGM48524C | | | | SGM48523C | | SGM48524C | |
|---|---|---|---|---|---|---|---|
| ENA | ENB | INA | INB | OUTA | OUTB | OUTA | OUTB |
| H | H | L | L | H | H | L | L |
| H | H | L | H | H | L | L | H |
| H | H | H | L | L | H | H | L |
| H | H | H | H | L | L | H | H |
| L | L | Any | Any | L | L | L | L |
| Any | Any | Floating | Floating | L | L | L | L |
| Floating | Floating | L | L | H | H | L | L |
| Floating | Floating | L | H | H | L | L | H |
| Floating | Floating | H | L | L | H | H | L |
| Floating | Floating | H | H | L | L | H | H |

## TYPICAL APPLICATION

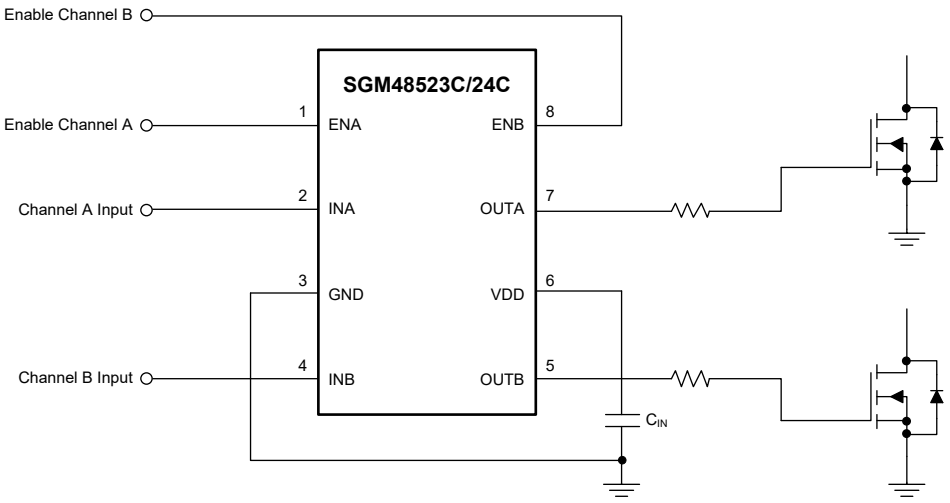



**Figure 1. Typical Application Circuit**

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 12V, $C_{IN}$ = 4.7μF, $T_J$ = -40℃ to +125℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Power Supplies** | | | | | | | |
| VDD Operating Supply Voltage | $V_{DD}$ | | | 8.5 | | 18 | V |
| VDD Operating Supply Current | $I_{DD}$ | SGM48523C | $V_{DD}$ = 3.4V, $V_{INA}$ = $V_{INB}$ = GND | | 110 | 169 | μA |
| | | | $V_{DD}$ = 3.4V, $V_{INA}$ = $V_{INB}$ = $V_{DD}$ | | 75 | 118 | |
| | | | INx and ENx floating | | 260 | 400 | |
| | | SGM48524C | $V_{DD}$ = 3.4V, $V_{INA}$ = $V_{INB}$ = GND | | 74 | 118 | |
| | | | $V_{DD}$ = 3.4V, $V_{INA}$ = $V_{INB}$ = $V_{DD}$ | | 110 | 169 | |
| | | | INx and ENx floating | | 285 | 439 | |
| VDD Under-Voltage Lockout Voltage | $V_{ON}$ | | | 7.6 | 8.05 | 8.5 | V |
| | $V_{OFF}$ | | | 6.6 | 7 | 7.4 | V |
| Supply Voltage Hysteresis | $V_{HYS}$ | | | 0.85 | 1.05 | 1.25 | V |
| **Inputs (INA, INB)** | | | | | | | |
| Input Signal High Threshold | $V_{IN\_H}$ | | | 1.9 | 2.1 | 2.3 | V |
| Input Signal Low Threshold | $V_{IN\_L}$ | | | 1 | 1.2 | 1.4 | V |
| Input Hysteresis | $V_{IN\_HYS}$ | | | 0.7 | 0.9 | 1.1 | V |
| Input Low Current | $I_{IL}$ | SGM48523C | $V_{DD}$ = 18V, $T_J$ = +25℃ | | 96 | 130 | μA |
| | | SGM48524C | | | 0.1 | 1 | |
| Input High Current | $I_{IH}$ | SGM48523C | $V_{DD}$ = 18V, $T_J$ = +25℃ | | 1.9 | 10 | μA |
| | | SGM48524C | | | 100 | 135 | |
| **Enable (ENA, ENB)** | | | | | | | |
| Enable Signal High Threshold | $V_{EN\_H}$ | | | 1.9 | 2.1 | 2.3 | V |
| Enable Signal Low Threshold | $V_{EN\_L}$ | | | 1 | 1.2 | 1.4 | V |
| Enable Hysteresis | $V_{EN\_HYS}$ | | | 0.7 | 0.9 | 1.1 | V |
| Enable Low Current | $I_{ENL}$ | $V_{DD}$ = 18V, $T_J$ = +25℃ | | | 96 | 130 | μA |
| Enable High Current | $I_{ENH}$ | $V_{DD}$ = 18V, $T_J$ = +25℃ | | | 1.9 | 10 | μA |
| **Outputs (OUTA, OUTB)** | | | | | | | |
| Output Pull-Up Resistance (1) | $R_{OH}$ | $I_{OUT}$ = 10mA | | | 4.6 | 7.2 | Ω |
| Output Pull-Down Resistance | $R_{OL}$ | $I_{OUT}$ = -10mA | | | 465 | 800 | mΩ |
| Peak Output Current | $I_{PK\_SOURCE}$ | $C_L$ = 0.22μF, $f_{SW}$ = 1kHz | | | 5 | | A |
| | $I_{PK\_SINK}$ | | | | 5 | | A |
| **Switching Characteristics** | | | | | | | |
| Rise Time | $t_R$ | $C_L$ = 1.8nF, see Figure 2 through Figure 5 | | | 7 | | ns |
| Fall Time | $t_F$ | $C_L$ = 1.8nF, see Figure 2 through Figure 5 | | | 7 | | ns |
| Delay Matching between 2 Channels | $t_M$ | INA = INB, OUTA and OUTB at 50% transition point | | | 1 | | ns |
| Input to Output Propagation Delay | $t_{D1}$ | SGM48523C | $C_L$ = 1.8nF, 4V input pulse, see Figure 2 and Figure 4 | | 21 | | ns |
| | $t_{D2}$ | | | | 17 | | |
| | $t_{D1}$, $t_{D2}$ | SGM48524C | | | 18 | | |
| EN to Output Propagation Delay | $t_{D3}$, $t_{D4}$ | $C_L$ = 1.8nF, 4V enable pulse, see Figure 3 and Figure 5 | | | 18 | | ns |
| **Protection Circuits** | | | | | | | |
| Thermal Shutdown Temperature | $T_{TSD}$ | | | | 165 | | ℃ |
| Thermal Shutdown Temperature Hysteresis | $T_{HYS}$ | | | | 25 | | ℃ |

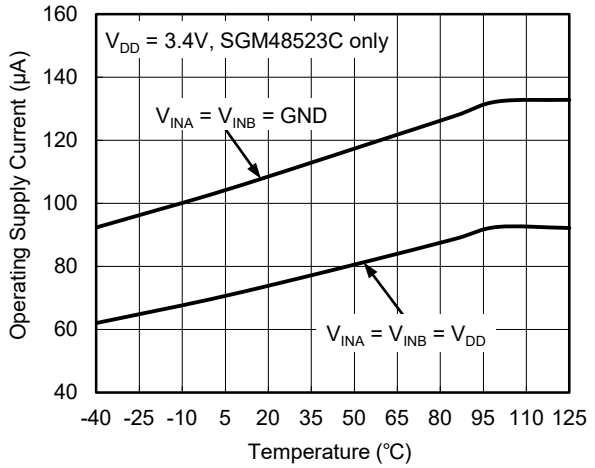
NOTE:

1. $R_{OH}$ represents constant pull-up resistance only. Pull-up resistance $R_{OH\_PULSE}$ operates in pulse mode during the output rising stage, $R_{OH\_PULSE}$ = 730mΩ (TYP).

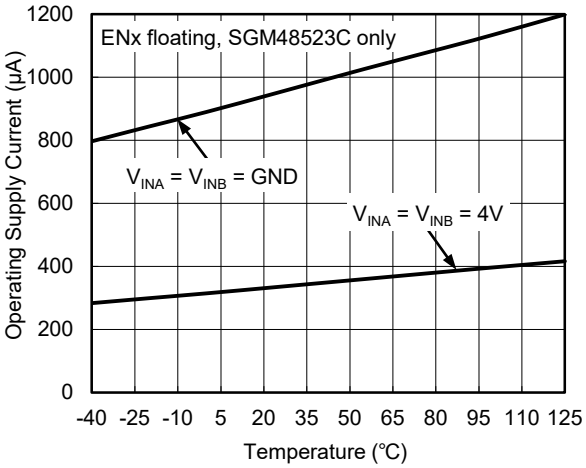
## TYPICAL PERFORMANCE CHARACTERISTICS

At $T_J$ = +25℃, $V_{DD}$ = 12V, $C_{IN}$ = 4.7μF, unless otherwise noted.

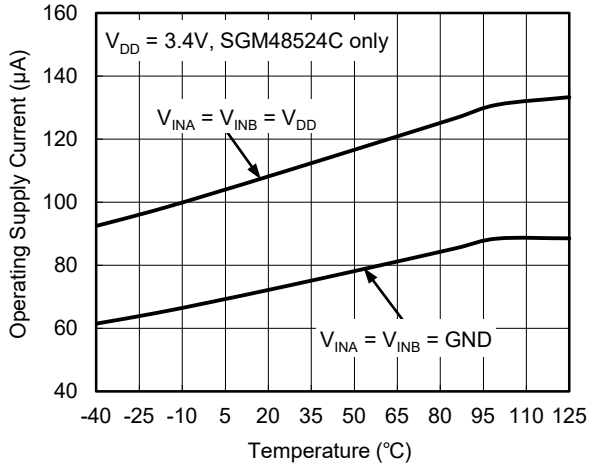
Operating Supply Current vs. Temperature



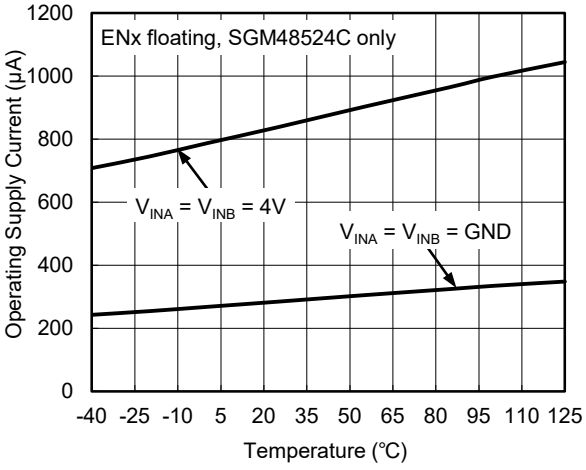

Operating Supply Current vs. Temperature



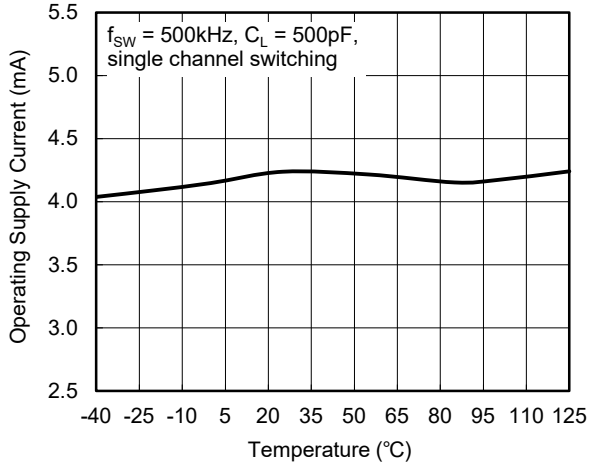

Operating Supply Current vs. Temperature



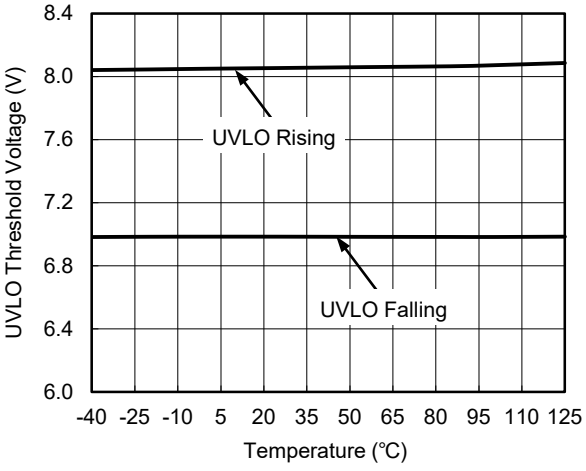

Operating Supply Current vs. Temperature




Operating Supply Current vs. Temperature (Output Switching)



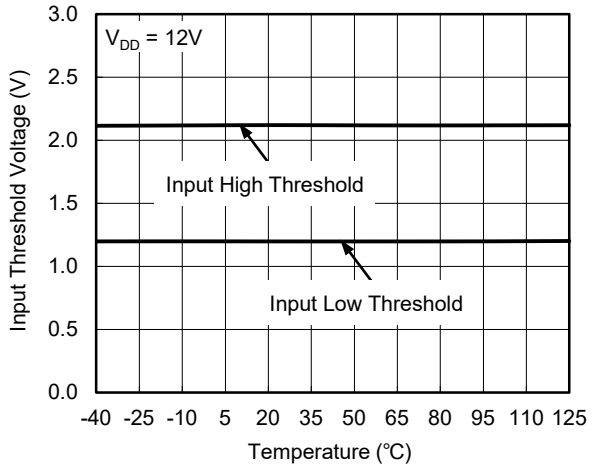

UVLO Threshold Voltage vs. Temperature



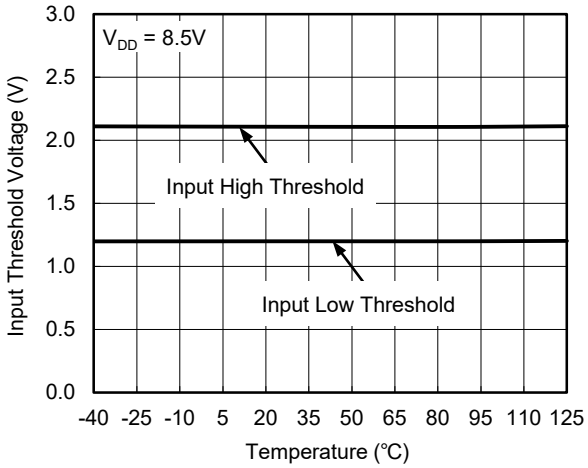
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J$ = +25℃, $V_{DD}$ = 12V, $C_{IN}$ = 4.7μF, unless otherwise noted.

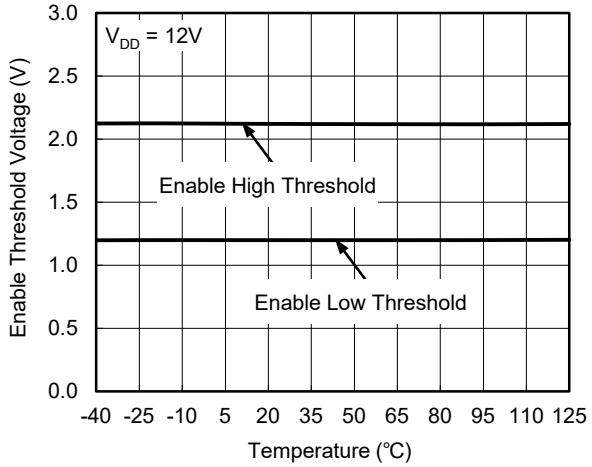
Input Threshold Voltage vs. Temperature



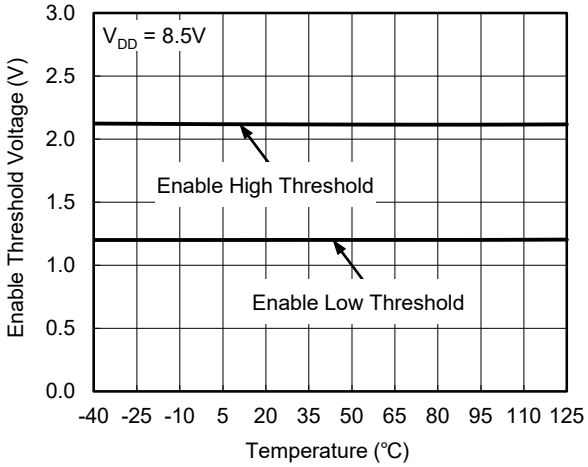

Input Threshold Voltage vs. Temperature



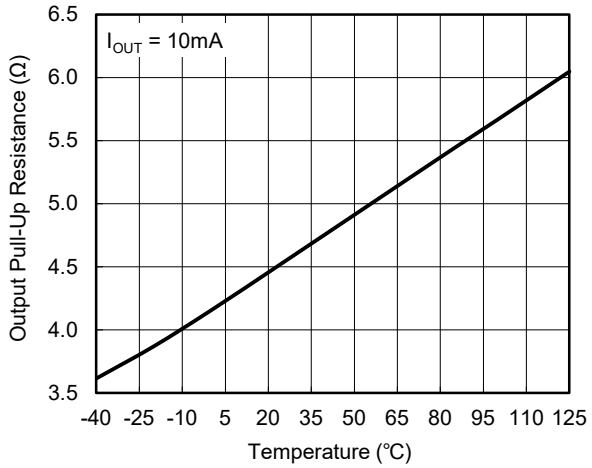

Enable Threshold Voltage vs. Temperature



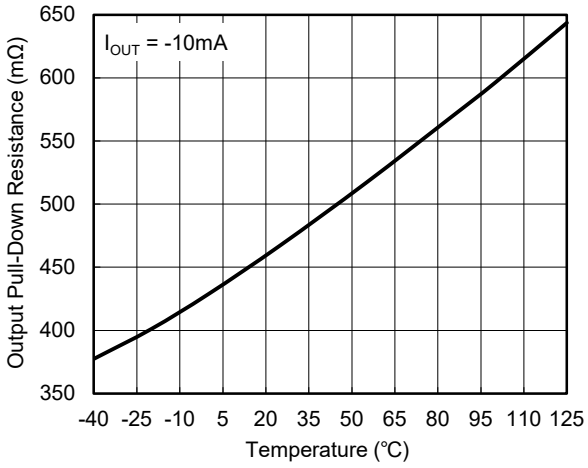

Enable Threshold Voltage vs. Temperature




Output Pull-Up Resistance vs. Temperature



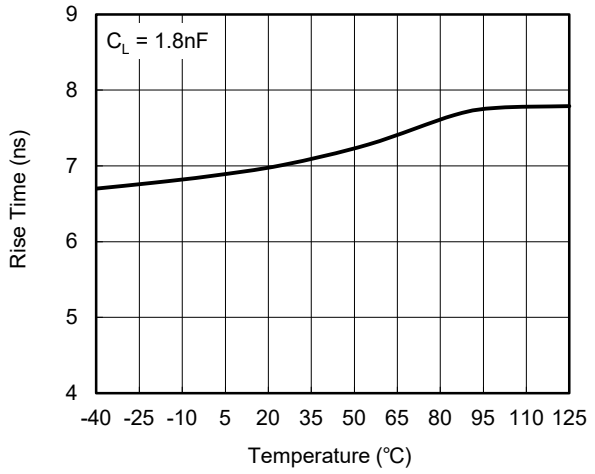

Output Pull-Down Resistance vs. Temperature



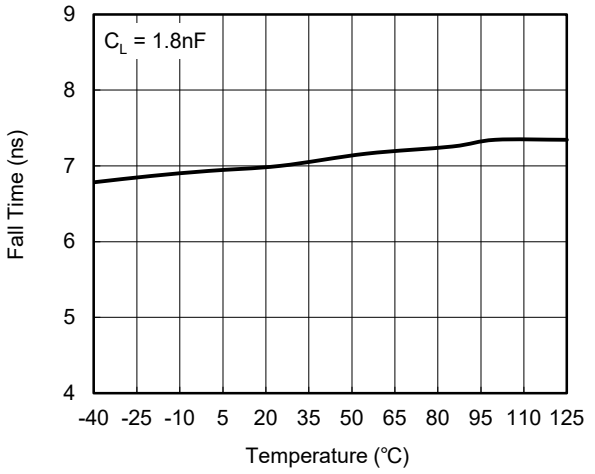
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J$ = +25℃, $V_{DD}$ = 12V, $C_{IN}$ = 4.7μF, unless otherwise noted.

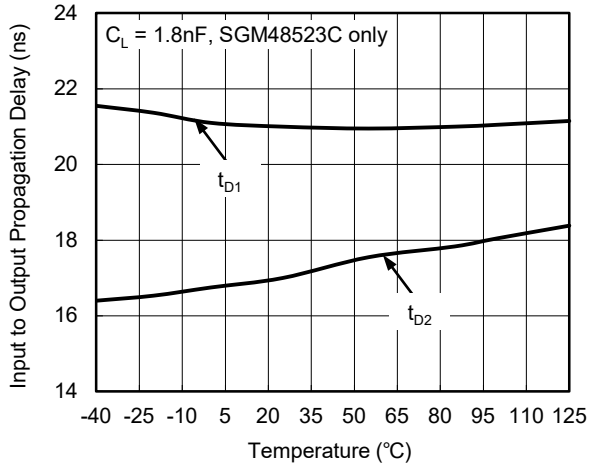
Rise Time vs. Temperature



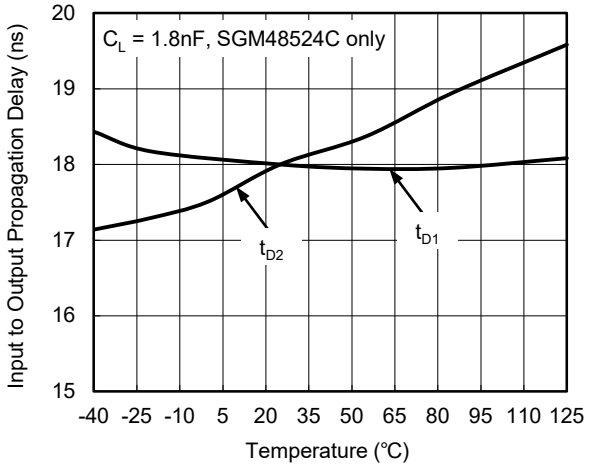

Fall Time vs. Temperature



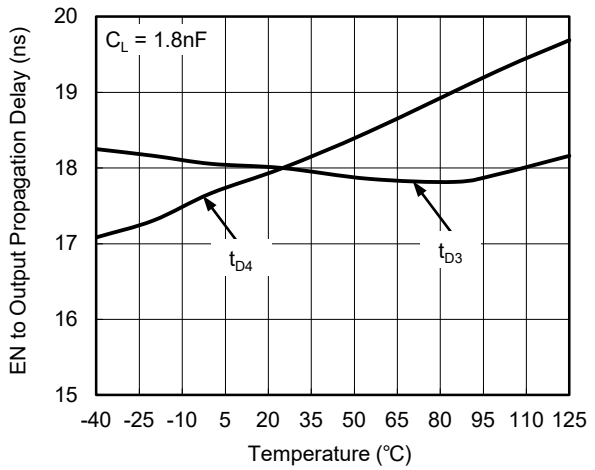

Input to Output Propagation Delay vs. Temperature



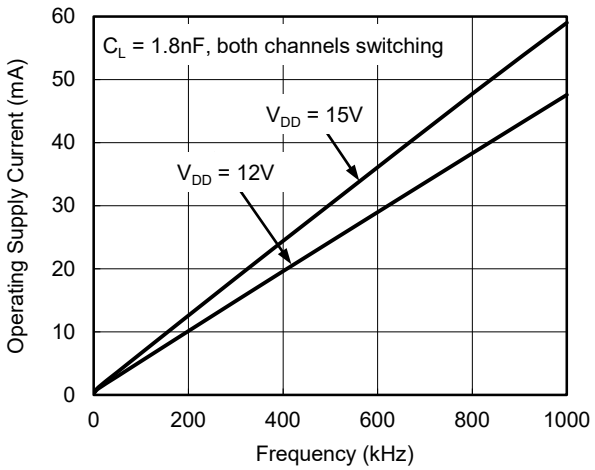

Input to Output Propagation Delay vs. Temperature




EN to Output Propagation Delay vs. Temperature



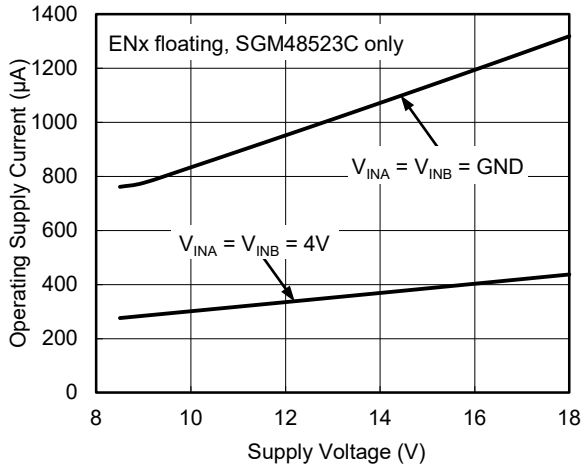

Operating Supply Current vs. Frequency



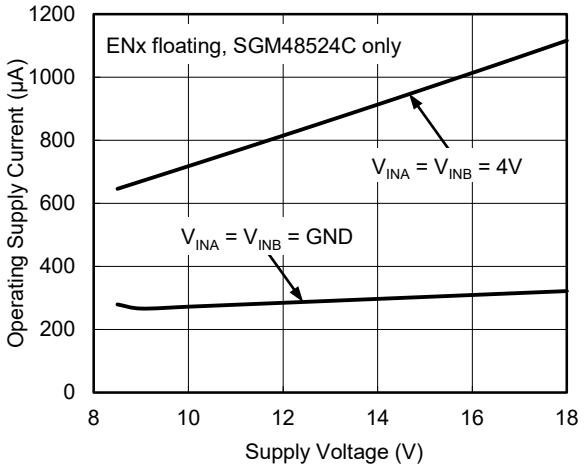
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J$ = +25℃, $V_{DD}$ = 12V, $C_{IN}$ = 4.7μF, unless otherwise noted.

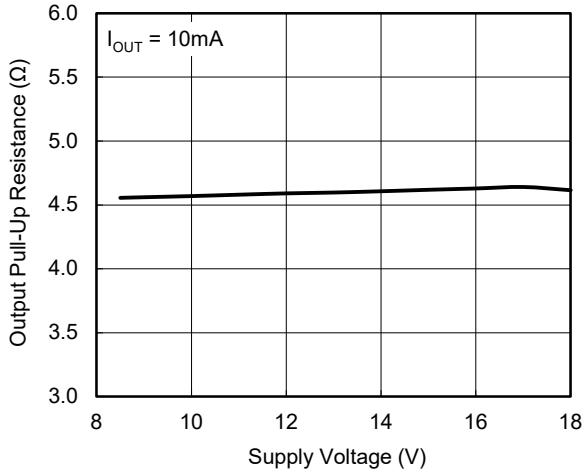
Operating Supply Current vs. Supply Voltage



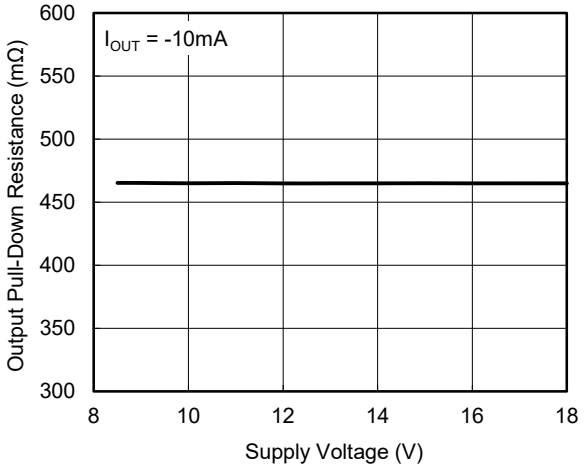

Operating Supply Current vs. Supply Voltage



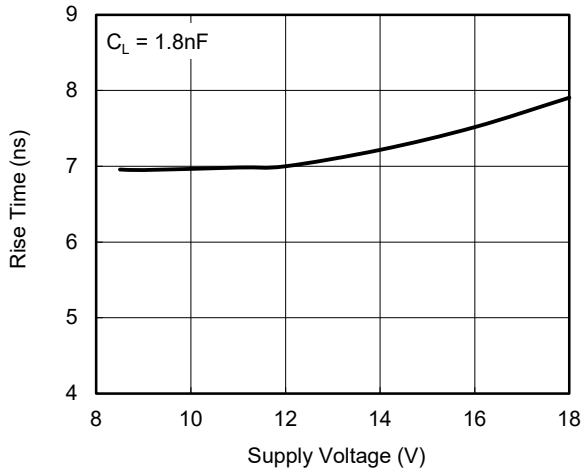

Output Pull-Up Resistance vs. Supply Voltage



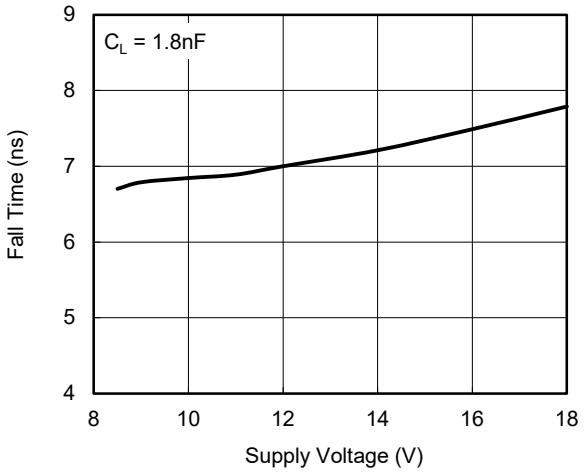

Output Pull-Down Resistance vs. Supply Voltage




Rise Time vs. Supply Voltage



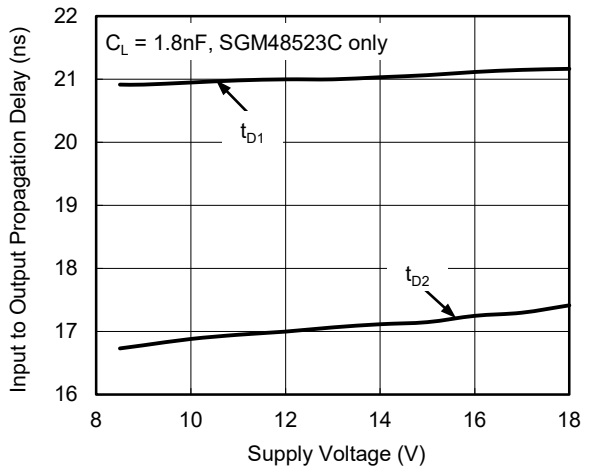

Fall Time vs. Supply Voltage



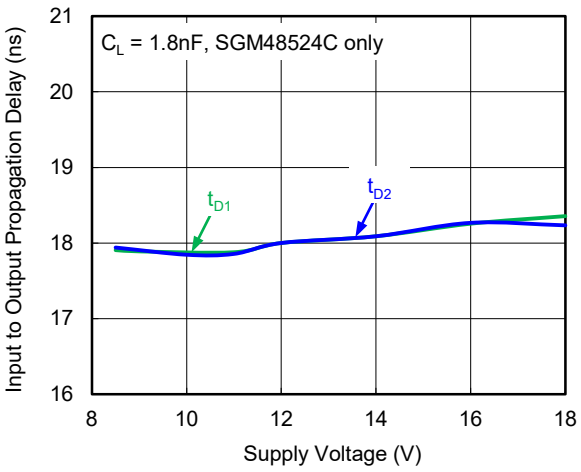
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J$ = +25℃, $V_{DD}$ = 12V, $C_{IN}$ = 4.7μF, unless otherwise noted.

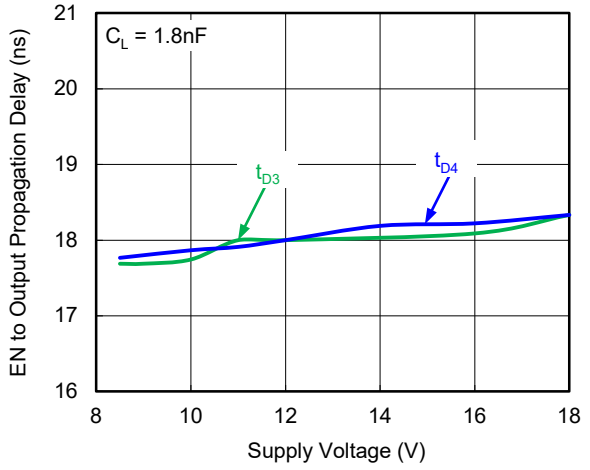
Input to Output Propagation Delay vs. Supply Voltage




Input to Output Propagation Delay vs. Supply Voltage



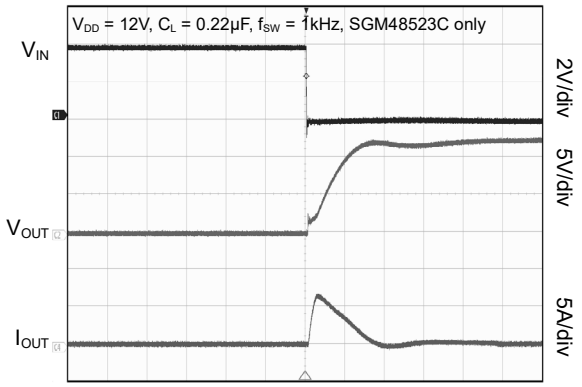

EN to Output Propagation Delay vs. Supply Voltage



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

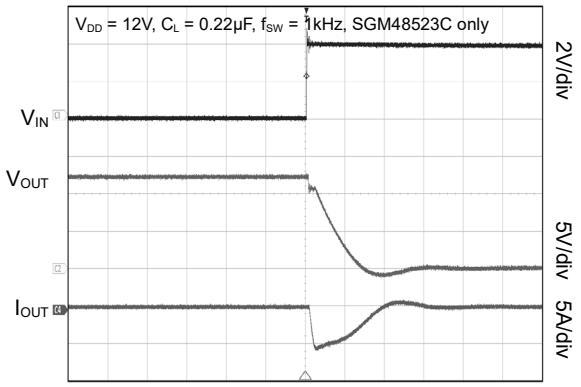
At $T_J$ = +25℃, $V_{DD}$ = 12V, $C_{IN}$ = 4.7μF, unless otherwise noted.

Quasi-Static Source Current



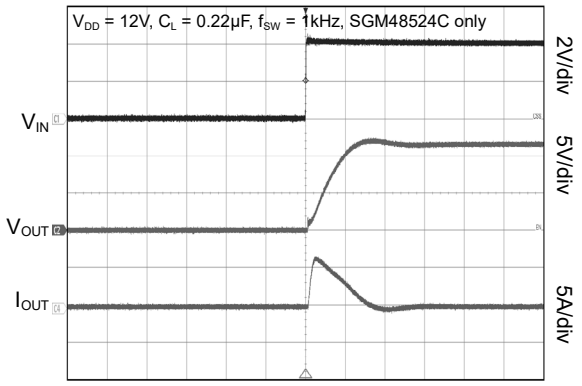

Time (500ns/div)

Quasi-Static Sink Current



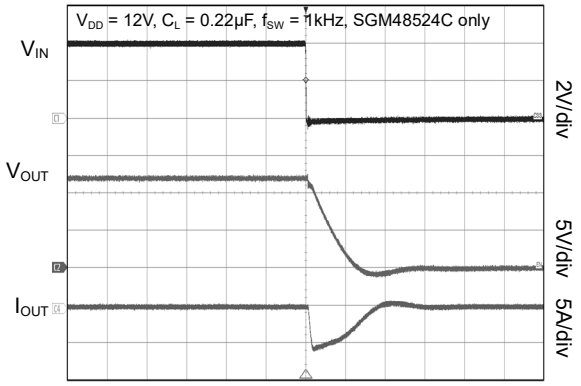

Time (500ns/div)

Quasi-Static Source Current




Time (500ns/div)

Quasi-Static Sink Current




Time (500ns/div)

## TIMING DIAGRAMS

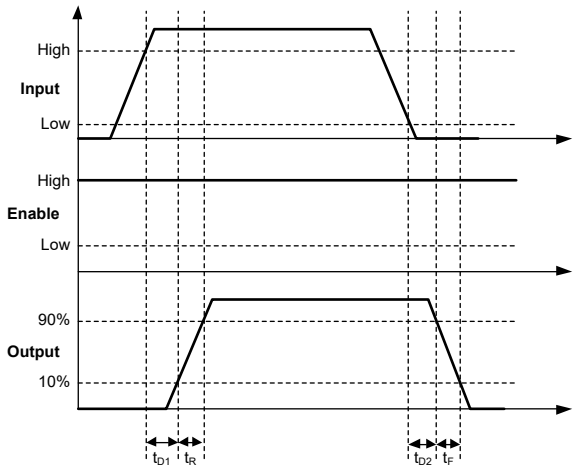



**Figure 2. Non-Inverting Input Driver Operation**

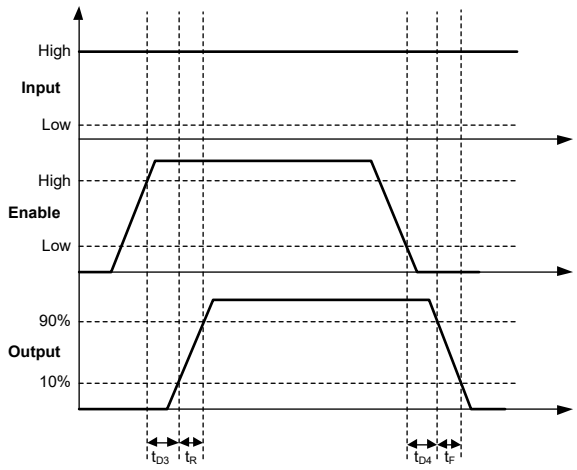



**Figure 3. Enable Function**
**(For Non-Inverting Input Driver Operation)**

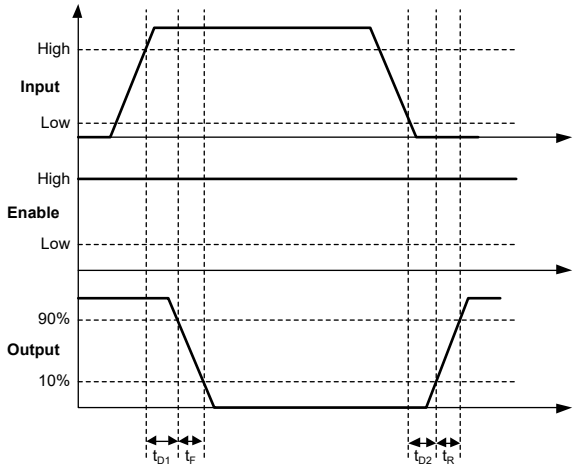



**Figure 4. Inverting Input Driver Operation**

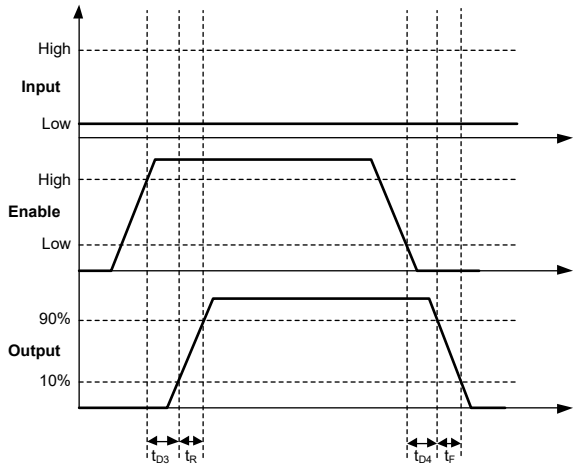



**Figure 5. Enable Function**
**(For Inverting Input Driver Operation)**

## FUNCTIONAL BLOCK DIAGRAM

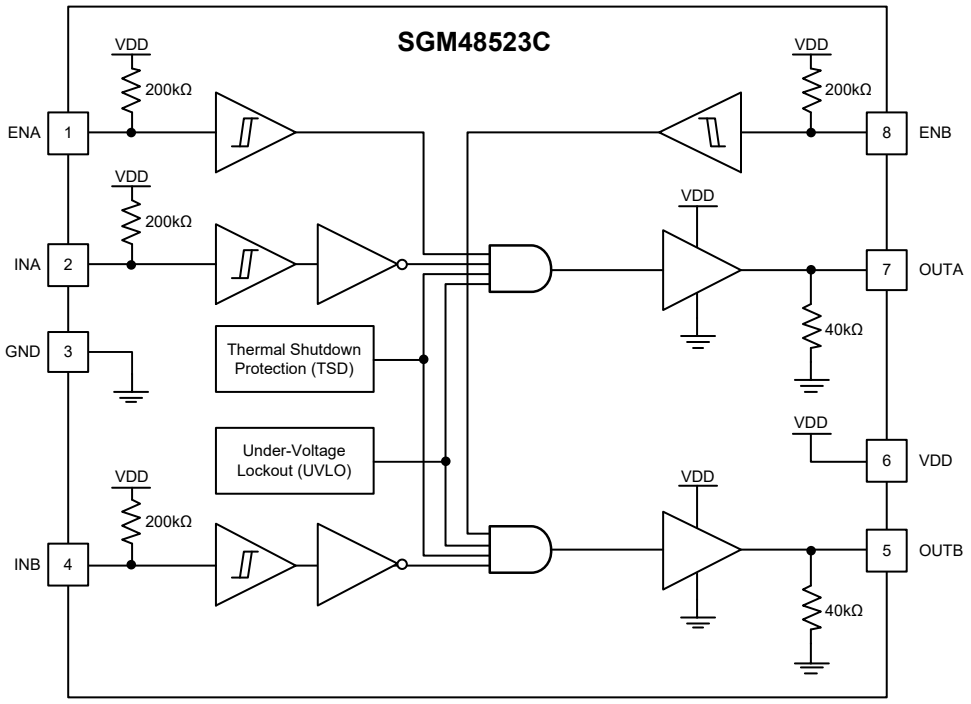



**Figure 6. SGM48523C Block Diagram**

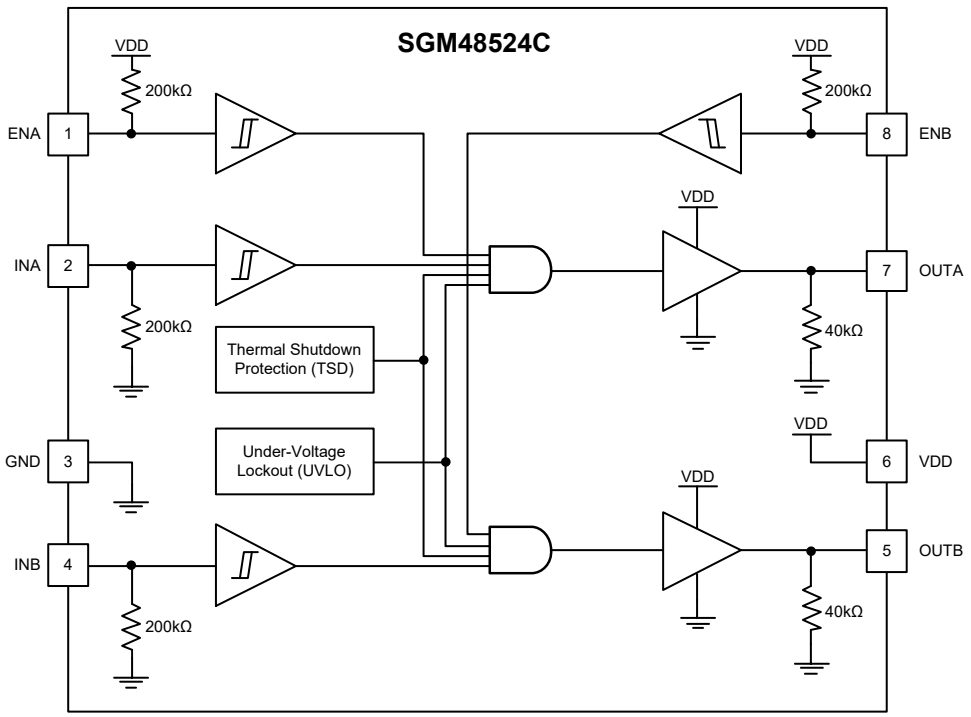



**Figure 7. SGM48524C Block Diagram**

# DETAILED DESCRIPTION

As dual-channel, low-side, high-speed gate drivers, the SGM48523C and SGM48524C are among the top level devices in the market featuring 5A source/sink current capability and industry best-in-class switching characteristics. They have several other prominent features as listed in Table 1 assuring that they are reliable and efficient gate driving solutions for power switches in high frequency applications.

## VDD and Under-Voltage Lockout

The internal under-voltage lockout (UVLO) protection keeps the outputs in low state when the VDD supply voltage is insufficient for proper operation of the chip. If $V_{DD}$ is rising but its level is still below UVLO threshold, the outputs are held low, ignoring the state of the inputs. The UVLO rising threshold level is 8.05V (TYP) and has a 1.05V (TYP) hysteresis band to prevent output from chattering when $V_{DD}$ is low and prone to droops, large superimposed noise or other fluctuations.

Because VDD pin is the supply source for the device internal circuits, it is recommended to use two $V_{DD}$ surface mount bypass capacitors to prevent noise problems due to high speed switching. A small 100nF ceramic capacitor must be soldered between the VDD and GND pins as close as possible. In addition, a larger low ESR capacitor (at least 4.7μF) must be placed in parallel and close to the same pins for delivery of the high peak driving currents with sharp rise time. The low impedance characteristic provided by these capacitors allows high frequency and high current driving of the outputs. Avoid using vias for connecting bypass capacitors to the device pins.

## Protection and Ringing Suppression

The SGM48523C and SGM48524C are reliable and high-speed gate drivers for power switches with a comprehensive set of protection features such as thermal shutdown protection (TSD) and under-voltage lockout (UVLO). Both TSD and UVLO are active. The outputs will be forced low when any threshold of the above two protections is reached and held low during hysteresis range. Only if both TSD and UVLO are released, the outputs follow the inputs again.

The SGM48523C and SGM48524C offer a unique output stage design. It can effectively suppress the output voltage ringing and the overshoot/undershoot on the outputs.

**Table 1. Features and Benefits of the SGM48523C and SGM48524C**

| Features | Benefits |
|---|---|
| Best-in-class propagation delay. | Very low delay and distortion in pulse transmission. |
| Excellent delay matching between channels (1ns, TYP). | Allow paralleling of the channel outputs for double current driving capability. It is especially useful for driving paralleled power switches. |
| Wide supply operating range ($V_{DD}$ from 8.5V to 18V). | Design Flexibility. |
| Wide operating temperature range (-40℃ to +125℃). | Wider system operating temperature range and smaller cooling system. |
| UVLO protection on VDD. | Driver outputs are actively held low in UVLO condition to ensure controlled and glitch-free driving during power-up and power-down. |
| Outputs are actively held low when inputs (INx) are floating. | This safety feature prevents unexpected gate pulses during abnormal situations such as the conditions tested in the safety certification. |
| Outputs are enabled when enable inputs (ENx) are floating. | This feature provides pin-to-pin compatibility with other similar products in those designs where pin 1 and 8 are floating. |
| Wide hysteresis CMOS/TTL compatible input and enable thresholds. | Improved noise immunity while compatible with digital logic. |
| Input/enable pin voltage levels are not restricted by $V_{DD}$. | Simplified system especially in the auxiliary bias supply architecture. |
| Ringing Suppression. | Reduce turn-on/off overshoot/undershoot amplitude and period. |

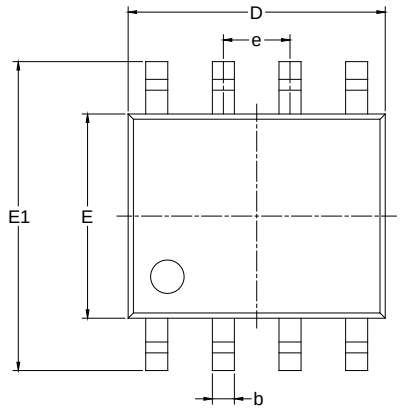
# REVISION HISTORY

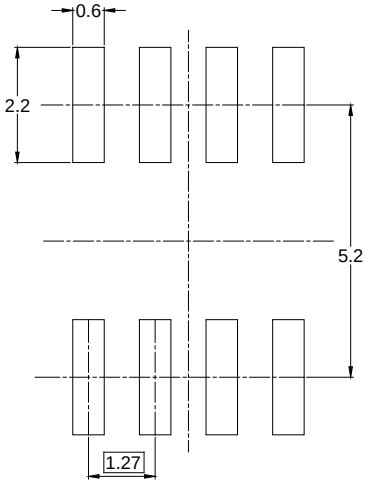
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (OCTOBER 2022) to REV.A | Page |
|---|---|
| Changed from product preview to production data | All |

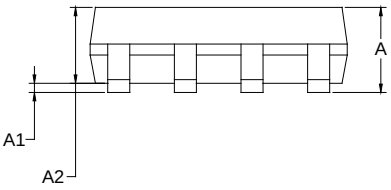
# PACKAGE OUTLINE DIMENSIONS

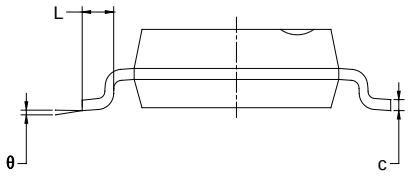
## SOIC-8




**RECOMMENDED LAND PATTERN** (Unit: mm)



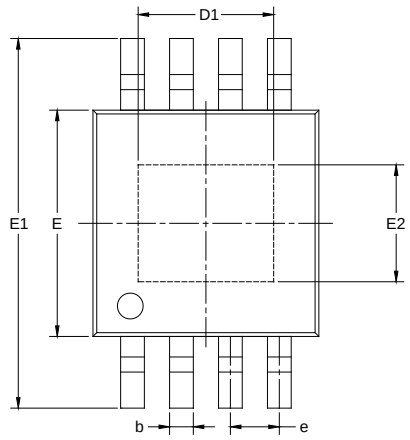



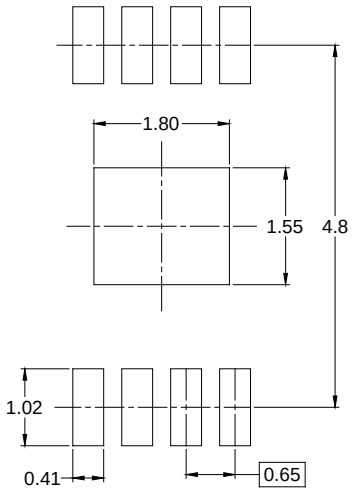

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.27 BSC | | 0.050 BSC | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

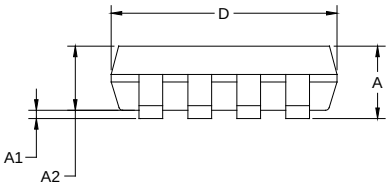
# PACKAGE OUTLINE DIMENSIONS

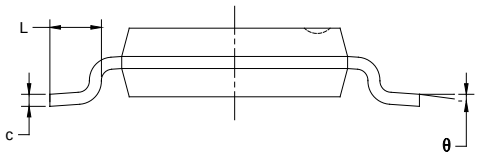
## MSOP-8 (Exposed Pad)




**RECOMMENDED LAND PATTERN** (Unit: mm)



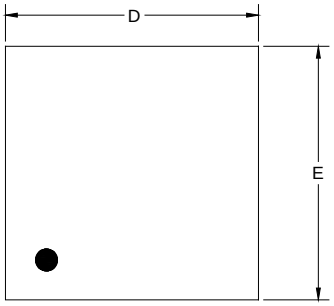




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.820 | 1.100 | 0.032 | 0.043 |
| A1 | 0.020 | 0.150 | 0.001 | 0.006 |
| A2 | 0.750 | 0.950 | 0.030 | 0.037 |
| b | 0.250 | 0.380 | 0.010 | 0.015 |
| c | 0.090 | 0.230 | 0.004 | 0.009 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D1 | 1.700 | 1.900 | 0.067 | 0.075 |
| e | 0.65 BSC | | 0.026 BSC | |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 4.750 | 5.050 | 0.187 | 0.199 |
| E2 | 1.450 | 1.650 | 0.057 | 0.065 |
| L | 0.400 | 0.800 | 0.016 | 0.031 |
| θ | 0° | 6° | 0° | 6° |

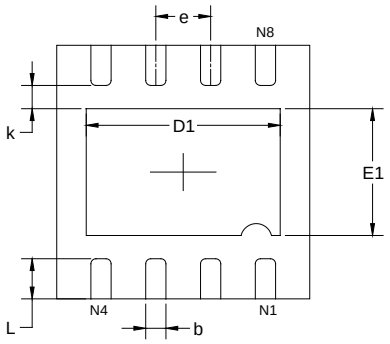
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

# PACKAGE OUTLINE DIMENSIONS

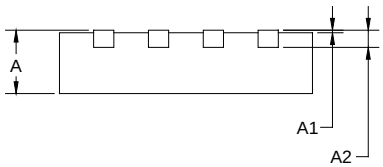
## TDFN-3×3-8L



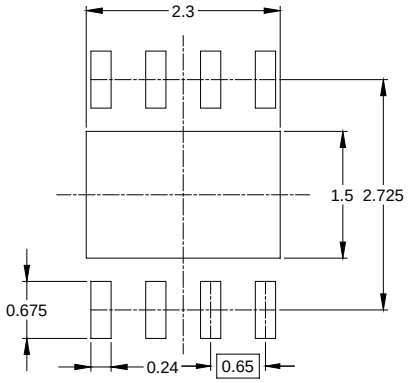

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**



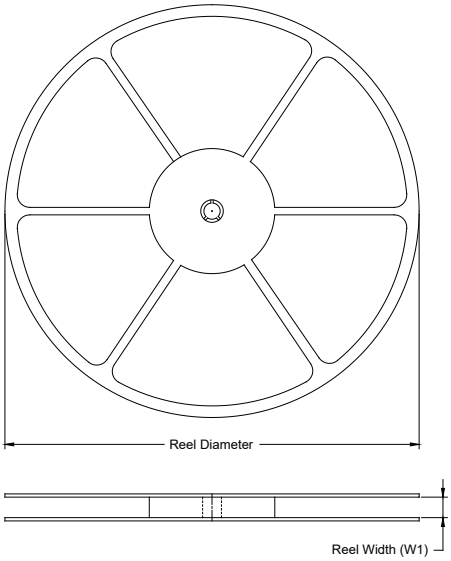

**RECOMMENDED LAND PATTERN** (Unit: mm)

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A2 | 0.203 REF | | 0.008 REF | |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D1 | 2.200 | 2.400 | 0.087 | 0.094 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 1.400 | 1.600 | 0.055 | 0.063 |
| k | 0.200 MIN | | 0.008 MIN | |
| b | 0.180 | 0.300 | 0.007 | 0.012 |
| e | 0.650 TYP | | 0.026 TYP | |
| L | 0.375 | 0.575 | 0.015 | 0.023 |

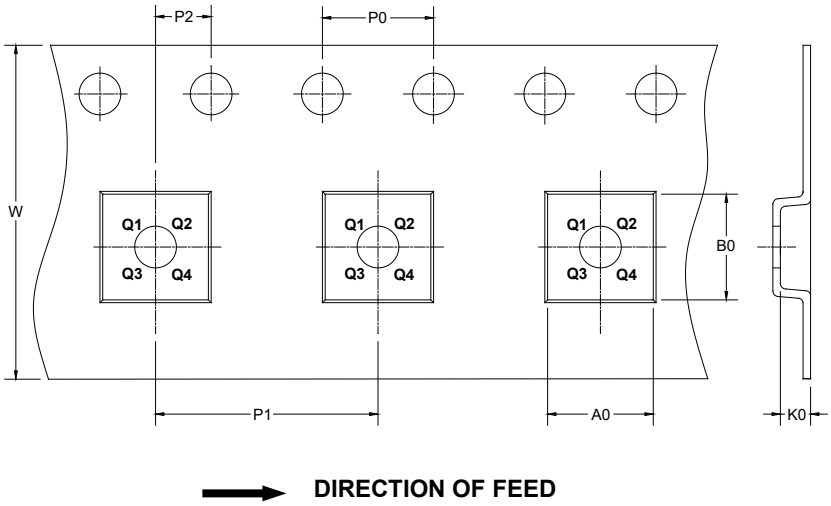
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



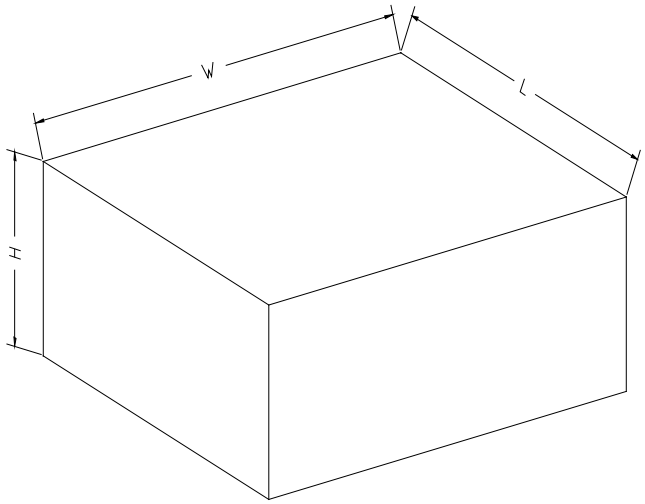

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| SOIC-8 | 13″ | 12.4 | 6.40 | 5.40 | 2.10 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |
| MSOP-8 (Exposed Pad) | 13″ | 12.4 | 5.20 | 3.30 | 1.50 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |
| TDFN-3×3-8L | 13″ | 12.4 | 3.35 | 3.35 | 1.13 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

DD0002