SGM48521
5V, 7A/6A Low-Side GaN and MOSFET Driver with 1ns Pulse Width

GENERAL DESCRIPTION

The high-speed, single-channel low-side driver SGM48521 is designed to drive GaN FETs and logic level MOSFETs. Application areas include LiDAR, time of flight, facial recognition, and power converters using low-side drivers. The SGM48521 provides 7A source and 6A sink output current capability. Split output configuration allows individual turn-on and turn-off time optimization depending on FET. Package and pinout with minimum parasitic inductances reduce the rise and fall time and limit the ringing. Additionally, the 2.2ns propagation delay with minimized tolerances and variations allows efficient operation at high frequencies.

The driver has internal under-voltage lockout and over-temperature protection against overload and fault events.

The SGM48521 is available in Green WLCSP-0.88×1.28-6B and TDFN-2×2-6AL packages.

FEATURES

- **5V Supply Voltage**
- **7A Peak Source and 6A Peak Sink Currents**
- **Ultra-Fast, Low-side Gate Driver for GaN and Si FETs**
- **Minimum Input Pulse Width: 1ns**
- **Up to 60MHz Operation**
- **Propagation Delay: 2.2ns (TYP), 3.6ns (MAX)**
- **Rise Time:**
  - **WLCSP-0.88×1.28-6B: 500ps (TYP)**
  - **TDFN-2×2-6AL: 620ps (TYP)**
- **Fall Time:**
  - **WLCSP-0.88×1.28-6B: 460ps (TYP)**
  - **TDFN-2×2-6AL: 610ps (TYP)**
- **Protection Features:**
  - **Under-Voltage Lockout (UVLO)**
  - **Over-Temperature Protection (OTP)**
- **Available in Green WLCSP-0.88×1.28-6B and TDFN-2×2-6AL Packages**

APPLICATIONS

Laser Distance Measuring System
5G RF Communication System
Wireless Charging System
GaN DC/DC Conversion System

TYPICAL APPLICATION

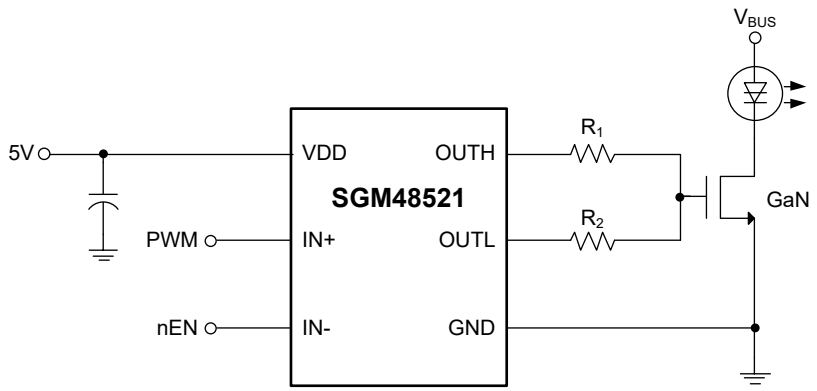


Figure 1. Typical Application Circuit

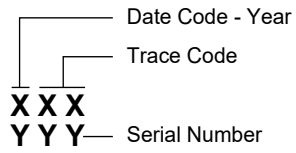
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48521	WLCSP-0.88×1.28-6B	-40℃ to +125℃	SGM48521XG/TR	XXX 063	Tape and Reel, 3000
	TDFN-2×2-6AL	-40℃ to +125℃	SGM48521XTDI6G/TR	062 XXXX	Tape and Reel, 3000

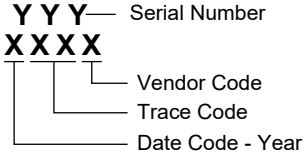
MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code. XXXX = Date Code, Trace Code and Vendor Code.

WLCSP-0.88×1.28-6B



TDFN-2×2-6AL



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} 6V
IN+, IN- Pin Voltage, V_{INx} ..... -0.3V to 6V
OUTH Pin Voltage, V_{OUTH} ..... -0.3V to V_{DD} + 0.3V
OUTL Pin Voltage, V_{OUTL} ..... -0.3V to 6V
Package Thermal Resistance
WLCSP-0.88×1.28-6B, θ_{JA} ..... 133℃/W
TDFN-2×2-6AL, θ_{JA} ..... 63℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1500V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{DD} ..... 4.5V to 5.5V
IN+, IN- Pin Voltage, V_{INx} ..... 0V to 5.5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

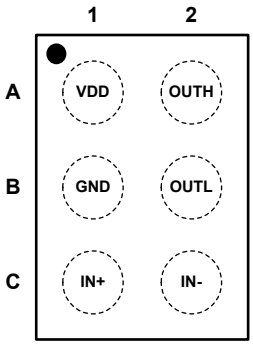
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

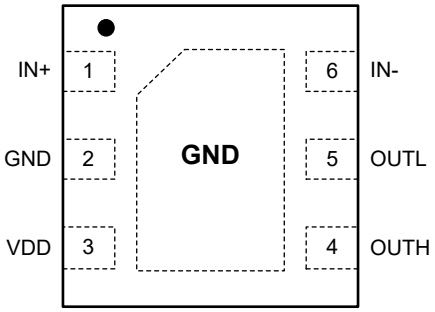
PIN CONFIGURATIONS

(TOP VIEW)



WLCSP-0.88×1.28-6B

(TOP VIEW)



TDFN-2×2-6AL

PIN DESCRIPTION

PIN		NAME	I/O	FUNCTION
WLCSP-0.88×1.28-6B	TDFN-2×2-6AL			
A1	3	VDD	I	Input Voltage Supply. Bypass to GND with a low inductance ceramic capacitor.
A2	4	OUTH	O	Pull-Up Gate Drive Output. Connect it to the gate of the target transistor with an optional resistor.
B1	2	GND	—	Ground.
B2	5	OUTL	O	Pull-Down Gate Drive Output. Connect it to the gate of the target transistor with an optional resistor.
C1	1	IN+	I	Non-Inverting Logic Input.
C2	6	IN-	I	Inverting Logic Input.
—	Exposed Pad	GND	—	Exposed Pad. It is internally connected to GND through substrate. Connect this pad to large copper area, generally a ground plane.

NOTE: I: input, O: output.

FUNCTION TABLE

IN- Pin	IN+ Pin	OUTH Pin	OUTL Pin
L	L	Open	L
L	H	H	Open
H	L	Open	L
H	H	Open	L

ELECTRICAL CHARACTERISTICS

(V_{DD} = 4.5V to 5.5V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics						
VDD Quiescent Current	I_{VDDQ}	V_{IN+} = V_{IN-} = 0V			75	μA
VDD Operating Current	I_{VDD_OP}	f_{SW} = 30MHz, no Load		58		mA
		f_{SW} = 30MHz, 100pF Load		80		
Under-Voltage Lockout Threshold	V_{DD_UVLO}	V_{DD} rising	3.95	4.16	4.35	V
UVLO Hysteresis	ΔV_{DD_UVLO}			75		mV
Over-Temperature Shutdown, Rising Edge Threshold	T_{OTP}			170		℃
Over-Temperature Hysteresis	ΔT_{OTP}			21		℃
Input DC Characteristics						
IN+, IN- High Threshold	V_{IH}		1.7	2.15	2.6	V
IN+, IN- Low Threshold	V_{IL}		1.1	1.4	1.8	V
IN+, IN- Hysteresis	V_{HYS}		0.45		1.1	V
Positive Input Pull-Down Resistance	R_{IN+}	To GND	100	200	280	kΩ
Negative Input Pull-Up Resistance	R_{IN-}	To VDD	100	200	280	kΩ
Input Pin Capacitance	C_{IN}	To GND		2.3		pF
Output DC Characteristics						
OUTL Voltage	V_{OL}	I_{OUTL} = 100mA, V_{IN+} = V_{IN-} = 0V			35	mV
OUTH Voltage	V_{DD} - V_{OH}	I_{OUTH} = 100mA, V_{IN+} = 3V, V_{IN-} = 0V			24	mV
Peak Source Current	I_{OH}	V_{OUTH} = 0V, V_{IN+} = 3V, V_{IN-} = 0V		7		A
Peak Sink Current	I_{OL}	V_{OUTL} = 5V, V_{IN+} = V_{IN-} = 0V		6		A

SWITCHING CHARACTERISTICS

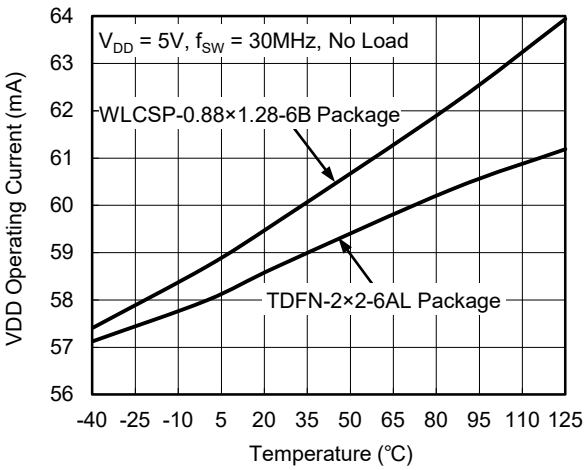
(V_{DD} = 4.5V to 5.5V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Startup Time, V_{DD} Rising above UVLO	t_{START}	IN- = GND, IN+ = VDD, V_{DD} rising to 4.4V to OUTH rising			55	78	μs
ULVO Falling	$t_{SHUTOFF}$	IN- = GND, IN+ = VDD , V_{DD} falling below 3.9V to OUTH falling		2	2.8	3.5	μs
Turn-On Propagation Delay	t_{PDR}	V_{IN-} = 0V, IN+ to OUTH, 100pF load, T_J = +25℃	TDFN-2×2-6AL	1.1	2.2	3.6	ns
			WLCSP-0.88×1.28-6B	1.1	1.9	3.6	
Turn-Off Propagation Delay	t_{PDF}	V_{IN-} = 0V, IN+ to OUTL, 100pF load, T_J = +25℃		1	1.7	3.5	ns
Pulse Positive Distrortion (t_{PDR} - t_{PDF})	Δt_{PD}	TDFN-2×2-6AL			500		ps
		WLCSP-0.88×1.28-6B			200		
Output Rise Time	t_{RISE}	0Ω series 100pF load (1)	TDFN-2×2-6AL		620		ps
			WLCSP-0.88×1.28-6B		500		
Output Fall Time	t_{FALL}	0Ω series 100pF load (1)	TDFN-2×2-6AL		610		ps
			WLCSP-0.88×1.28-6B		460		
Minimum Input Pulse Width	t_{MIN}	0Ω series 100pF load (1)			1		ns

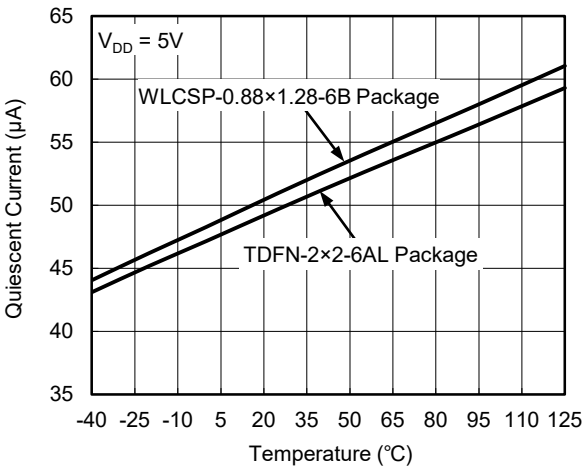
NOTE: 1. Rise and fall are calculated as a 20% to 80%.

TYPICAL PERFORMANCE CHARACTERISTICS

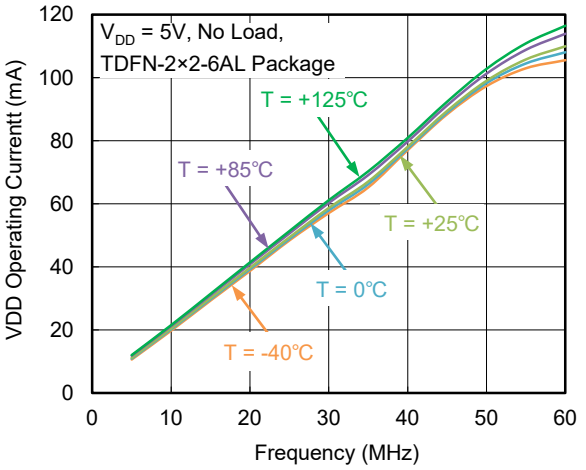
VDD Operating Current vs. Temperature



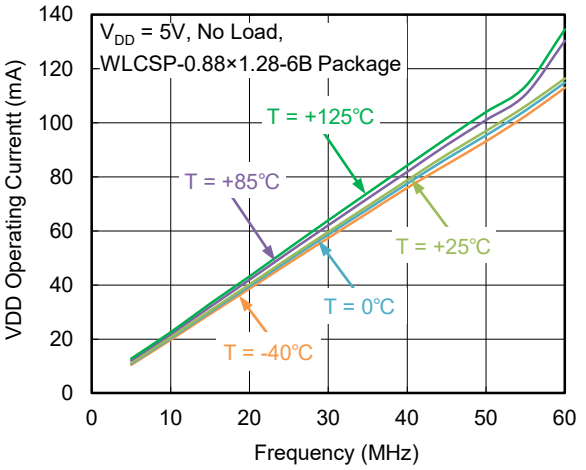
Quiescent Current vs. Temperature



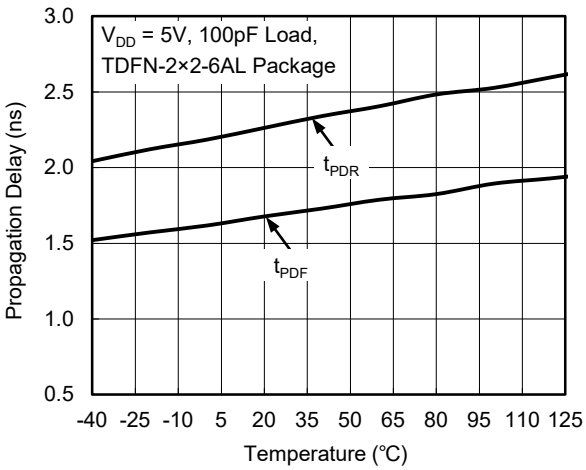
VDD Operating Current vs. Frequency



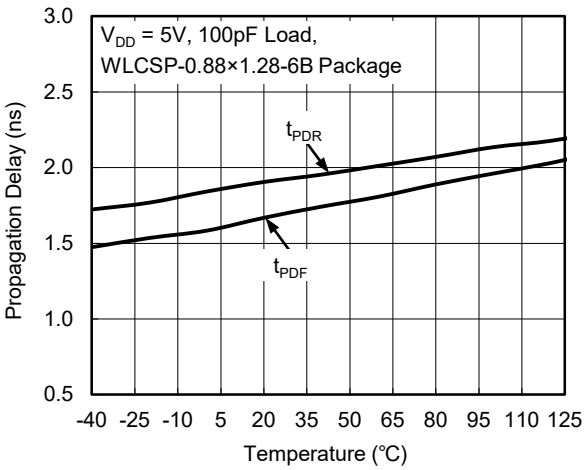
VDD Operating Current vs. Frequency



Propagation Delay vs. Temperature

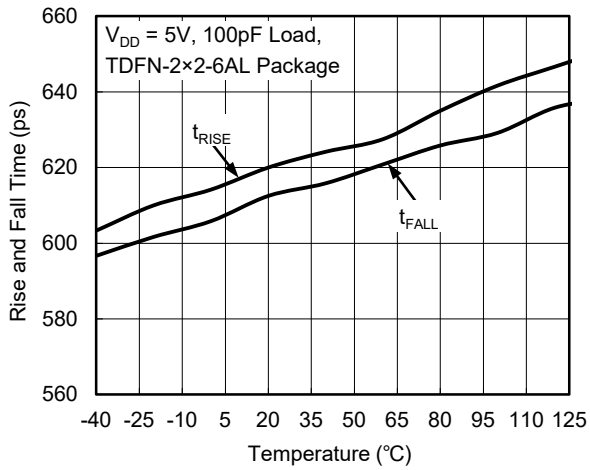


Propagation Delay vs. Temperature

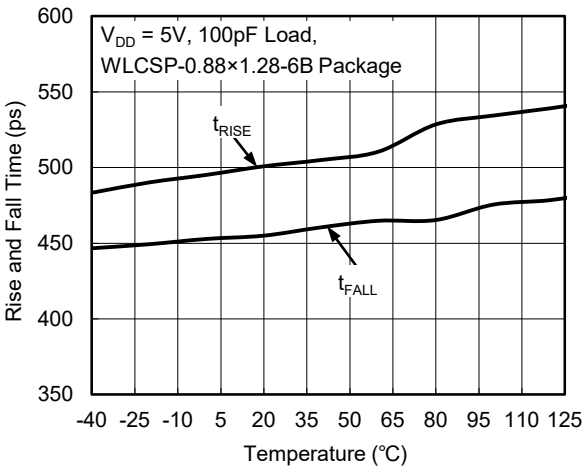


TYPICAL PERFORMANCE CHARACTERISTICS

Rise and Fall Time vs. Temperature



Rise and Fall Time vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

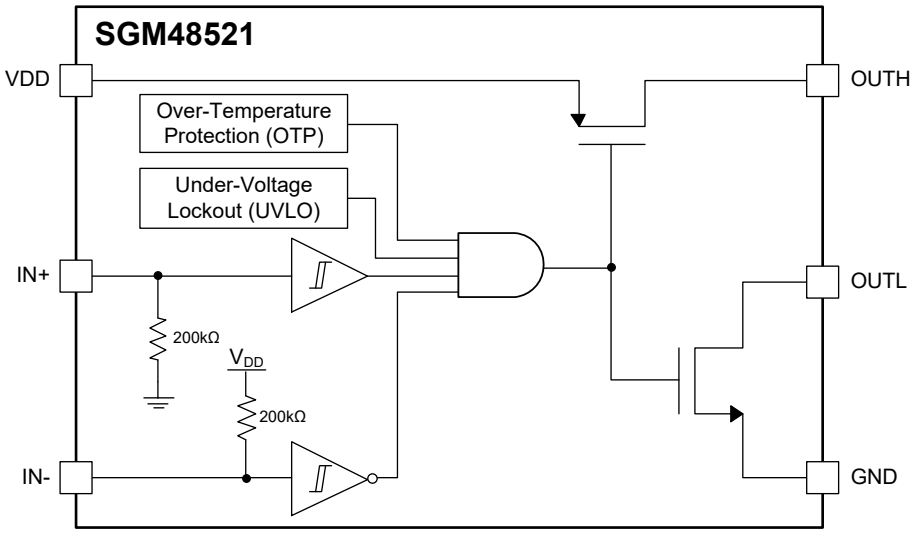


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

The high-speed, single-channel low-side driver SGM48521 is designed to drive GaN FETs and logic level MOSFETs. Application areas include LiDAR, time of flight, facial recognition, and power converters using low-side drivers.

The SGM48521 provides 2.2ns propagation delay from the driver to the power transistor.

Input Stage

There are two Schmitt triggers at the input pins IN+ and IN- to improve noise immunity. In order to prevent the output from accidentally turning on when the input is in the floating state, IN+ is internally connected to a pull-down resistor, and IN- is internally connected to a pull-up resistor. The output signal depends on the logic voltage levels on the IN+ and IN- pins (which are not a differential input pair).

Output Stage

The SGM48521 provides 7A peak source and 6A sink currents, and the outputs are separated to allow custom pull-up and pull-down drive strength to suit the application. Each of OUTH and OUTL pins can be connected to transistor gates with separate drive resistors, adjusting the driving speed of turning on and off to control the slew rate and EMI of the driving signal and the ringing on the gate signal. Controlling ringing as much as possible reduces the stress on the driver and switch device, which is very important for high-performance applications and reliability of GaN FETs. In order to prevent the device C_{ISS} from turning the FET on by mistake, the OUTL pin will be pulled low in under-voltage conditions.

VDD and Under-Voltage Lockout

The rated working voltage of SGM48521 is 5V ± 0.5V. In the application, the error of the power supply of the driver chip needs to be ensured within 10% (0.5V), and the transient overshoot voltage of the power supply cannot exceed the absolute maximum voltage of the part. In the VDD Overshoot Solution section, there are more specific design details.

The SGM48521 provides under-voltage lockout (UVLO) function to protect the circuit in the event of a fault condition. The UVLO rising trigger point is typically set at 4.16V, and the hysteresis voltage is 75mV. This UVLO level ensures that the GaN FET operates in the low R_{DSON} region. When UVLO is triggered, the output is low.

Over-Temperature Protection (OTP)

The SGM48521 provides an over-temperature protection (OTP) function with a trigger point of +170℃. The hysteresis temperature is 21℃. If the OTP is triggered, switching action is stopped with OUTL held low. Then when the junction temperature of the device falls below +149℃, normal operation resumes.

APPLICATION INFORMATION

Since the output of the PWM controller cannot often provide the voltage required by the gate of the power device, a high-performance gate driver is usually required between the PWM output of the controller and the gate of the GaN transistor, so that the GaN transistor can operate at correct gate voltages. In addition, the gate driver can reduce switching losses and maximize the performance of GaN transistors in high-frequency applications. Especially in the field of digital power control, it is common for the PWM signal of the digital controller to be a 3.3V logic signal, and GaN transistors cannot work optimally with this gate voltage. The gate driver boosts the 3.3V signal to the preferred gate drive voltage of 5V, which fully turns on the power device and minimizes conduction losses.

The good noise immunity of the SGM48521 gate driver also minimizes the effects of high frequency switching noise when the driver is placed near the power switch. Adding a gate driver also transfers the gate charge power loss from the controller to the driver, which effectively reduces the power consumption and thermal stress in the controller.

The SGM48521 is a low-side high-speed gate driver with a maximum operating frequency of 60MHz and an operating voltage of 5V. It is optimized to drive GaN FETs. The output has an independent configuration architecture, which can flexibly adjust the turn-on and turn-off speed, while providing a strong current sinking and sourcing capabilities.

The SGM48521 is primarily used to drive GaN transistors, which are used in various power converters, LiDAR, wireless chargers, and synchronous rectifiers. The SGM48521 can be used as a driver for high-speed pulsed laser diodes.

Typical Application

A typical application circuit for the SGM48521 is shown in Figure 1, with a single-channel, 5V drive voltage, specifically designed to drive GaN transistors or logic-level Si FETs. The output has a separated structure, so that the turn-on and turn-off speeds can be controlled separately by driving resistors. If it is not necessary to adjust the turn-on and turn-off speeds separately, OUTH and OUTL may be connected directly together (with a single gate drive resistor added if necessary).

In order to avoid voltage overstress caused by the parasitic inductance of the drive circuit, SGMICRO recommends using at least 2Ω resistors at OUTH and OUTL.

For applications requiring a smaller resistance value, please contact SGMICRO E2E for guidance.

Design Requirements

There are some key factors to consider when designing with the SGM48521 gate driver and GaN power FETs, especially for high MHz frequency (or nanosecond pulse) applications. These factors include circuit layout, PCB trace design, passive component selection, and maximum operating frequency.

Detailed Design Procedure

Handling Ground Bounce

Place the ground pin of the SGM48521 as close as possible to the source of the low-side FET to get the smallest gate current loop, the smallest parasitic inductance, and maximize the switching performance. However, this can cause ground bounce on the SGM48521, resulting in incorrect switching logic at the input and wrong level at the output.

In order to eliminate this effect, SGM48521 has built-in Schmitt triggers on the input terminals to increase the input hysteresis. Equation 1 shows the relationship between the input hysteresis and the maximum allowable di/dt:

$$\frac{di}{dt} = \frac{V_{HYS}}{L_P} \quad (1)$$

where

L_P: Parasitic inductance between source and Ground.

V_{HYS}: Hysteresis voltage of the input port.

di/dt: Current slew rate.

APPLICATION INFORMATION (continued)

Assuming that the parasitic inductance is 0.5nH and the hysteresis voltage is 0.5V, the maximum allowable current slew rate is 1A/ns by calculation. If the current slew rate generated in the application is higher than 1A/ns, this exceeds the hysteresis voltage range and causes the output signal to be unstable. Using the inverting input to accept the PWM signal and connecting the non-inverting input to VDD can reduce the possibility of false pulses or oscillations and improve stability. High di/dt produces high transient voltage spikes that affect the input of the SGM48521. In order to protect the device from a large current spike at IN-, a 100Ω current limiting resistor can be placed before the IN- input.

If the current slew rate is not too high, and the pulse width is not very short (for example, 1ns range), the extra delay can be accepted. The parasitic capacitance of the SGM48521 input can be used to create an RC filter to reduce high-frequency noise by adding a resistor in series with the input pin. The SGM48521 has stable input capacitance of about 2.3pF at the input pins, which is convenient for this purpose.

If the environment is more severe, using a common mode choke coil can increase the stability of the system.

In applications that use current sensing resistors, the ground bounce phenomenon is particularly serious. In the application circuit with current sense resistor shown in Figure 3, the ground of the SGM48521 is connected to the source of the GaN FET, and one side of the current sense resistor is connected to the controller ground. In the case of high-speed switching and large current, the potential rebound due to the parasitic inductance of the current detection resistor will cause the circuit to turn on/off by mistake, and in severe cases it may cause damage to the device. Figure 5 shows the solution for this situation: Use a common mode choke between the controller output and the SGM48521 input. When the pulse width is not extremely narrow, a resistor can also be added to the signal output line before SGM48521 to form an RC filter as a supplement. Although the circuit of Figure 4 improves the ground bounce problem by connecting the GND of the driver to the signal ground after the current sense resistor, this circuit is not recommended. The drawback of this circuit is that the voltage drop across the current sense resistor and its parasitic inductance reduce the transient and DC gate drive voltage to the FET, thus reducing efficiency. In severe cases, the voltage ringing caused by the inductance of the sense resistor path can even cause the FET to spuriously turn on and off. For these reasons, the circuit of Figure 5 is the preferred solution to ground bounce problems.

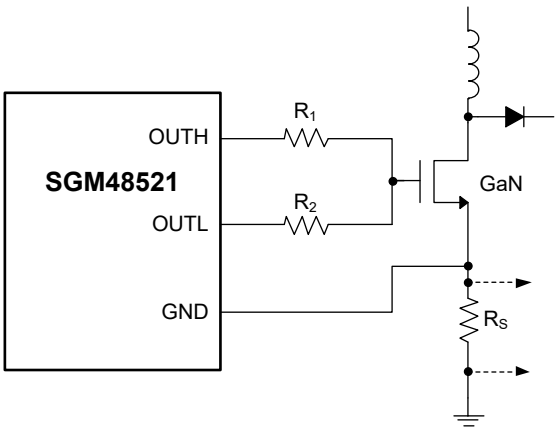


Figure 3. R_S Current Sense A Configuration

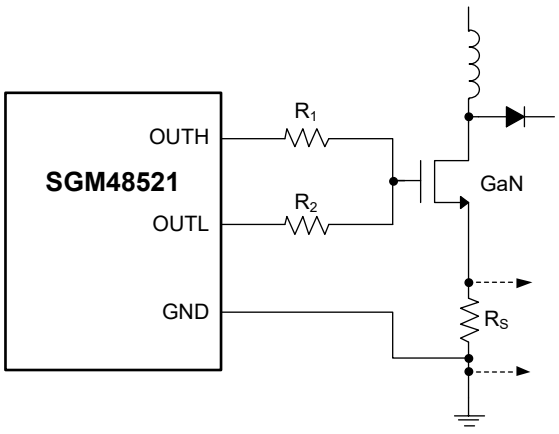


Figure 4. R_S Current Sense B Configuration

APPLICATION INFORMATION (continued)

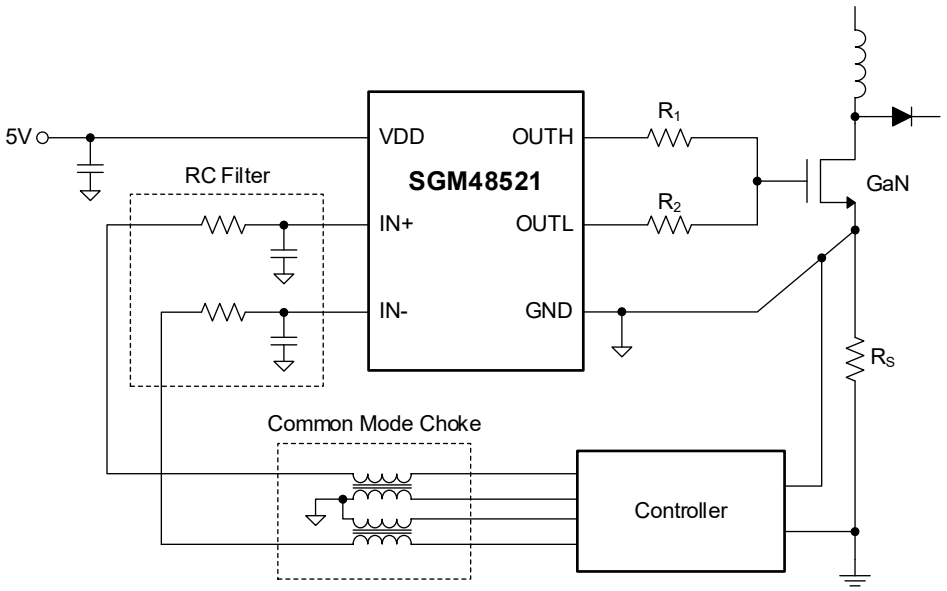


Figure 5. Filtering for Ground Bounce Noise Handling with SGM48521

Creating Nanosecond Pulse with SGM48521

SGM48521 can provide a minimum 1ns pulse width output to capacitive load. However, outputting such a small equivalent pulse width requires a very powerful digital driver and also needs to consider the influence of parasitic parameters from the digital output to the SGM48521 input. Using the two inputs of SGM48521 and the AND gate can get a method of generating short pulses at the output. As shown in Figure 6, connect one digital signal to IN+, and the other delayed digital signal to IN-, so that a narrow pulse will appear at the output, the width of which is equal to the delay time of the two digital signals. The digital controller only needs to control the delay time in the range of nanoseconds, which reduces the requirement for the SGM48521 input signal. If the digital signal has only one output, an RC low-pass filter can be used to generate a signal with an adjustable delay time, which is related to the RC time constant.

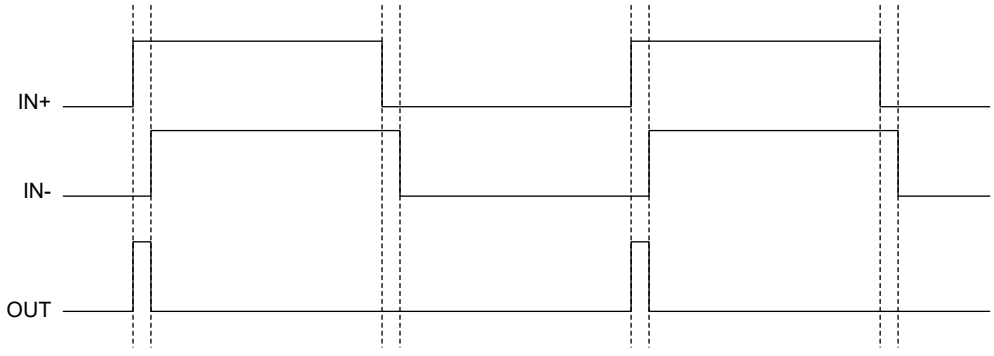


Figure 6. Timing Diagram of Creating Short Pulses

APPLICATION INFORMATION (continued)

VDD Overshoot Solution

Due to the existence of PCB parasitic inductance, inductance ringing and transient overshoot voltage are prone to occur under high current switching conditions. In the PCB design process, it is necessary to evaluate and control the overshoot caused by the ringing, so as not to exceed the stress of the device. The strength of the overshoot voltage and the percentage of the overshoot duration to the switching time are parameters that affect the stress. Keeping the overshoot below maximum allowable pin voltage is the best solution. The parasitic inductance can be decreased by optimizing PCB layout. To limit the voltage overshoot, low ESL components and series resistance can be helpful as well. If the overshoot is too large, the accuracy of the power supply needs to be considered. For example, if the overshoot voltage is 0.5V, the maximum error voltage of the power supply cannot exceed 5.5V (10% accuracy). Therefore, if the overshoot voltage is large, a power supply with higher accuracy is necessary.

Applications at High Frequencies

SGM48521 has fast rise/fall time, and provides a minimum output capability of 1ns pulse width and a maximum operating frequency of 60MHz. According to the capacitive load, different output modes and frequencies can be selected. Under the working condition of high-frequency pulse, in order to prevent the device from overheating, a high-frequency pulse train with a certain interval time can be used. This can increase the transient frequency and keep the effective value of the output current unchanged. At this time, a larger decoupling capacitor is needed to charge the capacitive load at a high frequency.

Power Supply Recommendations

In order to provide high peak current when the FET is turned on and improve the stability of the VDD pin supply voltage, a low ESR/ESL ceramic capacitor needs to be used as a bypass capacitor placed as close as possible to the IC's VDD and GND pins. To avoid ringing at the IC pins as much as possible, the decoupling capacitors need to be placed on the same side as the IC, and vias cannot be used.

In order to achieve the best transient performance, SGMICRO recommends choosing a three-terminal capacitor and a capacitor with a larger capacitance in parallel. The three-terminal capacitor needs to be placed close to the VDD and GND pins of the IC, and the other capacitor is placed close to the three-terminal capacitor. The three-terminal capacitor has the lowest ESL, and the larger capacitor provides enough drive peak current. Under normal circumstances, it is recommended to use 0.1μF 0402 or through-core capacitors in parallel with 1μF 0603 capacitors.

Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. SGM48521 provides WLCSP ball grid array package, which can reduce the parasitic inductance in the connection line with BGA type GaN FET.

In order to achieve the best performance, a PCB with at least four routing layers is recommended to minimize the parasitic inductance. Using resistors and capacitors in a smaller package (0201) can also minimize inductance and PCB space. It is necessary to calculate the resistor power of a small package to meet the requirements of gate drive power loss.

Drive Loop Inductance and Grounding

SGM48521 should be placed as close to the GaN FET as possible, and the trace of the gate drive circuit should be as wide as possible to reduce parasitic inductance.

To achieve minimum drive loop inductance, it is recommended to use the second layer of the PCB as the source loop of the GaN FET, near the bottom of the device (top layer). Both the vias connected to the GND pin and the source of the FET are connected to this layer with minimal impedance. Please note that the coupling of the ground plane will be decreased only when the GND plane is connected to the source power plane at the FET.

APPLICATION INFORMATION (continued)

Bypass Capacitor

The VDD pin requires a bypass capacitor connected to GND, as close to the pins of the SGM48521 as possible. The capacitor should be connected to VDD and GND power planes, which should be large and as close to the top layer of the PCB as possible. Due to the high operating frequency of the IC, the inductance of the bypass capacitor is critical, so the value of the bypass capacitor should be between 0.1μF and 1μF, and the material should be X7R or better. The best capacitors for the application are low inductance chip capacitors (LICC), interdigital capacitors (IDC), feedthrough and LGA capacitors. Finally, in order to meet the demand of driving peak current, an extra 1μF capacitor between VDD and GND should be added in parallel close to the IC.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

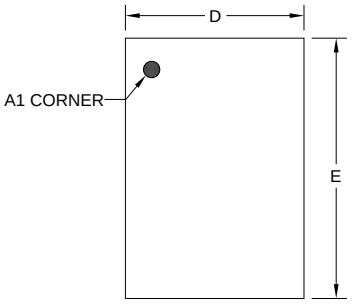
JANUARY 2024 – REV.A.1 to REV.A.2	Page
Changed Features section	1
Changed Switching Characteristics section	4
Changed Typical Performance Characteristics section	6

JULY 2023 – REV.A to REV.A.1	Page
Added WLCSP-0.88×1.28-6B package	All
Added Electrical Characteristics and Switching Characteristics sections	4
Added Typical Performance Characteristics section	5, 6

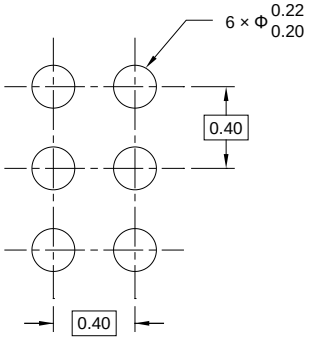
Changes from Original (MAY 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

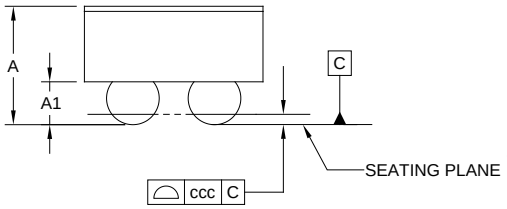
WLCSP-0.88×1.28-6B



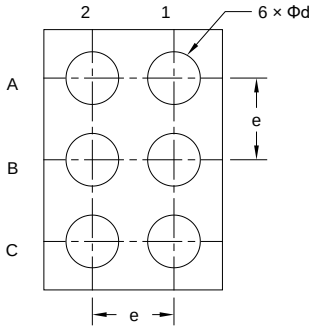
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



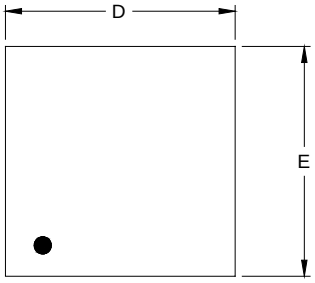
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.535	0.580	0.625
A1	0.190	0.210	0.230
D	0.845	0.875	0.905
E	1.245	1.275	1.305
d	0.238	0.258	0.278
e	0.400 BSC		
ccc	0.050		

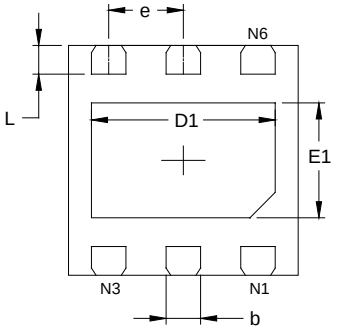
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

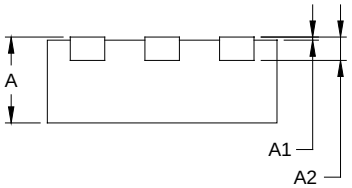
TDFN-2×2-6AL



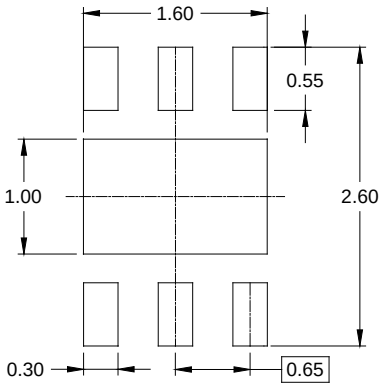
TOP VIEW



BOTTOM VIEW



SIDE VIEW



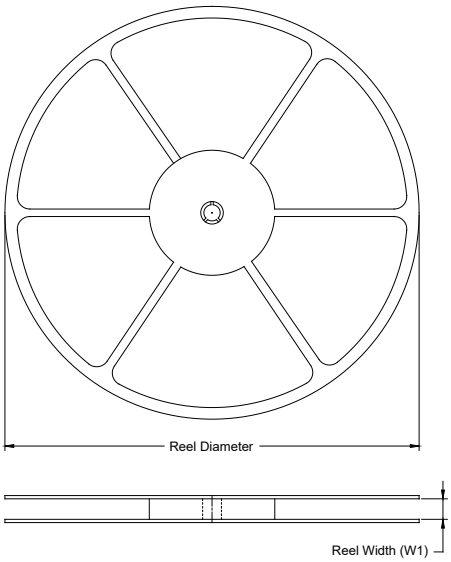
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.500	1.700	0.059	0.067
E	1.900	2.100	0.075	0.083
E1	0.900	1.100	0.035	0.043
b	0.250	0.350	0.010	0.014
e	0.650 BSC		0.026 BSC	
L	0.174	0.326	0.007	0.013

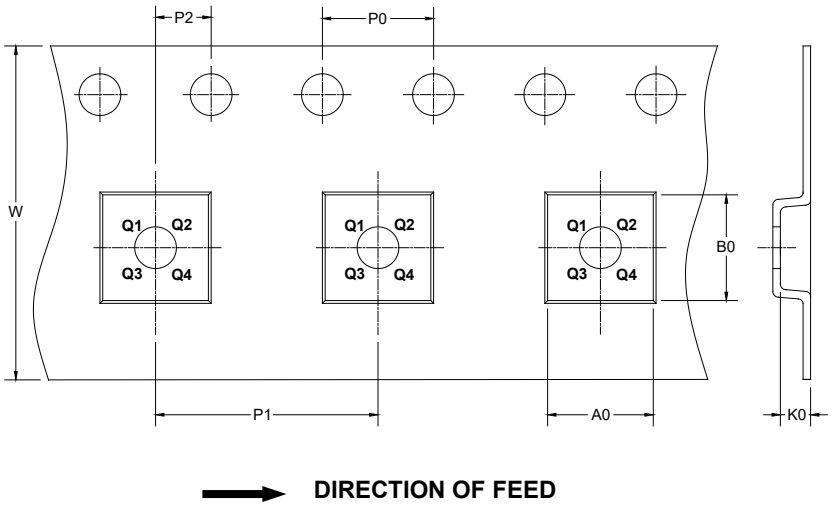
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



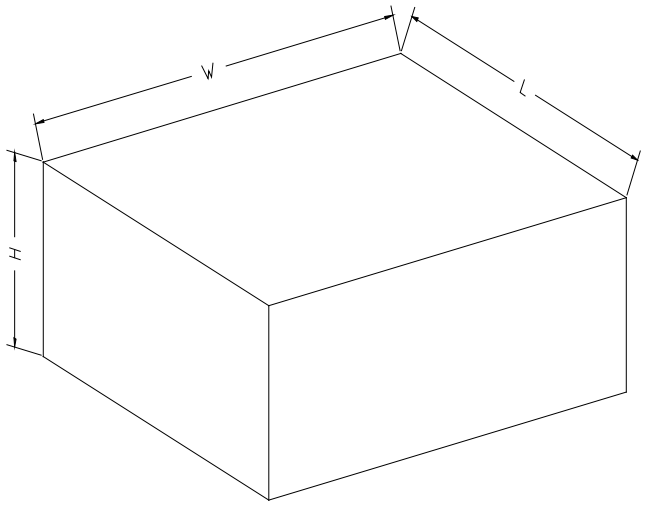
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-0.88×1.28-6B	7″	9.5	0.99	1.38	0.69	4.0	4.0	2.0	8.0	Q1
TDFN-2×2-6AL	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002