SGM64620
3.5V to 65V Dual Synchronous Buck DC/DC Controller with Ultra-Low I_Q

GENERAL DESCRIPTION

The SGM64620 is a 65V dual-channel synchronous Buck controller using peak current mode control, which can provide 3.3V or 5V fixed output voltage or adjustable 0.6V to 55V voltage range. It is capable to drive external N-MOSFETs over the whole voltage range.

The device has optional hiccup mode or cycle-by-cycle current limiting in PWM mode. Power-save mode (PSM) is optional at light load to improve efficiency. Optional spread spectrum frequency modulation (SSFM) is provided to optimize the EMI.

Switching frequency can be programmed by external resistor or synchronized to an external clock. 180° interleaved clock is provided for two channels to reduce the input current ripple. Other functions such as adjustable soft-start time, SYNCOUT signal, open-drain power-good indication (PG), UVLO protection, over-voltage protection (OVP), current limit protection (OCP) and thermal shutdown are included in the SGM64620.

The SGM64620 is available in a Green TQFN-6×6-40EL package.

FEATURES

- **Wide 3.5V to 65V Input Voltage Range**
- **Fixed 3.3V or 5V, or Adjustable 0.6V to 55V Output Voltage**
- **Integrated Four N-MOSFET Drivers**
- **0.85μA Typical Shutdown Current**
- **100kHz to 2.2MHz Adjustable Frequency Range**
- **Adjustable Soft-Start Time**
- **Independent Enable Input**
- **180° Interleaved Out-of-Phase Clock**
- **Synchronous Output (SYNCOUT) with 90° Phase Shift**
- **Power-Good (PG) Indicator**
- **External Power Supply (VCCX) for Internal LDO**
- **Programmable PSM and FPWM Operations**
- **Optional Spread Spectrum Frequency Modulation**
- **VCC, VDDA UVLO Protection**
- **Output Over-Voltage Protection**
- **Optional Hiccup Mode or Cycle-by-Cycle Current Limit Over-Current Protection**
- **Thermal Shutdown**
- **Available in a Green TQFN-6×6-40EL Package**

APPLICATIONS

Communication Systems: Remote Radio Unit (RRU), Wireless Infrastructure

Enterprise Systems: High-Performance Computing

Industrial: Factory Automation and Control, Robotics

SIMPLIFIED SCHEMATIC

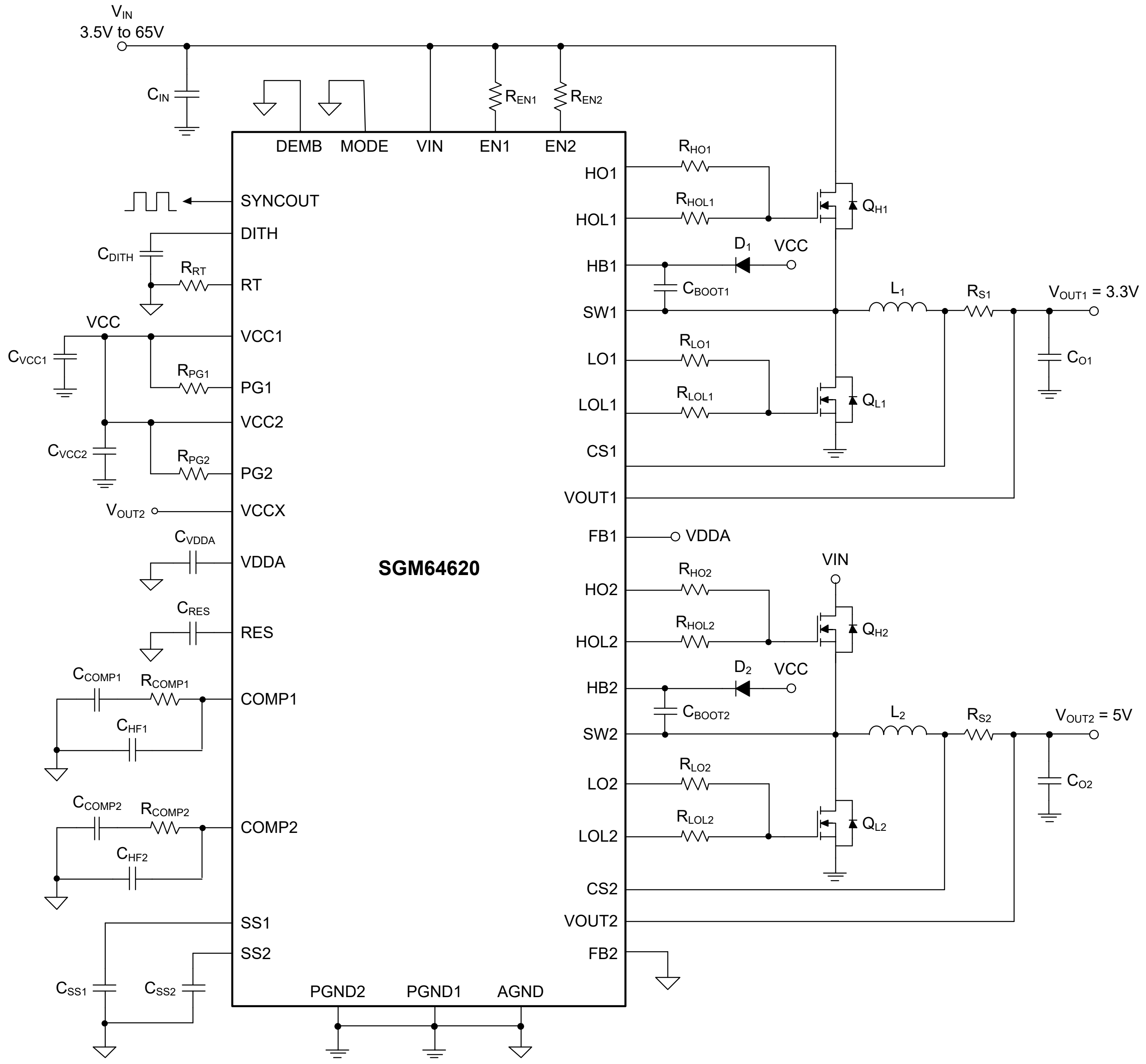


Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM64620	TQFN-6×6-40EL	-40℃ to +150℃	SGM64620TTVZ40G/TR	SGM64620 TTVZ40 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX
- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN to PGND .... -0.3V to 70V
SW1, SW2 to PGND.. -0.3V to 70V
SW1, SW2 to PGND (20ns Transient)..............................-5V
HB1 to SW1, HB2 to SW2 .... -0.3V to 6.5V
HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2..... ....-0.3V to V_{CBOOT} + 0.3V
LO1, LOL1, LO2, LOL2 to PGND ....-0.3V to V_{CC} + 0.3V
SS1, SS2, COMP1, COMP2, RES, RT, MODE, DITH to AGND .... -0.3V to V_{VDDA} + 0.3V
EN1, EN2 to PGND .... -0.3V to 70V
VCC, VCCX, VDDA, PG1, PG2, DEMB, FB1, FB2 to AGND .... -0.3V to 6.5V
VOUT1, VOUT2, CS1, CS2 to AGND................ -0.3V to 60V
VOUT1 to CS1, VOUT2 to CS2 .... -0.3V to 0.3V
PGND to AGND.. -0.3V to 0.3V
Package Thermal Resistance
TQFN-6×6-40EL, θ_{JA}... 26.5℃/W
TQFN-6×6-40EL, θ_{JB}.. 8.8℃/W
TQFN-6×6-40EL, $\theta_{JC\ (TOP)}$ .... 17.2℃/W
TQFN-6×6-40EL, $\theta_{JC\ (BOT)}$ .... 0.9℃/W
Junction Temperature...+150℃
Storage Temperature Range ....-65℃ to +150℃
Lead Temperature (Soldering, 10s)............................+260℃
ESD Susceptibility [(1) (2)]
HBM..±3000V
CDM ....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VIN to PGND ....-0.3V to 65V
SW1, SW2 to PGND ....-0.3V to 65V
HB1 to SW1, HB2 to SW2..............................-0.3V to 5.25V
HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2 ....-0.3V to V_{CBOOT} + 0.3V
LO1, LOL1, LO2, LOL2 to PGND ....-0.3V to 5.25V
FB1, FB2, SS1, SS2, COMP1, COMP2, RES, DEMB, RT, MODE, DITH to AGND ....-0.3V to 5.25V
EN1, EN2 to PGND ....-0.3V to 65V
VCC, VCCX, VDDA to PGND..........................-0.3V to 5.25V
VOUT1, VOUT2, CS1, CS2 to PGND ....-0.3V to 55V
PGND to AGND...-0.3V to 0.3V
Operating Junction Temperature, T_J .... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

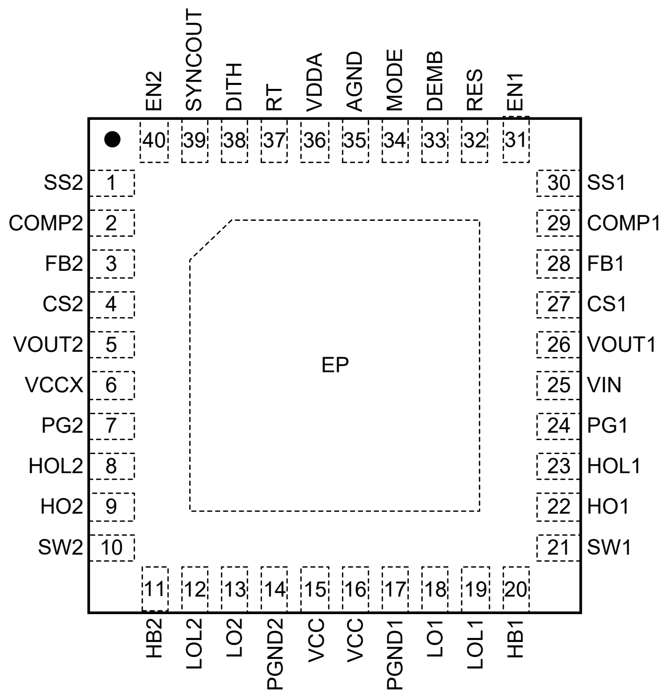
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-6×6-40EL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	SS2	O	Channel 2 Soft-Start Pin. Place an external capacitor (C_{SS2}) between this pin and AGND to set the channel 2 soft-start time.
2	COMP2	O	Channel 2 Compensation Pin. Place an RC network between COMP2 pin and AGND to compensate the loop.
3	FB2	I	Channel 2 Feedback Input Pin. Short FB2 to AGND for channel 2 5V output, and short FB2 to VDDA for channel 2 3.3V output. Place external resistive divider from VOUT2 to FB2 sets channel 2 adjustable output voltage.
4	CS2	I	Channel 2 Current Sense Positive Input.
5	VOUT2	I	Channel 2 Output Voltage Sense and Current Sense Negative Input.
6	VCCX	P	Optional Input for the Internal VCC Regulator. If V_{VCCX} is above its UVLO, the internal VCC input from VIN is disabled. Place a 2.2μF ceramic capacitor between VCCX and PGND.
7	PG2	O	Channel 2 Open-Drain Power-Good Output. Place a 100kΩ pull-up resistor between PG2 and VCC.
8	HOL2	O	Channel 2 High-side Switch Gate Driver Turn-Off Output.
9	HO2	O	Channel 2 High-side Switch Gate Driver Turn-On Output.
10	SW2	P	Switching Node of the Channel 2. Connect to the switching node of the channel 2 converter and acts as return for the V_{BOOT} supply and provides a path for the high-side switch high bootstrapping currents.
11	HB2	P	Channel 2 High-side Switch Driver Supply for the Bootstrap Gate Drive. The bootstrap capacitor is placed between HB2 and SW2 pins.
12	LOL2	O	Channel 2 Low-side Switch Gate Driver Turn-Off Output.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
13	LO2	O	Channel 2 Low-side Switch Gate Driver Turn-On Output.
14	PGND2	G	Power Ground. Power ground return for the input supply, channel 2 external low-side switch, load and internal low-side switch driver.
15, 16	VCC	P	VCC Bias Supply Pin. Pins 15 and 16 must to be connected together on the PCB. Connect ceramic capacitors between VCC and PGND1 and between VCC and PGND2.
17	PGND1	G	Power Ground. Power ground return for the input supply, channel 1 external low-side switch, load and internal low-side switch driver.
18	LO1	O	Channel 1 Low-side Switch Gate Driver Turn-On Output.
19	LOL1	O	Channel 1 Low-side Switch Gate Driver Turn-Off Output.
20	HB1	P	Channel 1 High-side Switch Driver Supply for the Bootstrap Gate Drive. The bootstrap capacitor is placed between HB1 and SW1 pins.
21	SW1	P	Switching Node of the Channel 1. Connect to the switching node of the channel 1 converter and act as return for the V_{BOOT} supply and provides a path for the high-side switch high bootstrapping currents.
22	HO1	O	Channel 1 High-side Switch Gate Driver Turn-On Output.
23	HOL1	O	Channel 1 High-side Switch Gate Driver Turn-Off Output.
24	PG1	O	Channel 1 Open-Drain Power-Good Output. Place a 100kΩ pull-up resistor between PG1 and VCC.
25	VIN	P	Power Supply Input Pin. Place a 0.47μF decoupling ceramic capacitor between VIN pin and PGND.
26	VOUT1	I	Channel 1 Output Voltage Sense and Current Sense Negative Input.
27	CS1	I	Channel 1 Current Sense Positive Input.
28	FB1	I	Channel 1 Feedback Input Pin. Short FB1 to AGND for channel 1 5V output, and short FB1 to VDDA for channel 1 3.3V output. Place external resistive divider from VOUT1 to FB1 sets channel 1 adjustable output voltage.
29	COMP1	O	Channel 1 Compensation Pin. Use an RC network from COMP1 pin to AGND to compensate the loop.
30	SS1	O	Channel 1 Soft-Start Pin. Place an external capacitor (C_{SS1}) between this pin and the AGND to set the channel 1 soft-start time.
31	EN1	I	Channel 1 Enable Input Pin.
32	RES	O	Hiccup Restart Time Setting Pin. Place an external capacitor between RES pin to AGND setting the hiccup off-time. If not used, connect it to VDDA pin.
33	DEMB	I	PSM/FPWM Selection Pin. Connect DEMB to AGND to enable PSM mode or connect DEMB to VDDA to enable FPWM mode at light load. An external clock also can be connected to DEMB pin as a synchronization input.
34	MODE	I	Working Mode Selection Pin. Connect MODE to AGND for dual-output operation. Connect MODE to AVDD for interleaved Single-Output operation. Connecting a 10kΩ resistor between MODE and AGND sets an ultra-low I_Q mode at dual-output operation.
35	AGND	G	Analog Ground Pin.
36	VDDA	P	Internal Analog Bias Regulator Output. Connect a ceramic capacitor from VDDA to AGND.
37	RT	I	Switching Frequency Set Pin. A resistor from RT to AGND sets the oscillator frequency between 100kHz and 2.2MHz.
38	DITH	I	Spread Spectrum Frequency Modulation Set Pin. A capacitor connected between DITH Pin and AGND is charged and discharged with a current source. If not used, connect it to VDDA.
39	SYNCOUT	O	SYNC Clock Output Pin. It is a logic level signal with a rising edge approximately 90° lagging HO2 (or 90° Leading HO1). When the SYNCOUT signal is used to synchronize a second SGM64620, all phases are 90° out of phase.
40	EN2	I	Channel 2 Enable Input Pin.
Exposed Pad	EP	G	Exposed Pad. Connect this pin to ground at PCB for chip heat dissipation.

NOTE: P = Power, G = Ground, I = Input, O = Output.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +150℃, typical values are at V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5V, V_{EN1} = V_{EN2} = 5V, R_{RT} = 10kΩ, f_{SW} = 2.2MHz, no load on the drive outputs, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage (VIN)						
Shutdown Mode Current	I_{SD}	V_{EN1} = V_{EN2} = 0V		0.85	2.5	μA
Input Current, Channel 1, Normal I_Q Mode	I_{Q_CH1}	V_{VCCX} = 0V, V_{EN1} = 5V, V_{EN2} = 0V, V_{FB1} = 0.63V, DEMB = MODE = GND		66	110	μA
	$I_{Q\_CH1\_VCCX}$	V_{VCCX} = 5V, V_{EN1} = 5V, V_{EN2} = 0V, V_{FB1} = 0.63V, DEMB = MODE = GND		4.8	8.5	μA
	I_{VCCX}			62	100	μA
Input Current, Channel 2, Normal I_Q Mode	I_{Q_CH2}	V_{VCCX} = 0V, V_{EN1} = 0V, V_{EN2} = 5V, V_{FB2} = 0.63V, DEMB = MODE = GND		66	110	μA
	$I_{Q\_CH2\_VCCX}$	V_{VCCX} = 5V, V_{EN1} = 0V, V_{EN2} = 5V, V_{FB2} = 0.63V, DEMB = MODE = GND		4.8	8.5	μA
	I_{VCCX}			62	100	μA
Input Current, Channel 1, Ultra-Low I_Q Mode	I_{ULQ_CH1}	V_{VCCX} = 0V, V_{EN1} = 5V, V_{EN2} = 0V, V_{FB1} = 0.63V, DEMB = GND, MODE = 10kΩ to GND		48	80	μA
	$I_{ULQ\_CH1\_VCCX}$	V_{VCCX} = 5V, V_{EN1} = 5V, V_{EN2} = 0V, V_{FB1} = 0.63V, DEMB = GND, MODE = 10kΩ to GND		4.8	8.5	μA
	I_{VCCX}			42	75	μA
Input Current, Channel 2, Ultra-Low I_Q Mode	I_{ULQ_CH2}	V_{VCCX} = 0V, V_{EN1} = 0V, V_{EN2} = 5V, V_{FB2} = 0.63V, DEMB = GND, MODE = 10kΩ to GND		48	80	μA
	$I_{ULQ\_CH2\_VCCX}$	V_{VCCX} = 5V, V_{EN1} = 0V, V_{EN2} = 5V, V_{FB2} = 0.63V, DEMB = GND, MODE = 10kΩ to GND		4.8	8.5	μA
	I_{VCCX}			42	75	μA
Bias Regulator (VCC)						
VCC Regulation Voltage	V_{VCC_REG}	I_{VCC} = 100mA, V_{VCCX} = 0V	4.65	4.82	5.05	V
VCC UVLO Rising Threshold	V_{VCC_UVLO}	V_{VCC} rising, V_{VCCX} = 0V	3.2	3.37	3.5	V
VCC UVLO Hysteresis	V_{VCC_HYS}	V_{VCCX} = 0V		150		mV
VCC Sourcing Current Limit	I_{VCC_LIM}	V_{VCCX} = 0V, VCC falls to 90%		320		mA
Analog Bias (VDDA)						
VDDA Regulation Voltage	V_{VDDA_REG}		4.45	4.6	4.85	V
VDDA UVLO Rising Threshold	V_{VDDA_UVLO}	V_{VDDA} rising, V_{VCCX} = 0V	3.05	3.2	3.35	V
VDDA UVLO Hysteresis	V_{VDDA_HYS}	V_{VCCX} = 0V		145		mV
VDDA Resistance	R_{VDDA}	V_{VCCX} = 0V		15		Ω
External Bias (VCCX)						
VCCX_ON Rising Threshold	V_{VCCX_ON}	V_{VCCX} rising	4.1	4.3	4.45	V
VCCX Hysteresis Voltage	V_{VCCX_HYS}			135		mV
VCCX Resistance	R_{VCCX}	V_{VCCX} = 5V		2.1		Ω
Current Limit (CS1, CS2)						
Current Limit Threshold 1	V_{CS1}	Measured from CS1 to VOUT1	63	73	85	mV
Current Limit Threshold 2	V_{CS2}	Measured from CS2 to VOUT2	63	73	85	mV
CS Delay to Output (1)	t_{CS_DLY}			30		ns
CS Amplifier Gain	G_{CS}		10.9	11.5	12.1	V/V
CS Amplifier Input Bias Current	I_{CS_B}				150	nA

NOTE:
1. Not tested in production, guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +150℃, typical values are at V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5V, V_{EN1} = V_{EN2} = 5V, R_{RT} = 10kΩ, f_{SW} = 2.2MHz, no load on the drive outputs, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Good (PG1, PG2)						
PG1 Rising Threshold	$PG1_{VTH\_RISING}$	V_{FB1} Rising, % of V_{REF}	84	90	95.5	%
		V_{FB1} falling, % of V_{REF}	101.5	106.5	112.5	%
PG1 Falling Threshold	$PG1_{VTH\_FALLING}$	V_{FB1} Rising, % of V_{REF}	106	110	116	%
		V_{FB1} falling, % of V_{REF}	81	86.5	92	%
PG2 Rising Threshold	$PG2_{VTH\_RISING}$	V_{FB2} Rising, % of V_{REF}	84	90	95.5	%
		V_{FB2} falling, % of V_{REF}	101.5	106.5	112.5	%
PG2 Falling Threshold	$PG2_{VTH\_FALLING}$	V_{FB2} Rising, % of V_{REF}	106	110	116	%
		V_{FB2} falling, % of V_{REF}	81	86.5	92	%
PG1 Voltage	V_{OL_PG1}	Open collector, I_{PG1} = 1mA			0.4	V
PG2 Voltage	V_{OL_PG2}	Open collector, I_{PG2} = 1mA			0.4	V
PG Rising Delay Time (1)	$t_{PG\_R\_DLY}$	V_{OUT} rising		25		μs
PG Falling Delay Time (1)	$t_{PG\_F\_DLY}$	V_{OUT} falling		25		μs
High-side Gate Driver (HO1, HO2, HOL1, HOL2)						
HO Pull-Up Resistance	R_{HO_PULLUP}	Source 100mA		0.9		Ω
HO Pull-Down Resistance	R_{HO_PULLDN}	Sink 100mA		0.51		Ω
HO Rise Time (10% to 90%) (1)	t_{HO_R}	C_{LOAD} = 2.7nF		8		ns
HO Fall Time (90% to 10%) (1)	t_{HO_F}	C_{LOAD} = 2.7nF		4.6		ns
HO Peak Source Current (1)	I_{HO_SRC}	V_{HO} = V_{SW} = 0V, V_{HB} = 4.8V		1.7		A
HO Peak Sink Current (1)	I_{HO_SINK}	V_{SW} = 0V, V_{HOL} = 4.8V		2.6		A
BOOT UVLO	V_{BT_UV}	VDDA > 4V, CBOOT voltage falling threshold		2.37		V
BOOT UVLO Hysteresis	$V_{BT\_UV\_HYS}$			150		mV
BOOT Quiescent Current	I_{BOOT}			1.2		μA
Low-side Gate Driver (LO1, LO2, LOL1, LOL2)						
LO Pull-Up Resistance	R_{LO_PULLUP}	Source 100mA		0.87		Ω
LO Pull-Down Resistance	R_{LO_PULLDN}	Sink 100mA		0.63		Ω
LO Rise Time (10% to 90%) (1)	t_{LO_R}	C_{LOAD} = 2.7nF		6.2		ns
LO Fall Time (90% to 10%) (1)	t_{LO_F}	C_{LOAD} = 2.7nF		4.7		ns
LO Peak Source Current (1)	I_{LO_SOURCE}	V_{LO} = 0V, V_{CC} = 4.8V		2.1		A
LO Peak Sink Current (1)	I_{LO_SINK}	V_{LOL} = 4.8V		2.5		A
Restart (RES)						
RES Current Source	I_{RES_SRC}			20		μA
RES Threshold (1)	V_{RES_TH}			1.15		V
Hiccup Mode Fault (1)	HIC_{CYC}	Switching cycles		512		Cycle
RES Pull-Down Resistance	R_{RES_PD}			3.6		Ω
Output Voltage Setpoint (VOUT1, VOUT2)						
3.3V Output Voltage Setpoint	$V_{OUT\_3.3}$	FB = VDDA, V_{IN} = 3.5V to 65V	3.25	3.3	3.34	V
5V Output Voltage Setpoint	V_{OUT_5}	FB = AGND, V_{IN} = 5.5V to 65V	4.92	5	5.05	V

NOTE:

1. Not tested in production, guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +150℃, typical values are at V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5V, V_{EN1} = V_{EN2} = 5V, R_{RT} = 10kΩ, f_{SW} = 2.2MHz, no load on the drive outputs, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Feedback (FB1, FB2)						
3.3V Output Select, V_{FB} Threshold	$V_{FB\_3.3\_SEL}$		4.4			V
5V Output Select, FB to AGND Resistance [1]	R_{FB_5}	V_{MODE} = 0V or R_{MODE} = 10kΩ			500	Ω
FB External Equivalent Resistance for Adjustable Output Voltage [1]	$R_{FB\_EXT\_RES}$	V_{MODE} = 0V or R_{MODE} = 10kΩ, V_{FB} < 2V	5			kΩ
Input Low Level of FB2 Pin in Master/Slave Selection	V_{FB2_L}	MODE = VDDA			0.8	V
Input High Level of FB2 Pin in Master/Slave Selection	V_{FB2_H}	MODE = VDDA	2			V
Input Low Level of Slave FB1 Pin in PSM Selection	V_{FB1_L}	MODE = FB2 = VDDA			0.8	V
Input High Level of Slave FB1 Pin in FPWM Mode Selection	V_{FB1_H}	MODE = FB2 = VDDA	2			V
FB Reference Voltage	V_{REF}		0.594	0.6	0.606	V
Error Amplifier (COMP1, COMP2)						
EA Transconductance	gm_1	R_{MODE} = 0Ω to AGND	800	1200	1600	μS
EA Transconductance, Ultra-Low I_Q Mode	gm_2	MODE = GND, R_{MODE} = 10kΩ to AGND		125		μS
Error Amplifier Input Bias Current	I_{FB}				50	nA
COMP Clamp Voltage [1]	V_{COMP_CLMP}	V_{FB} = 0V		2.5		V
Slave COMP pin Leakage	I_{COMP_SLAVE}	V_{COMP} = 1V, MODE = FB2 = VDDA			50	nA
COMP2 Pin Leakage in Interleaved Mode	I_{COMP_INTLV}	V_{COMP} = 1V, MODE = VDDA, V_{FB2} = AGND			50	nA
EA Source Current	I_{COMP_SRC1}	V_{COMP} = 1V, V_{FB} = 0.4V, V_{MODE} = 0V		150		μA
EA Sink Current	I_{COMP_SINK1}	V_{COMP} = 1V, V_{FB} = 0.8V, V_{MODE} = 0V		150		μA
EA Source Current, Ultra-Low I_Q Mode	I_{COMP_SRC2}	V_{COMP} = 1V, V_{FB} = 0.4V, R_{MODE} = 10kΩ to AGND		12		μA
EA Sink Current, Ultra-Low I_Q Mode	I_{COMP_SINK2}	V_{COMP} = 1V, V_{FB} = 0.8V, R_{MODE} = 10kΩ to AGND		12		μA
EA SS Offset with V_{FB} = 0V [1]	V_{SS_OFFSET}			36		mV
Adaptive Deadtime Control						
VGS Detection Threshold [1]	V_{GS_DET}	VGS falling, no-load		2.3		V
HO Off to LO on Dead-Time [1]	t_{DEAD1}			20		ns
LO Off to HO on Dead-Time [1]	t_{DEAD2}			20		ns
Diode Emulation (DEMB)						
DEMB Input Low Level	V_{DEMB_L}				0.8	V
DEMB Input High Level	V_{DEMB_H}		2			V
Zero-Cross Threshold	V_{ZC_SW}	DEMB = AGND		-7		mV
Zero-Cross Threshold during Soft-Start [1]	V_{ZC_SS}	DEMB = VDDA, 64 switching cycles after first HO pulse		-7		mV
Negative Current limit Threshold [1]	V_{NEG_SW}	DEMB = VDDA		180		mV
Enable (EN1, EN2)						
EN1 Input Low Level	V_{EN1_L}	V_{VCCX} = 0V			0.8	V
EN1 Input High Level	V_{EN1_H}		2			V
EN2 Input Low Level	V_{EN2_L}				0.8	V
EN2 Input High Level	V_{EN2_H}		2			V
EN1/2 Leakage Current	I_{EN_LEAK}	EN1, EN2 logic inputs only		5	100	nA

NOTE:

1. Not tested in production, guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +150℃, typical values are at V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5V, V_{EN1} = V_{EN2} = 5V, R_{RT} = 10kΩ, f_{SW} = 2.2MHz, no load on the drive outputs, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency (RT)						
RT Regulation Voltage	V_{RT}			0.8		V
Mode						
R_{MODE} Resistance Value for Ultra-Low I_Q Mode [1]	R_{MODE_H}		5			kΩ
R_{MODE} Resistance Value for Normal I_Q Mode [1]	R_{MODE_L}				0.5	kΩ
Non-Interleaved Mode Input Low Level	V_{MODE_L}				0.8	V
Interleaved Mode Input High Level	V_{MODE_H}		2			V
Synchronization Input (SYNCIN)						
SYNCIN Clock Input Low Level	V_{SYNC_L}				0.8	V
SYNCIN Clock Input High Level	V_{SYNC_H}		2			V
SYNCIN Minimum Pulse Width	t_{SYNC_MIN}	V_{MODE} = 0V or R_{MODE} = 10kΩ	20			ns
External SYNCIN Frequency Range	f_{SYNCIN}	% of the nominal frequency set by R_{RT}	-20		20	%
Delay from SYNCIN Rising to HO1 Rising Edge [1]	$t_{SYNCIN\_R\_DLY}$			150		ns
Delay from SYNCIN Falling Edge to HO2 Rising Edge [1]	$t_{SYNCIN\_F\_DLY}$	Secondary mode, MODE = FB2 = VDDA		150		ns
Delay time from SYNCIN Low to PSM Mode Enable [1]	t_{SYNCIN_PSM}	V_{MODE} = 0V or R_{MODE} = 10kΩ		55		μs
Delay time from SYNCIN signal to internal clock [1]	t_{PLL}			55		μs
Synchronization Output (SYNCOUT)						
SYNCOUT Low-State Voltage [1]	$V_{SYNCOUT\_LO}$	$I_{SYNCOUT}$ = 1mA			0.8	V
SYNCOUT Frequency in Slave [1]	$f_{SYNCOUT}$	MODE = FB2 = VDDA			0	Hz
Delay from HO2 Rising Edge to SYNCOUT Rising Edge [1]	$t_{SYNCOUT1}$	V_{DEMB} = 0V, f_{SW} = 100kHz		2.5		μs
Delay from HO2 Rising Edge to SYNCOUT Falling Edge [1]	$t_{SYNCOUT2}$	V_{DEMB} = 0V, f_{SW} = 100kHz		7.5		μs
Dither (DITH)						
Dither Source and Sink Current	I_{DITH}			20		μA
Dither High-Level Threshold [1]	V_{DITH_H}			1.25		V
Dither Low-Level Threshold [1]	V_{DITH_L}			1.15		V
Soft Start (SS1, SS2)						
Soft-Start Current	I_{SS}	V_{MODE} = 0V	14	21	34	μA
Soft-Start Pull-Down Resistance	R_{SS_PD}	V_{MODE} = 0V		3.5		Ω
SS to FB Clamp Voltage [1]	V_{SS_FB}	V_{CS} - V_{OUT} > 73mV		190		mV
Slave SS pin Leakage	I_{SS_SLAVE}	V_{SS} = 0.8V, MODE = FB2 = VDDA		5		nA
SS2 Pin Leakage in Interleaved Mode	I_{SS_INTLV}	V_{SS} = 0.8V, MODE = VDDA, V_{FB2} = 0V		5		nA
Thermal Shutdown						
Thermal Shutdown [1]	T_{SD}			175		℃
Thermal Shutdown Hysteresis [1]	T_{SD_HYS}			20		℃

NOTE:
1. Not tested in production, guaranteed by design and characterization.

SWITCHING CHARACTERISTICS

(T_J = -40℃ to +150℃, typical values are at V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5V, V_{EN1} = V_{EN2} = 5V, R_{RT} = 10kΩ, f_{SW} = 2.2MHz, no load on the drive outputs, T_J = +25℃, unless otherwise noted.)

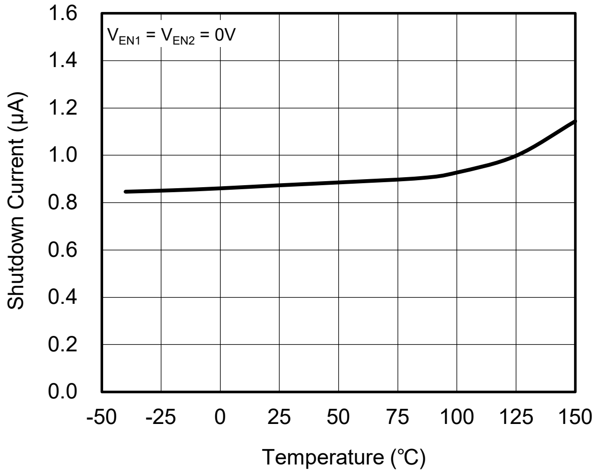
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency 1	f_{SW1}	R_{RT} = 100kΩ	220	275	325	kHz
Switching Frequency 2	f_{SW2}	R_{RT} = 10kΩ	2.0	2.2	2.35	MHz
Switching Frequency 3	f_{SW3}	R_{RT} = 220kΩ	100	125	155	kHz
Internal Slope Compensation 1 (1)	V_{SLOPE1}	R_{RT} = 10kΩ		840		mV/μs
Internal Slope Compensation 2 (1)	V_{SLOPE2}	R_{RT} = 100kΩ		85		mV/μs
Minimum On-Time (1)	t_{ON_MIN}			98		ns
Minimum Off-Time (1)	t_{OFF_MIN}			99		ns
Phase between HO1 and HO2 (1)	$PH_{HO1-HO2}$	DEMB = MODE = AGND		180		°

NOTE:
1. Not tested in production, guaranteed by design and characterization.

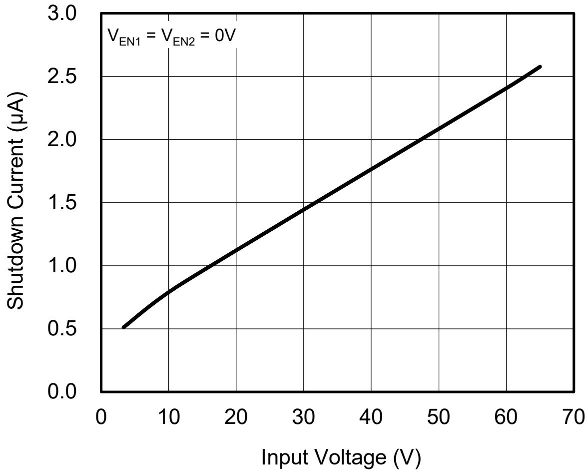
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{EN1} = V_{EN2} = 5V, f_{SW} = 400kHz, V_{OUT1} = 3.3V (FB1 to VDDA), V_{OUT2} = 5V (FB2 to GND), VCCX = V_{OUT2}, L = 3.3μH (DCR = 9.9mΩ), T_A = +25℃, unless otherwise noted.

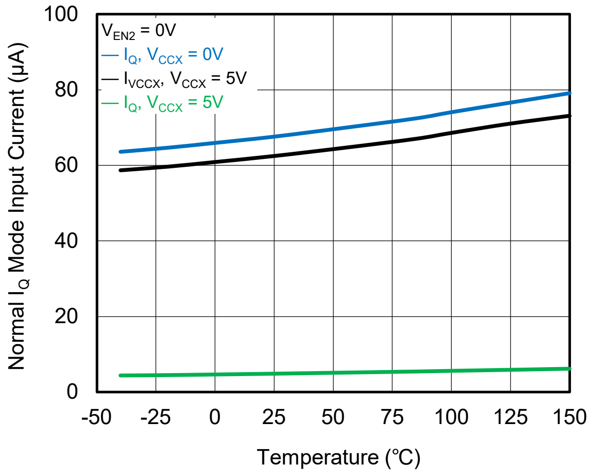
Shutdown Current vs. Temperature



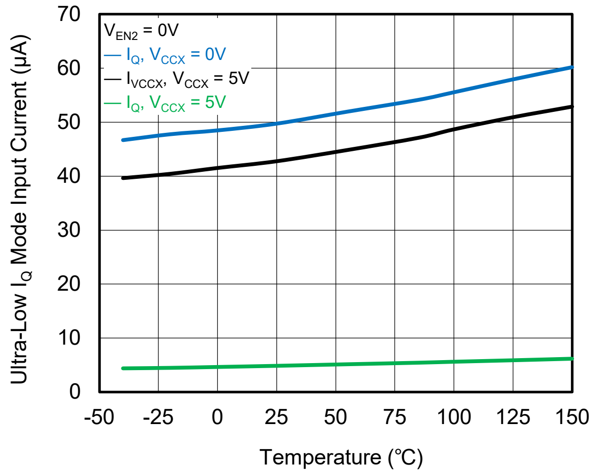
Shutdown Current vs. Input Voltage



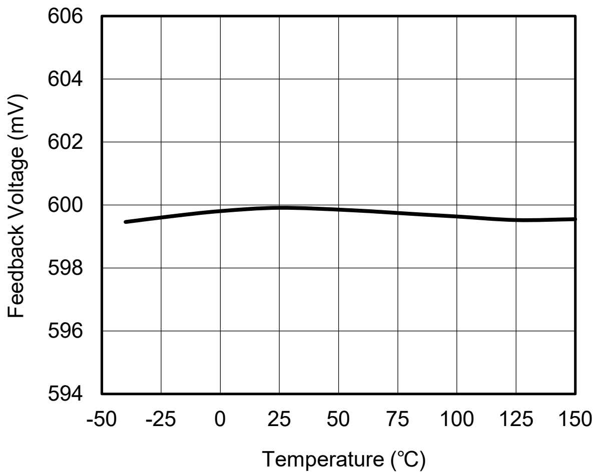
Normal I_Q Mode Input Current vs. Temperature (Channel 1)



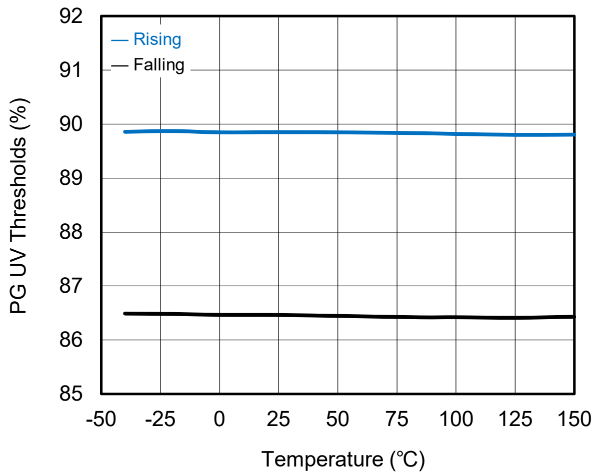
Ultra-Low I_Q Mode Input Current vs. Temperature (Channel 1)



Feedback Voltage vs. Temperature



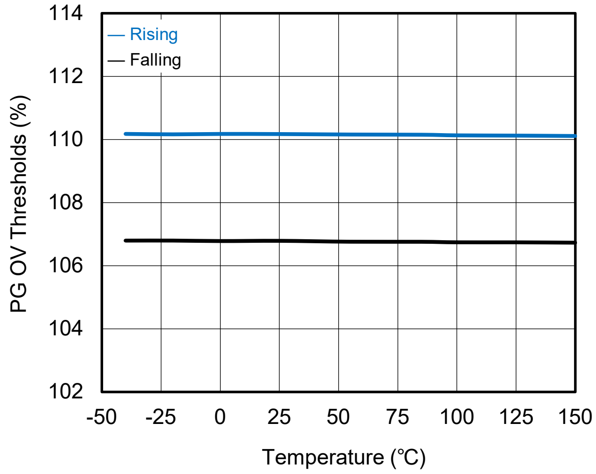
PG UV Thresholds vs. Temperature



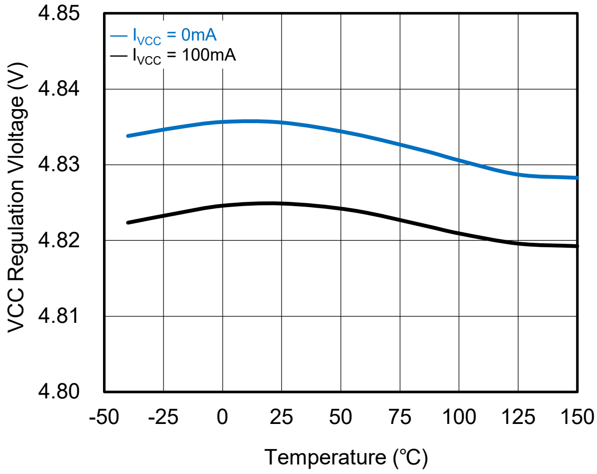
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{EN1} = V_{EN2} = 5V, f_{SW} = 400kHz, V_{OUT1} = 3.3V (FB1 to VDDA), V_{OUT2} = 5V (FB2 to GND), VCCX = V_{OUT2}, L = 3.3μH (DCR = 9.9mΩ), T_A = +25℃, unless otherwise noted.

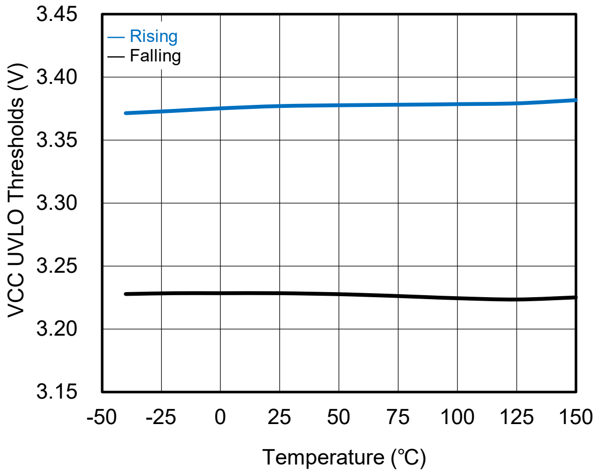
PG OV Thresholds vs. Temperature



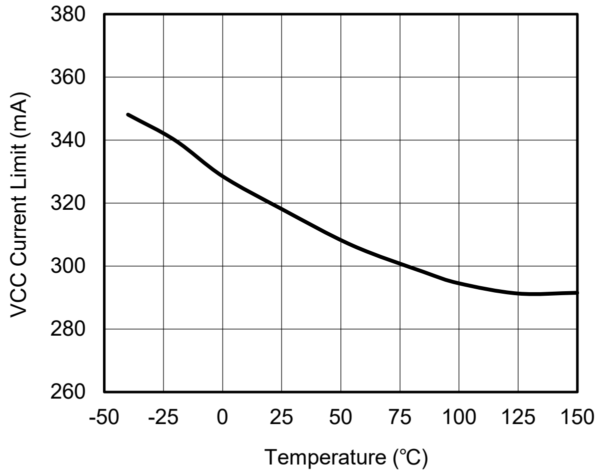
VCC Regulation Voltage vs. Temperature



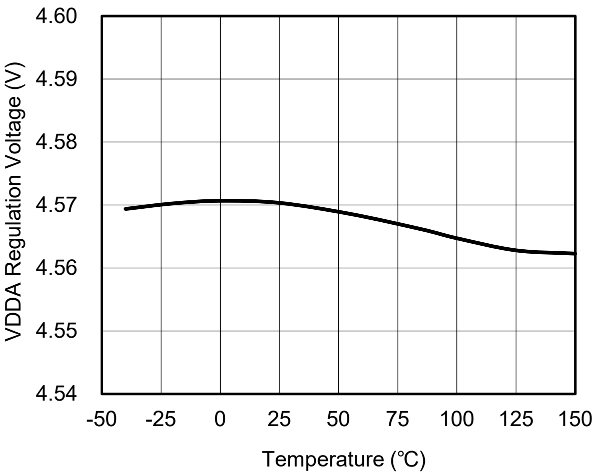
VCC UVLO Thresholds vs. Temperature



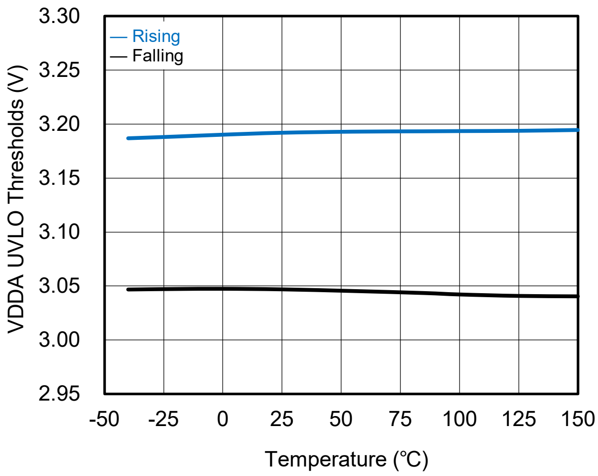
VCC Current Limit vs. Temperature



VDDA Regulation Voltage vs. Temperature



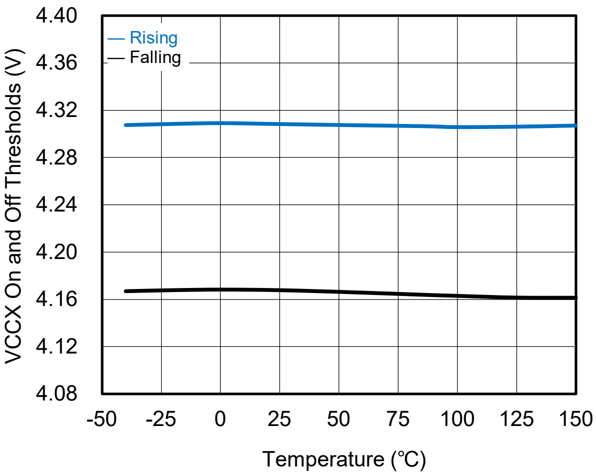
VDDA UVLO Thresholds vs. Temperature



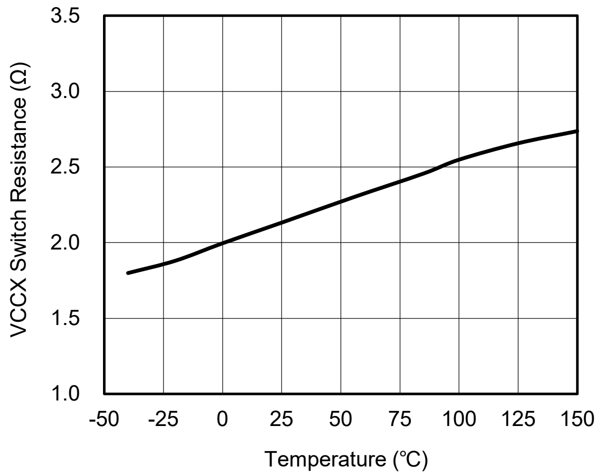
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{EN1} = V_{EN2} = 5V, f_{SW} = 400kHz, V_{OUT1} = 3.3V (FB1 to VDDA), V_{OUT2} = 5V (FB2 to GND), VCCX = V_{OUT2}, L = 3.3μH (DCR = 9.9mΩ), T_A = +25℃, unless otherwise noted.

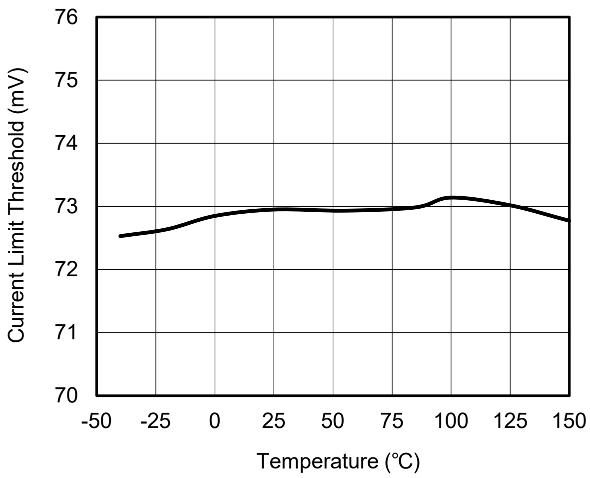
VCCX On and Off Thresholds vs. Temperature



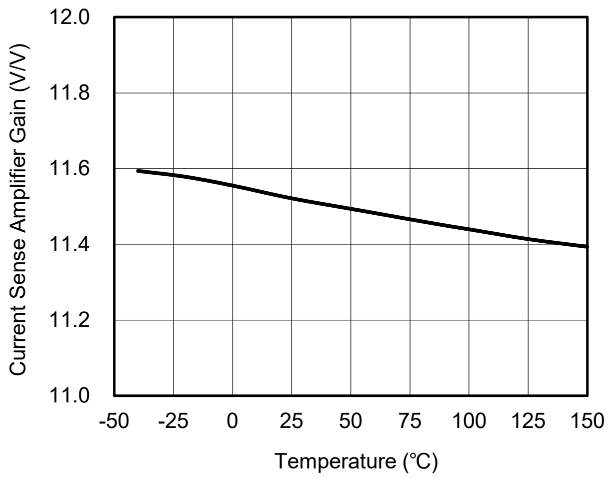
VCCX Switch Resistance vs. Temperature



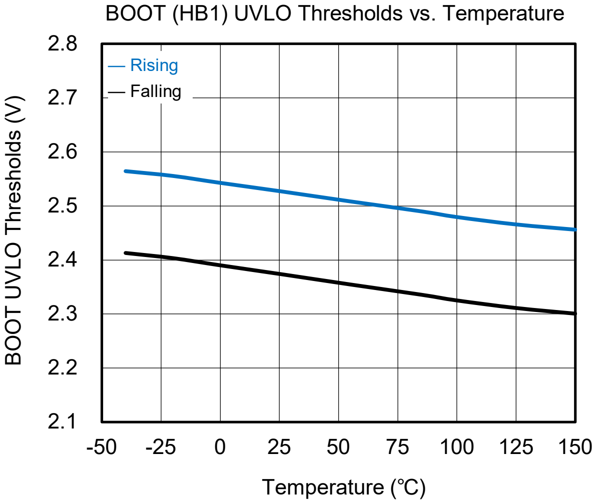
Current Limit (CS1) Thresholds vs. Temperature



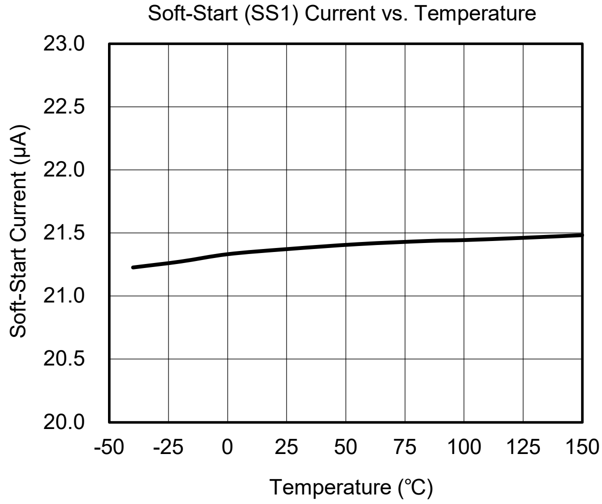
Current Sense (CS1) Amplifier Gain vs. Temperature



BOOT (HB1) UVLO Thresholds vs. Temperature



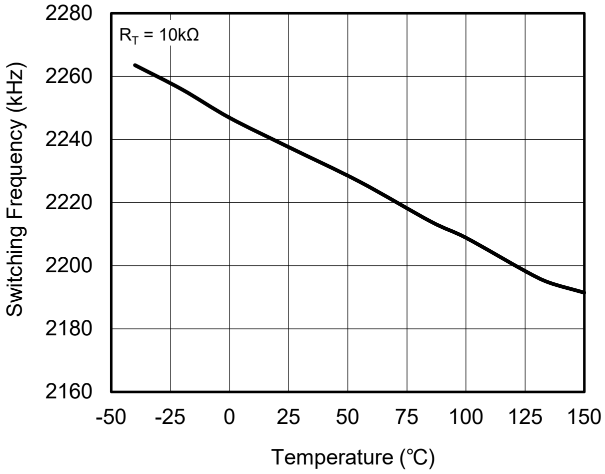
Soft-Start (SS1) Current vs. Temperature



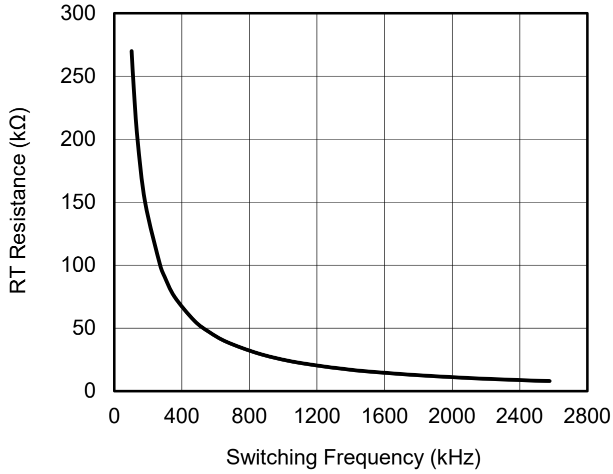
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{EN1} = V_{EN2} = 5V, f_{SW} = 400kHz, V_{OUT1} = 3.3V (FB1 to VDDA), V_{OUT2} = 5V (FB2 to GND), VCCX = V_{OUT2}, L = 3.3μH (DCR = 9.9mΩ), T_A = +25℃, unless otherwise noted.

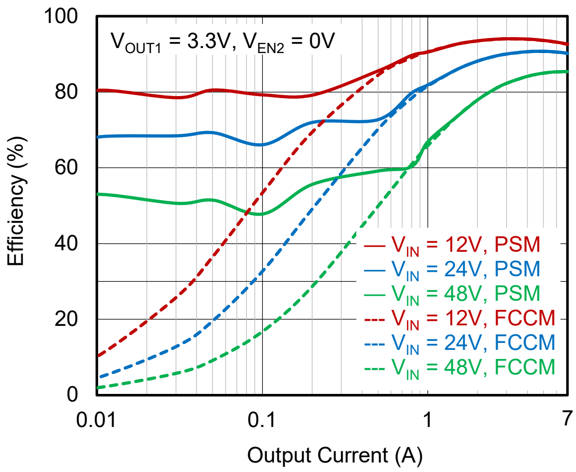
Switching Frequency vs. Temperature



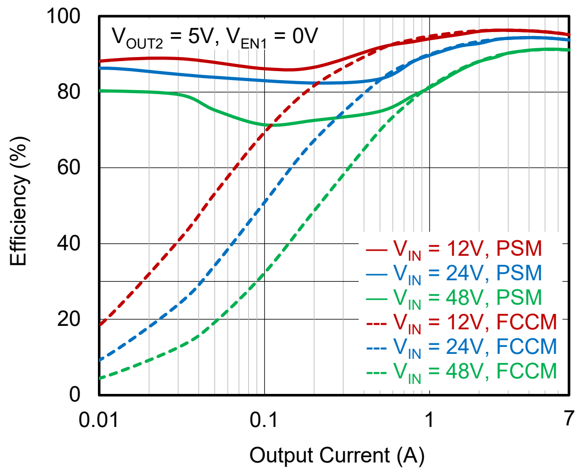
RT Resistance vs. Switching Frequency



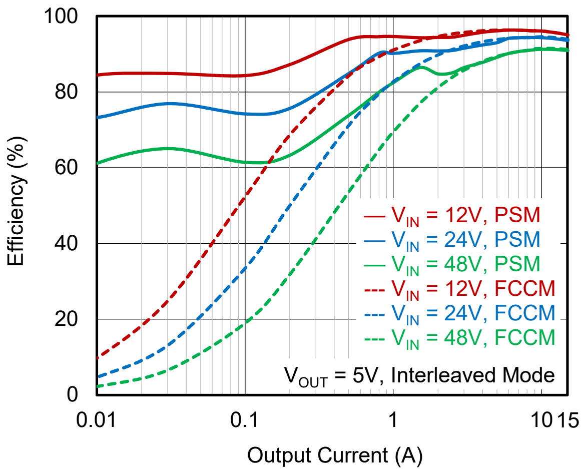
Efficiency vs. Output Current



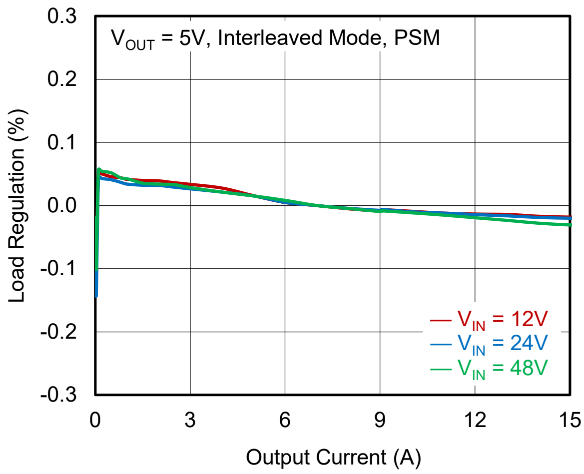
Efficiency vs. Output Current



Efficiency vs. Output Current



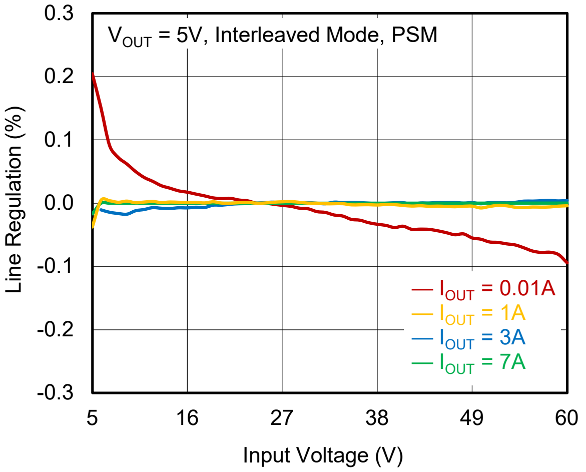
Load Regulation



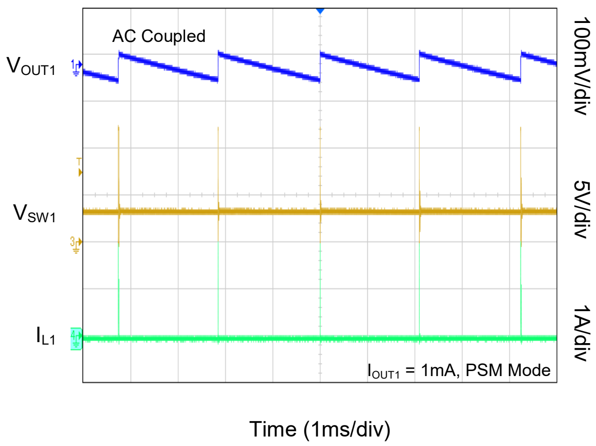
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{EN1} = V_{EN2} = 5V, f_{SW} = 400kHz, V_{OUT1} = 3.3V (FB1 to VDDA), V_{OUT2} = 5V (FB2 to GND), VCCX = V_{OUT2}, L = 3.3μH (DCR = 9.9mΩ), T_A = +25℃, unless otherwise noted.

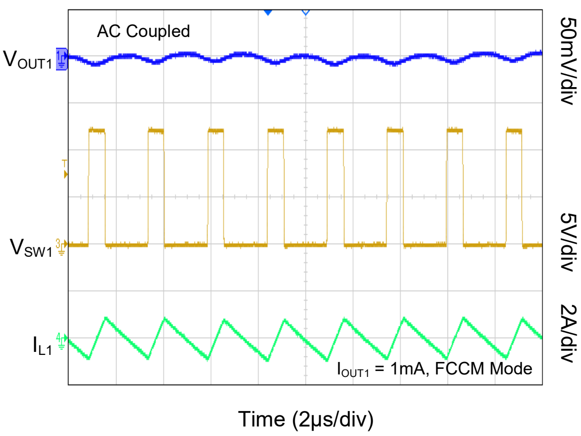
Line Regulation



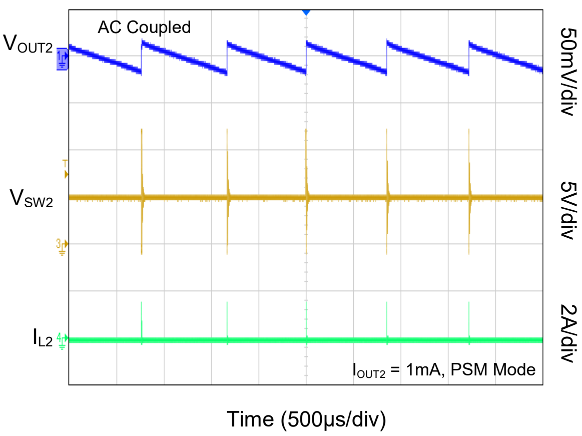
Steady State



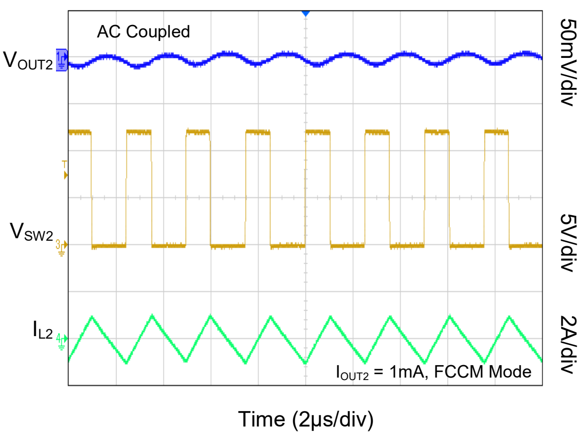
Steady State



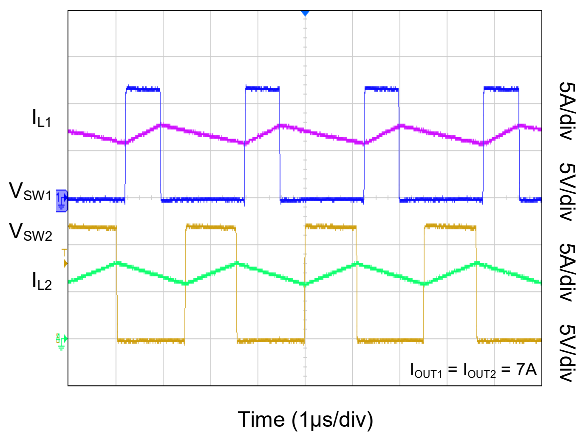
Steady State



Steady State



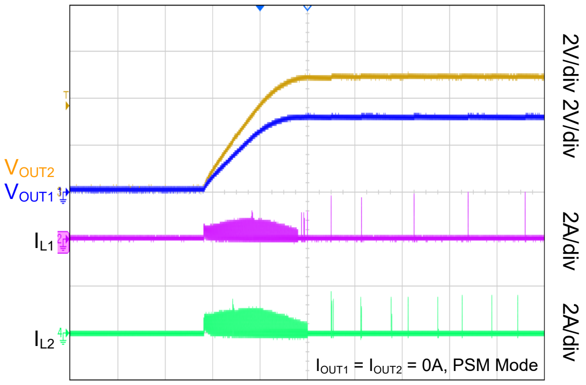
Steady State



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

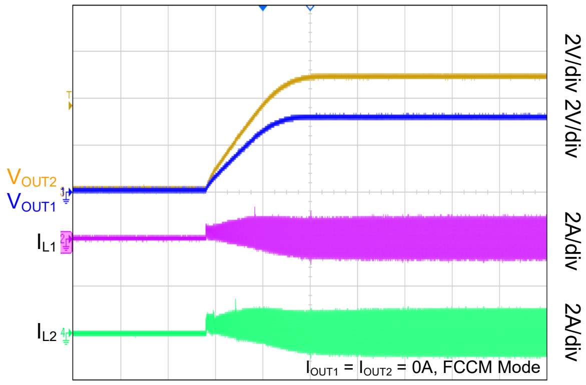
V_{IN} = 12V, V_{EN1} = V_{EN2} = 5V, f_{SW} = 400kHz, V_{OUT1} = 3.3V (FB1 to VDDA), V_{OUT2} = 5V (FB2 to GND), VCCX = V_{OUT2}, L = 3.3μH (DCR = 9.9mΩ), T_A = +25℃, unless otherwise noted.

Startup through VIN



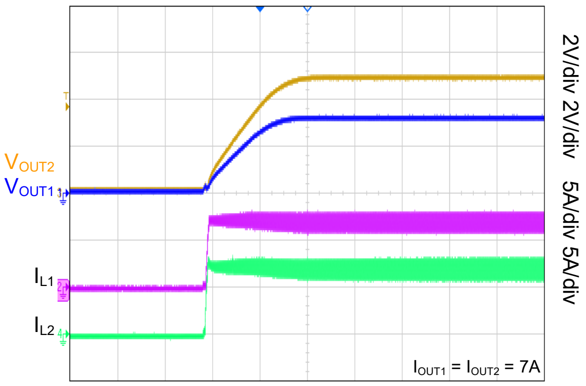
Time (1ms/div)

Startup through VIN



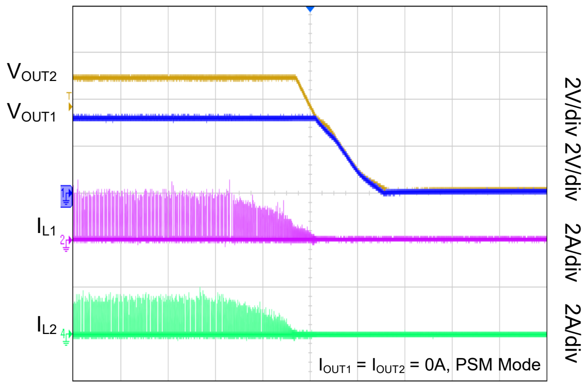
Time (1ms/div)

Startup through VIN



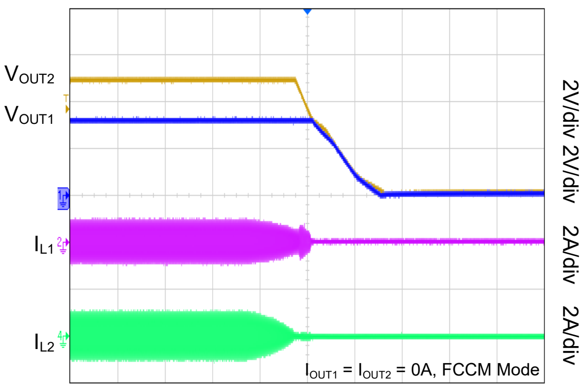
Time (1ms/div)

Shutdown through VIN



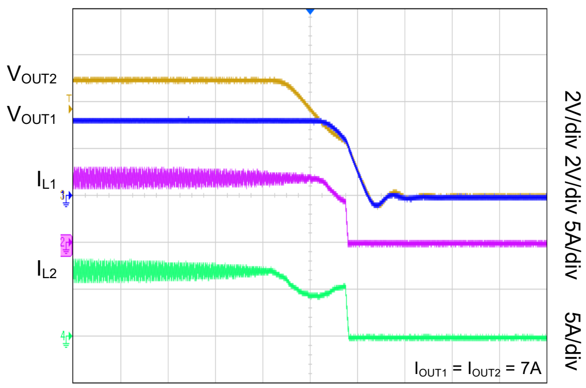
Time (50ms/div)

Shutdown through VIN



Time (50ms/div)

Shutdown through VIN

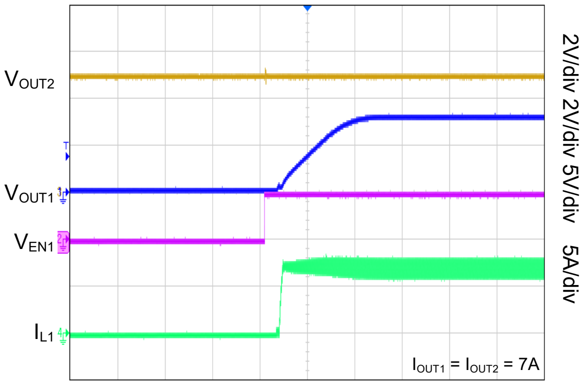


Time (100μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

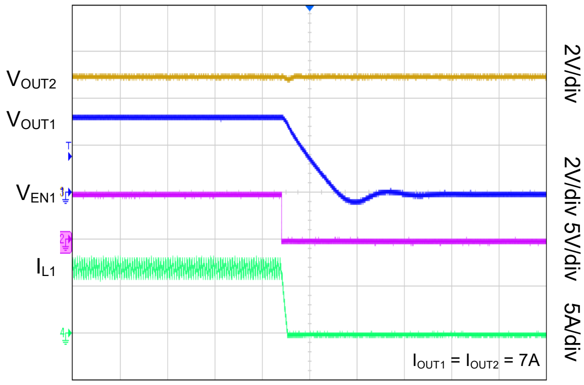
V_{IN} = 12V, V_{EN1} = V_{EN2} = 5V, f_{SW} = 400kHz, V_{OUT1} = 3.3V (FB1 to VDDA), V_{OUT2} = 5V (FB2 to GND), VCCX = V_{OUT2}, L = 3.3μH (DCR = 9.9mΩ), T_A = +25℃, unless otherwise noted.

Startup through EN1



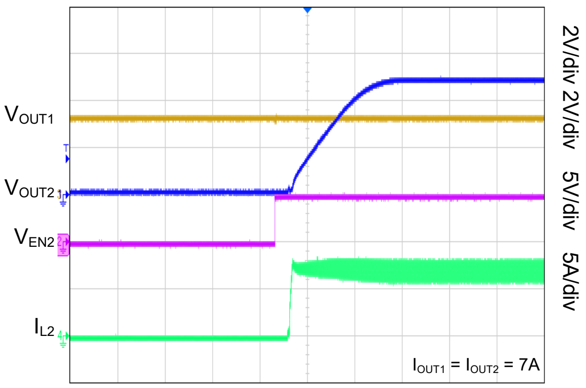
Time (1ms/div)

Shutdown through EN1



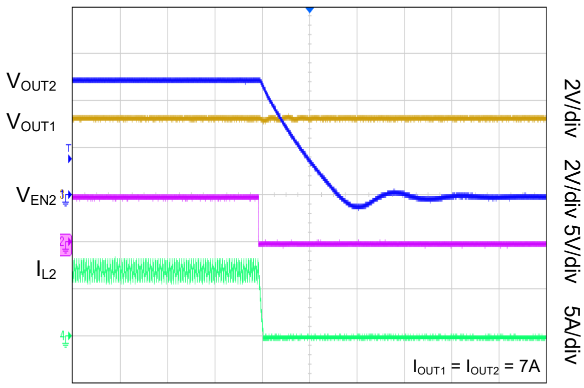
Time (50μs/div)

Startup through EN2



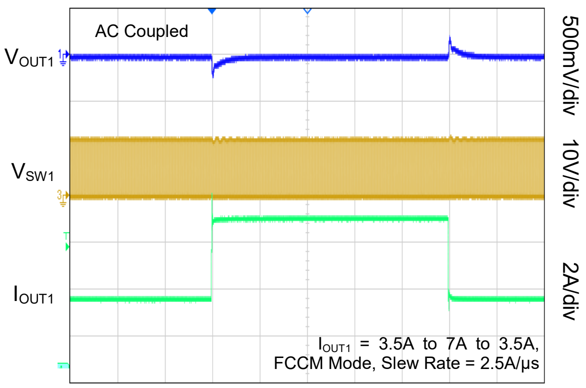
Time (1ms/div)

Shutdown through EN2



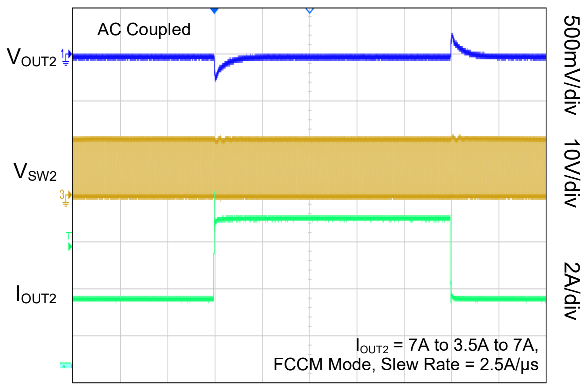
Time (50μs/div)

Load transient



Time (200μs/div)

Load transient

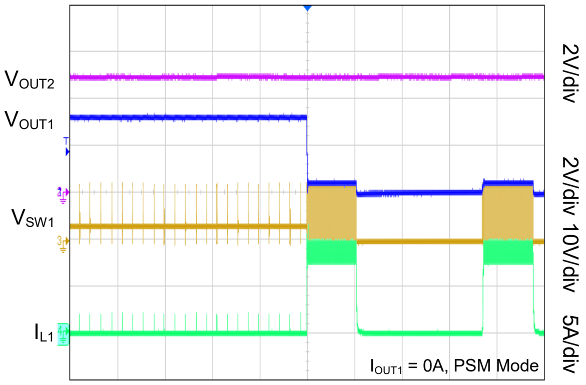


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

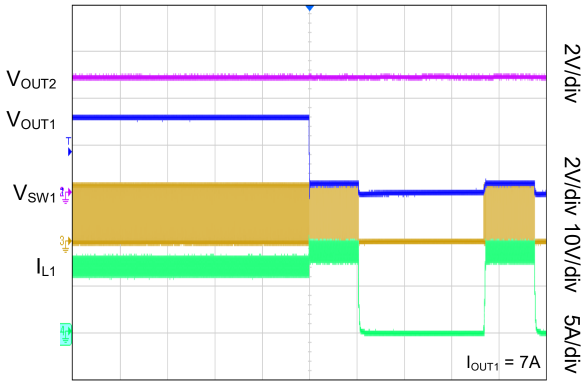
V_{IN} = 12V, V_{EN1} = V_{EN2} = 5V, f_{SW} = 400kHz, V_{OUT1} = 3.3V (FB1 to VDDA), V_{OUT2} = 5V (FB2 to GND), VCCX = V_{OUT2}, L = 3.3μH (DCR = 9.9mΩ), T_A = +25℃, unless otherwise noted.

SCP Entry



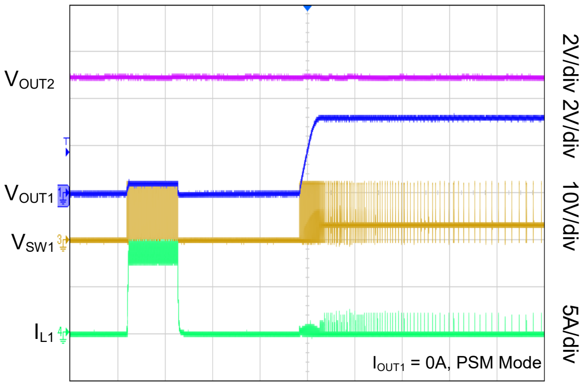
Time (5ms/div)

SCP Entry



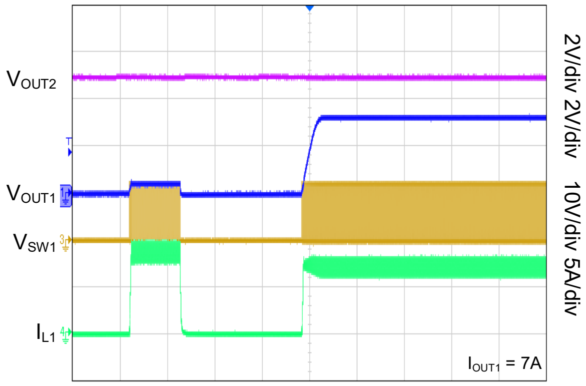
Time (5ms/div)

SCP Recovery



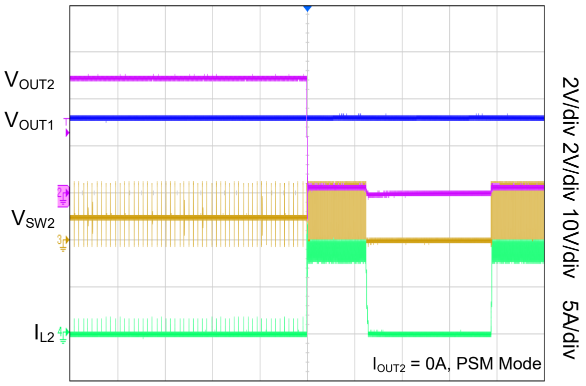
Time (5ms/div)

SCP Recovery



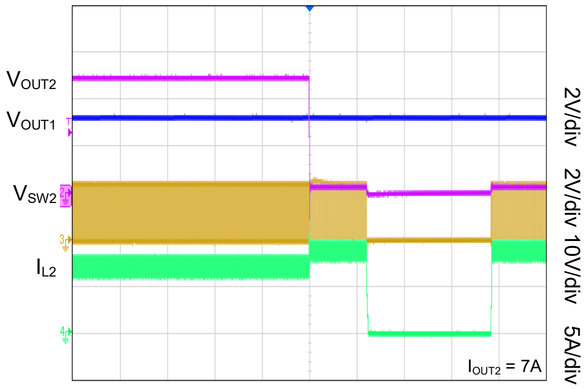
Time (5ms/div)

SCP Entry



Time (5ms/div)

SCP Entry

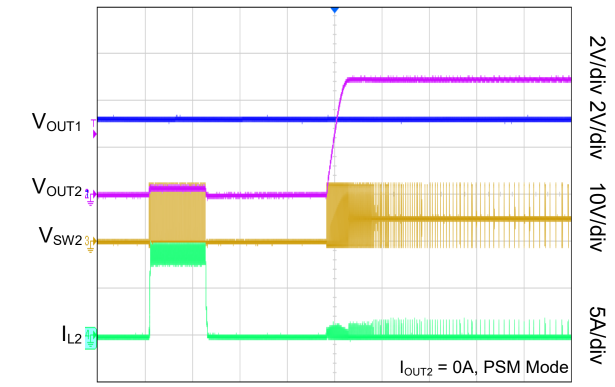


Time (5ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

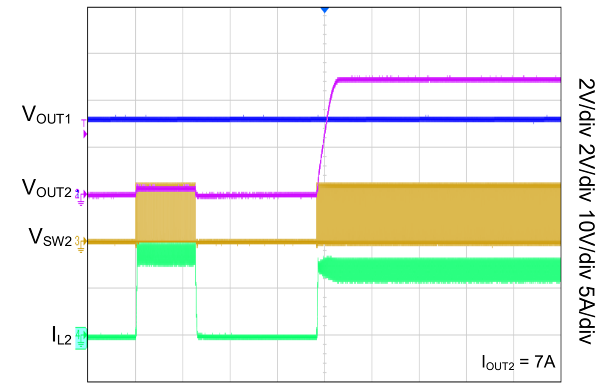
V_{IN} = 12V, V_{EN1} = V_{EN2} = 5V, f_{SW} = 400kHz, V_{OUT1} = 3.3V (FB1 to VDDA), V_{OUT2} = 5V (FB2 to GND), VCCX = V_{OUT2}, L = 3.3μH (DCR = 9.9mΩ), T_A = +25℃, unless otherwise noted.

SCP Recovery



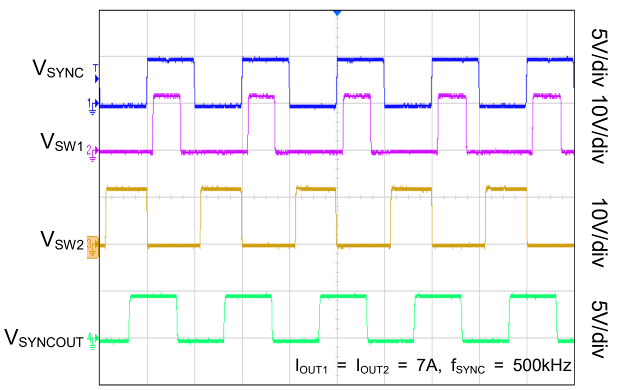
Time (5ms/div)

SCP Recovery



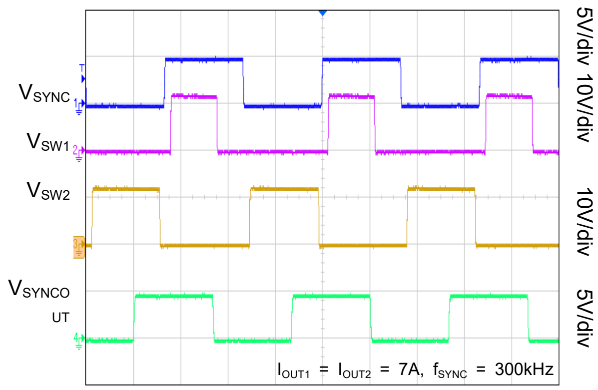
Time (5ms/div)

SYNCIN and SYNCOUT Function



Time (1μs/div)

SYNCIN and SYNCOUT Function



Time (1μs/div)

FUNCTIONAL BLOCK DIAGRAM

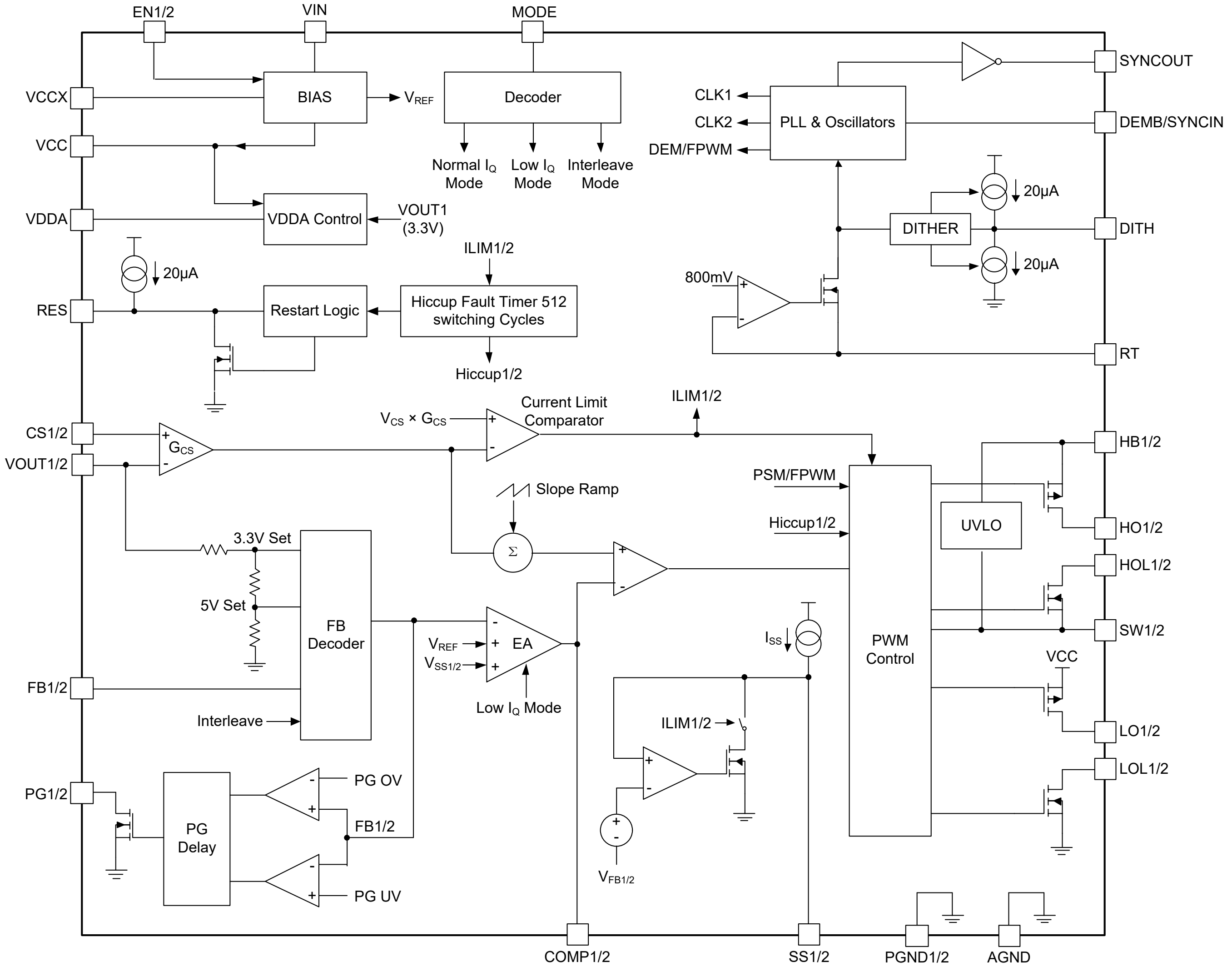


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM64620 is a wide input dual-channel controller for synchronous Buck converter using peak current mode control architecture and adjustable switching frequency. The SGM64620 can provide fixed 3.3V or 5V output voltage, or adjustable output voltage in range of 0.6V to 55V. It is capable to drive external N-MOSFETs efficiently over the whole voltage range.

A wide range of switching frequency from 100kHz to 2.2MHz can be programmed by RT pin. The switching frequency also can be synchronized to external signal up to 2.5MHz at DEMB pin. At light load, a selectable Power-Save Mode (PSM) control can improve the efficiency or FPWM control can decrease the output ripple. The external compensation network of COMP pin makes the loop design more flexible.

An external supply voltage can be connected to VCCX pin to improve the efficiency in high input voltage conditions. The SGM64620 provides protection features for fault events, such as over-current protection, UVLO and thermal shutdown. Optional spread spectrum frequency modulation (SSFM) technique can optimize the EMI and 180° interleaved phase of two channels can reduce the input current ripple.

Voltage Supply Regulator (VCC, VCCX, VDDA)

A VCC regulator from VIN is provided to supply for the PWM controller and the MOSFET gate drivers. When the input voltage falls below the VCC regulate value, then the VCC voltage will drop along with input voltage. At VIN power-up (EN1/2 > 2V), CH1 and CH2 are enabled if VCC voltage exceeds 3.37V (TYP). Then the CH1 and CH2 keep working until VCC voltage falls below the UVLO threshold (3.22V, TYP) or EN1 and EN2 are pulled down.

The SGM64620 has two VCC pins, SGMICRO recommends that the two VCC pins connect capacitor to PGND1 and PGND2 respectively, and must connect the two VCC pins together on the PCB. A 2.2μF to 10μF capacitor is recommended to connect from each VCC pin to PGND.

An internal regulator from VCC generates the VDDA, which provides the pull-up bias for SGM64620. A 0.47μF capacitor is recommended to connect from VDDA to GND. At the condition of V_{OUT1} is set to fixed 3.3V and CH2 is disabled, the VDDA is regulated to 3.3V if CH1 enters to sleep state in PSM mode.

The VCCX pin can be connected to a 5V bias (VOUT1 or VOUT2 or external 5V power supply) to reduce the internal linear regulator power dissipation. If VCCX pin voltage is higher than 4.3V (TYP), the VCC input from Vin is disabled and VCCX is supplied for VCC regulator. VCCX voltage must not be higher than 6.5V or less than -0.3V. If VCCX is not used, connect VCCX pin to AGND. If VCCX pin is connected to external DC bias, the input voltage must be higher than the external DC bias voltage during all conditions to avoid damaging the SGM64620.

Enable (EN1, EN2)

The SGM64620 contains two enable pins. EN1 controls the CH1 startup and shutdown, EN2 controls the CH2 startup and shutdown. The EN1/2 pins can be pulled up to VIN or a voltage higher than 2V to enable the CH1/2. If EN1 or EN2 pin voltage is less than 0.8V, the corresponding channel is disabled. If both CH1 and CH2 are disabled, the SGM64620 enters shutdown mode with a low I_Q (0.85μA, TYP). SGMICRO recommends not floating EN1 or EN2 pin during operation.

Power-Good Indicator

Two open-drain power-good outputs (PG1 and PG2) are included in SGM64620. It is recommended that the PG1 and PG2 pins are pulled up to VCC or an external 5V bias with 100kΩ resistor.

In the independent dual-output operation, the PG1 or PG2 is high level when V_{OUT1} or V_{OUT2} is in regulation voltage range. The PG1 or PG2 pin goes to low level when the corresponding output voltage (V_{OUT1} or V_{OUT2}) rises above 110% (TYP) or falls below 86.5% (TYP) regulation voltage.

In the single-output interleaved (two phase) operation, the PG2 pin maintains high-impedance state, this pin is not recommended for use as output voltage indicator signals. Only PG1 can be used as the output voltage indicator signal.

DETAILED DESCRIPTION (continued)

In the single-output multiphase (four phase) operation, the PG2 pin of master SGM64620 and PG1/2 pins of slave SGM64620 all maintain high-impedance state, these pins are not recommended for use as output voltage indicator signals. Only PG1 pin of master SGM64620 can be used as the output voltage indicator signal.

Switching Frequency

A range of 100kHz to 2.2MHz oscillation frequency is programmed by a resistor connected from RT pin to GND. CLK1 and CLK2 are the clock for CH1 and CH2 respectively. The CLK1 and CLK2 are 180° out of phase. The RT resistance is calculated by Equation 1 for a given switching frequency.

$$R_{RT}(k\Omega) = \frac{48000}{f_{SW}^{1.1}(kHz)} \quad (1)$$

The SGM64620 does not work if the RT pin floating and the switching is out of the normal frequency range if the RT pin is shorted to GND. Therefore, it is not recommended to leave the RT pin floating or short to GND.

Low Dropout Mode

SGM64620 includes a low dropout mode to minimize the converter dropout when input voltage is close to output voltage. If CH1 or CH2 is at low dropout mode, the duty cycle is kept at maximum as much as bootstrap UVLO voltages allows. The off-time must be sufficient to recharge the bootstrap capacitor such that the bootstrap voltage remains above its UVLO voltage. If it falls below UVLO the high-side switch (HS) is turned off and the low-side switch (LS) is turned on to recharge the bootstrap capacitor. After the recharge, the HS is turned again to regulate the output voltage.

In low dropout mode, the phase between CH1 and CH2 is not 180°. The maximum on-time of HS is 8 clock period set by RT resistor. The lower the clock frequency, the longer the maximum on-time of HS.

PSM Mode

An optional power-save mode (PSM) is provided in SGM64620 to improve the light efficiency. This option can be enabled by connecting DEMB pin to AGND. In PSM mode with heavy load current, the SGM64620 continues operation like PWM. With the load decreases, the SGM64620 first enters no-synchronous operations without frequency reduction in which the low-side switch turns off when inductor current reaches zero in each cycle. If the load is further decreased to very light load, the switching frequency decreases when the V_{COMP} falls below the internal PSM voltage threshold in which time the internal clock is masked. A new cycle starts when the V_{COMP} exceeds the PSM threshold. With the load gets heavier, if the V_{COMP} is fully higher than the PSM threshold, the SGM64620 will operate with fixed frequency again.

If a forced PWM (FPWM) mode is desired in light load or no load, connect DEMB pin to VDDA to enable FPWM. Figure 3 and Figure 4 show the FPWM and PSM waveform at different load condition.

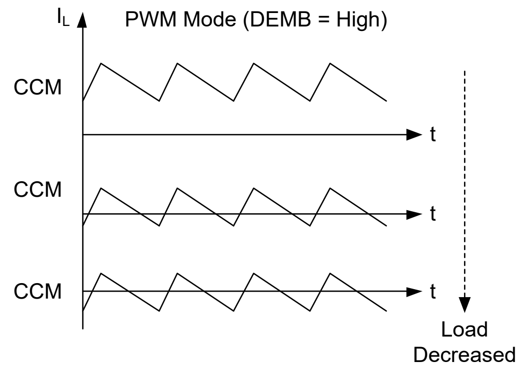


Figure 3. Converter Operation with Forced PWM (PSM Disabled)

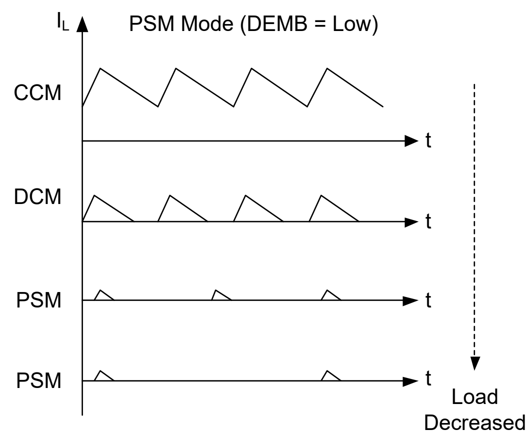


Figure 4. Converter Operation with PSM Enabled

DETAILED DESCRIPTION (continued)

Synchronization (SYNC Input)

The SGM64620 can be synchronized to an external PWM signal (higher than 2V) at DEMB pin. The range of synchronized frequency is ±20% of the programmed frequency set by RT resistor and the maximum synchronized frequency is 2.5MHz. The RT resistor is ignored if there is external PWM signal connected to DEMB pin. At low VIN condition, if the mini-off-time is triggered, the switching frequency will not be synchronized to external PWM signal.

Synchronization Output (SYNCOUT)

The SYNCOUT output is a 50% duty signal and the frequency is the same as CLK1 and CLK2 if mini-off-time is not triggered. The SYNCOUT rising edge is 90° lagging CLK2 or 90° leading CLK1. When the SYNCOUT is used to second SGM64620 controller, all four channels clock is 90° out of phase. When both CH1 and CH2 enter sleep state, the SYNCOUT stops outputting.

Spread Spectrum Frequency Modulation

To optimize EMI performance, the SGM64620 provides a frequency spectrum frequency option. It can be enabled by connecting a capacitor (C_{DITH}) from DITH pin to GND, as shown in Figure 5. The internal source and sink current charge or discharge the capacitor repeatedly to generate a triangular ramp waveform between 1.15V and 1.25V on DITH pin. The triangular DITH voltage modulates the internal clock frequency by ±5% of the frequency set by RT resistor.

Use Equation 2 to calculate the DITH capacitance for spread spectrum frequency (f_{MOD}):

$$C_{DITH} = \frac{20\mu A}{2 \times f_{MOD}(Hz) \times 0.1V}(\mu F) \quad (2)$$

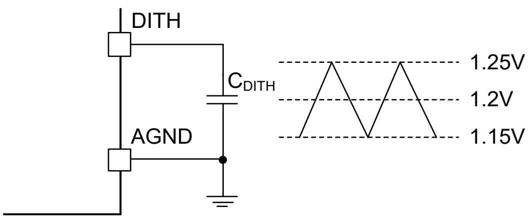


Figure 5. Switching Frequency Dithering

If DITH is connected to VDDA before startup, the DITH feature is disabled until DITH pin is removed from VDDA. If DITH is connected to GND before startup, the DITH feature is also disabled, the C_{DITH} is prevented from charging or discharging. Also, the DITH feature is disabled when the SGM64620 is synchronized to an external signal.

Soft-Start (SS1, SS2)

Soft-start feature is necessary to have a smooth start without over-current, output voltage over-shoot. The SGM64620 has the soft-start feature which makes the output voltage rise up smoothly during power-up. Soft-start is implemented by a ramp voltage which rises slowly from 0V to 0.6V and replaces the V_{REF} during startup for the output voltage regulation. During startup, the internal source current charges the soft-start capacitor connected to SS pin. Use Equation 3 to calculate the soft-start time capacitance:

$$C_{SS}(nF) = 35 \times t_{SS}(ms) \quad (3)$$

SGMICRO does not recommend pulling the SS pin low during operation. In PSM mode, if SS1 or SS2 pin is pulled low by external circuit, the CH1 or CH2 stops switching. In FCCM mode, if SS1 or SS2 pin is pulled low by external circuit, a large negative inductor current occurs to discharge output capacitor.

Output Voltage Setting (FB1, FB2)

The SGM64620 output voltages can be set fixed voltage (5V or 3.3V) without external divider resistor or adjustable desired voltage with divider resistor. VOUT1 and VOUT2 are configured as 3.3V output when FB1 and FB2 pins are pulled up to VDDA before power-up. VOUT1 and VOUT2 are configured as 5V output when FB1 and FB2 pins are pulled up to AGND before power-up. The FB1 and FB2 pins connections (VDDA or AGND) are detected during power-up. The FB1 and FB2 settings are latched and cannot be changed until VIN powers down and VCC falls below its UVLO threshold and then VIN powers up again.

The SGM64620 output voltages also can be configured using external divider resistors as shown in Figure 6. The adjustable output voltage range is 0.6V to 55V. Use Equation 4 to calculate the divider resistors for a desired output voltage ($V_{OUT1/2}$).

$$R_{FB1} = (\frac{V_{OUT}}{V_{REF}} - 1) \times R_{FB2} \quad (4)$$

DETAILED DESCRIPTION (continued)

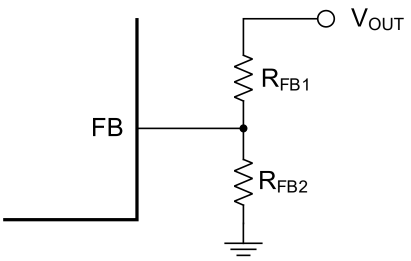


Figure 6. Output Voltage ($V_{OUT1/2}$) Setting

SGMICRO recommends the equivalent impedance of the divider resistor must be greater than 5kΩ to detect for setting the channel in adjustable output voltage mode such as Equation 5.

$$R_{EQU} = \frac{R_{FB1} \times R_{FB2}}{R_{FB1} + R_{FB2}} > 5k\Omega \quad (5)$$

If a low I_Q mode is required, take care of selecting the external divider resistor, too small resistance results in a large power loss.

Transconductance Error Amplifier (EA1, EA2)

The SGM64620 has two independent high-gain transconductance amplifiers. Each channel, the difference between V_{FB} and V_{REF} (0.6V) is amplified to an output current signal at COMP pin. This current is injected in the compensation network to generate the V_{COMP} control signal that determines the inductor current by controlling duty cycle.

The amplifier has two gain setting (1200µS and 125µS). If MODE pin is connected to GND, the SGM64620 operates in normal mode with gm is 1200µS. By connecting MODE pin to GND through a 10kΩ resistor, the SGM64620 operates in ultra-low I_Q mode with gm is 125µS.

Inductor Current Sense (CS1, VOUT1, CS2, VOUT2)

Accurate current sense is important for peak current mode control mode. For the SGM64620 controller, there are two methods to sense the inductor current. One is using a current sense resistor (shunt) in series with the inductor, and the other is via the inductor DCR current sensing.

Shunt Current Sensing

Figure 7 shows the shunt current sensing inductor current structure. The shunt resistor monitors the inductor current in real time. SGMICRO recommends selecting a shunt resistor with low inductance and high precision, which is connected to SGM64620 CS and VOUT pins with a Kelvin connection.

If the different voltage between CS1/2 and VOUT1/2 pins exceeds V_{CS}, the current limit comparator immediately turns off the high side HO output signal for current limiting. Use Equation 6 to calculate the shunt resistance.

$$R_S = \frac{V_{CS}}{I_{OUT\_CL} + \Delta I_L / 2} \quad (6)$$

Where:

- V_{CS} is the current limit sense threshold.
- I_{OUT_CL} is the over current setpoint that is higher than maximum load current.
- ΔI_L is the peak-to-peak inductor ripple current.

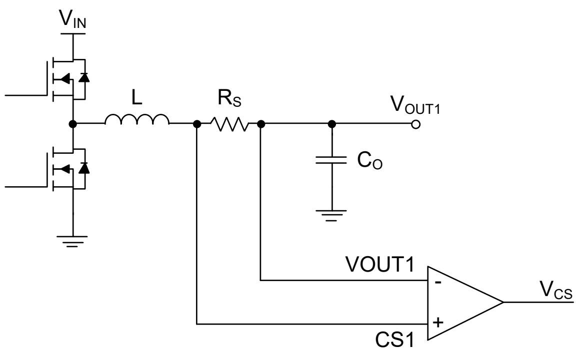


Figure 7. Shunt Current Sensing Implementation

Inductor DCR Current Sensing

For applications requiring the highest possible efficiency at high load currents, the SGM64620 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 8.

Use Equation 7 to calculate the voltage across the sense capacitor C_{CS}. When the $R_{CS}C_{CS} = L/R_{DCR}$, the sensed voltage of C_{CS} is a replica of the inductor DCR voltage and accurate inductor current sensing is achieved.

If the $R_{CS}C_{CS} < L/R_{DCR}$, the sense DC voltage is accurate, but AC voltage of C_{CS} is greater than the AC voltage of DCR.

If the $R_{CS}C_{CS} > L/R_{DCR}$, the sense DC voltage is accurate, but AC voltage of C_{CS} is less than the AC voltage of DCR.

DETAILED DESCRIPTION (continued)

$$V_{CS}(s) = I_L(s) \times R_{DCR} \times \frac{(1 + s \times L / R_{DCR})}{(1 + s \times R_{CS} \times C_{CS})} \quad (7)$$

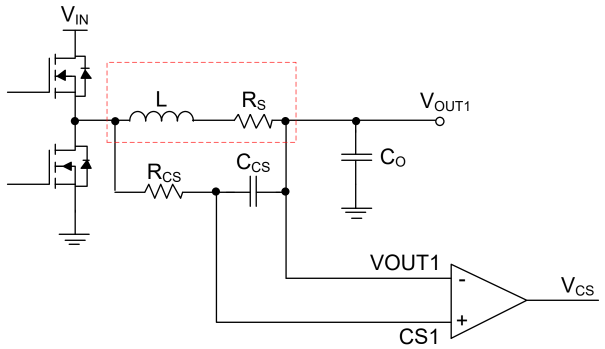


Figure 8. Inductor DCR Current Sensing Implementation

SGMICRO recommends selecting a capacitor (C_{CS}) greater than 0.1μF to maintain a low-independence sensing network. The C_{CS} is connected to CS and VOUT pins with a Kelvin connection.

Hiccup Mode Current Limiting (RES)

The SGM64620 provides an optional hiccup mode over current protection when a capacitor (C_{RES}) is connected from RES pin to GND. In normal mode, RES capacitor is discharged to GND. When an over-current event occurs at the output, the output voltage drops. If the FB voltage falls below 0.2V and the current limit is triggered 512 times consecutively, the SS pin is pulled low and the HO and LO gate outputs are disabled. Then, a source current charges the C_{RES}. When the voltage of C_{RES} exceeds 1.15V, the HO and LO gate outputs are enabled again, and SS capacitor begins to charge. If output short condition still exists, after 512 switching cycles of cycle-by-cycle current limit is triggered, the RES and SS capacitor is discharged simultaneously and RES is charged again, as shown in Figure 9.

The 512 switching cycles hiccup count is reset if 4 consecutive switching cycles occur without exceeding the current limit. The SGM64620 provides separate hiccup count for each channel, but the RES pin is shared for both channels. One channel can be in hiccup mode and the other channel is in normal. If both channels are in short condition, the last hiccup count to expire pulls RES low and charges the RES capacitor. Then both channels restart together when RES pin voltage exceeds 1.15V. If RES pin is connected to VDDA before power-up, the hiccup mode protection is disabled for both channels.

Use Equation 8 to calculate the RES capacitance,

$$C_{RES}(nF) = 17.4 \times t_{RES}(ms) \quad (8)$$

t_{RES} is hiccup no switching time, as shown in Figure 9.

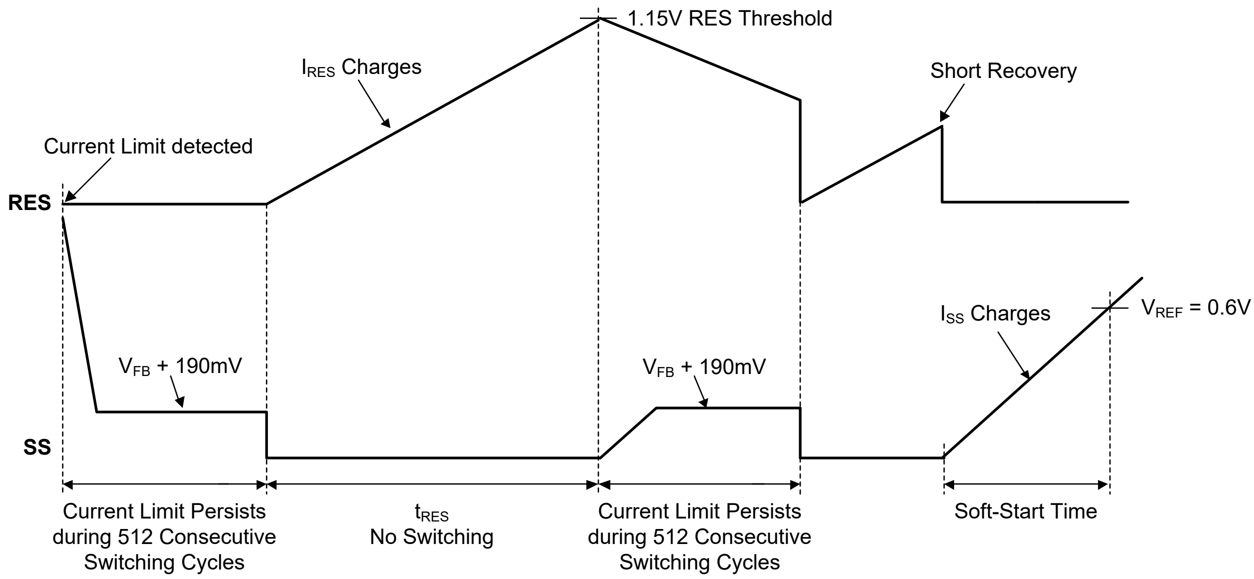


Figure 9. Hiccup Mode Timing Diagram

DETAILED DESCRIPTION (continued)

Gate Drivers and Bootstrap Charging

The SGM64620 contains gate drivers to drive the external N-MOSFETs, the high-side floating gate drivers are power by external bootstrap capacitors (C_{BOOT}). When the high-side MOSFET is off and low-side MOSFET is on, the C_{BOOT} is charged from VCC through external diode. A 0.1μF ceramic capacitor is recommended to be connected between HB1/2 and SW1/2 pins. The floating gate driver has its own UVLO protection, if C_{BOOT} voltage falls below the UVLO threshold, the low-side MOSFET turns on to refresh the C_{BOOT}.

To optimize the EMI performance, a 0Ω ~ 10Ω resistor (R_{BOOT}) can be connected in series with C_{BOOT} to adjust the turn-on driving speed of the high-side MOSFET. Alternatively, a resistor can be connected in series between the driving output pin and the gate of the MOSFET to adjust the turn-on and turn-off speeds of the MOSFET, such as $R_{HO1/2}$, $R_{HOL1/2}$, $R_{LO1/2}$, $R_{LOL1/2}$.

Output Configurations (MODE, FB1, FB2)

Independent Dual-Output Operation

The SGM64620 can provide both channels independently fixed 3.3V or 5V output voltage, or adjustable output voltage in range of 0.6V to 55V.

Table 1 and Figure 10 show the independent dual-outputs operation configurations.

Table 1. Independent Dual-Outputs Voltage Configurations

VOUT1	FB1 Connected to	VOUT2	FB2 Connected to	MODE Connected to	Error Amplifier gm
3.3V	VDDA	3.3V	VDDA		
5V	AGND	5V	AGND		
3.3V	VDDA	5V	AGND	AGND	1200μS
5V	AGND	3.3V	VDDA		
0.6V to 55V	R_{FB1}, R_{FB2} Divider	0.6V to 55V	R_{FB1}, R_{FB2} Divider		
3.3V	VDDA	3.3V	VDDA		
5V	AGND	5V	AGND		
3.3V	VDDA	5V	AGND	10kΩ to AGND	125μS
5V	AGND	3.3V	VDDA		
0.6V to 55V	R_{FB1}, R_{FB2} Divider	0.6V to 55V	R_{FB1}, R_{FB2} Divider		

DETAILED DESCRIPTION (continued)

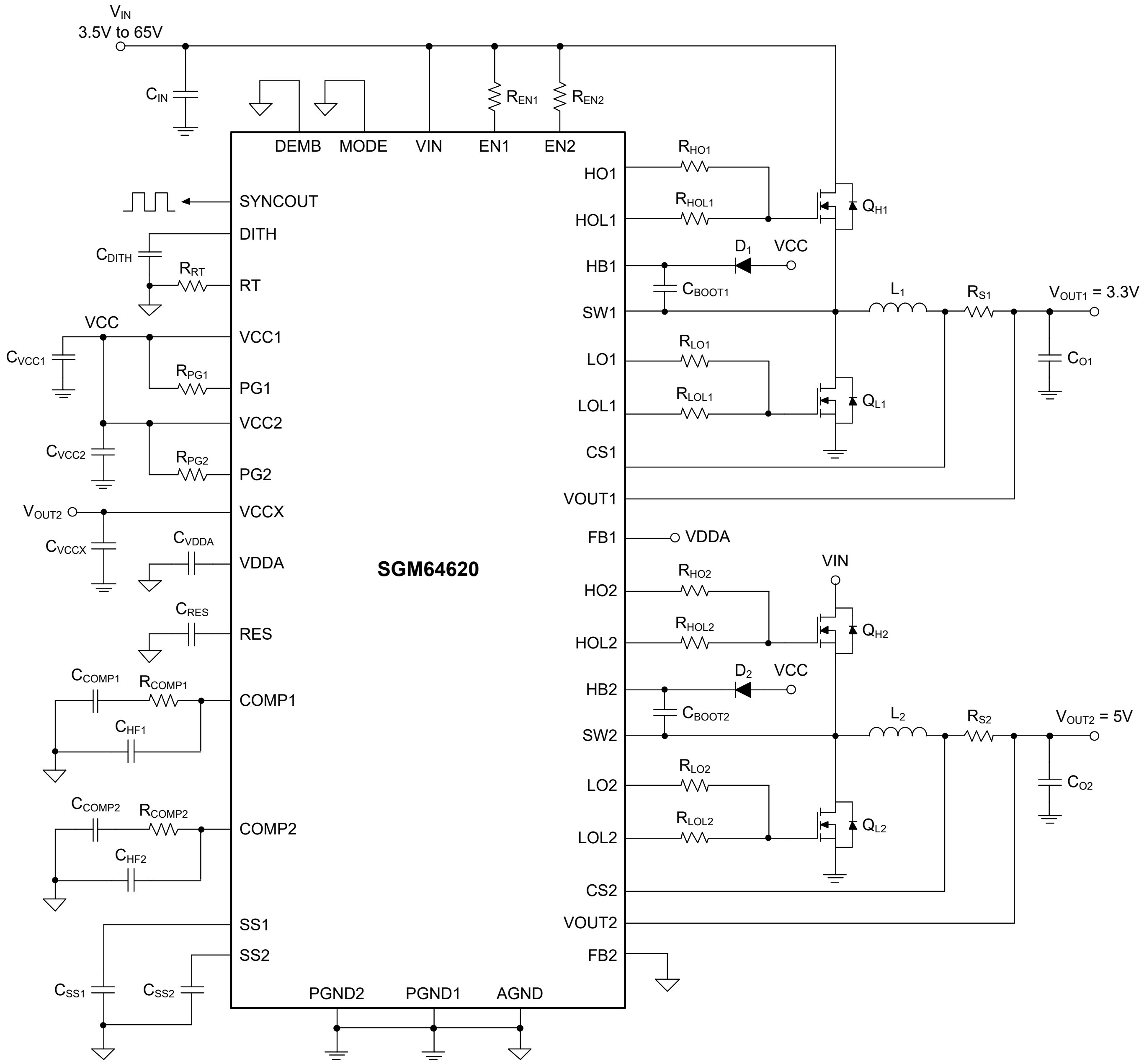


Figure 10. Independent Dual-Outputs Configurations Simplified Schematic

DETAILED DESCRIPTION (continued)

Single-Output Interleaved Operation

The SGM64620 can be set as single-output interleaved operations. In this operation, connect FB2 pin to AGND, MODE pin to VDDA, short SS1 and SS2, short COMP1 and COMP2 together. In single-output interleaved operation, the channel 2 error amplifier is disabled and PG2 maintains high-impedance state. Therefore, it is recommended to use PG1 as the output voltage indicator signal and leave PG2 floating. Table 2 and Figure 11 show the single-output interleaved configurations.

Table 2. Single-Output Interleaved Configurations

V_{OUT}	FB1	FB2	MODE
3.3V	VDDA	AGND	VDDA
5V	AGND		
0.6V to 55V	R_{FB1}, R_{FB2} Divider		

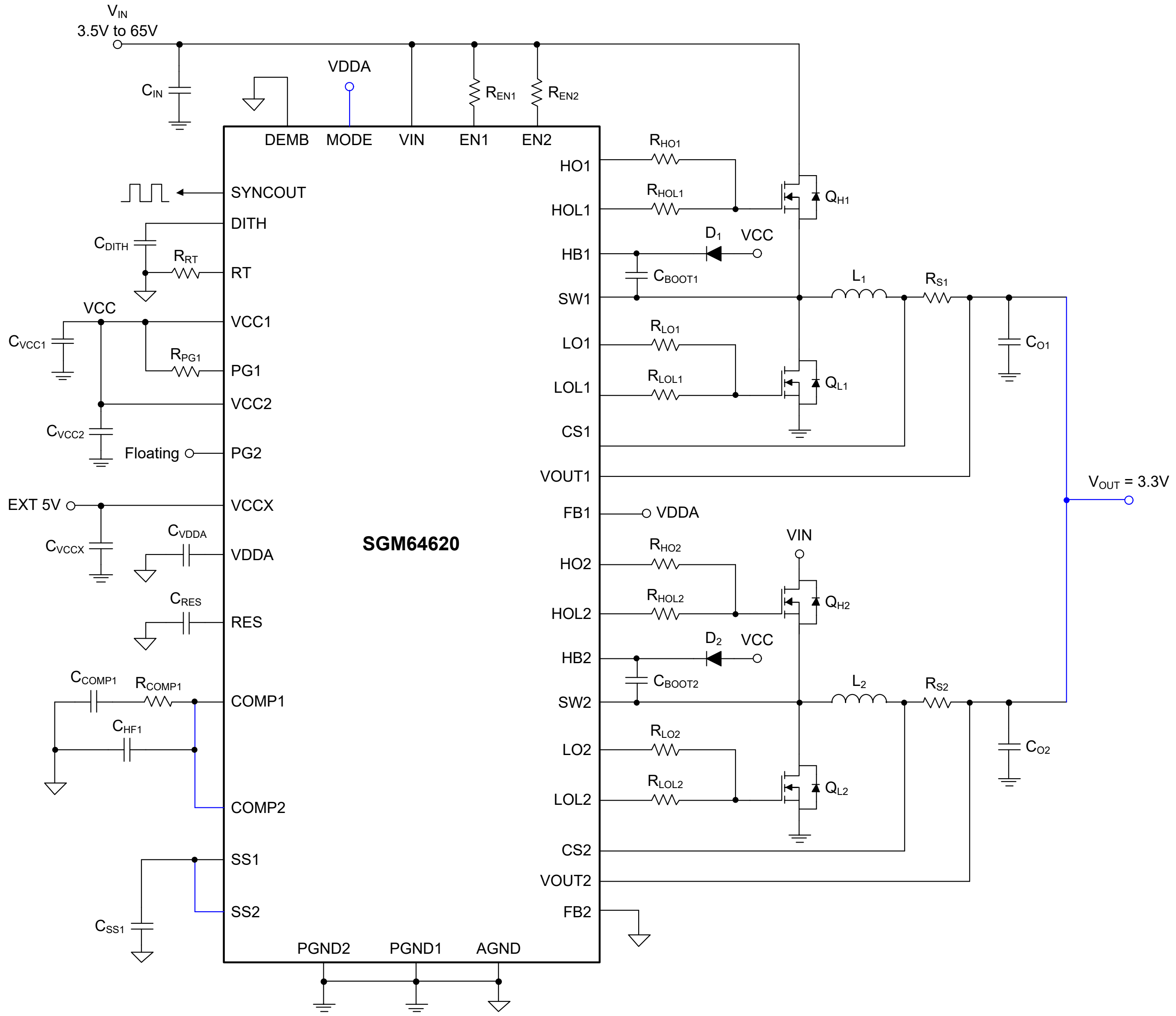


Figure 11. Single-Output Interleaved Configuration Simplified Schematic

DETAILED DESCRIPTION (continued)

Single-Output Multiphase Operation

The SGM64620 also can be set as multiphase (four-phase) operation for large output current requirements. Configure the first SGM64620 as master device and second SGM64620 as slave device.

First connect the FB2 pin to AGND and MODE pin to VDDA of master device, this operation disables the master device's channel 2 error amplifier and maintains PG2 pin to high-impedance state. Then connect the FB2 and MODE pins of slave device to VDDA, this operation disables the slave device both channels error amplifier and maintains PG1 and PG2 pins to high-impedance state.

Then short COMP1 and COMP2 pins of master and slave device together. Short SS1 and SS2 pins of master and slave device together. Connect SYNCOUT pin of master device to DEMB pin of slave device as the clock synchronization signal. The switching frequency is determined by RT of master device. The RT of slave device is only used for slope compensation. It is recommended to select the same RT resistor.

In the four-phase operation mode, only the PG1 pin of the master device can serve as the output voltage indicator signal. PG2 of the master device, along with PG1 and PG2 of the slave device, will remain at a high-impedance state. Therefore, it is recommended to leave these pins floating.

Connecting FB1 pin of slave device to AGND or VDDA determines the light mode (PSM or FPWM) of slave device. The light mode of master device is determined by connecting its DEMB pin to AGND or VDDA. SGMICRO recommends setting the master and slave devices to the same light mode (PSM or FPWM).

Table 3 and Figure 12 show the single-output multiphase configurations.

Thermal Shutdown

To protect the device from overheating damage, the junction temperature is constantly monitored and if it reaches the +175℃ limit, the device will shut down. It will automatically recover normal operation with a soft-start when the die temperature falls below +155℃ (TYP). If the thermal shutdown occurs, the VDDA regulator is turned off and VCC regulator keeps on.

Table 3. Single-Output Multiphase Configurations

MODE (Master and Slave)	FB2 (Master)	FB2 (Slave)	V_{OUT}	FB1 (Master)	FB1 (Slave)	Light Mode
VDDA	AGND	VDDA	3.3V	VDDA	AGND	PSM
			3.3V	VDDA	VDDA	FPWM
			5V	AGND	AGND	PSM
			5V	AGND	VDDA	FPWM

DETAILED DESCRIPTION (continued)

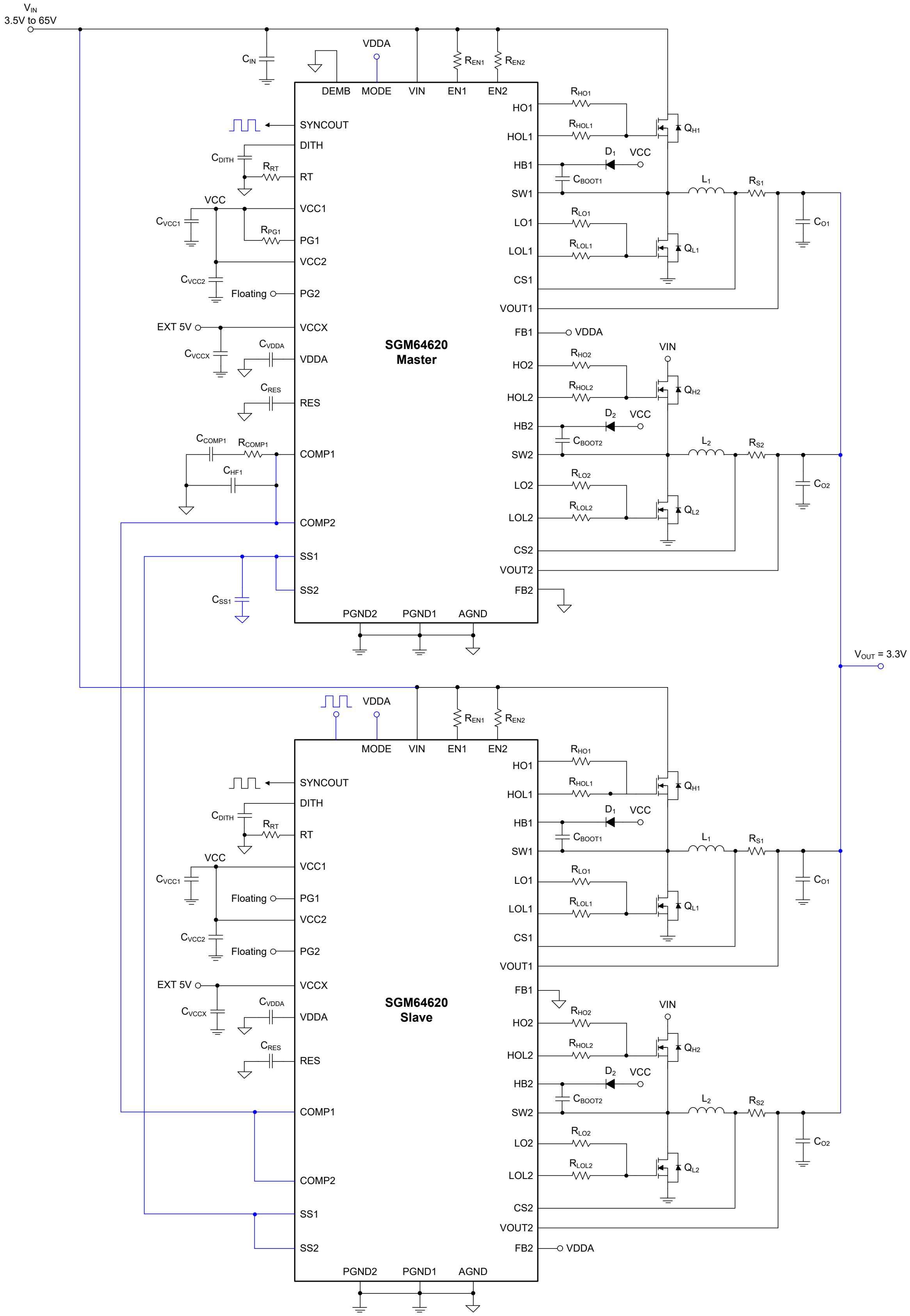


Figure 12. Single-Output Multiphase Interleaved Configuration Simplified Schematic

APPLICATION INFORMATION

The SGM64620 is dual-channel synchronous Buck controller using a peak current mode control architecture. This device supports fixed 3.3V or 5V output voltage or adjustable output voltage. The following section can be used to select the external components for SGM64620.

Inductor

The inductor selection is usually important for a Buck converter, too large or too small is inappropriate. Usually, selecting the ripple current of inductor (ΔI_L) between 20% and 40% of output current at typical V_{IN} and V_{OUT} condition. And the selected inductor DC current rating should be at least 25% above the maximum output current. The saturation current of selected inductor should be higher enough than the current limit. Use Equation 9 to calculate the inductance.

$$L = \frac{V_{OUT}}{\Delta I_L \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

The maximum inductor peak current for a given load current (I_{LOAD}) is calculated by Equation 10:

$$I_{L\_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (10)$$

Input Capacitor (C_{IN})

The input capacitor is necessary to reduce the converter input voltage ripple due to the high switching frequency. The selected capacitors must have the enough RMS current rating to absorb all AC current on the input. Equation 11 can be used to calculate the input capacitor current ripple.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad (11)$$

The worst case occurs at only one channel works at 50% duty cycle where $V_{IN} = 2 \times V_{OUT}$.

Output Capacitor (C_{OUT})

The output capacitor is designed based on the required output voltage ripple, stability, and transient response peaks and settling times. C_{OUT} impedance must be lower than the load at the switching frequency. The output voltage ripple is estimated from Equation 12:

$$\Delta V_{OUT} \approx \frac{V_{OUT}}{L \times f_{SW}} \times (1 - D) \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_{SW}}) \quad (12)$$

R_{ESR} is the equivalent series resistance (ESR) of the output capacitor. For tantalum or electrolytic capacitors, the ESR is high and dominates the capacitor impedance at the switching frequency, so, the ripple can be approximated by Equation 13 for high ESR capacitors:

$$\Delta V_{OUT} \approx \frac{V_{OUT}}{L \times f_{SW}} \times (1 - D) \times R_{ESR} \quad (13)$$

Compensation Network

The SGM64620 is a current mode controller simplifies compensation and provides faster transient response compared to the voltage mode control. The COMP1 and COMP2 pins are the error amplifier outputs and control stability and loop response of both channels. For each channel, a series RC network sets a pole-zero combination and determines control loop characteristics. The DC gain of the voltage feedback loop is shown in Equation 14:

$$A_{VDC} = R_{LOAD} \times G_S \times A_O \times \frac{V_{FB}}{V_{OUT}} \quad (14)$$

Where A_O = 3160V/V (70dB) is the error amplifier voltage gain, G_S is the current sense transconductance ($1/(11.5 \times R_{SENSE})$), and R_{LOAD} is the load resistance.

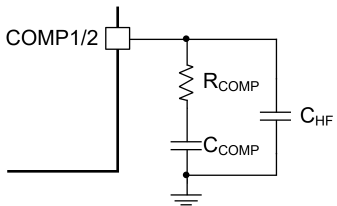


Figure 13. SGM64620 External Compensation

For SGM64620 each channel, the Buck system has three poles. One is determined by the converter and load (C_{OUT} and R_{LOAD}) as given in Equation 15, the other two are determined by the RC compensation network, as given in Equation 16 and 17.

$$f_{P1} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}} \quad (15)$$

$$f_{P2} = \frac{gm}{2\pi \times C_{COMP} \times A_O} \quad (16)$$

$$f_{P3} = \frac{1}{2\pi \times R_{COMP} \times C_{HF}} \quad (17)$$

APPLICATION INFORMATION (continued)

Where gm is the error amplifier transconductance, R_{LOAD} is the load resistance and C_{OUT} is the output capacitance.

The system has two zeros, one is determined by the ESR of output capacitor, as given in Equation 18. The other is determined by the RC compensation network (R_{COMP} and C_{COMP}), as given in Equation 19.

$$f_{Z1} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \quad (18)$$

$$f_{Z2} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \quad (19)$$

The main goal of the compensation network is to adjust the shape of the converter transfer function to get a desired loop gain. The crossover frequency is an important factor that determines the bandwidth (how fast is the converter transient response). Setting the crossover at a too high frequency, results in instability. Usually, the crossover frequency is initially set to around 10% of the switching frequency (0.1 × f_{SW}), and then the following steps are taken to design the compensation network with the sufficient phase margin:

1. Select the R_{COMP} based on the desired crossover frequency (f_C) value:

$$R_{COMP} = \frac{2\pi \times C_{OUT} \times f_C}{gm \times G_S} \times \frac{V_{OUT}}{V_{FB}} \quad (20)$$

2. Select C_{COMP} to get sufficient phase margin. Placing the f_{Z2} at around 0.25 × f_C would be sufficient and C_{COMP} can be calculated using Equation 21.

$$C_{COMP} = \frac{4}{2\pi \times R_{COMP} \times f_C} \quad (21)$$

3. If ESR zero is located below $f_{SW}/2$, as shown in Equation 22, selecting the C_{HF} f_{P3} at the ESR zero (f_{Z1}) location, the C_{HF} can be calculated at Equation 23.

$$\frac{1}{2 \times \pi \times C_{OUT} \times R_{ESR}} < \frac{f_{SW}}{2} \quad (22)$$

$$C_{HF} = \frac{C_{OUT} \times R_{ESR}}{R_{COMP}} \quad (23)$$

If output capacitor is ceramic capacitor, the ESR is very small. The f_{Z1} is far greater than the f_{SW}. In this case, the C_{HF} is not needed or choose a small value C_{HF} which the f_{P3} is at high frequency location.

Power MOSFET Selection

The MOSFET's V_{DS}, I_{DS}, Q_G, R_{DSON} are the critical parameters during choosing the main power MOSFET for SGM64620. First, the V_{DS} must be higher than the maximum SW node voltage, and the I_{DS} is higher than the MOSFET RMS current during operation. Normally, the lower R_{DSON} of a MOSFET, the higher total gate charge Q_G. When the MOSFET has higher V_{DS}, the Q_G × R_{DSON} is larger.

If Q_G is too large and the switching speed is too slow, the SGM64620 may not turn on the MOSFET successfully finally. SGMICRO recommends choosing appropriate Q_G and R_{DSON} for a best efficiency at different applications.

Current Sense Resistor Selection

The shunt resistor (R_{CS}) is connected in series with inductor to sense the inductor current. When the current sensing information exceeds the V_{COMP}, the high-side switch turns off. To avoid the current limit being triggered falsely at normal operation, the shunt resistor should not be too large. The Equation 24 is used to calculate the R_{CS}.

$$R_{CS} = \frac{V_{LIMIT}}{I_{L\_PEAK}} \quad (24)$$

Where V_{LIMIT} is the current limit threshold, I_{L_PEAK} is the inductor peak current limit.

APPLICATION INFORMATION (continued)

Typical 3.3V and 5V, 400kHz Dual-Output Buck Converter Applications

Figure 14 shows a typical application circuit: 3.3V and 5V dual-output and 7A load current for each channel. The switching frequency is 400kHz programmed by RT resistor. The VCCX is connected to 5V output to improve the efficiency.

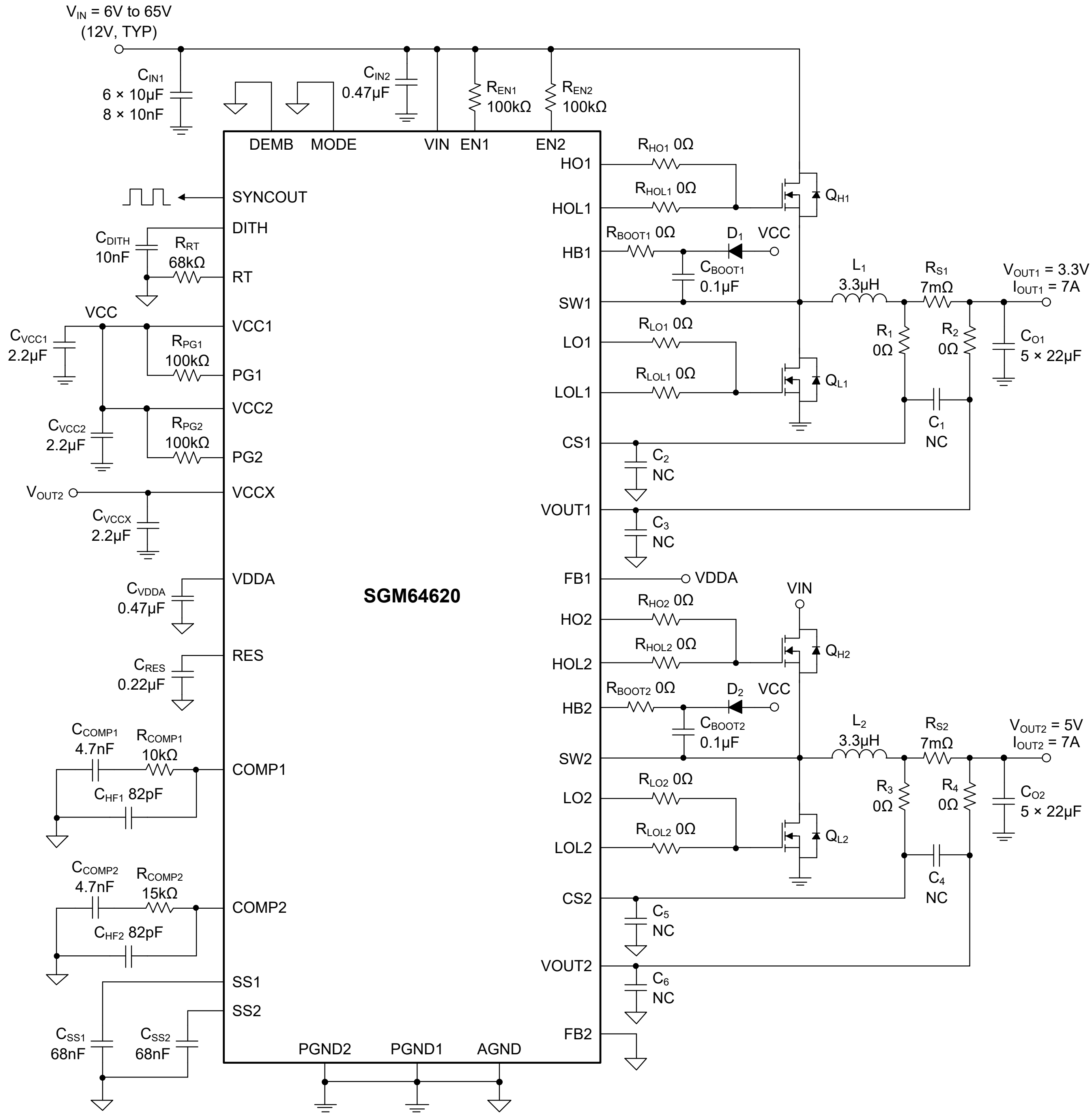


Figure 14. Application Circuit for 3.3V and 5V Dual-Output with 400kHz

APPLICATION INFORMATION (continued)

Typical Two-Phase 5V/15A, 400kHz Single-Output Buck Converter Applications

Figure 15 shows an application circuit: two-phase 5V single-output with 15A load current. The switching frequency is 400kHz programmed by RT resistor. The VCCX is connected to 5V output to improve the efficiency. The output voltage also can be set to 3.3V by connecting FB1 to VDDA.

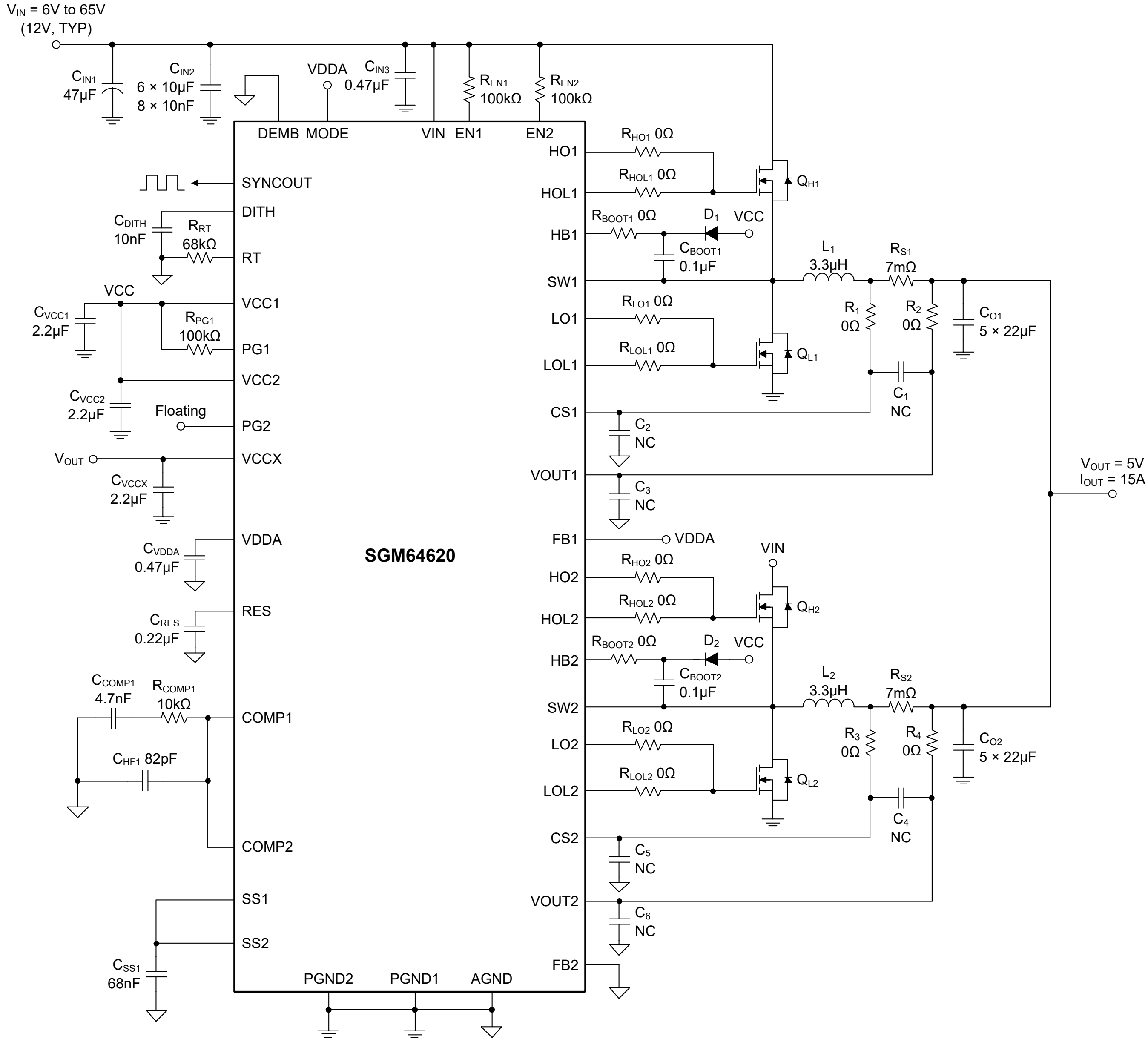


Figure 15. Application Circuit for Two-Phase 5V Single-Output with 400kHz

APPLICATION INFORMATION (continued)

Typical Two-Phase 3.3V/40A, 400kHz Single-Output Buck Converter Applications

Figure 16 shows an application circuit: two-phase 3.3V single-output with 40A load current, meeting the requirements of high-current applications. The switching frequency is 400kHz programmed by RT resistor. The output voltage also can be set to 5V by connecting FB1 to GND.

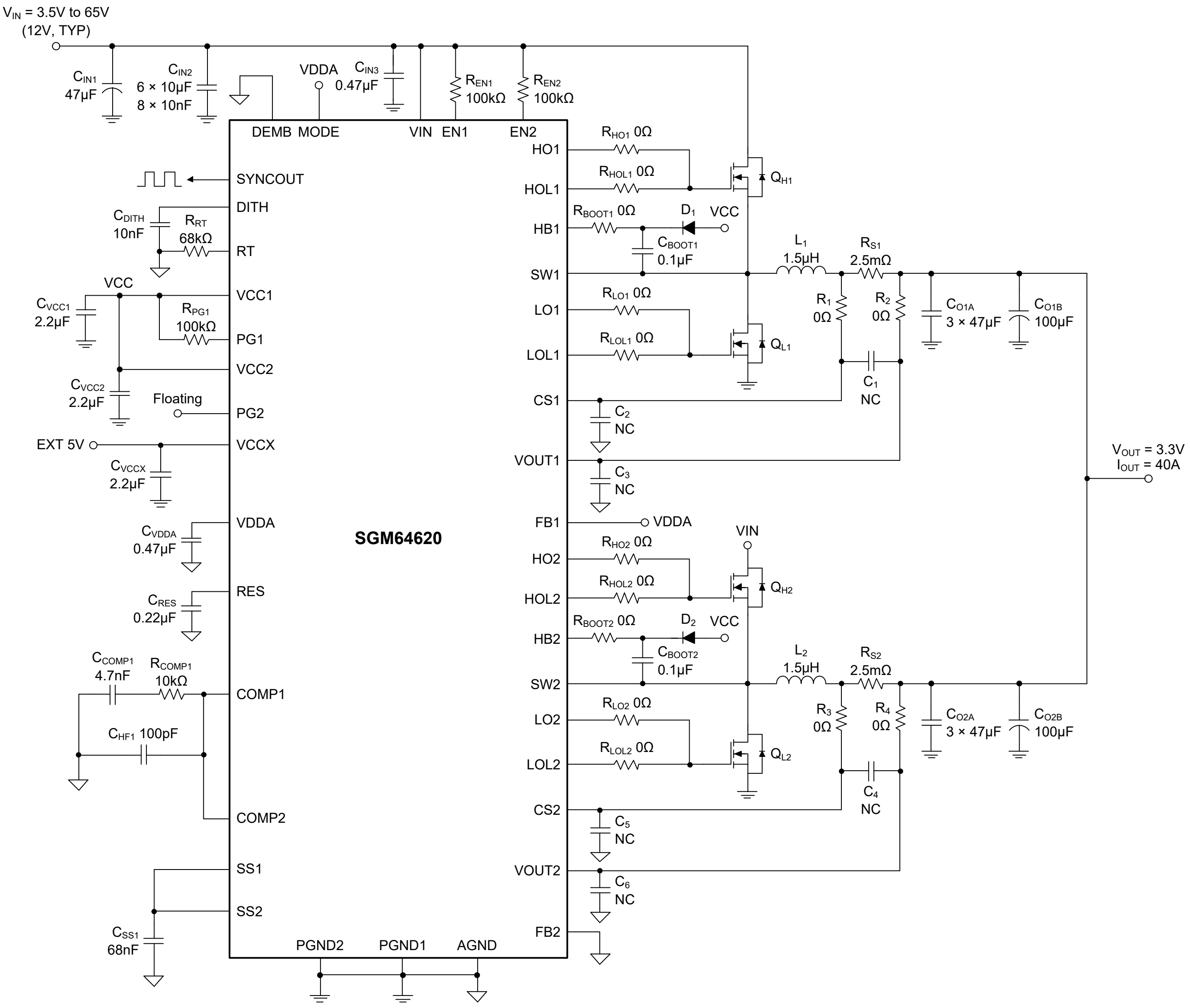


Figure 16. Application Circuit for Two-Phase 3.3V Single-Output with 400kHz

LAYOUT GUIDELINES

A proper PCB design and layout are crucial for achieving a reliable design in high-current, fast-switching DC-DC converter circuits. Several key considerations must be taken into account before designing a PCB layout with the SGM64620:

1. Place the input capacitors, high-side switch MOSFET, and low-side switch MOSFET in close to shorten the impedance of input power loop, thereby reducing the impact caused by parasitic parameters, as shown in the Figure 17.

2. Minimize the area of the output power loop, reduce electromagnetic interference (EMI), and reduce the impedance between the output capacitor's GND and the low-side MOSFET's source terminal.

3. The SW node is a significant dv/dt noise source, and the area of the SW region must be minimized (short and wide).

4. The gate driver outputs HO1/2, HOL1/2, LO1/2, LOL1/2 to the MOSFET gates traces must be short as possible to reduce parasitic inductance. The traces that carry forward and return currents must be close together.

5. Place small size high frequency decoupling capacitors on input capacitors.

6. Place decoupling capacitors as close as possible to VIN, VCC1, VCC2 and VDDA pins.

7. Route the power traces and analog signal traces separately, and use a ground plane for shielding as much as possible.

8. Place all sensitive analog traces, such as COMP1, COMP2, FB1, FB2, CS1, CS2, SS1, SS2, RES, and RT away from high-voltage switching nodes such as SW1, SW2, HB1, HB2, HO1, HO2, LO1, LO2.

9. Route the CS1/2, VOUT1/2 as paired traces with smallest distance and loop area. And use Kelvin connection to sense shunt resistor voltage. Use a filter capacitor across sense signals close to the IC pins. Place two capacitors separately. One is between the CS1/2 pin and AGND, and the other is between the VOUT1/2 pin and AGND. These filter capacitors also should be close to the SGM64620.

10. AGND and PGND1/2 are connected to a single point on the exposed pad of the IC.

11. Use large copper areas on all layers and stich them with thermal vias for better heat transfer and dissipation especially for heavy load applications.

12. The layout of the two channels of SGM64620 should be laid out as symmetrically as possible.

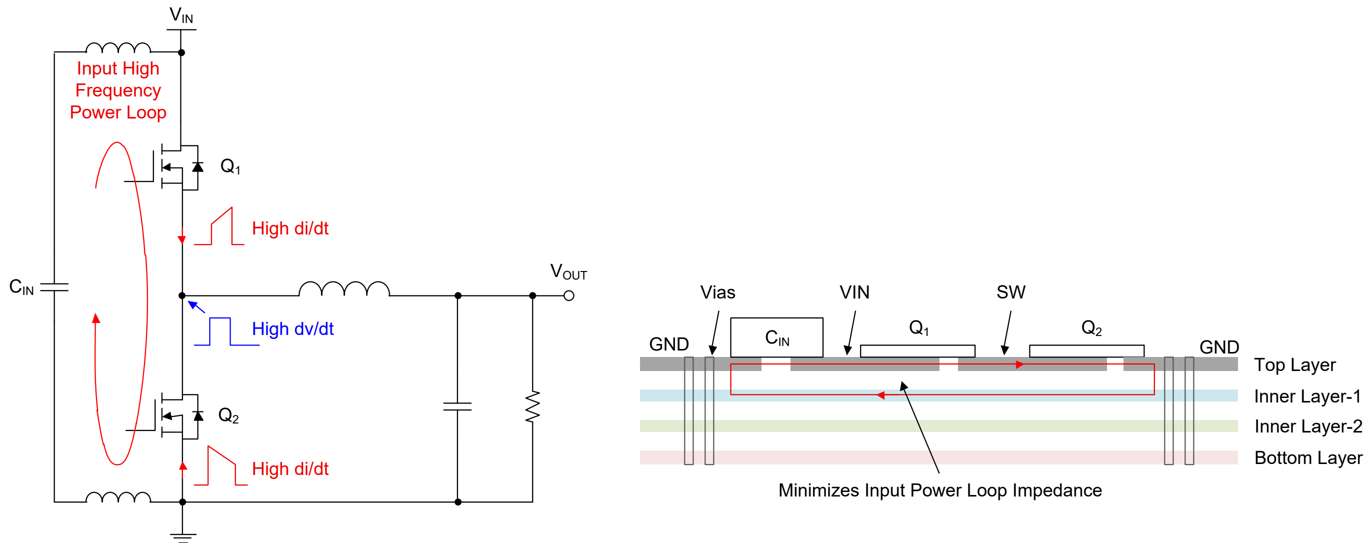
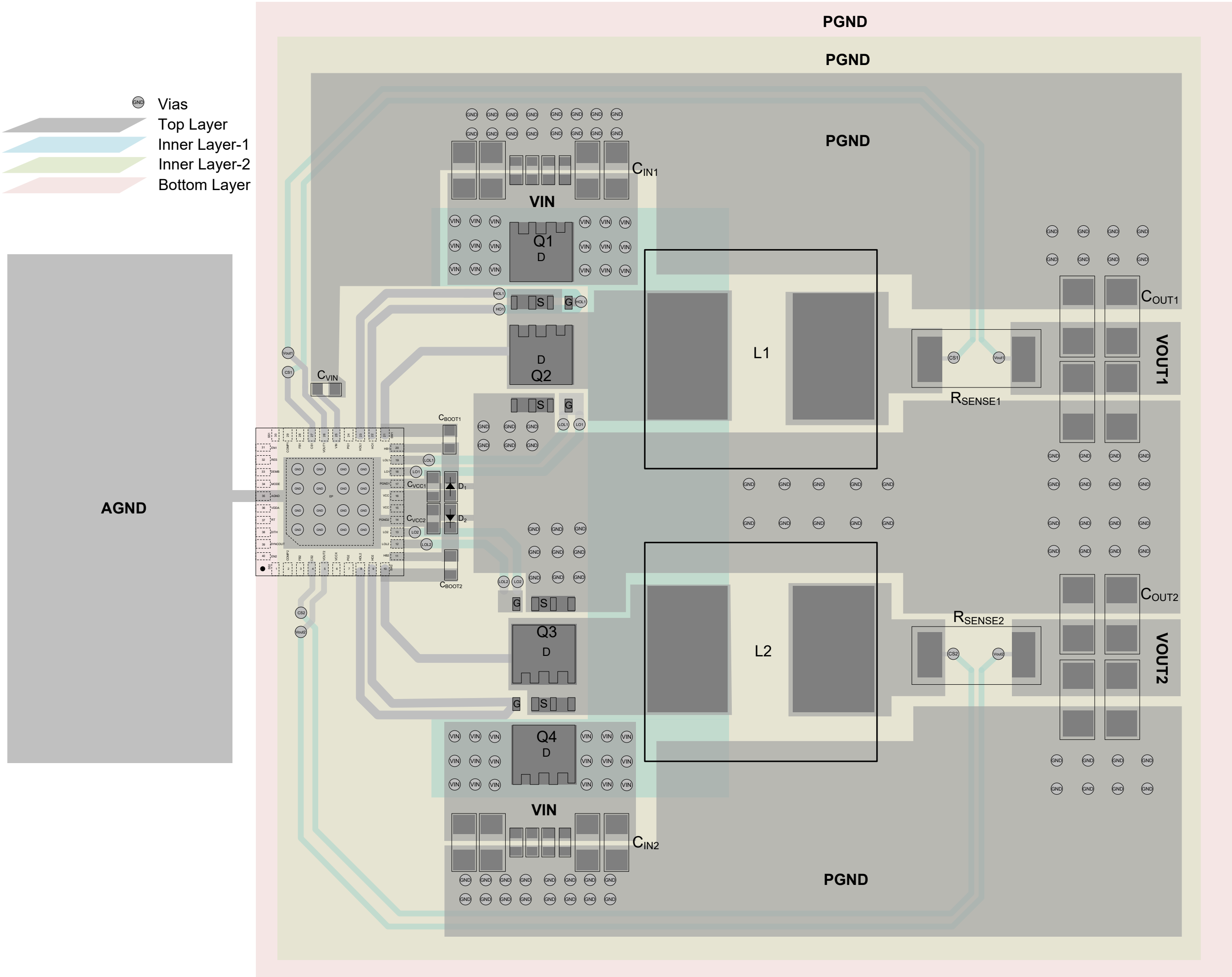


Figure 17. The Input Power Loop Layout Recommendation

LAYOUT GUIDELINES (continued)



NOTE: This example is provided to demonstrate the power loop layout of the SGM64620 and is for reference only.

Figure 18. Layout Example

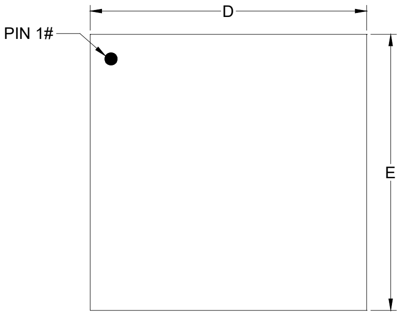
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

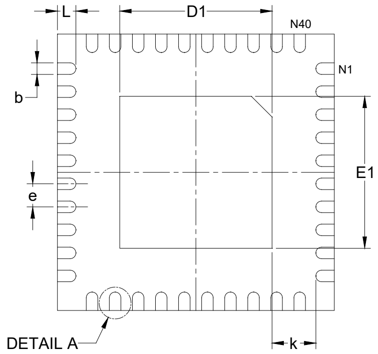
Changes from Original to REV.A (MARCH 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

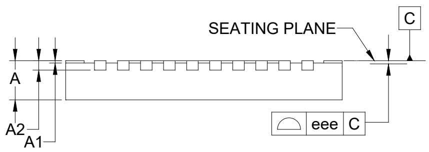
TQFN-6×6-40EL



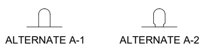
TOP VIEW



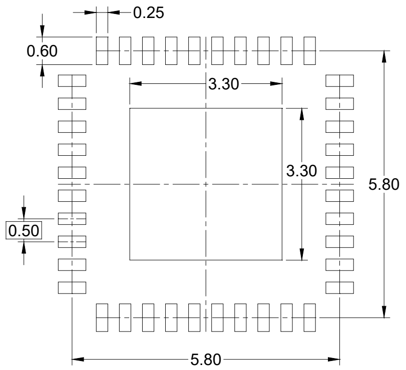
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



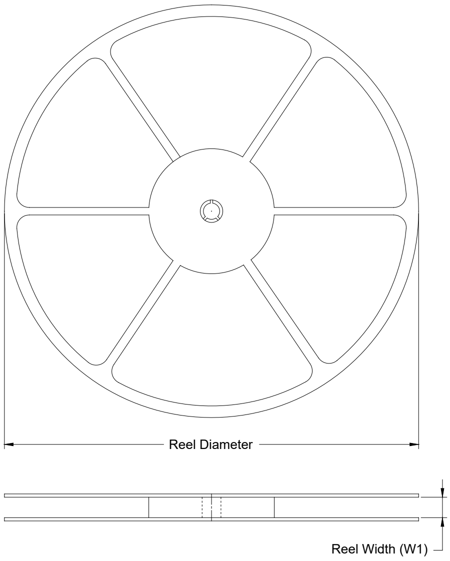
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.800	-	0.900
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	5.900	-	6.100
E	5.900	-	6.100
D1	3.200	-	3.400
E1	3.200	-	3.400
e	0.500 BSC		
k	0.950 REF		
L	0.300	-	0.500
eee	0.080		

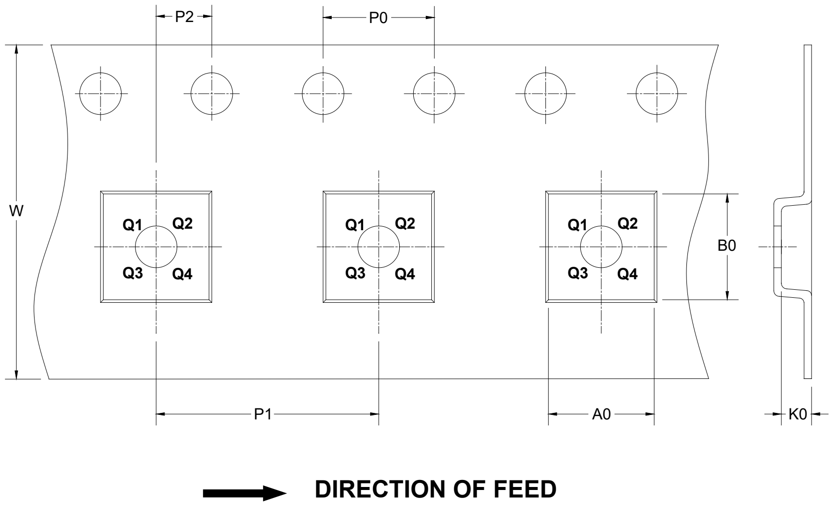
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



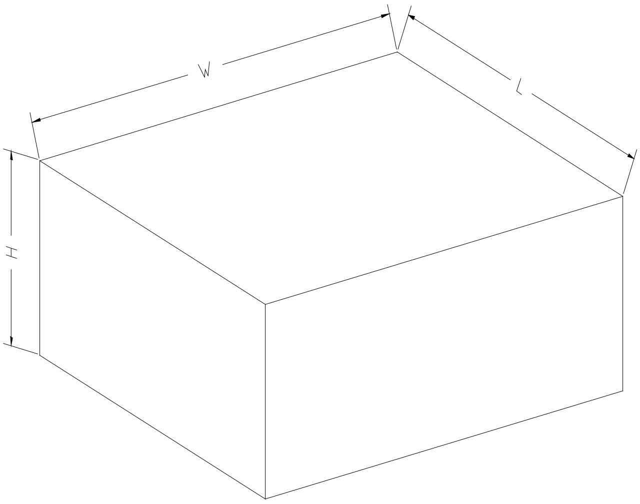
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-6×6-40EL	13"	16.4	6.30	6.30	1.40	4.0	12.0	2.0	16.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002