74LV164
8-Bit Serial-In and Parallel-Out Shift Register

GENERAL DESCRIPTION

The 74LV164 is an 8-bit serial-in and parallel-out shift register which can accept a wide supply voltage range from 1.0V to 5.5V.

This device provides gated serial inputs (DSA and DSB) and parallel data outputs (Q0 to Q7). DSA and DSB support serial data entry, where either input can allow data to enter through another input as an active high input. CP is a clock input. When the device is on low-to-high clock transition of the CP, data can be shifted. $\overline{MR}$ is the master reset input that is separated from the other inputs. When $\overline{MR}$ is held low, it can make the register clear and all outputs must be low level.

FEATURES

- **Wide Operating Voltage Range: 1.0V to 5.5V**
- **Inputs Accept Voltages Higher than the Supply Voltage**
- **+12mA/-12mA Output Current**
- **CMOS Low Power Consumption**
- **Gated Serial Data Inputs**
- **Asynchronous Master Reset Input**
- **Outputs in High-Impedance State when V_{CC} = 0V**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-14 and TSSOP-14 Packages**

APPLICATIONS

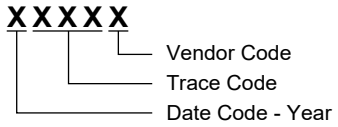
IP Routers
Enterprise Switches

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LV164	SOIC-14	-40℃ to +125℃	74LV164XS14G/TR	74LV164XS14 XXXXX	Tape and Reel, 2500
	TSSOP-14	-40℃ to +125℃	74LV164XTS14G/TR	74LV164 XTS14 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, V_{CC} ..... -0.5V to 7.0V
Input Voltage Range, V_I (2) ..... -0.5V to 7.0V
Output Voltage Range, V_O (2)
High State or Low State ..... -0.5V to MIN(7.0V, V_{CC} + 0.5V)
High-Impedance or Power-Off State ..... -0.5V to 7.0V
Input Clamp Current, I_{IK} (V_I < 0V) .....-20mA
Output Clamp Current, I_{OK} (V_O < 0V).....-50mA
Continuous Output Current, I_O .....±25mA
Continuous Current through V_{CC} or GND.....±50mA
Junction Temperature (3) .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....5000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC} (4) .....1.0V to 5.5V
Input Voltage, V_I.....0V to 5.5V
Output Voltage Range, V_O
High State or Low State ..... 0V to V_{CC}
High-Impedance or Power-Off State .....0V to 5.5V
Output Current, I_O ..... ±12mA
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 1.0V to 2.0V ..... 500ns/V (MAX)
V_{CC} = 2.0V to 2.7V ..... 200ns/V (MAX)
V_{CC} = 2.7V to 3.6V ..... 100ns/V (MAX)
V_{CC} = 3.6V to 5.5V ..... 50ns/V (MAX)
Operating Temperature Range .....-40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

4. The electrical characteristics can be ensured within the V_{CC} range of 1.2V to 5.5V, but the 74LV164 can also operate normally at V_{CC} = 1.0V (input level is GND or V_{CC}).

ESD SENSITIVITY CAUTION

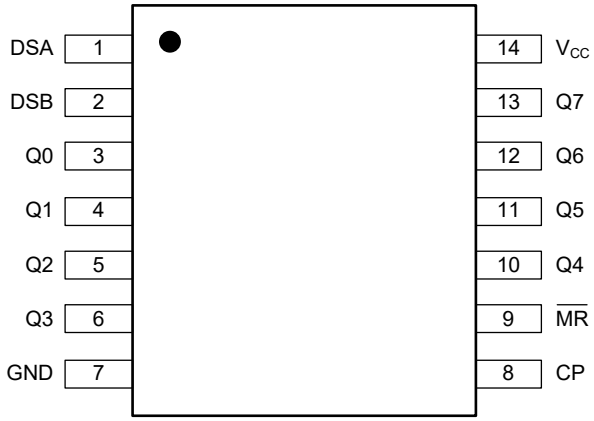
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

(TOP VIEW)

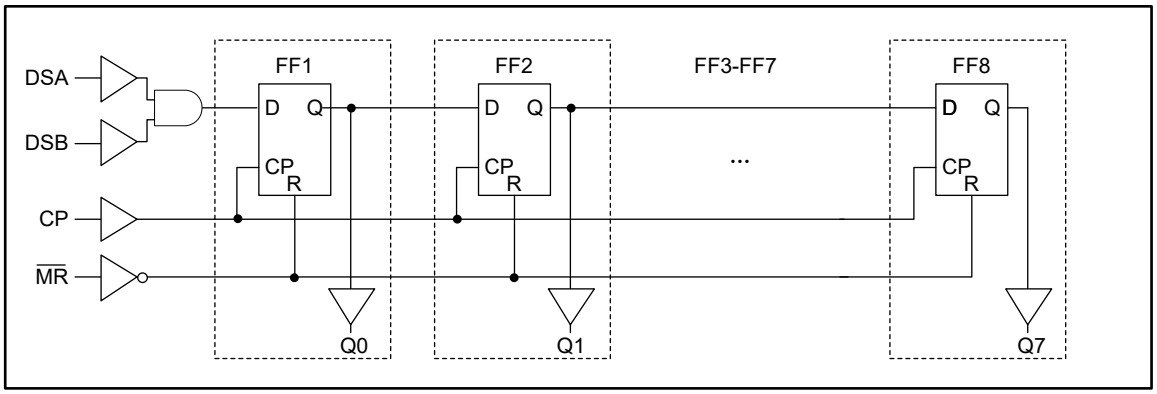


SOIC-14/TSSOP-14

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	DSA	Serial Data Input A.
2	DSB	Serial Data Input B.
3, 4, 5, 6, 10, 11, 12, 13	Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	Parallel Data Outputs.
7	GND	Ground.
8	CP	Clock Input (Low-to-High Clock Transition, Edge-Triggered).
9	$\overline{MR}$	Master Reset Input (Active Low).
14	V_{CC}	Supply Voltage.

LOGIC DIAGRAM



FUNCTION TABLE

INPUT				OUTPUT	
$\overline{MR}$	CP	DSA	DSB	Q0	Q1 to Q7
L	*X*	*X*	*X*	L	L to L
H	↑	l	l	L	q0 to q6
H	↑	l	h	L	q0 to q6
H	↑	h	l	L	q0 to q6
H	↑	h	h	H	q0 to q6

H = High voltage level.

h = High voltage level one set-up time before clock rising edge ↑.

L = Low voltage level.

l = Low voltage level one set-up time before clock rising edge ↑.

q = The state of the referenced output one set-up time before clock rising edge ↑.

↑ = Low-to-high clock transition.

X = Don't care.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 1.2V		Full	1.0			V
		V_{CC} = 2.0V		Full	1.4			
		V_{CC} = 2.7V to 3.6V		Full	2.0			
		V_{CC} = 4.5V to 5.5V		Full	0.7 × V_{CC}			
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.2V		Full			0.2	V
		V_{CC} = 2.0V		Full			0.6	
		V_{CC} = 2.7V to 3.6V		Full			0.8	
		V_{CC} = 4.5V to 5.5V		Full			0.3 × V_{CC}	
High-Level Output Voltage	V_{OH}	V_I = V_{IH}	V_{CC} = 1.2V to 4.5V, I_O = -100μA	Full	V_{CC} - 0.2	V_{CC} - 0.02		V
			V_{CC} = 3.0V, I_O = -6mA	Full	2.2	2.80		
			V_{CC} = 4.5V, I_O = -12mA	Full	3.5	4.22		
			V_{CC} = 5.5V, I_O = -12mA	Full	4.6	5.25		
Low-Level Output Voltage	V_{OL}	V_I = V_{IL}	V_{CC} = 1.2V to 4.5V, I_O = 100μA	Full		0.01	0.20	V
			V_{CC} = 3.0V, I_O = 6mA	Full		0.18	0.50	
			V_{CC} = 4.5V, I_O = 12mA	Full		0.30	0.65	
			V_{CC} = 5.5V, I_O = 12mA	Full		0.28	0.60	
Input Leakage Current	I_I	V_{CC} = 5.5V, V_I = V_{CC} or GND		Full			±1	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, V_I = V_{CC} or GND, I_O = 0A		Full			10	μA
Power-Off Leakage Current	I_{OFF}	V_{CC} = 0V, V_I or V_O = V_{CC} or GND		Full			±5	μA
Additional Supply Current	ΔI_{CC}	Per input, V_{CC} = 2.7V to 3.6V, V_I = V_{CC} - 0.6V		Full			50	μA
Input Capacitance	C_I			+25℃		4		pF

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at C_L = 50pF and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay (2)	t_{PD}	CP to Qn, see Figure 2	V_{CC} = 1.2V	+25℃		80		ns
			V_{CC} = 2.0V	Full	7	22	49	
			V_{CC} = 2.7V	Full	5	15	36	
			V_{CC} = 3.0V to 3.6V	Full	4	14	29	
			V_{CC} = 4.5V to 5.5V	Full	3	11	24	
High to Low Propagation Delay (2)	t_{PHL}	$\overline{MR}$ to Qn, see Figure 3	V_{CC} = 1.2V	+25℃		52		ns
			V_{CC} = 2.0V	Full	7	19	49	
			V_{CC} = 2.7V	Full	5	14	36	
			V_{CC} = 3.0V to 3.6V	Full	4	13	29	
			V_{CC} = 4.5V to 5.5V	Full	3	11	24	
Pulse Width	t_W	CP high or low, see Figure 2	V_{CC} = 2.0V	Full	41			ns
			V_{CC} = 2.7V	Full	30			
			V_{CC} = 3.0V to 3.6V	Full	24			
			V_{CC} = 4.5V to 5.5V	Full	16			
		$\overline{MR}$ low, see Figure 3	V_{CC} = 2.0V	Full	41			ns
			V_{CC} = 2.7V	Full	30			
			V_{CC} = 3.0V to 3.6V	Full	24			
			V_{CC} = 4.5V to 5.5V	Full	16			
Recovery Time	t_{REC}	$\overline{MR}$ to CP, see Figure 3	V_{CC} = 1.2V	+25℃		-10		ns
			V_{CC} = 2.0V	Full	24			
			V_{CC} = 2.7V	Full	18			
			V_{CC} = 3.0V to 3.6V	Full	14			
			V_{CC} = 4.5V to 5.5V	Full	10			
Set-Up Time	t_{SU}	DSA, DSB to CP, see Figure 4	V_{CC} = 1.2V	+25℃		10		ns
			V_{CC} = 2.0V	Full	26			
			V_{CC} = 2.7V	Full	19			
			V_{CC} = 3.0V to 3.6V	Full	15			
			V_{CC} = 4.5V to 5.5V	Full	10			
Hold Time	t_H	DSA, DSB to CP, see Figure 4	V_{CC} = 1.2V	+25℃		-3		ns
			V_{CC} = 2.0V	Full	5			
			V_{CC} = 2.7V	Full	5			
			V_{CC} = 3.0V to 3.6V	Full	5			
			V_{CC} = 4.5V to 5.5V	Full	5			

DYNAMIC CHARACTERISTICS (continued)

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at C_L = 50pF and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Maximum Frequency	f_{MAX}	See Figure 2	V_{CC} = 2.0V	Full	12			MHz
			V_{CC} = 2.7V	Full	16			
			V_{CC} = 3.0V to 3.6V	Full	20			
			V_{CC} = 4.5V to 5.5V	Full	30			
Power Dissipation Capacitance (3)	C_{PD}	V_{CC} = 3.3V, C_L = 50pF, f_i =1MHz, V_I = GND to V_{CC}		+25℃		70		pF

NOTES:

1. Specified by design and characterization, not production tested.
2. t_{PD} is the same as t_{PLH} and t_{PHL}.
3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

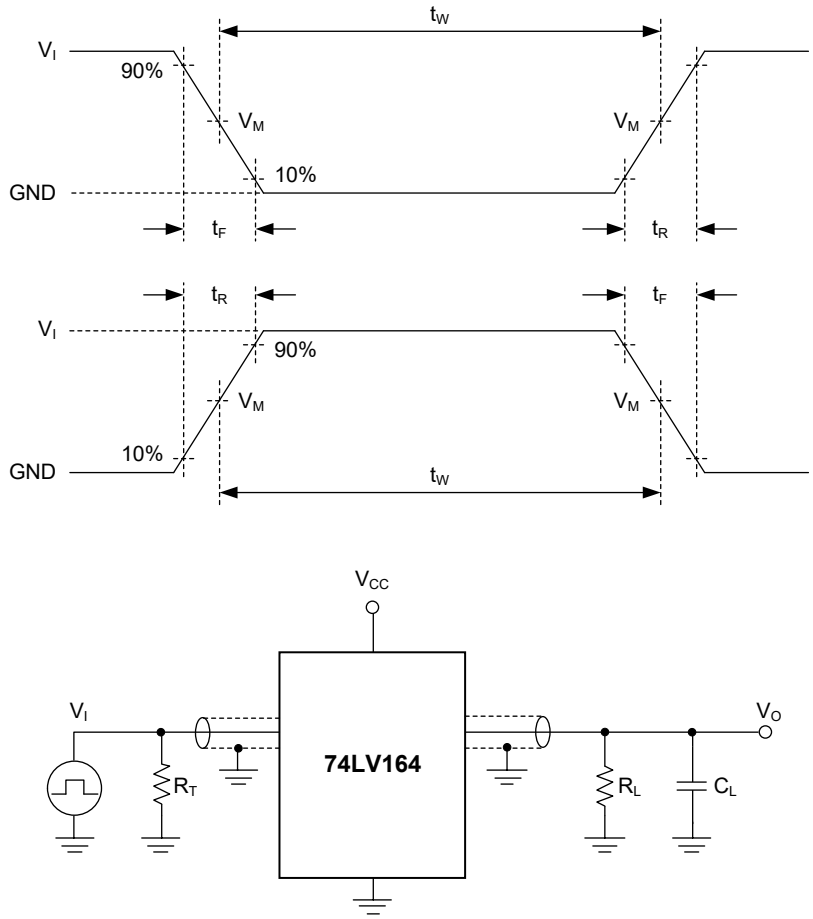
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of the outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

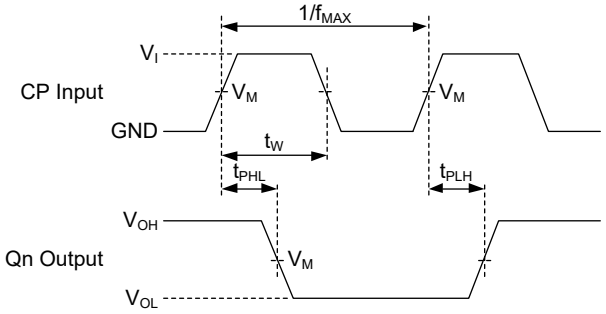
R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

Figure 1. Test Circuit for Measuring Switching Times

Table 1.Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD		TEST
V_{CC}	V_I	t_R, t_F	C_L	R_L	
1.2V	V_{CC}	≤ 2.5ns	50pF	1kΩ	t_{PHL}, t_{PLH}
2.0V	V_{CC}	≤ 2.5ns	50pF	1kΩ	t_{PHL}, t_{PLH}
2.7V	2.7V	≤ 2.5ns	50pF	1kΩ	t_{PHL}, t_{PLH}
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	1kΩ	t_{PHL}, t_{PLH}
4.5V to 5.5V	V_{CC}	≤ 2.5ns	50pF	1kΩ	t_{PHL}, t_{PLH}

WAVEFORMS

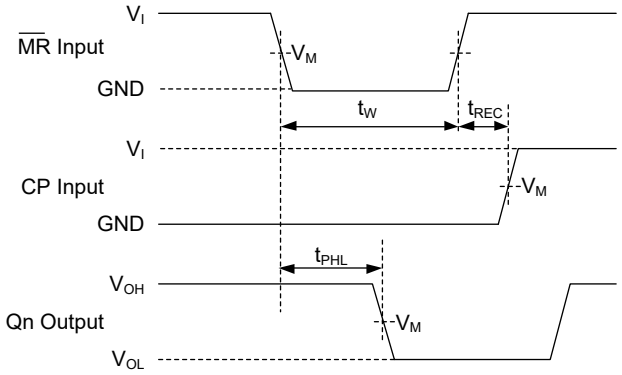


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Clock Pulse Width, Maximum Frequency and Clock Input to Output Propagation Delays

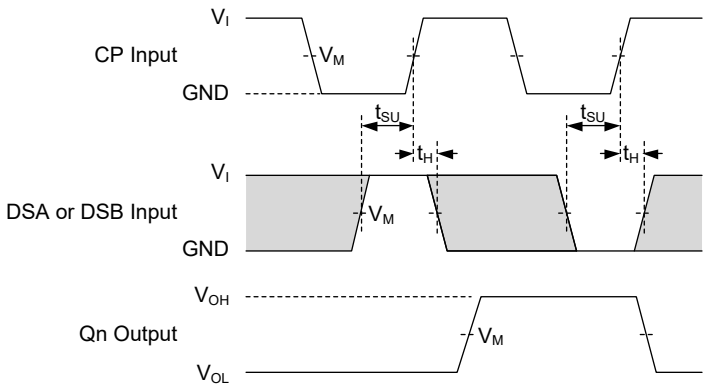


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Master Reset to Output Propagation Delays, Pulse Width and Recovery Time



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas refer to when the input is allowed to change for predictable output performance.

Figure 4. Data Set-Up and Hold Times

WAVEFORMS (continued)

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT
V_{CC}	V_I	V_M (1)	V_M
1.2V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
2.0V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
2.7V	2.7V	1.5V	1.5V
3.0V to 3.6V	2.7V	1.5V	1.5V
4.5V to 5.5V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.

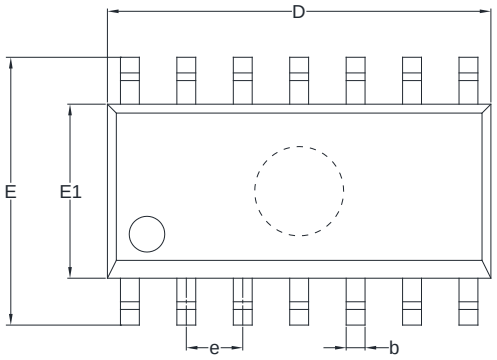
REVISION HISTORY

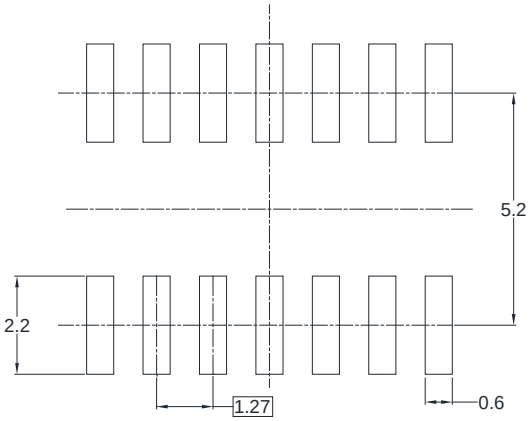
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (AUGUST 2023) to REV.A	Page
Changed from product preview to production data	All

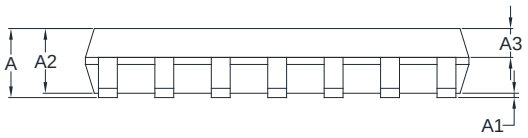
PACKAGE OUTLINE DIMENSIONS

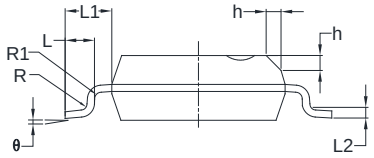
SOIC-14





RECOMMENDED LAND PATTERN (Unit: mm)



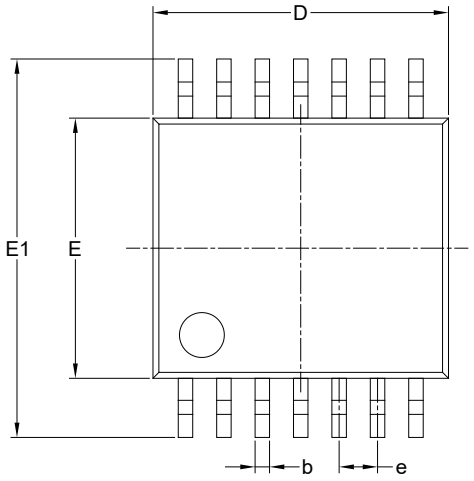


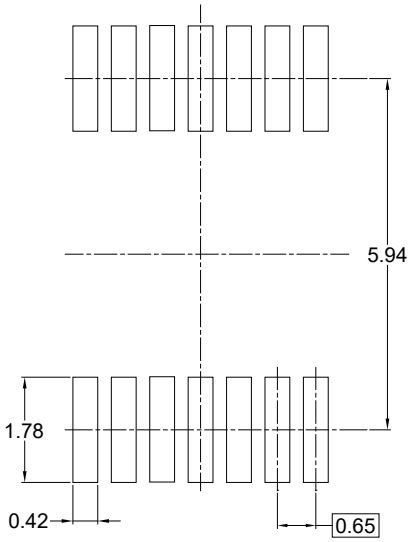
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.049	0.065
A3	0.55	0.75	0.022	0.030
b	0.36	0.49	0.014	0.019
D	8.53	8.73	0.336	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.45	0.80	0.018	0.032
L1	1.04 REF		0.040 REF	
L2	0.25 BSC		0.01 BSC	
R	0.07		0.003	
R1	0.07		0.003	
h	0.30	0.50	0.012	0.020
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

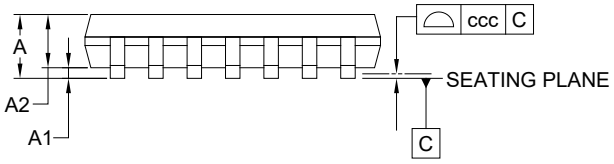
PACKAGE OUTLINE DIMENSIONS

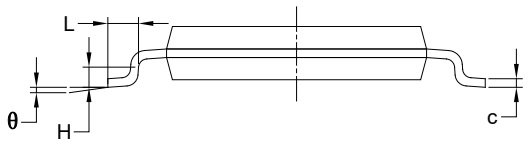
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)



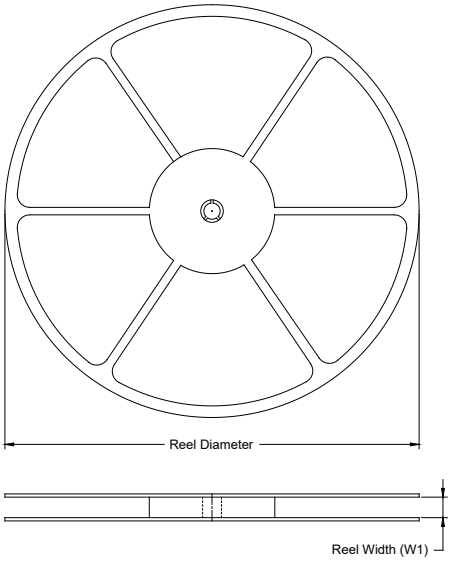


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

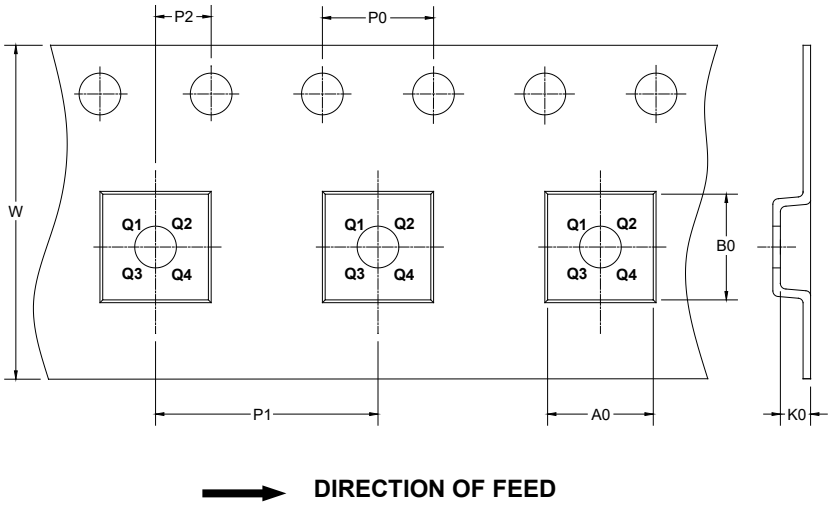
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

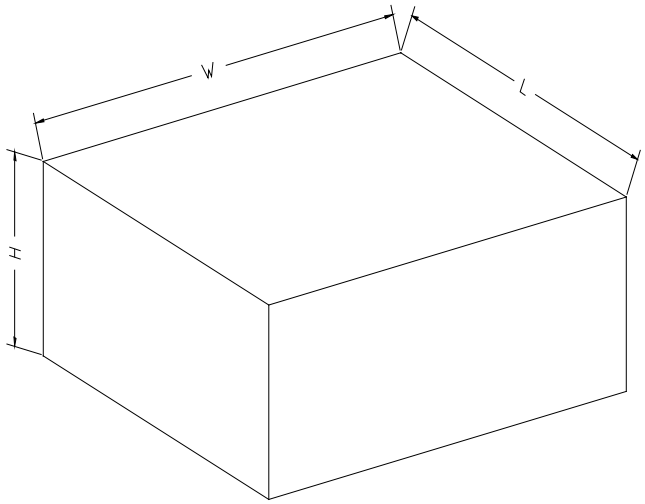
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-14	13"	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP-14	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002