SGM52410S
Low-Power, SPI-Compatible, 24-Bit ADC with Internal Reference and Temperature Sensor

GENERAL DESCRIPTION

The SGM52410S is a highly precise and efficient 24-bit analog-to-digital converter (ADC) that has been designed to meet the needs of modern sensor measurement applications. The ADC is available in a Green MSOP-10 package or UTQFN-2×1.5-10L package and comes equipped with all the essential features necessary for measuring common sensor signals. These features include a programmable gain amplifier (PGA), voltage reference, oscillator, and high-accuracy temperature sensor. With a wide power supply range of 2V to 5.5V, the SGM52410S is ideal for space and power-constrained applications that demand precision and efficiency.

The SGM52410S can achieve conversion rates of up to 960 samples per second (SPS) with single-cycle settling. The ADC features a programmable gain amplifier (PGA) that supports input ranges from ±256mV to ±6.144V, enabling accurate measurement of both large and small signals with high resolution. In addition, the input multiplexer (MUX) allows for the measurement of two differential or four single-ended inputs. The SGM52410S also comes equipped with a high-precision temperature sensor that can be used for system-level temperature monitoring or cold junction compensation for thermocouples.

The SGM52410S can operate in either continuous conversion mode or single-shot mode, which automatically powers down after a conversion to significantly reduce current consumption during idle periods. The SGM52410S is designed to operate within a temperature range of -40℃ to +125℃, making them suitable for use in a wide range of applications.

FEATURES

- **Four Single-Ended or Two Differential Inputs**
- **Wide Supply Range: 2V to 5.5V**
- **Low Current Consumption:**
  - **Continuous Mode: 207μA (TYP)**
  - **Single-Shot Mode: Automatic Power-Down**
- **Programmable Output Data Rate:**
  5SPS to 960SPS
- **Single-Cycle Settling**
- **50/60Hz Line Rejection**
- **CRC for SPI Communication**
- **CRC Enable/Disable Register**
- **Robust Encryption for Factory Mode Entry**
- **Internal PGA**
- **Internal Oscillator**
- **Internal Low-Drift Voltage Reference**
- **Internal Temperature Sensor:**
  0.2℃ (TYP) Error at 0℃ to 70℃
- **Available in Green MSOP-10 and UTQFN-2×1.5-10L Packages**

APPLICATIONS

Automotive Applications
- Battery Current Measurement
- BMS Insulation Detection
- HMI

Temperature Measurement
- Thermocouple with Cold Junction Compensation
- Thermistor Measurement

Portable Instrumentation

Process Controls and Factory Automation

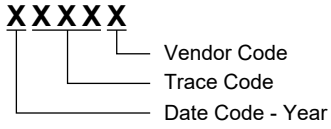
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM52410S	MSOP-10	-40℃ to +125℃	SGM52410SXMS10G/TR	SGM1AQ XMS10 XXXXX	Tape and Reel, 4000
			SGM52410SXMS10SG/TR	SGM1AQ XMS10 XXXXX	Tape and Reel, 500
	UTQFN-2×1.5-10L	-40℃ to +125℃	SGM52410SXURA10G/TR	1AO XXXX	Tape and Reel, 3000
			SGM52410SXURA10SG/TR	1AO XXXX	Tape and Reel, 500

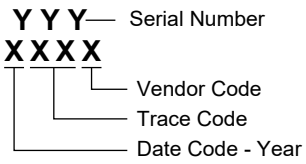
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XXXX = Date Code, Trace Code and Vendor Code.

MSOP-10



UTQFN-2×1.5-10L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range (VDD to GND) ..... -0.3V to 7V
Analog Input Voltage Range (AIN0, AIN1, AIN2, AIN3)
.....GND - 0.3V to V_{DD} + 0.3V
Digital Input Voltage Range (DIN, DOUT/nDRDY, SCLK, nCS)
.....GND - 0.3V to V_{DD} + 0.3V
Input Current, Continuous (Any Pin except Power Supply Pins)
..... -10mA to 10mA
Package Thermal Resistance
MSOP-10, θ_{JA} ..... 142.9℃/W
MSOP-10, θ_{JB} ..... 92.4℃/W
MSOP-10, θ_{JC} ..... 47.7℃/W
UTQFN-2×1.5-10L, θ_{JA} ..... 82.4℃/W
UTQFN-2×1.5-10L, θ_{JB} ..... 15.6℃/W
UTQFN-2×1.5-10L, θ_{JC} ..... 49.8℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM.....±4000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage (VDD to GND), V_{DD} .....2V to 5.5V
Full-Scale Input Voltage Range (3) (4) (V_{IN} = V_{AINP} - V_{AINN}), FSR
..... See Table 4
Absolute Input Voltage Range, V_{AINx} ..... GND to V_{DD}
Digital Input Voltage Range..... GND to V_{DD}
Operating Temperature Range..... -40℃ to +125℃

NOTES:

3. AIN_P and AIN_N refer to the chosen positive and negative inputs respectively, while AIN_x represents any of the four analog inputs that are available.

4. The ADC scaling's full-scale range is indicated by this parameter. It is essential to ensure that no more than V_{DD} + 0.3V or 5.5V (whichever is lower) is applied to the device.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

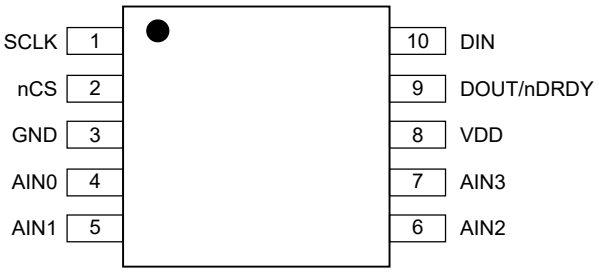
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

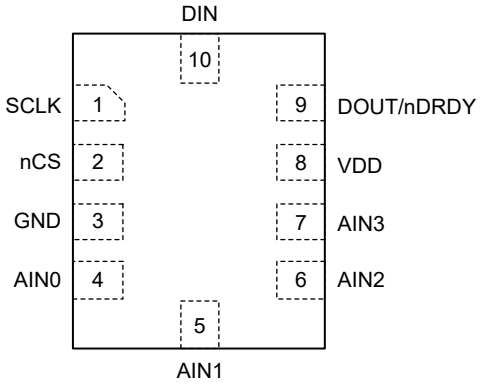
PIN CONFIGURATIONS

(TOP VIEW)



MSOP-10

(TOP VIEW)



UTQFN-2×1.5-10L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	SCLK	DI	Serial Clock Input.
2	nCS	DI	Chip Select. Active low. Tie to GND if unused.
3	GND	G	Ground.
4	AIN0	AI	Analog Input 0. Keep float or connect to VDD if unused.
5	AIN1	AI	Analog Input 1. Keep float or connect to VDD if unused.
6	AIN2	AI	Analog Input 2. Keep float or connect to VDD if unused.
7	AIN3	AI	Analog Input 3. Keep float or connect to VDD if unused.
8	VDD	P	Power Supply. A 100nF decoupling capacitor is required from power supply to GND.
9	DOUT/nDRDY	DO	Serial Data Output Combined with Data Ready. Active low.
10	DIN	DI	Serial Data Input.

NOTE: DI = digital input, DO = digital output, AI = analog input, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, Data Rate (DR) = 5SPS, and Full-Scale Range (FSR) = ±2.048V, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Inputs							
Full-Scale Input Voltage (1)		V_{IN} = AIN_P - AIN_N			±4.096/PGA		V
Analog Input Voltage		AIN_P or AIN_N to GND		GND - 0.1		V_{DD} + 0.1	V
Differential Input Impedance					See Table 3		
System Performance							
Resolution		No missing codes		24			Bits
Data Rate	DR				See Table 6		SPS
Data Rate Variation		All data rates		-4		4	%
Output Noise					See Noise Performance section		
Integral Nonlinearity	INL	DR = 5SPS, FSR = ±2.048V (2)			9	50	ppm
Offset Error	E_O	FSR = ±2.048V	Differential inputs		20	±250	μV
			Single-ended inputs		35		
Offset Drift		FSR = ±2.048V			0.4		μV/℃
Offset Power Supply Rejection		FSR = ±2.048V			12		μV/V
Offset Channel Match		Match between any two differential inputs			20		μV
Gain Error (3)	E_G	FSR = ±2.048V, T_A = +25℃			0.01	0.15	%
Gain Drift (3)(4)		FSR = ±0.256V			5		ppm/℃
		FSR = ±2.048V			5	15	
		FSR = ±6.144V (1)			5		
Gain Power Supply Rejection					45		ppm/V
Gain Match (3)		Match between any two PGA gains			0.01	0.1	%
Gain Channel Match		Match between any two inputs			0.01	0.1	%
Common Mode Rejection Ratio	CMRR	At DC, FSR = ±2.048V			115		dB
		At DC, FSR = ±6.144V (1)			110		
		f_{CM} = 50Hz, DR = 960SPS			106		
		f_{CM} = 60Hz, DR = 960SPS			105		
Normal Mode Rejection Ratio	NMRR	ODR = 10SPS, 50Hz ± 1Hz			95		dB
Temperature Sensor							
Temperature Range				-40		125	℃
Temperature Resolution					0.03125		℃/LSB
Accuracy		T_A = 0℃ to +70℃			0.2	±1.5	℃
		T_A = -40℃ to +125℃			0.7	±2	
		vs. supply			0.1	±1	℃/V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, Data Rate (DR) = 5SPS, and Full-Scale Range (FSR) = ±2.048V, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Inputs/Outputs						
High-Level Input Voltage	V_{IH}		0.7 × V_{DD}			V
Low-Level Input Voltage	V_{IL}				0.2 × V_{DD}	V
High-Level Output Voltage	V_{OH}		0.8 × V_{DD}			V
Low-Level Output Voltage	V_{OL}				0.2 × V_{DD}	V
High Input Leakage	I_H	V_{IH} = 5.5V	-1		1	μA
Low Input Leakage	I_L	V_{IL} = GND	-1		1	μA
Power Supply						
Supply Current	I_{VDD}	Power-down current at +25℃		0.5	1	μA
		Power-down current up to +125℃			5	
		Operating current at +25℃		207	240	
		Operating current up to +125℃			300	
Power Dissipation	P_D	V_{DD} = 5V		1.30		mW
		V_{DD} = 3.3V		0.68		
		V_{DD} = 2V		0.34		

NOTES:

1. This parameter specifies the maximum range of the ADC scaling. The device should not be subjected to more than V_{DD} + 0.3V or 5.5V (whichever is lower).
2. The best-fit INL is used to cover 99% of the full-scale range.
3. The parameter includes all errors originating from the onboard PGA and voltage reference.
4. The maximum value is specified by the characterization process.

TIMING REQUIREMENTS: SERIAL INTERFACE

(V_{DD} = 2V to 5.5V, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Delay Time, nCS Falling Edge to the First SCLK Rising Edge (1)	t_1		100			ns
Delay Time, Final SCLK Falling Edge to nCS Rising Edge	t_6		1000			ns
Pulse Duration, nCS High	t_{10}		200			ns
SCLK Period	t_2		350			ns
Pulse Duration, SCLK High	t_3		250			ns
Pulse Duration, SCLK Low (2)	t_4		100			ns
					28	ms
Setup Time, DIN Valid before SCLK Falling Edge	t_5		50			ns
Hold Time, DIN Valid after SCLK Falling Edge	t_7		50			ns
Hold Time, SCLK Rising Edge to DOUT Invalid	t_8		0			ns

NOTES:

1. If the serial bus is not shared with any other device, nCS can be permanently tied low.

2. Resetting the SPI interface is possible by holding SCLK low for more than 28ms.

SWITCHING CHARACTERISTICS: SERIAL INTERFACE

(T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, nCS Falling Edge to DOUT Driven	t_9	DOUT load = 20pF || 100kΩ to GND			100	ns
Propagation Delay Time, SCLK Rising Edge to Valid New DOUT	t_{11}	DOUT load = 20pF || 100kΩ to GND	0		50	ns
Propagation Delay Time, nCS Rising Edge to DOUT High Impedance	t_{12}	DOUT load = 20pF || 100kΩ to GND			100	ns

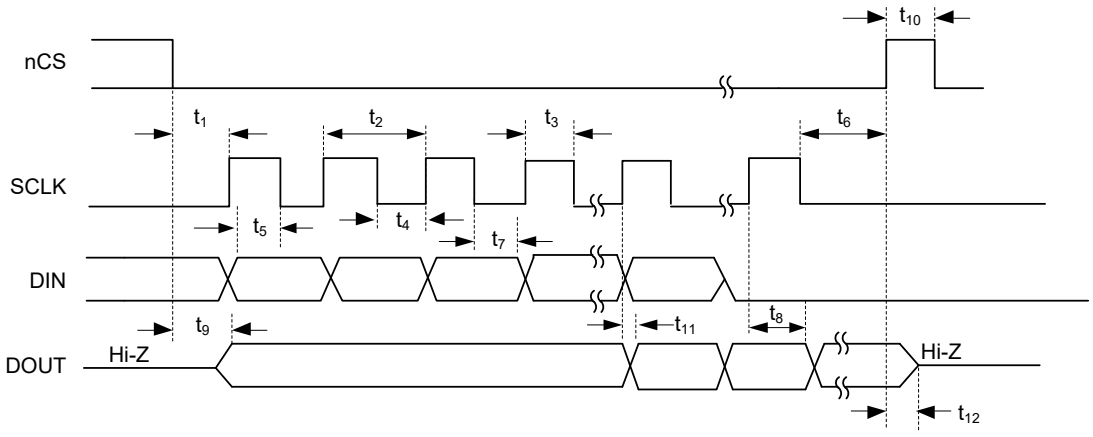
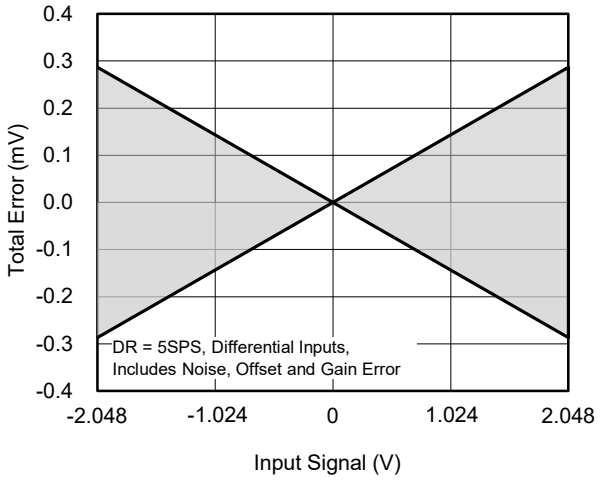


Figure 1. Serial Interface Timing Diagram

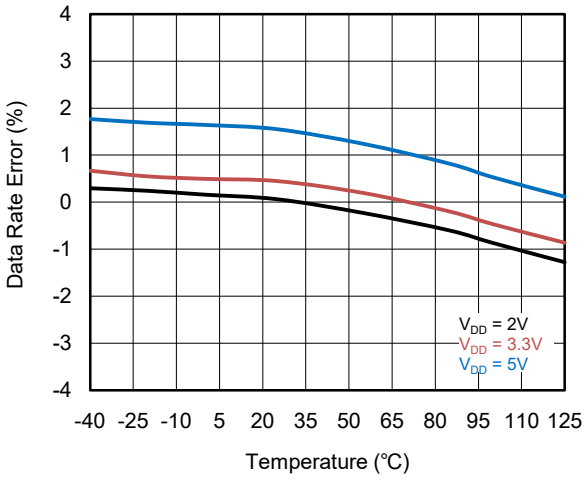
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_{DD} = 3.3V, FSR = ±2.048V, unless otherwise noted.

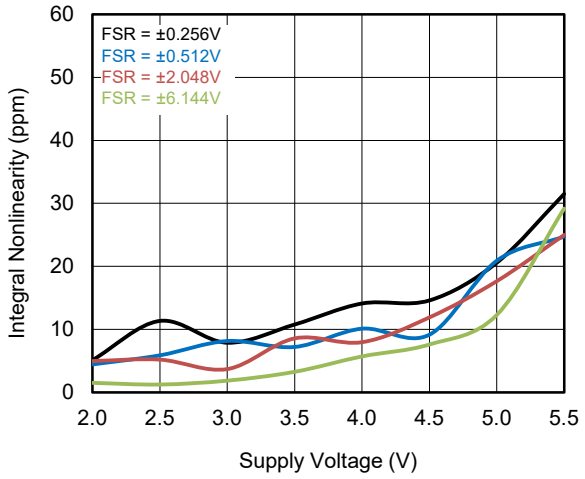
Total Error vs. Input Signal



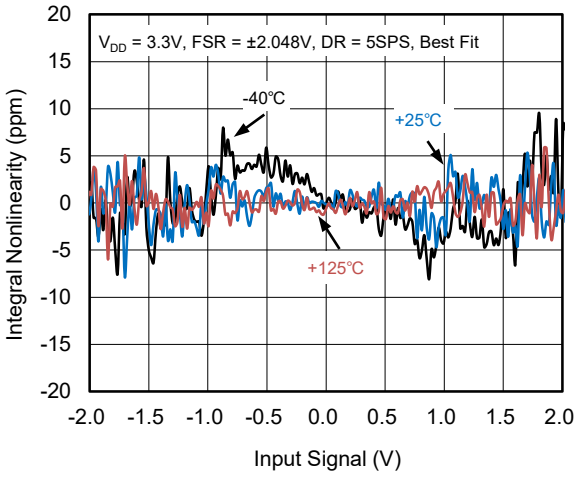
Data Rate vs. Temperature



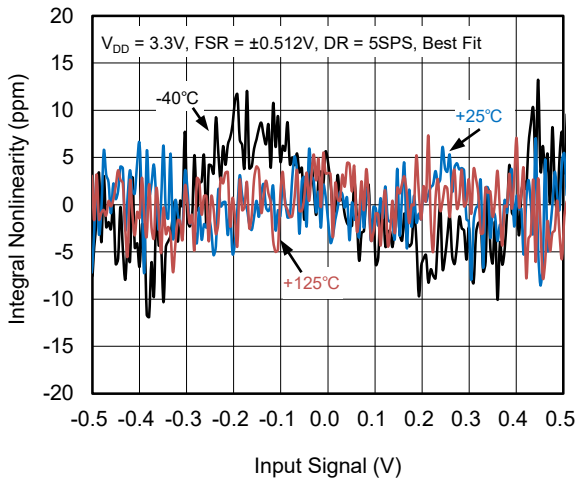
Integral Nonlinearity vs. Supply Voltage



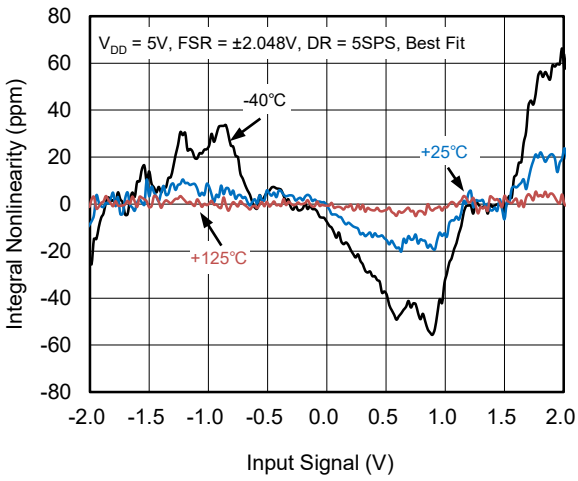
Integral Nonlinearity vs. Input Signal



Integral Nonlinearity vs. Input Signal



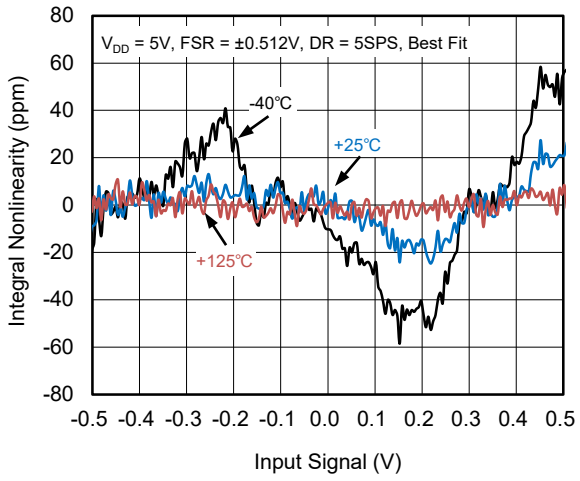
Integral Nonlinearity vs. Input Signal



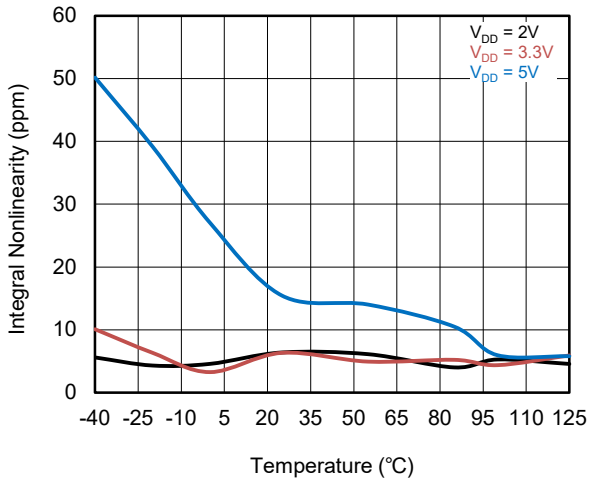
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_{DD} = 3.3V, FSR = ±2.048V, unless otherwise noted.

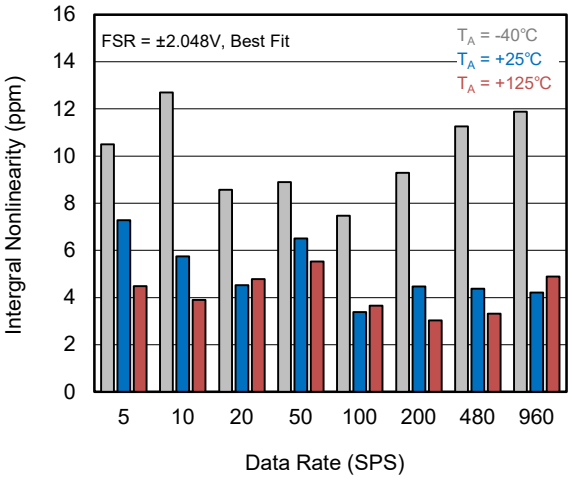
Integral Nonlinearity vs. Input Signal



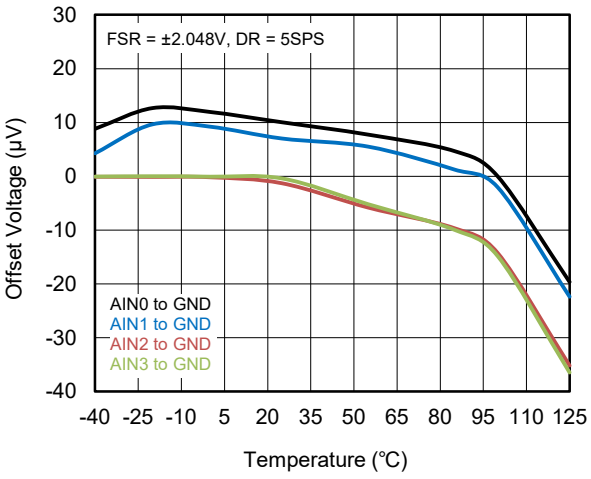
Integral Nonlinearity vs. Temperature



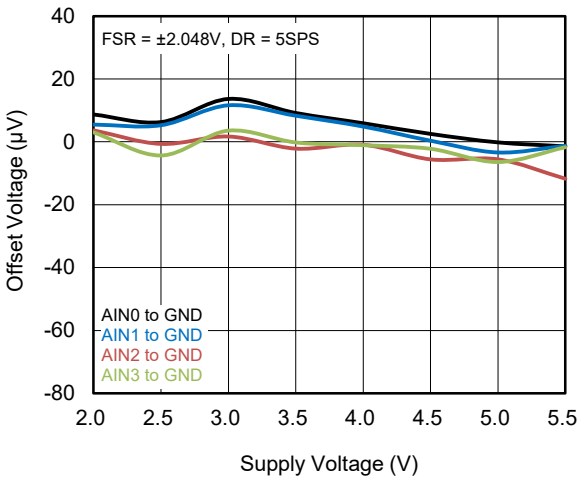
Integral Nonlinearity vs. Data Rate



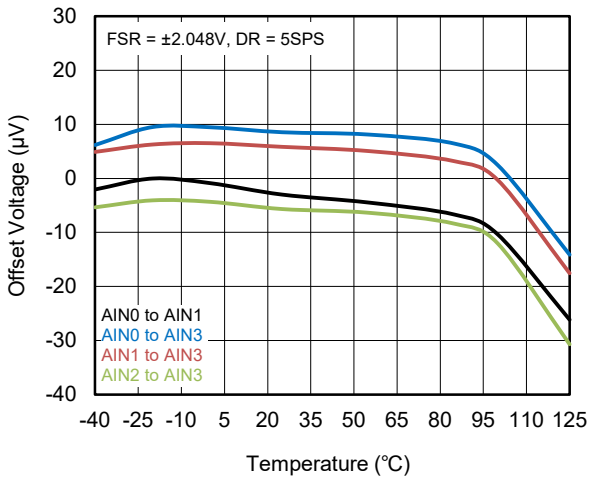
Single-Ended Offset Voltage vs. Temperature



Single-Ended Offset Voltage vs. Supply Voltage



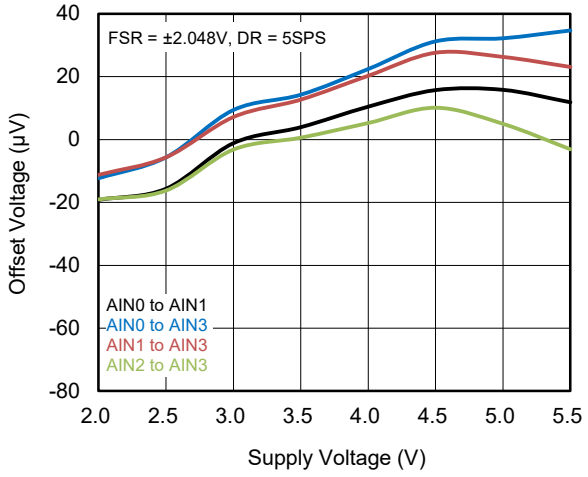
Differential Offset Voltage vs. Temperature



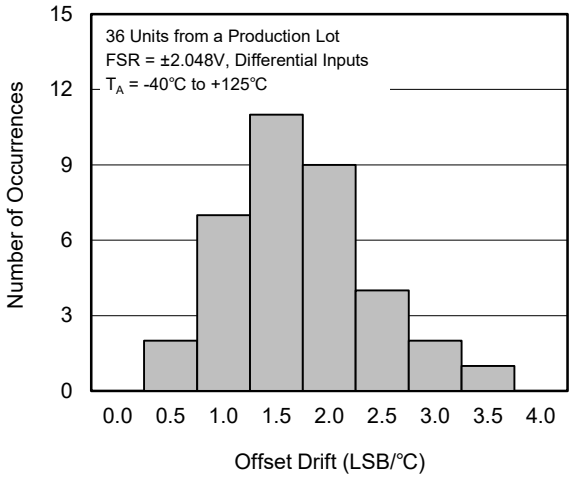
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_{DD} = 3.3V, FSR = ±2.048V, unless otherwise noted.

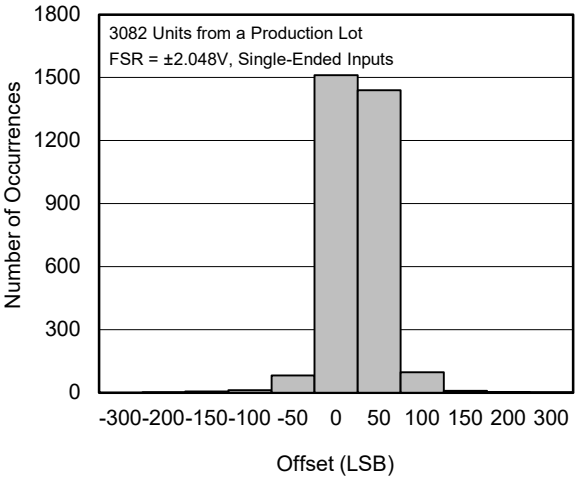
Differential Offset Voltage vs. Supply Voltage



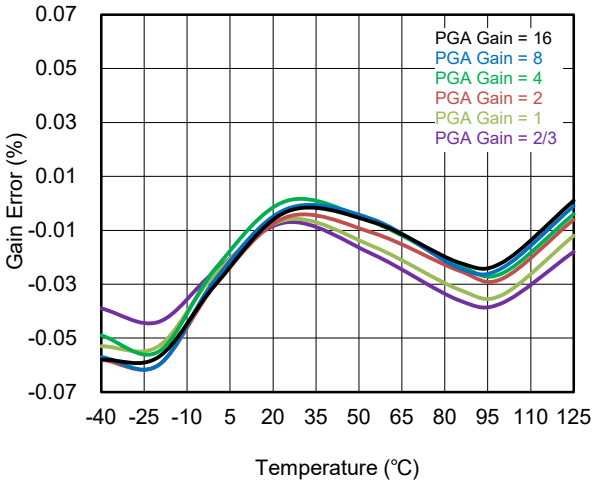
Offset Drift Histogram



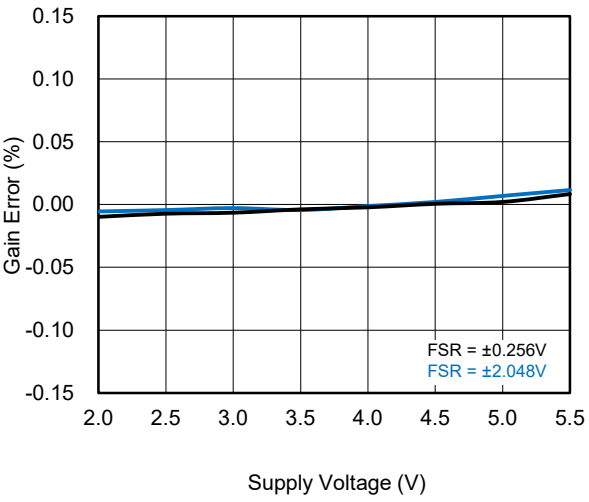
Offset Histogram



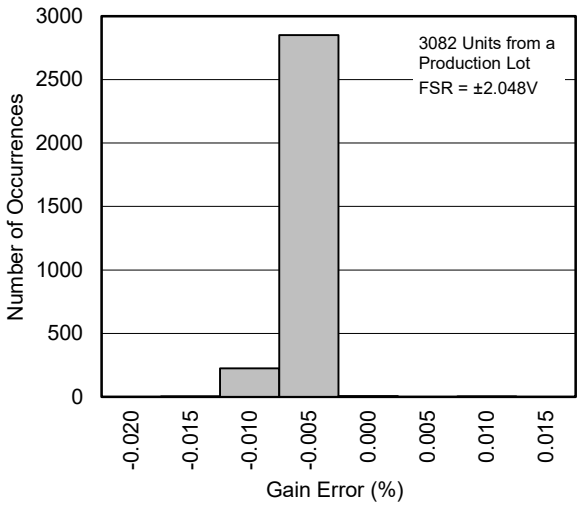
Gain Error vs. Temperature



Gain Error vs. Supply Voltage



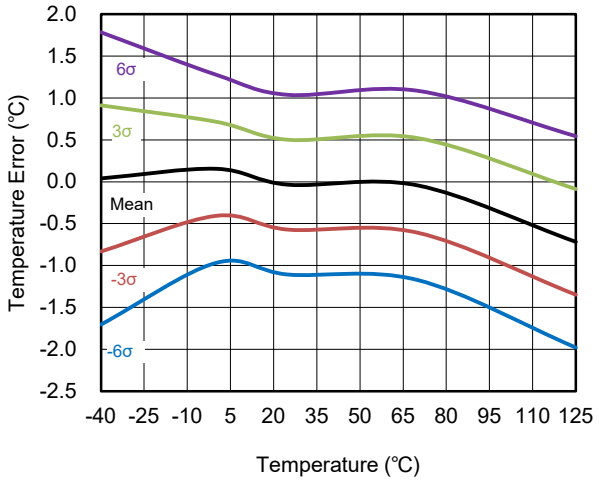
Gain Error Histogram



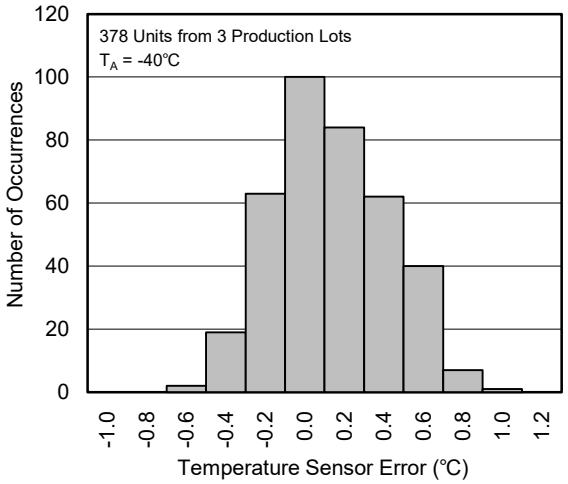
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_{DD} = 3.3V, FSR = ±2.048V, unless otherwise noted.

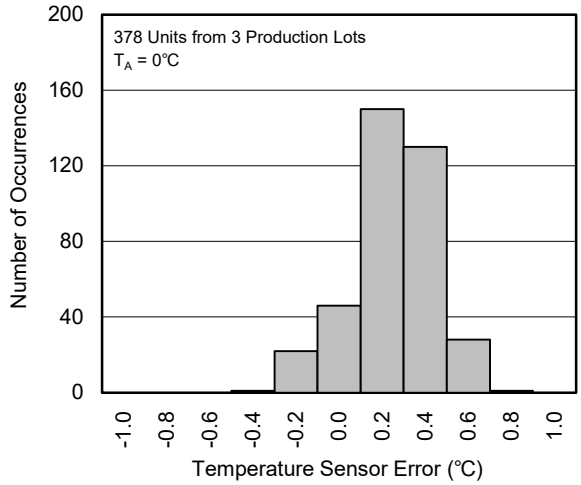
Temperature Sensor Error vs. Temperature (MSOP)



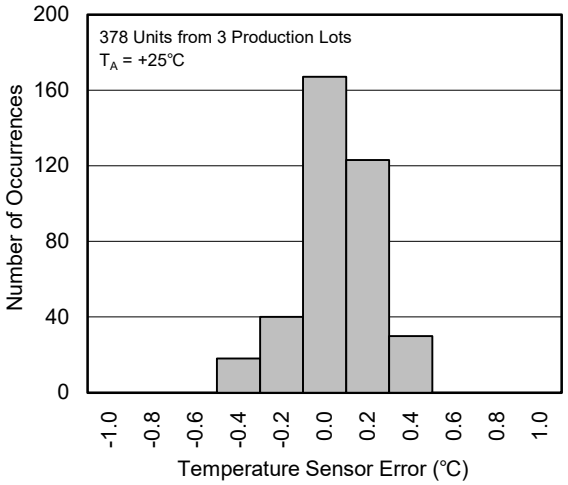
Temperature Sensor Error Histogram (MSOP)



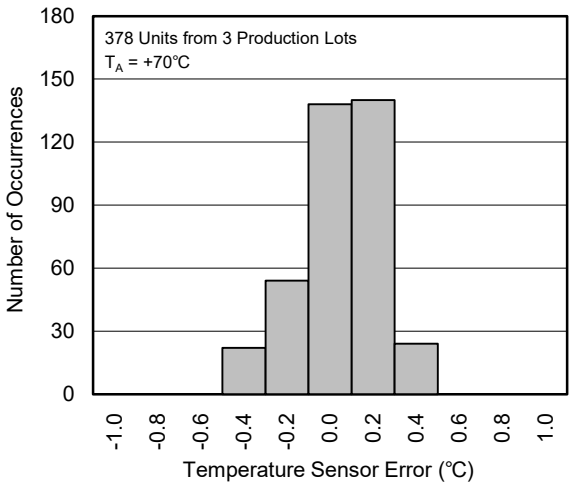
Temperature Sensor Error Histogram (MSOP)



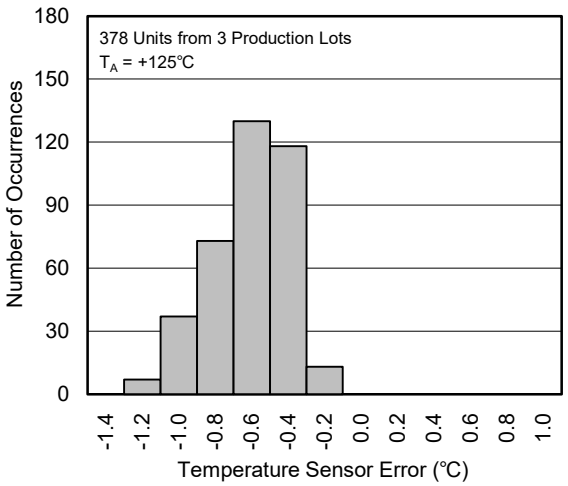
Temperature Sensor Error Histogram (MSOP)



Temperature Sensor Error Histogram (MSOP)



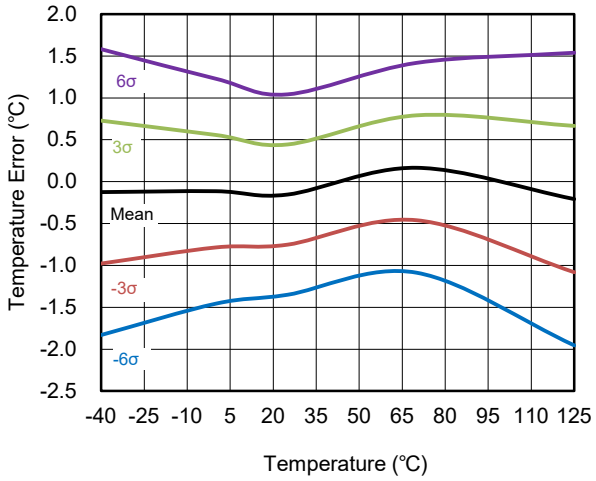
Temperature Sensor Error Histogram (MSOP)



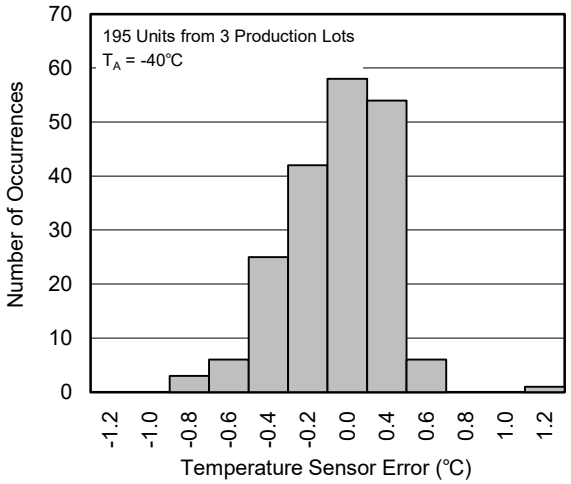
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_{DD} = 3.3V, FSR = ±2.048V, unless otherwise noted.

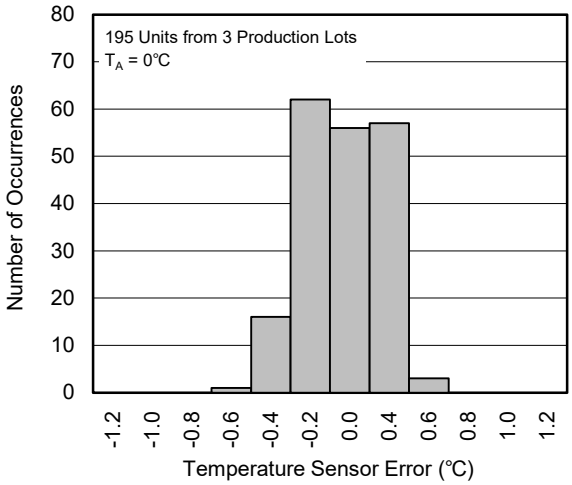
Temperature Sensor Error vs. Temperature (UTQFN)



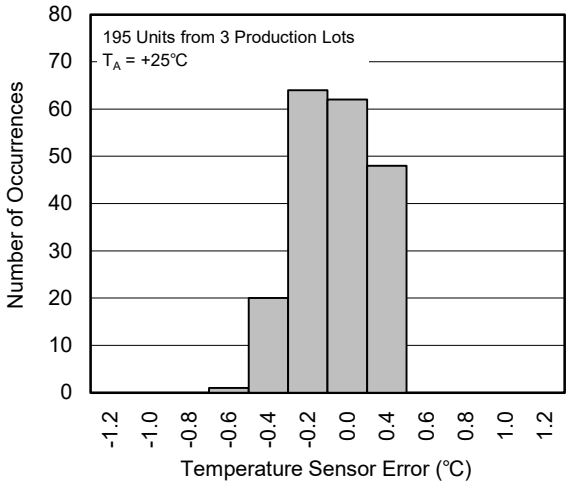
Temperature Sensor Error Histogram (UTQFN)



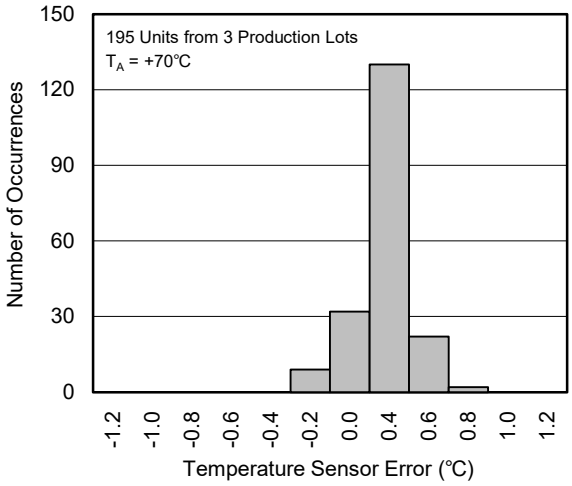
Temperature Sensor Error Histogram (UTQFN)



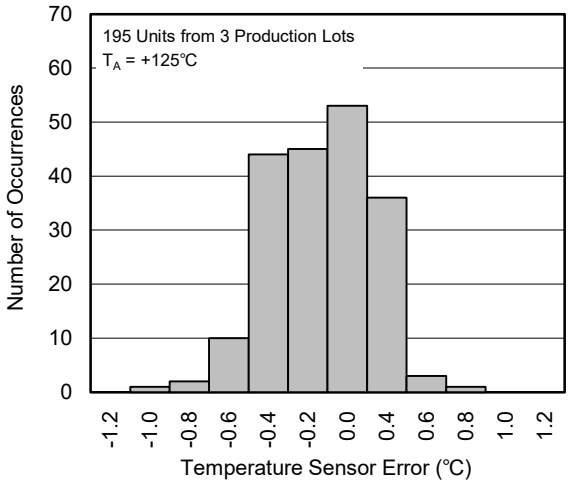
Temperature Sensor Error Histogram (UTQFN)



Temperature Sensor Error Histogram (UTQFN)



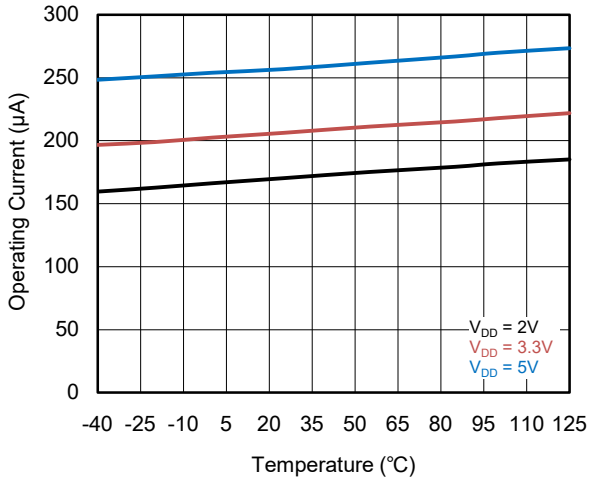
Temperature Sensor Error Histogram (UTQFN)



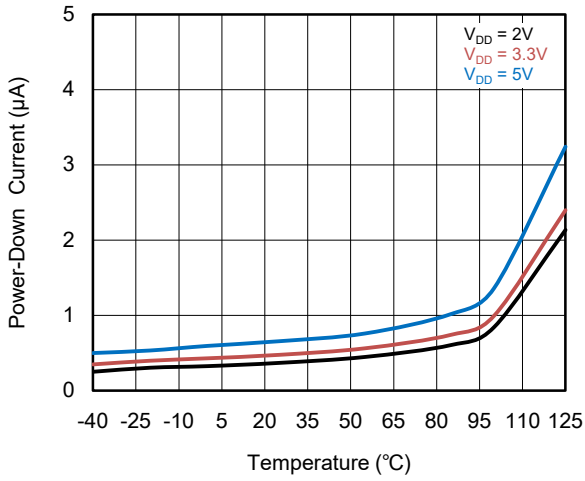
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_{DD} = 3.3V, FSR = ±2.048V, unless otherwise noted.

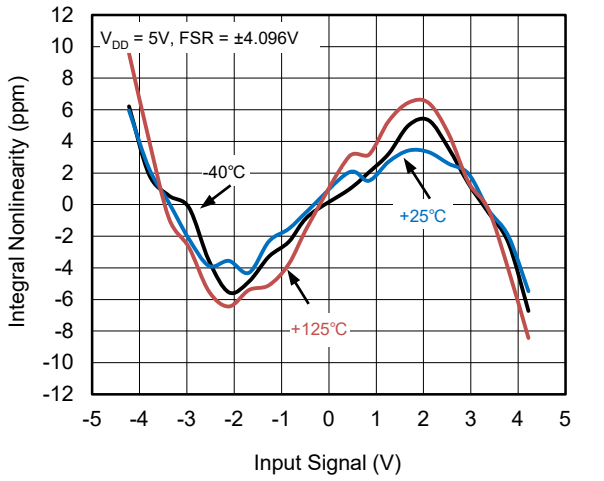
Operating Current vs. Temperature



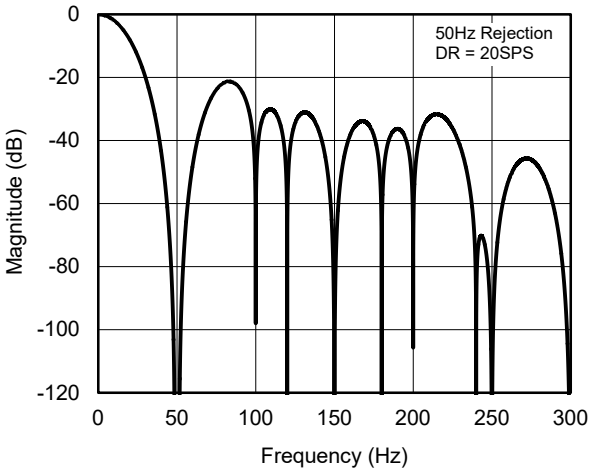
Power-Down Current vs. Temperature



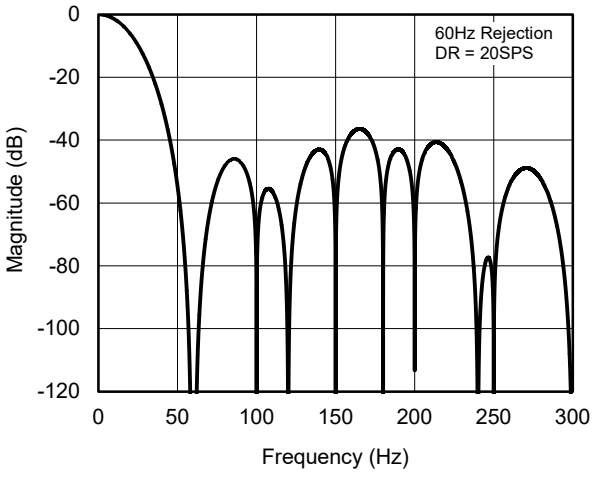
Integral Nonlinearity vs. Input Signal (External Reference)



Digital Filter Frequency Response



Digital Filter Frequency Response



APPLICATION CIRCUITS SAMPLE

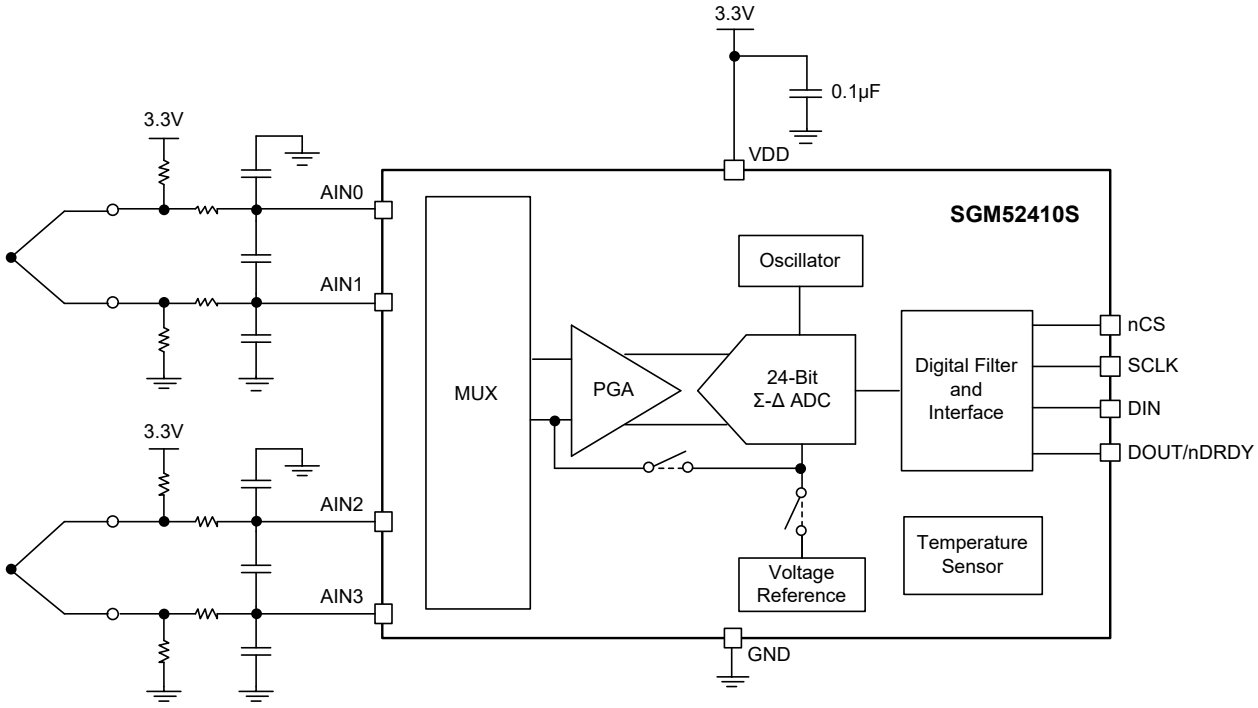


Figure 2. Thermocouple Measurement Using Cold-Junction Compensation by Integrated Temperature Sensor

FUNCTIONAL BLOCK DIAGRAM

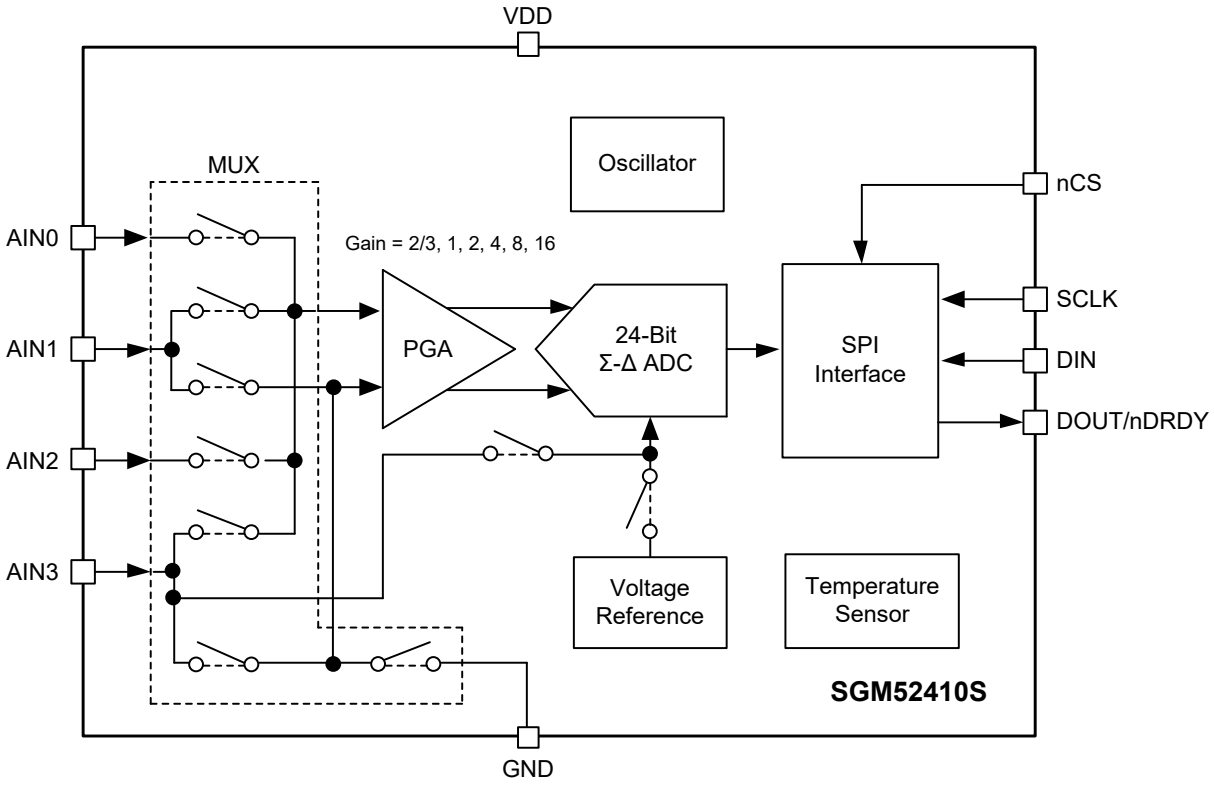


Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM52410S is a compact, energy-efficient, 24-bit ADC that utilizes sigma-delta technology. It consists of a core ADC with an adjustable gain, a clock oscillator, an internal voltage reference, and an SPI. Additionally, this device functions as a precise and linear temperature sensor. These features are designed to minimize the need for external circuitry and enhance overall performance. The functional block diagram of the SGM52410S is illustrated in Figure 3.

The SGM52410S provides two unique conversion modes: single-shot and continuous. In single-shot mode, the ADC executes a single conversion of the input signal upon receiving a request, saves the result in an internal Conversion register, and then enters a power-down state. This mode is ideal for systems that require periodic conversions or have long idle periods between conversions, as it significantly reduces power consumption. On the other hand, continuous conversion mode automatically initiates a new conversion of the input signal as soon as the previous one is completed, with the conversion rate matching the programmed data rate. Data can be accessed instantly and will consistently represent the most recently finished conversion.

Noise Performance

Sigma-delta (Σ-Δ) analog-to-digital converters (ADCs) utilize oversampling to function. The input signal of a Σ-Δ ADC is sampled at a high frequency, known as the modulator frequency. This signal is then filtered and decimated in the digital domain to produce a conversion result at the output data rate. The oversampling ratio (OSR), which is the ratio between the modulator frequency and output data rate, can be adjusted to optimize the ADC's noise performance by increasing the OSR and decreasing the output data rate. With an increase in OSR, a greater number of internal modulator samples are averaged to produce one conversion result, leading to a decrease in input-referred noise furthermore. Amplifying the ADC can also reduce input-referred noise, proving advantageous for measuring low-level signals.

Table 1 and Table 2 provide a concise overview of the device's noise performance, showcasing the typical noise performance at T_A = +25℃ with external shorted inputs. Table 1 exhibits the input-referred noise in μVRMS units, accompanied by μV_{PP} values in parentheses, while Table 2 showcases the corresponding data in effective number of bits (ENOB) derived from μVRMS values using Equation 1. The noise-free bits, determined from peak-to-peak noise values using Equation 2, are displayed in parentheses.

$$ENOB = \ln (FSR/V_{RMS\text{-}Noise})/\ln (2) \quad (1)$$

$$\text{Noise-Free Bits} = \ln (FSR/V_{PP\text{-}Noise})/\ln (2) \quad (2)$$

Table 1. Noise with Internal Reference (RMS in μV)

DR / FS (V)	960	480	200	100	50	20	10	5
6.144	137.60	72.21	47.48	24.27	18.01	12.04	8.84	6.83
4.096	93.99	47.90	29.56	15.40	12.06	8.49	6.53	4.36
2.048	45.57	23.17	15.60	8.25	6.10	4.10	3.22	1.96
1.024	24.93	13.50	8.77	4.73	3.49	2.67	1.67	1.09
0.512	12.22	6.78	4.55	2.51	1.75	1.24	0.90	0.54
0.256	6.32	3.60	2.39	1.22	0.96	0.70	0.44	0.30

Table 2. ADC ENOB (ENOB = ln (FSR/$V_{RMS\text{-}Noise}$)/ln (2))

DR / FS (V)	960	480	200	100	50	20	10	5
6.144	16.45	17.38	17.98	18.95	19.38	19.96	20.41	20.78
4.096	16.41	17.38	18.08	19.02	19.37	19.88	20.26	20.84
2.048	16.46	17.43	18.00	18.92	19.36	19.93	20.28	21.00
1.024	16.33	17.21	17.83	18.72	19.16	19.55	20.22	20.85
0.512	16.35	17.20	17.78	18.64	19.16	19.66	20.12	20.85
0.256	16.31	17.12	17.71	18.67	19.02	19.49	20.16	20.71

DETAILED DESCRIPTION (continued)

Multiplexer

The SGM52410S has an input multiplexer (MUX) shown in Figure 4, which can measure up to four single-ended or two differential signals. Additionally, the differential measurement of AIN0, AIN1, and AIN2 to AIN3 is possible. The MUX[2:0] bits in the Config register are responsible for configuring the multiplexer. In the case of single-ended signals, the ADC's negative input is internally connected to GND via the multiplexer's switch.

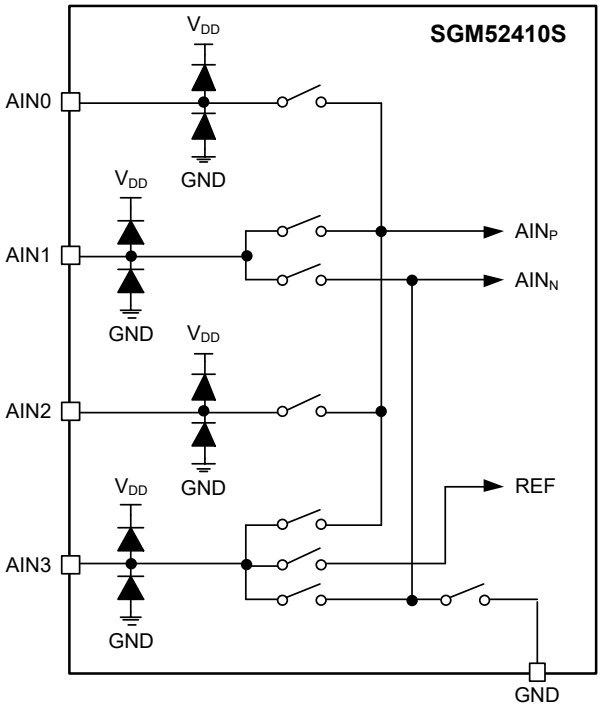


Figure 4. Input Multiplexer

In the event of measuring single-ended inputs, negative codes are not generated by the device, as they signify negative differential signals where (V_{AINP} - V_{AINN}) < 0. The SGM52410S inputs are safeguarded by ESD diodes to VDD and GND. To prevent the activation of ESD diodes, it is crucial to keep the voltage on each input within the specified limits defined in Equation 3.

$$GND - 0.3V < V_{AINx} < V_{DD} + 0.3V \quad (3)$$

If there is a possibility of the voltages on the input pins violating these conditions, it is advisable to use external Schottky diodes and series resistors to limit the input current to safe levels, as stated in the Absolute Maximum Ratings table. Overdriving an unused input on the SGM52410S can affect ongoing conversions on other input pins, so if overdriving unused inputs cannot be avoided, it is recommended to use external Schottky diodes to control the signal.

Analog Inputs

The SGM52410S has a switched capacitor input stage. There are charge and discharge current when ADC is working. The equal effective input impedance can be estimated by $R_{EFF} = V_{IN}/I_{AVERAGE}$.

The differential input impedance is Z_{DIFF} in Figure 5. Table 3 shows the typical differential input impedance.

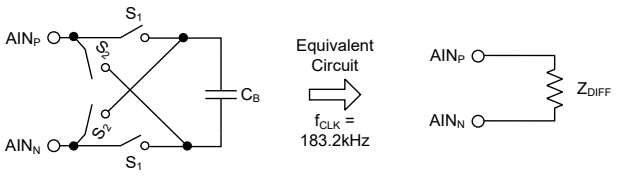


Figure 5. Simplified Analog Input Circuit

Table 3. Differential Input Impedance

FS (V)	Differential Input Impedance (MΩ)
±6.144 (1)	3.3
±4.096 (1)	2.7
±2.048	1.8
±1.024	1.8
±0.512	1
±0.256	0.6

NOTE:

1. FS = Full-scale range of the ADC scaling. In any event, it should not exceed V_{DD} + 0.3V applied to this device.

DETAILED DESCRIPTION (continued)

Full-Scale Input

The SGM52410S has an internal PGA. The PGA can be set to gains of 2/3, 1, 2, 4, 8 or 16. Table 4 and Table 5 show the corresponding full-scale (FS) ranges. Analog input voltages can never exceed the analog input voltage limits.

Table 4. PGA Gain Full-Scale Range with Internal Reference

PGA Setting	FS (V)
2/3	±6.144 (1)
1	±4.096 (1)
2	±2.048
4	±1.024
8	±0.512
16	±0.256

NOTE:

1. FS = Full-scale range of the ADC scaling. In any event, it should not exceed V_{DD} + 0.3V applied to this device.

Table 5. PGA Gain Full-Scale Range with External Reference

PGA Setting	FS (V)
2/3	±6.144 × V_{REF}/1.2
1	±4.096 × V_{REF}/1.2
2	±2.048 × V_{REF}/1.2
4	±1.024 × V_{REF}/1.2
8	±0.512 × V_{REF}/1.2
16	±0.256 × V_{REF}/1.2

NOTE:

1. It is important to ensure that the full-scale range of the ADC scaling is not exceeded. The device should not be subjected to voltages greater than V_{DD} + 0.3V.

Digital Filter

The device uses a linear-phase finite impulse response (FIR) digital filter that performs both filtering and decimation of the digital data stream coming from the modulator. The digital filter is automatically adjusted for the different data rates and always settles within a single cycle. At data rates of 5SPS, 10SPS and 20SPS, the filter can be configured to reject 50Hz or 60Hz line frequencies or to simultaneously reject 50Hz and 60Hz. Two bits (50/60[1:0]) in the configuration register are used to configure the filter accordingly. The frequency responses of the digital filter are illustrated in Typical Performance Characteristics section.

Output Data Rate (ODR)

Table 6. ADC Output Data Rate (SPS)

DR[2:0] Bits in Config Register	ODR (Hz)
000	5
001	10
010	20
011	50
100	100
101	200
110	480
111	960

Voltage Reference

The SGM52410S features an integrated voltage reference, and it is suitable for use with an external reference (default 1.208V). The gain error and gain drift specifications in the Electrical Characteristics section take into consideration any errors related to the initial voltage reference accuracy and reference drift with temperature.

Internal Oscillator

The SGM52410S comes equipped with an integrated oscillator that runs at 1MHz, eliminating the need for an external clock to operate the device. However, it is important to note that the internal oscillator may experience drift over time and temperature. The output data rate will adjust accordingly in proportion to the oscillator frequency.

DETAILED DESCRIPTION (continued)

Temperature Sensor

The SGM52410S is equipped with an integrated precision temperature sensor. To activate the temperature sensor mode, configure bit TS_MODE = 1 in the Config register. The temperature data is presented as a 14-bit outcome, aligned to the left within the 24-bit conversion result, with the most significant byte (MSB) being output first. The temperature measurement result can be determined by examining the first 14 bits when reading the two data bytes. Each 14-bit LSB is equivalent to 0.03125℃. Binary two's complement format is used to represent negative numbers, and Table 7 provides an illustration of this representation.

Table 7. 14-Bit Temperature Data Format

Temperature (℃)	Digital Output	
	Binary	Hex
128	01 0000 0000 0000	1000
127.96875	00 1111 1111 1111	0FFF
100	00 1100 1000 0000	0C80
75	00 1001 0110 0000	0960
50	00 0110 0100 0000	0640
25	00 0011 0010 0000	0320
0.25	00 0000 0000 1000	0008
0.03125	00 0000 0000 0001	0001
0	00 0000 0000 0000	0000
-0.25	11 1111 1111 1000	3FF8
-25	11 1100 1110 0000	3CE0
-40	11 1011 0000 0000	3B00

Converting from Temperature to Digital Codes

For positive temperatures:

When dealing with positive numbers, there is no need to use two's complement. Instead, the number can be converted to binary code using a 14-bit, left justified format with the most significant bit (MSB) set to 0 to indicate a positive sign.

Example: 50℃/(0.03125℃/count) = 1600 = 0640h = 00 0110 0100 0000

For negative temperatures:

To obtain the two's complement of a negative number, invert all the bits of the absolute binary number and add 1, and indicate the negative sign by setting the most significant bit (MSB) to 1.

Example: |-25℃|/(0.03125℃/count) = 800 = 0320h = 00 0011 0010 0000

Two's complement format: 11 1100 1101 1111 + 1 = 11 1100 1110 0000

Converting from Digital Codes to Temperature

To convert from digital codes to temperature, the first step is to check the value of the MSB. If the MSB is 0, the decimal code can be multiplied by 0.03125 ℃ to obtain the temperature value. However, if the MSB is 1, the result must be complemented and 1 must be subtracted before multiplying by -0.03125℃ to obtain the temperature value.

Example: The device reads back 0960h: 0960h has an MSB = 0.
0960h × 0.03125℃ = 2400 × 0.03125℃ = 75℃

Example: The device reads back 3CE0h: 3CE0h has an MSB = 1.
Subtract 1 and complement the result: 3CE0h → 0320h
0320h × (-0.03125℃) = 800 × (-0.03125℃) = -25℃

Device Functional Modes

Reset and Power-Up

Upon power-up, the SGM52410S undergoes a reset process that results in all bits in the Config register being set to their default values. The default behavior of the SGM52410S is to enter a power-down state upon start-up, where the device interface and digital blocks are active but no data conversions are performed. This initial power-down state is designed to prevent power surges during start-up, particularly for systems with strict power supply requirements.

Operating Modes

The operating mode of the SGM52410S can be either continuous-conversion or single-shot, and it is determined by the state of the MODE bit in the Config register.

Single-Shot Mode and Power-Down

When the MODE bit in the Config register is set to 1, the SGM52410S goes into a power-saving mode and performs a single conversion when the SS bit in the Config register is set to 1. This is the default state when the device is first powered on, but it still responds to commands. The SGM52410S will stay in this power-saving mode until the SS bit is set to 1. Once the SS bit is set, the device powers up, performs a single conversion, and then powers down again. If a conversion is already in progress, setting the SS bit to 1 will have no effect. In order to switch to continuous conversion mode, the MODE bit in the Config register should be set to 0.

Continuous-Conversion Mode

When the MODE bit in the Config register is set to 0, the SGM52410S operates in continuous-conversion mode, performing conversions continuously. After each conversion, the result is stored in the Conversion register, and the device immediately starts another conversion. To activate the single-shot mode, either set the MODE bit to 1 in the Config register or perform a device reset.

DETAILED DESCRIPTION (continued)

Duty Cycling for Low Power

Lowering the output data rate of a Σ-Δ ADC can improve its noise performance because more samples of the internal modulator can be averaged to produce a single conversion result. However, for applications focused on power efficiency, the enhanced noise performance at lower data rates may not be a critical requirement. To address this, the SGM52410S supports duty cycling, which can significantly reduce power consumption by periodically requesting high data rate readings at an effectively lower data rate. For example, an SGM52410S with a data rate set to 960SPS can be instructed by a microcontroller to perform a single-shot conversion every 200ms (5SPS) while in power-down state. Since a conversion at 960SPS takes only about 1.1ms, the SGM52410S can enter power-down state for the remaining 198.9ms. This configuration can reduce power consumption to approximately 1/200th of what is consumed in continuous conversion mode. The duty cycling rate is entirely up to the master controller and can be adjusted as needed. The SGM52410S also offers lower data rates without duty cycling and improved noise performance if required.

Programming

Serial Interface

The SPI-compatible serial interface can be configured with either four signals (nCS, SCLK, DIN, and DOUT/nDRDY) or three signals (with nCS tied low). This interface enables various functions including reading conversion data, reading and writing registers, and controlling device operation.

Chip Select (nCS)

The SGM52410S can be selected for SPI communication using the chip select pin (nCS), which is particularly useful when multiple devices share the same serial bus. During communication, nCS should be kept low. Raising nCS resets the serial interface, causing SCLK to be ignored and DOUT/nDRDY to enter a high-impedance state, preventing it from providing data-ready indication. To monitor DOUT/nDRDY in situations where multiple devices are present, nCS should be lowered periodically. When this occurs, DOUT/nDRDY will either instantly go high to indicate the absence of new data or instantly go low to indicate the presence of new data in the Conversion register, ready for transfer. Data can be transferred without concern about data corruption. Throughout the transmission process, the current result remains locked in the output shift register and remains unchanged until the communication is completed, ensuring data integrity and preventing any potential data corruption.

Serial Clock (SCLK)

The SCLK is a Schmitt-triggered input that is responsible for clocking data on the DIN and DOUT/nDRDY pins into and out of the SGM52410S. Although the input features hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. By holding SCLK low for 28ms, the serial interface resets, and a new communication cycle starts with the next SCLK pulse, providing an opportunity to recover interrupted serial interface transmissions using this time-out feature. When the serial interface is idle, SCLK should be held low.

Data Input (DIN)

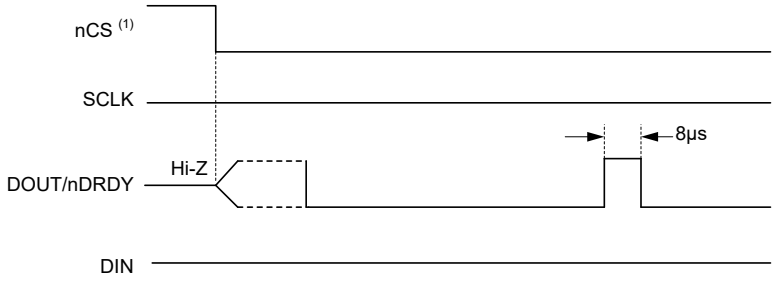
The DIN pin is used in conjunction with SCLK to transmit data to the SGM52410S. The SGM52410S latches data on DIN during the falling edge of SCLK, with the crucial distinction that the device never actively drives the DIN pin.

Data Output and Data Ready (DOUT/nDRDY)

The DOUT/nDRDY pin is utilized in conjunction with SCLK to extract conversion and register data from the SGM52410S. On the SCLK rising edge, the data is shifted out through DOUT/nDRDY. Additionally, DOUT/nDRDY indicates the completion of a conversion and the availability of new data. When new data is ready for retrieval, DOUT/nDRDY transitions low. It can also initiate the reading of data from the SGM52410S by triggering a microcontroller. In continuous-conversion mode, if no data is retrieved from the device, DOUT/nDRDY transitions high 8μs before the next data ready signal (DOUT/nDRDY low). This transition is depicted in Figure 6. It is important to complete the data transfer before DOUT/nDRDY returns high.

When nCS is set to a high state, DOUT/nDRDY is equipped with a weak internal pull-up resistor as a default configuration. By incorporating this functionality, the aim is to reduce the likelihood of DOUT/nDRDY floating around the midsupply level, which could potentially cause leakage current in the master device. To deactivate this pull-up resistor and switch the device to a high-impedance state, the PULL_UP_EN bit in the Config register should be set to 0.

DETAILED DESCRIPTION (continued)



NOTE:

1. nCS may be held low. When nCS is in a low state, DOUT/nDRDY is also low, indicating the availability of new data.

Figure 6. DOUT/nDRDY Behavior without Data Retrieval in Continuous Conversion Mode

Data Format

The SGM52410S produces data in a 24-bit binary two's complement format. An input signal at full-scale produces an output code with a positive value of 7FFFFFh and a negative value of 800000h. When the input signal exceeds full-scale, the output clips at these codes. Table 8 provides an overview of the ideal output codes for various input signals.

Table 8. Input Signal versus Ideal Output Code

Input Signal, V_{IN} (AIN_P - AIN_N)	Ideal Output Code (1)
≥ +FS (2^{23} - 1)/2^{23}	7FFFFFh
+FS/2^{23}	000001h
0	0
-FS/2^{23}	FFFFFFh
≤ -FS	800000h

NOTE:

1. Except for the impact of noise, integral nonlinearity (INL), offset, and gain errors.

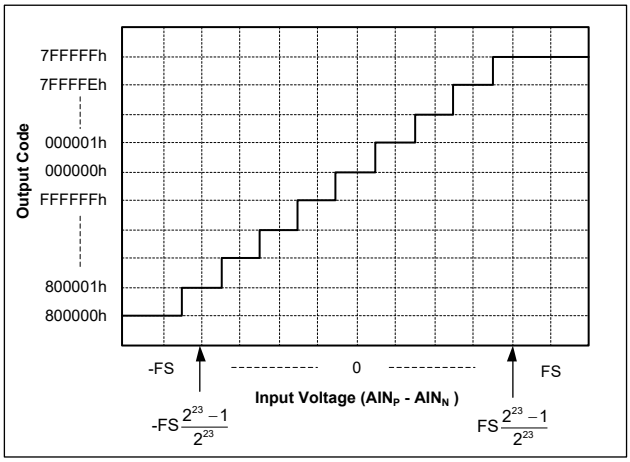


Figure 7. Code Transition Diagram

Data Retrieval

Data transfer to and from the SGM52410S is performed in the same way for both single-shot and continuous conversion modes, without requiring any commands to be issued. The MODE bit in the Config register is used to select the operating mode for the SGM52410S.

To activate continuous-conversion mode, set the MODE bit to 0. In this mode, the device initiates new conversions continuously, even when nCS is high.

Activate single-shot mode by setting the MODE bit to 1, and initiate a new conversion by setting the SS bit to 1.

The conversion data is continuously buffered and remains unchanged until new conversion data replaces it. Therefore, there is no risk of data corruption when reading the data at any time. When DOUT/nDRDY goes low, it indicates the availability of new conversion data. This data is obtained by shifting it out on DOUT/nDRDY, with the most significant bit (bit 23) being clocked out on the first SCLK rising edge. Additionally, new configuration register data is latched on DIN during the SCLK falling edge, simultaneously with the conversion result being clocked out of DOUT/nDRDY.

The SGM52410S offers the added advantage of direct readback of Config register settings within the same data transmission cycle, which is 64 bits (when Config register data readback is enabled), with or without CRC enablement.

DETAILED DESCRIPTION (continued)

Chip Software Reset

The SGM52410S supports software reset function to reset the chip by sending data 0x1100 1011 0xxx xxxx to Config2 register D[15:7], and then a reset flag will be set in Config2 register D[0] for an indication during next read operation.

64-Bit Data Transmission Cycle with CRC

In a 64-bit data transmission cycle with CRC (7-bit), the data is comprised of eight bytes. Three bytes are for the conversion result, and the remaining four bytes are for the Config1 and Config2 register readback. The device always reads the most significant byte (MSB) first.

Please note that, as CRC function is only available on DOUT, so to achieve an improved data exchange robustness, suggest the processor verifies all the configuration data read from DOUT with what processor sends to DIN, to make sure the ADC receive the correct configuration data from DIN without corruption.

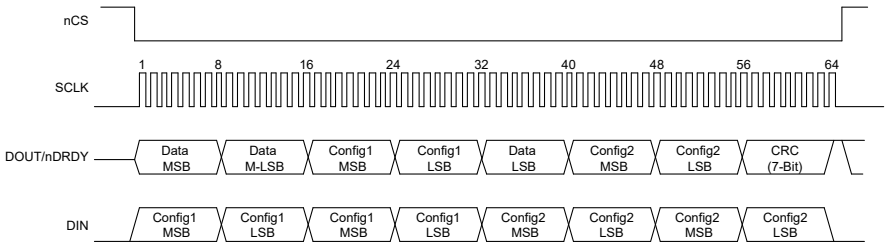


Figure 8. 64-Bit Data Transmission Cycle with Config1 + Config2 + CRC Register Readback

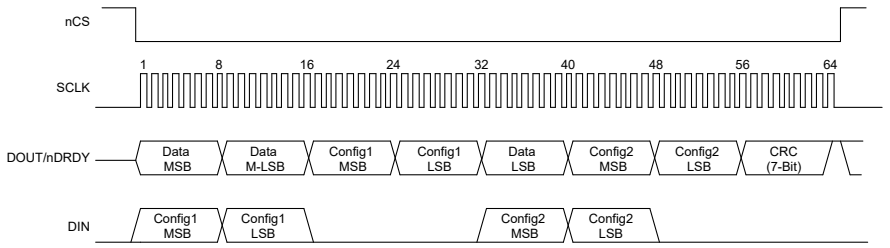


Figure 9. 64-Bit Data Transmission Cycle: DIN Held Low

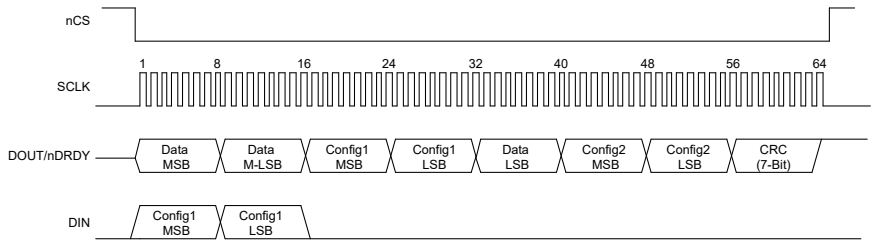


Figure 10. 64-Bit Data Transmission Cycle with Config1: DIN Held Low

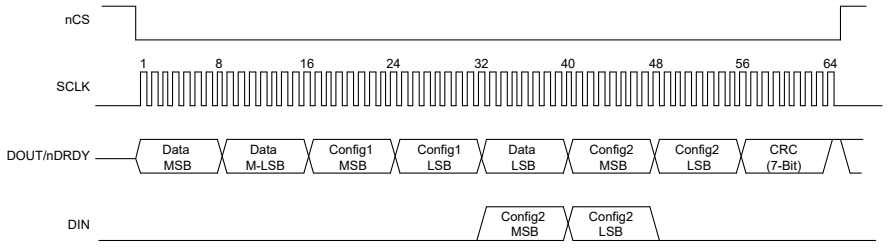


Figure 11. 64-Bit Data Transmission Cycle with Config2: DIN Held Low

DETAILED DESCRIPTION (continued)

64-Bit Data Transmission Cycle without CRC

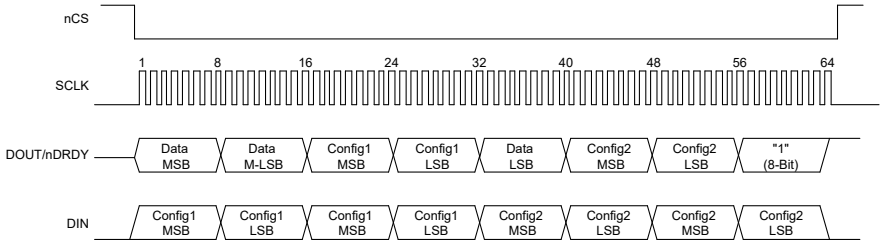


Figure 12. 64-Bit Data Transmission Cycle with Config1 + Config2 Register Readback

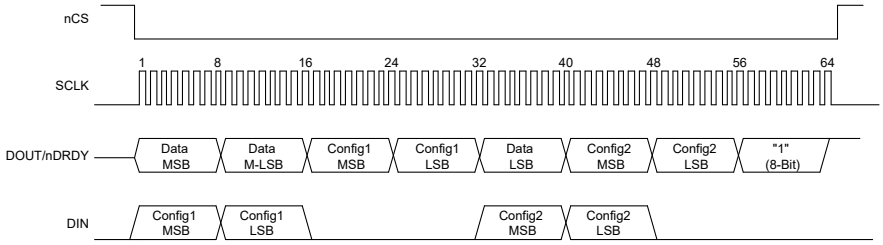


Figure 13. 64-Bit Data Transmission Cycle: DIN Held Low (without CRC)

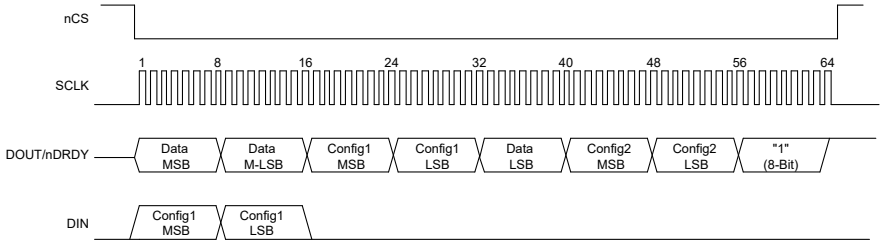


Figure 14. 64-Bit Data Transmission Cycle with Config1: DIN Held Low (without CRC)

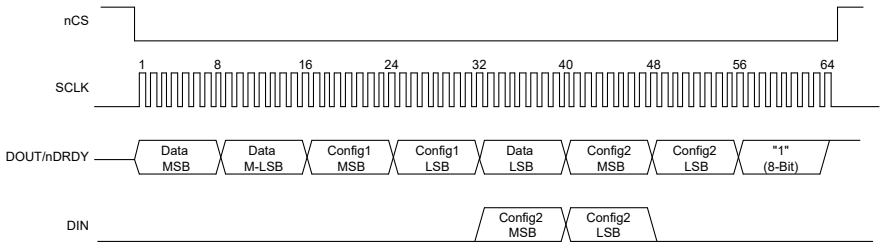


Figure 15. 64-Bit Data Transmission Cycle with Config2: DIN Held Low (without CRC)

CRC Calculation

The checksum, which is 7 bits wide, is generated using the polynomial $x^7 + x^2 + x^1 + 1$. To generate the checksum, the data is left shifted by seven bits to create a number ending in seven Logic 0s. The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An XOR (exclusive OR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This is the 7-bit checksum.

REGISTER MAPS

The SGM52410S can be controlled and monitored through the SPI interface, which provides access to two registers. The Conversion register stores the outcome of the latest conversion, while the Config register allows users to modify the device's operating modes and obtain its status information.

Conversion Register [Reset = 0x0000]

The Conversion register of the SGM52410S is a 24-bit register that stores the result of the latest conversion in binary two's complement format. When the device is powered on, the Conversion register is set to 0 and remains at 0 until the first conversion is finished. Table 9 displays the register format.

Config1 Register [Reset = 0x058B]

Table 11 displays the details of the 16-bit Config register, which allows users to control various aspects of the SGM52410S operation, such as input selection, data rate, full-scale range, temperature sensor mode, and operating mode.

Table 9. 24-Bit Conversion Register (Read-Only)

MSB LSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 10. Conversion Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[23:0]	Bit 23 to Bit 0	000000h	R	24-bit conversion result.

Table 11. 16-Bit Config1 Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	SS	0	R/W	Single-Shot Conversion Start The SS bit is used to initiate a single conversion and can only be modified when the device is powered down, without affecting an ongoing conversion. When writing: 0 = No effect (default) 1 = Start a single conversion (when in power-down state) Always reads back 0 (default).
D[14:12]	MUX[2:0]	000	R/W	Input Multiplexer Configuration These bits are responsible for configuring the input multiplexer. 000 = AIN_P is AIN0 and AIN_N is AIN1 (default) 001 = AIN_P is AIN0 and AIN_N is AIN3 010 = AIN_P is AIN1 and AIN_N is AIN3 011 = AIN_P is AIN2 and AIN_N is AIN3 100 = AIN_P is AIN0 and AIN_N is GND 101 = AIN_P is AIN1 and AIN_N is GND 110 = AIN_P is AIN2 and AIN_N is GND 111 = AIN_P is AIN3 and AIN_N is GND
D[11:9]	PGA[2:0]	010	R/W	Programmable Gain Amplifier Configuration These bits are responsible for configuring the programmable gain amplifier. 000 = FSR is ±6.144V (1) 001 = FSR is ±4.096V (1) 010 = FSR is ±2.048V (default) 011 = FSR is ±1.024V 100 = FSR is ±0.512V 101 = FSR is ±0.256V 110 = FSR is ±0.256V 111 = FSR is ±0.256V
D[8]	MODE	1	R/W	Device Operating Mode This bit is responsible for controlling the SGM52410S operating mode. 0 = Continuous conversion mode 1 = Power-down and single-shot mode (default)

NOTE:

1. This parameter specifies the full-scale range of the ADC scaling and indicates the maximum voltage that can be applied to the device, which is V_{DD} + 0.3V.

REGISTER MAPS (continued)

Table 11. 16-Bit Config1 Register Details (continued)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	DR[2:0]	100	R/W	Data Rate These bits are responsible for controlling the data rate setting. 000 = 5SPS 001 = 10SPS 010 = 20SPS 011 = 50SPS 100 = 100SPS (default) 101 = 200SPS 110 = 480SPS 111 = 960SPS
D[4]	TS_MODE	0	R/W	Temperature Sensor Mode This bit is responsible for configuring the ADC to convert temperature or input signals. 0 = ADC mode (default) 1 = Temperature sensor mode
D[3]	PULL_UP_EN	1	R/W	Pull-Up Enable When the nCS is high, this bit enables a weak internal pull-up resistor specifically on the DOUT/nDRDY pin, connecting the bus line to the power supply with a 400kΩ internal resistor. When disabled, the DOUT/nDRDY pin remains unconnected. 0 = Pull-up resistor disabled on DOUT/nDRDY pin 1 = Pull-up resistor enabled on DOUT/nDRDY pin (default)
D[2:1]	NOP[1:0]	01	R/W	No Operation The NOP[1:0] bits determine whether data is written to the Config register or not, based on their specific configuration. To write data to the Config register, the NOP[1:0] bits must be set to '01'. Any different value will lead to a NOP command. It is possible to hold DIN high or low during SCLK pulses without any data being written to the Config register. 00 = The data is invalid and should not be used to update the contents of the Config register 01 = Valid data, update the Config register (default) 10 = The data is invalid and should not be used to update the contents of the Config register 11 = The data is invalid and should not be used to update the contents of the Config register
D[0]	Reserved	1	R	Reserved Writing a value of either 0 or 1 to this bit will not have any effect. The bit will always read back as 1.

REGISTER MAPS (continued)

Config2 Register [Reset = 0x4080]

Table 12 displays the details of the 16-bit Config2 register, which allows users to control various aspects of the SGM52410S operation, such as chip ID, versions, CRC enable, EXT_REF and reset function.

Table 12. 16-Bit Config2 Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:12]	ID[3:0]	0100	R/W	Chip ID (Write operation only use for reset)
D[11:9]	ID_VER[2:0]	000	R/W	Chip Version Number (Write operation only use for reset)
D[8:7]	NOP[1:0]	01	R/W	No Operation The NOP[1:0] bits determine whether data is written to the Config register or not, based on their specific configuration. To write data to the Config register, the NOP[1:0] bits must be set to '01'. Any different value will lead to a NOP command. It is possible to hold DIN high or low during SCLK pulses without any data being written to the Config register. 00 = The data is invalid and should not be used to update the contents of the Config register 01 = Valid data, update the Config register (default) 10 = The data is invalid and should not be used to update the contents of the Config register 11 = The data is invalid and should not be used to update the contents of the Config register
D[6:5]	Reserved	00	R/W	Reserved
D[4]	CRC_EN	0	R/W	0 = CRC disabled (default) 1 = CRC enabled (7 bits)
D[3]	EXT_REF	0	R/W	0 = None (default) 1 = Use AIN3 as external reference for ADC
D[2:1]	50/60[1:0]	00	R/W	FIR Filter Configuration These bits configure the filter coefficients for the internal FIR filter. Only use these bits together with the 20SPS setting in normal mode and the 5SPS setting in duty-cycle mode. Set to 00 for all other data rates. 00 = No 50Hz or 60Hz rejection (default) 01 = Simultaneous 50Hz and 60Hz rejection 10 = 50Hz rejection only 11 = 60Hz rejection only
D[0]	RES_FG	0	RC (1)	Reset Flag 0 = No reset occur (default) 1 = Reset occur (resume to 0 after reading)

NOTE:

1. RC = Read Clear.

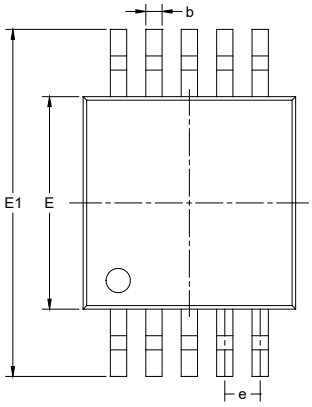
REVISION HISTORY

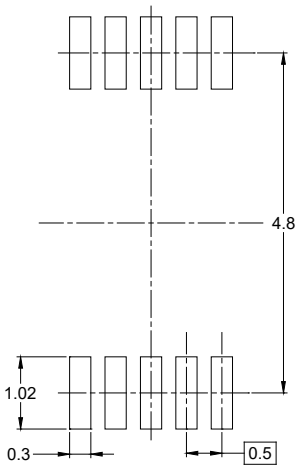
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (APRIL 2025) to REV.A	Page
Changed from product preview to production data	All

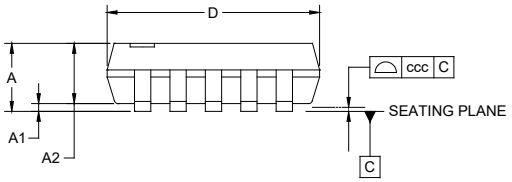
PACKAGE OUTLINE DIMENSIONS

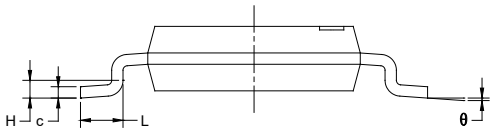
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)



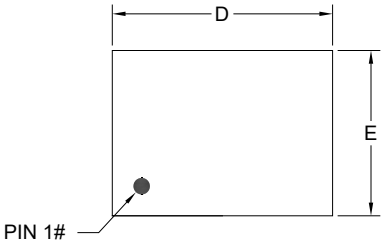


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.170	-	0.330
c	0.080	-	0.230
D	2.900	-	3.100
E	2.900	-	3.100
E1	4.750	-	5.050
e	0.500 BSC		
H	0.250 TYP		
L	0.400	-	0.800
θ	0°	-	8°
ccc	0.100		

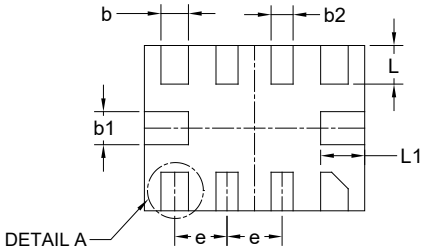
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

PACKAGE OUTLINE DIMENSIONS

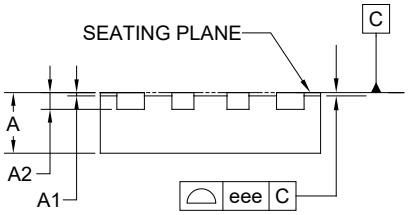
UTQFN-2×1.5-10L



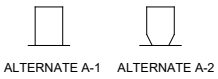
TOP VIEW



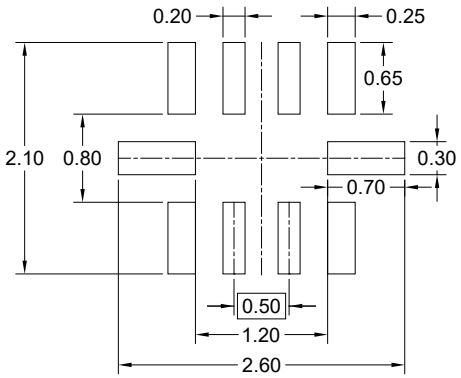
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



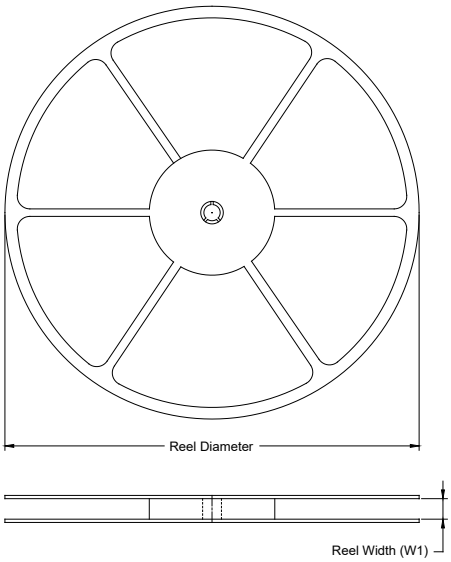
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.000	-	0.050
A2	0.152 REF		
b	0.200	0.250	0.300
b1	0.250	0.300	0.350
b2	0.150	0.200	0.250
D	1.900	2.000	2.100
E	1.400	1.500	1.600
L	0.250	0.350	0.450
L1	0.300	0.400	0.500
e	0.500 BSC		
eee	0.050		

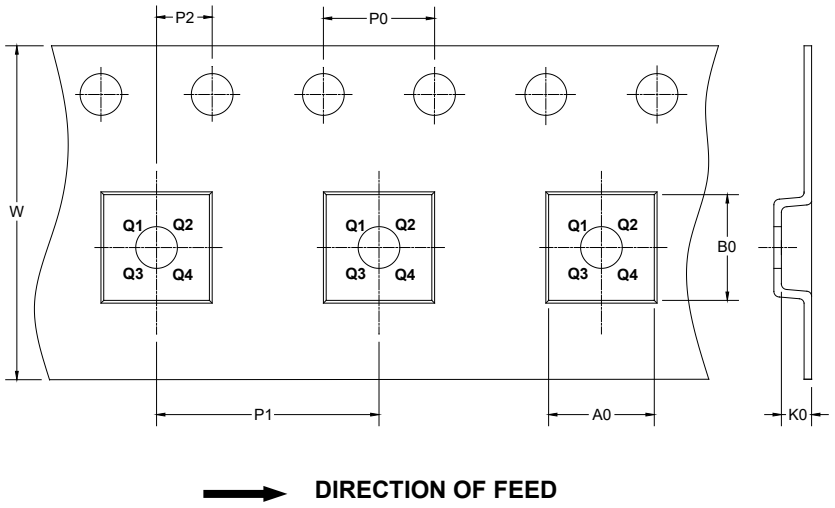
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



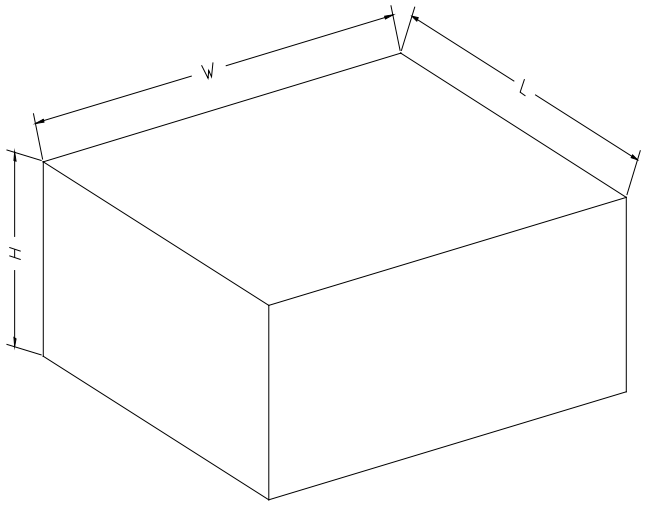
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
UTQFN-2×1.5-10L	7″	9.5	1.70	2.30	0.75	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002