SGM4551B
Dual Bidirectional I²C Bus and SMBus Voltage-Level Translator

GENERAL DESCRIPTION

The SGM4551B is a 2-bit, SMBus, dual, bidirectional, I^2C voltage translator with the ability of enable (EN) function. For V_{REF1}, the typical operation range is from 1.2V to 3.3V and the typical operation for V_{REF2} is from 1.8V to 5.5V.

The signal can be transmitted bilaterally from 1.2V to 5V. The propagation delay is significant small as the low on-resistance of SGM4551B. Also, if the EN pin is in high position, the voltage translator is transparent and then it allows the connection between SCL1 and SCL2, SDA1 and SDA2 respectively. In addition, in this state, the transmitting direction is bidirectional. However, the transmitting will be suspended if the EN pin is in low state as the high-impedance property at this moment.

For the applications, the connections of the devices and bus length are limited as the 400pF capacitance of the bus pin. However, SGM4551B allows the isolation between two sides of I^2C bus so that more and more I^2C devices can be added and connected with SGM4551B.

Two different kinds of bus frequencies are supported by SGM4551B, one is 400kHz and the other is 100kHz. Also, if two frequencies for the buses are required, the priority of 400kHz should be always higher than that of 100kHz. Because of the adding of the additional delay, the operational frequency of the device must be lower than 400kHz if the frequency of the master is equal to 400kHz.

For the application of standard I^2C, the pull-up resistor is required for the logic high levels, which means that the operation for I^2C in this case is open-drain. Each side of the repeater requires a pull-up resistor and the value of resistor depends on the operation of SGM4551B. Also, when multiple masters are connected with SGM4551B, the standard operation current is 3mA, and high current can be taken into account under the specific conditions.

The resistance between SDA1 and SDA2 is low when the state of them is low. However, if the state of SDA1 or SDA2 is high, the level of high position depends on the corresponding voltage reference. In the transparent mode, when the position of SDA1 is high, SDA2 must be pulled to a high level through the pull-up resistor. In addition, the transition for high and low voltage is seamless which can be selected by the users.

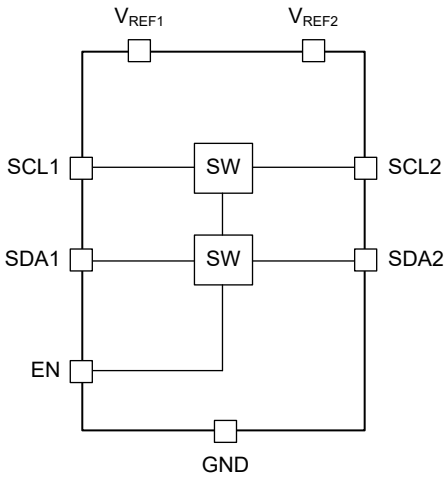
Because of the same electrical characteristics for all the outputs of SGM4551B, so that the deviations of the propagation delay and voltage is extremely small. In addition, this advantage is good for the transition of discrete transistors as the symmetrical switch inside SGM4551B. On top of this, SGM4551B can also provide the protection of ESD for the devices with weak ESD ability.

The SGM4551B is available in Green SOT-23-8 and VSSOP-8 packages. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- Bidirectional I²C Translator
- Support I²C and SMBus Compatible
- Propagation Delay: Less than 5.5ns
- Acceptable Voltage Reference
  - 1.2V V_{REF1} and 1.8V, 2.5V, 3.3V, or 5V V_{REF2}
  - 1.8V V_{REF1} and 2.5V, 3.3V, or 5V V_{REF2}
  - 2.5V V_{REF1} and 3.3V or 5V V_{REF2}
  - 3.3V V_{REF1} and 5V V_{REF2}
- Low On-Resistance: 3.5Ω (TYP)
- GPIO Ports with I²C Open-Drain Logic (SCL1, SDA1, SCL2 and SDA2)
- Mixed-Mode Signal be Supported by I/O Ports with 5V Tolerant
- When EN is Low, SGM4551B is in High-Impedance Mode
- Lock-Up-Free Operation for Isolation when EN = Low
- The Pinout of the Internal Material is Beneficial for PCB Layout
- Available in Green SOT-23-8 and VSSOP-8 Packages

LOGIC DIAGRAM



FUNCTION TABLE

EN (1)	FUNCTION
H	SCL1 = SCL2, SDA1 = SDA2.
L	Disconnect.

NOTE:

1. The transparent mode will be launched if the voltage of EN pin is 1V higher than the voltage of SCL1 and SCL2. And so does the condition of SDA. H = HIGH level, L = LOW level.

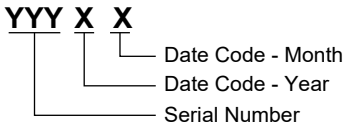
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM4551B	SOT-23-8	-40℃ to +85℃	SGM4551BYN8G/TR	SZ6XX	Tape and Reel, 3000
	VSSOP-8	-40℃ to +85℃	SGM4551BYVS8G/TR	1J6 XXXX	Tape and Reel, 3000

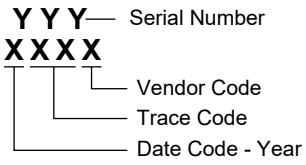
MARKING INFORMATION

NOTE: XX = Date Code. XXXX = Date Code, Trace Code and Vendor Code.

SOT-23-8



VSSOP-8



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

DC Reference Voltage Range

V_{REF1} ..... -0.3V to 6V

V_{REF2} ..... -0.3V to 6V

Input Voltage Range (1), V_I ..... -0.3V to 6V

Input/Output Voltage Range (1), $V_{I/O}$ ..... -0.3V to 6V

Continuous Channel Current 64mA

Input Clamp Current, I_{IK} (V_I < 0) ..... -50mA

Package Thermal Resistance

SOT-23-8, θ_{JA} ..... 198.3℃/W

SOT-23-8, θ_{JB} ..... 102.6℃/W

SOT-23-8, θ_{JC} ..... 157℃/W

VSSOP-8, θ_{JA} ..... 189℃/W

VSSOP-8, θ_{JB} ..... 123℃/W

VSSOP-8, θ_{JC} ..... 56.5℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (2) (3)

HBM ..... ±3000V

CDM ..... ±1000V

NOTES:

1. When the input and output current ratings are observed, the input and I/O negative voltage ratings may be exceeded.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

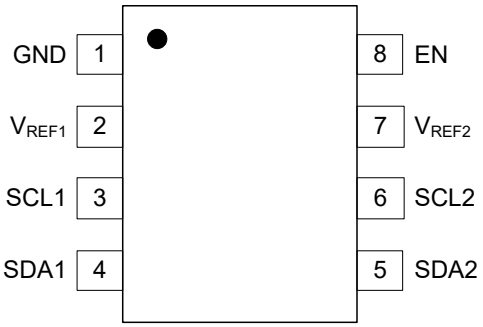
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

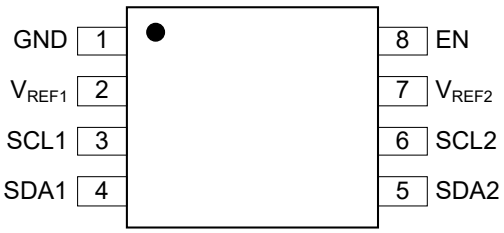
PIN CONFIGURATIONS

(TOP VIEW)



SOT-23-8

(TOP VIEW)



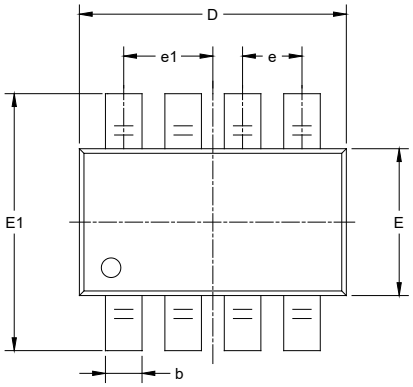
VSSOP-8

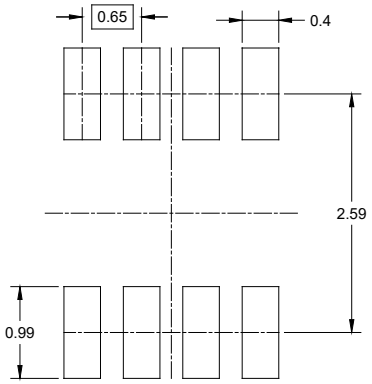
PIN DESCRIPTION

PIN		NAME	FUNCTION
SOT-23-8	VSSOP-8		
1	1	GND	Ground.
2	2	V_{REF1}	Low-side Reference Supply Voltage for SCL1 and SDA1.
3	3	SCL1	Low-side Clock Signal.
4	4	SDA1	Low-side Data Signal.
5	5	SDA2	High-side Data Signal.
6	6	SCL2	High-side Clock Signal.
7	7	V_{REF2}	High-side Reference Supply Voltage for SCL2 and SDA2.
8	8	EN	Enable Control Pin.

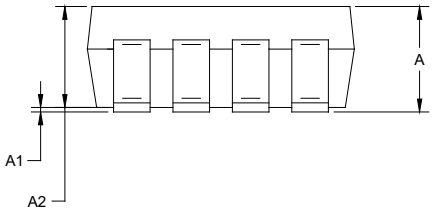
PACKAGE OUTLINE DIMENSIONS

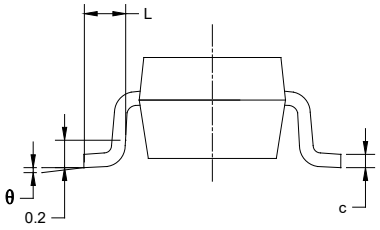
SOT-23-8





RECOMMENDED LAND PATTERN (Unit: mm)



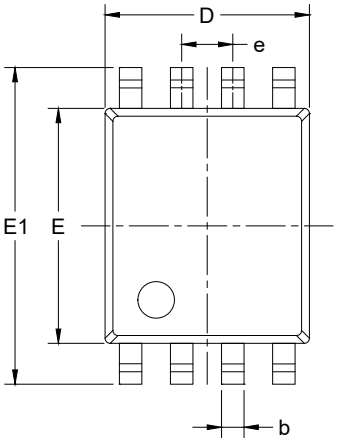


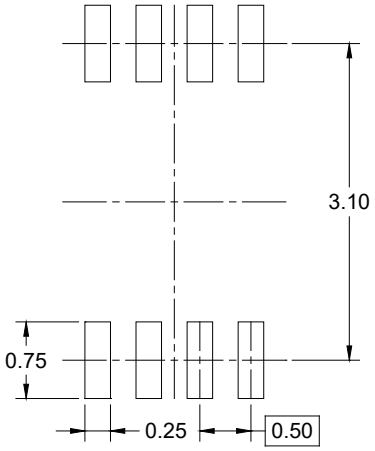
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.650 BSC		0.026 BSC	
e1	0.975 BSC		0.038 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

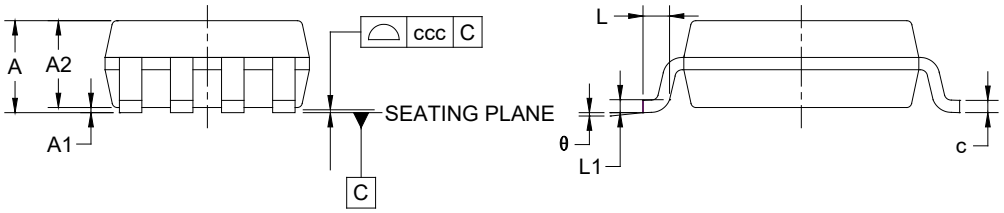
PACKAGE OUTLINE DIMENSIONS

VSSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)

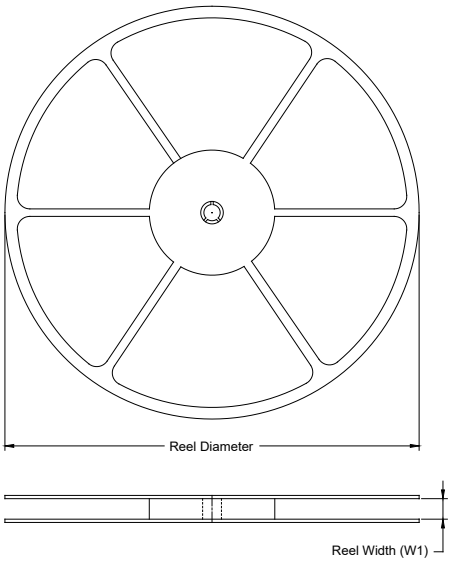


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.000
A1	0.000	-	0.150
A2	0.600		0.850
b	0.170	-	0.270
c	0.080		0.230
D	1.900	-	2.100
E	2.200	-	2.400
E1	3.000	-	3.200
e	0.500 BSC		
L	0.150	-	0.400
L1	0.120 BSC		
θ	0°	-	8°
ccc	0.100		

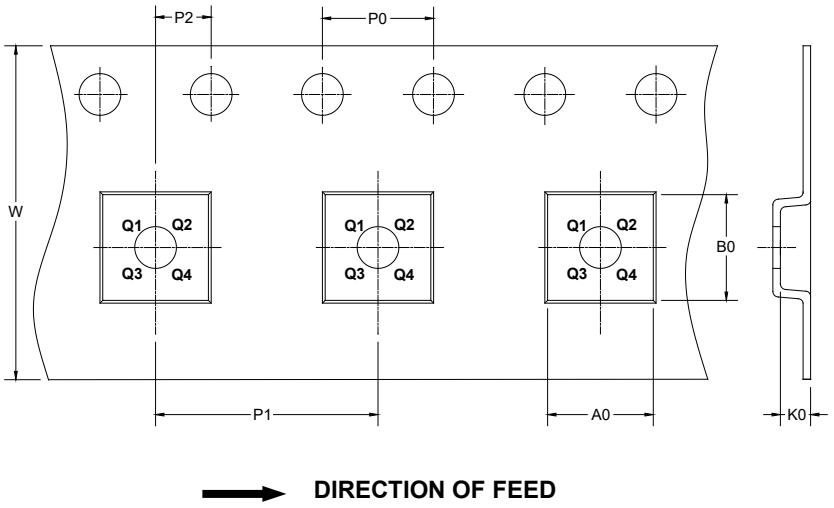
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187 CA.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



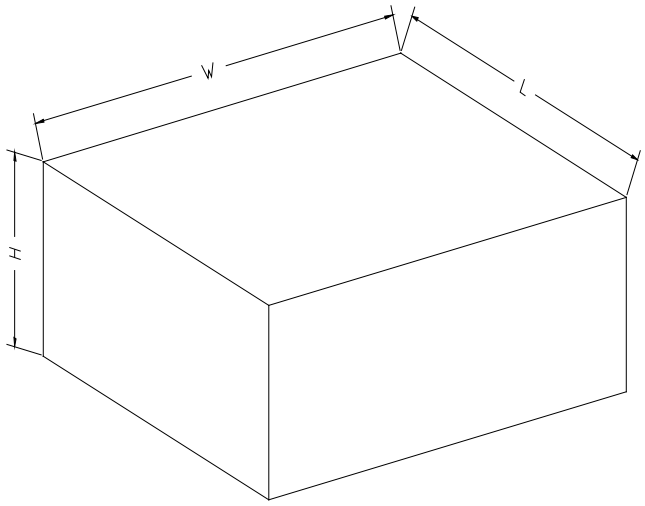
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-8	7″	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3
VSSOP-8	7″	9.5	2.25	3.35	1.05	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002