# SGM41517A
# Fully Integrated Switch-Mode Charger with USB Compliance and USB OTG Support

## GENERAL DESCRIPTION

The SGM41517A is a tiny, high-efficiency, USB supported switch-mode charger, which can be used to charge the single-cell Li-Ion and Li-polymer batteries in portable applications.

The SGM41517A has the $I^2C$ interface to program the charging parameters. It integrates a synchronous PWM controller, input and output current sensing, high-accuracy voltage and current regulation, power MOSFETs, and charge termination.

The SGM41517A charges the battery in three stages: short charging current, constant current charging, and constant voltage charging. The input current is automatically limited to the value set by host. The device terminates the charging based on the battery voltage and user selectable minimum current level. The charging safety timer provides the additional protection for the battery. During normal operation, if the battery voltage drops below the internal threshold, the IC will automatically restart the charging cycle and enter the sleep mode or the high-impedance mode when the input power is disconnected. The charging status can be read back to the host by the $I^2C$ interface. This device also features thermal regulation in which the charge current is reduced if the junction temperature exceeds 120℃.

For supporting the USB OTG device, the SGM41517A can boost the battery voltage to 5.05V by default at VBUS node.

The SGM41517A is available in a Green UTQFN-2×2-20L package.

## APPLICATIONS

Portable Audio Speaker
Mobile Phone
Wearables
EPOS

## FEATURES

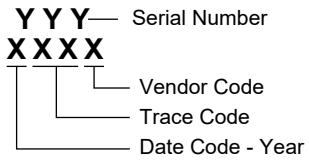
- **4V to 13.2V Operating Input Voltage Range**
- **19V Absolute Maximum Input Voltage Rating**
- **Instant-On with No Battery**
- **Maximum Power Tracking by Programmable Input Voltage Limit (VINDPM)**
- **Bad Adapter Detection and Recognition**
- **Safety Limit Register for Maximum Charge Voltage and Current Limiting**
- **Integrated Input Current Sensing and Limiting**
- **Integrated Power FETs for up to 2A Charge Current**
- **Programmable Charging Parameters via $I^2C$-Compatible Interface (up to 1Mbps):**
  - **VINDPM Threshold**
  - **Input Current Limit**
  - **Fast-Charge/Termination Current**
  - **Charge Regulation Voltage: 3.5V to 4.6V**
  - **Termination Function**
- **Integrated Charging Current Sensing Resistor**
- **Operating at 1.5MHz/500kHz in Charger Mode, 1.5MHz in Boost Mode**
- **Status Indication for Charging and Faults**
- **USB Friendly Startup Sequence**
- **JEITA Guideline Compliance**
  - **Optional Charge Current at T1 - T2**
  - **Optional Charge Prohibited when > T3**
- **Boost Mode Range**
  - **Battery Input Voltage Range: 3.2V to 4.6V**
  - **1.4A Output Current**
- **High-Accuracy**
  - **±5% Input Current Regulation at 500mA**
  - **±0.4% Charge Voltage Regulation at $T_J$ = +25℃**
  - **±0.5% Charge Voltage Regulation at $T_J$ = 0℃ to +85℃**
- **Safety**
  - **Reverse Leakage Protection from BAT to VBUS**
  - **Thermal Regulation and Thermal Shutdown**
  - **VBUS/VBAT Over-Voltage Protection**
- **Available in a Green UTQFN-2×2-20L Package**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM41517A | UTQFN-2×2-20L | -40℃ to +85℃ | SGM41517AYUVQ20G/TR | 2TH<br>XXXX | Tape and Reel, 3000 |

## MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to PGND)

Supply Voltage: VBUS ($V_{PMID}$ ≥ $V_{VBUS}$ - 0.3V) ..... -2V (1) to 19V

Input Voltage: SCL, SDA, OTG, BAT, CD_TS ..... -0.3V to 6V

Output Voltage:

PMID ..... -0.3V to 19V

VREF, STAT ..... 6V

BOOT ..... -0.7V to 19V

SW ..... -2V (1) to 16V

Voltage Difference between BOOT and SW Inputs

$V_{BOOT}$ - $V_{SW}$ ..... -0.3V to 6V

Voltage Difference between VBUS and PMID Inputs

$V_{VBUS}$ - $V_{PMID}$ ..... -6V to 0.7V

Voltage Difference between PMID and SW Inputs

$V_{PMID}$ - $V_{SW}$ ..... -0.7V to 19V

Output Sink, STAT ..... 10mA

Package Thermal Resistance

UTQFN-2×2-20L, $\theta_{JA}$ ..... 65.7℃/W

UTQFN-2×2-20L, $\theta_{JB}$ ..... 7.1℃/W

UTQFN-2×2-20L, $\theta_{JC}$ ..... 32.5℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (2) (3)

HBM ..... ±2000V

CDM ..... ±1000V

NOTES:

1. 20ns duration.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 4V to 13.2V

Fast Charging Current, $I_{BATOP}$ ..... 2A (MAX)

Operating Ambient Temperature Range ..... -40℃ to +85℃

Operating Junction Temperature Range ..... -40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

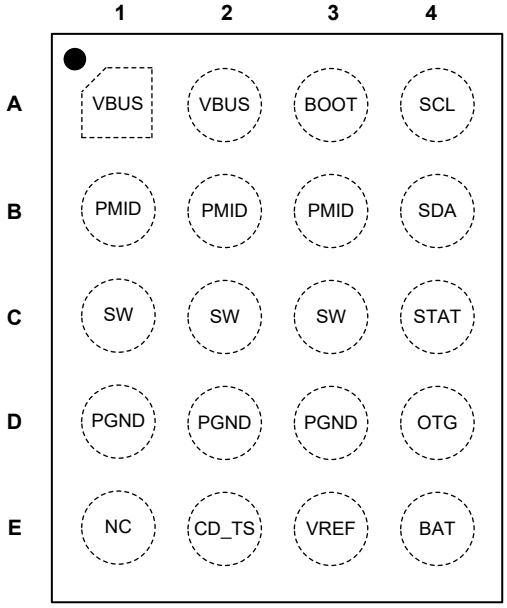
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




UTQFN-2×2-20L

## PIN DESCRIPTION

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| A1, A2 | VBUS | P | Charger Input (VIN). The internal N-channel reverse blocking MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1μF ceramic capacitor from VBUS pin to PGND close to the device. |
| A3 | BOOT | P | High-side Driver Positive Supply. It is internally connected to the bootstrap diode cathode. Use a 33nF ceramic capacitor from SW pin to BOOT pin. |
| A4 | SCL | DI | $I^2C$ Clock Signal. Use a 10kΩ pull-up to the logic high rail. |
| B1, B2, B3 | PMID | P | PMID Pin. PMID is the actual higher voltage port of converter (Buck or Boost) and is connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Connect at least a 4.7μF ceramic capacitor from PMID pin to PGND. It is the proper point for decoupling of high frequency switching currents. |
| B4 | SDA | DIO | $I^2C$ Data Signal. Use a 10kΩ pull-up to the logic high rail. |
| C1, C2, C3 | SW | P | Switching Node Output. Connect SW pin to the output inductor. Connect a 33nF bootstrap capacitor from SW pin to BOOT pin. |
| C4 | STAT | AO | Charge Status Indication Pin. This pin is used to drive a LED or communicate with a host processor.<br>During charge: low<br>Other normal conditions: open-drain<br>During faults: a 128μs low-level pulse is sent out.<br>The function can be disabled via EN_STAT register. |
| D1, D2, D3 | PGND | — | Power Ground. |
| D4 | OTG | AI | Input Current Limiting Selection or Boost Mode Enable Control Pin. During power-on reset in default mode, the OTG pin is used as the input current limiting selection pin. When OTG = High, $I_{IN\_LIMIT}$ = 800mA and when OTG = Low, $I_{IN\_LIMIT}$ = 500mA. When the $I^2C$ link to the host is established, the host can program a different input current limit value by writing to the IIN_LIMIT_2 and IIN_LIMIT_1 bits. Also, the OTG pin is together with the EN_OTG and OTG_PL bits to activate the Boost regulator. |

## PIN DESCRIPTION (continued)

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| E1 | NC | — | No Connection. |
| E2 | CD_TS | AI | 1. Charge Disable Control Pin when EN_JEITA Bit = 0 (Default). CD_TS = LOW, charge is enabled. CD_TS = HIGH, charge is disabled and VBUS pin is high-impedance to GND.<br>2. Temperature Qualification Voltage Input (Supports JEITA Profile) when EN_JEITA Bit = 1. Connect to the battery NTC thermistor that is grounded on the other side. To program operating temperature window, it can be biased by a resistor divider between VREF and GND. |
| E3 | VREF | AO | LDO Output that Powers LSFET Driver and Internal Circuits. Place at least a 1μF ceramic capacitor from this output to PGND. It is not recommended to connect the external load on VREF. |
| E4 | BAT | P | Battery Positive Terminal. If there is a long wire connection to battery, bypass to PGND with the ceramic capacitors (minimum 0.1μF + 22μF). |

NOTE: AI = analog input, AO = analog output, AIO = analog input and output, DI = digital input, DO = digital output, DIO = digital input and output, P = power.

# ELECTRICAL CHARACTERISTICS

($V_{VBUS}$ = 5V, HZ_MODE = 0, OPA_MODE = 0 (CD_TS = LOW), $T_J$ = -40℃ to +125℃, typical values are at $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Input Currents** | | | | | | |
| VBUS Supply Current Control | $I_{VBUS}$ | VBUS > VBUS (min), PWM switching | | 10 | | mA |
| | | VBUS > VBUS (min), PWM not switching | | | 2.5 | |
| | | CD_TS = HIGH or HZ_MODE = 1, 0℃ < $T_J$ < +85℃ | | 15 | 25 | μA |
| Leakage Current from Battery to VBUS Pin | $I_{LGK}$ | $V_{BAT}$ = 4.2V, high-impedance mode, $V_{VBUS}$ = 0V | | | 1 | μA |
| Battery Discharge Current in High-Impedance Mode (BAT, SW Pins) | | $V_{BAT}$ = 4.2V, high-impedance mode, $V_{VBUS}$ = 0V, SCL, SDA, OTG = 0V or 1.8V, 0℃ < $T_J$ < +85℃ | | | 20 | μA |
| **Voltage Regulation** | | | | | | |
| VBAT Regulation Voltage Programmable Range | $V_{BAT\_REG\_RANGE}$ | Operating in voltage regulation, programmable | 3.5 | | 4.6 | V |
| Voltage Regulation Accuracy | $V_{BAT\_REG\_ACC}$ | $V_{BAT\_REG}$ = 4.2V, 0℃ < $T_J$ < +85℃ | -0.5 | | 0.5 | % |
| **Current Regulation (Fast Charge)** | | | | | | |
| Fast Charge Current Programmable Range | $I_{CHG\_RANGE}$ | $V_{SHORT} \le V_{BAT} < V_{BAT\_REG}$, $V_{VBUS} - V_{BAT} > V_{SLP}$, programmable by ICHGR[3:0] | 200 | | 2000 | mA |
| Fast Charge Current Regulation Setting | $I_{CHG}$ | $V_{BAT}$ = 3.8V, $I_{CHG}$ = 500mA (ICHGR[3:0] = 000) | 475 | | 625 | mA |
| | | $V_{BAT}$ = 3.8V, $I_{CHG}$ = 2A (ICHGR[3:0] = 1111) | 1890 | | 2110 | |
| **CD_TS, OTG Pin Logic Level** | | | | | | |
| Input Low Threshold Level | $V_{IL}$ | | | | 0.5 | V |
| Input High Threshold Level | $V_{IH}$ | 1.2V I/O, I2C_HI_DETC = 1, -40℃ < $T_J$ < +85℃ | 0.848 | | | V |
| | | 1.8V I/O, I2C_HI_DETC = 0 | 1.1 | | | |
| Input Bias Current | $I_{BIAS}$ | Voltage on control pin is 5V | | 0.1 | 1 | μA |
| **Charge Termination Detection** | | | | | | |
| Termination Charge Current Programmable Range | $I_{TERM\_RANGE}$ | $V_{BAT} > V_{BAT\_REG} - V_{RCH}$, $V_{VBUS} - V_{BAT} > V_{SLP}$, programmable | 50 | | 400 | mA |
| Termination Current Regulation Setting | $I_{TERM}$ | $I_{TERM}$ = 100mA, $T_J$ = +25℃ | 35 | | 190 | mA |
| **Bad Adapter Detection** | | | | | | |
| Input Voltage Lower Limit | $V_{IN(MIN)}$ | Bad adapter detection | 3.75 | 3.9 | 4.05 | V |
| Hysteresis for $V_{IN(MIN)}$ | $V_{IN(MIN)\_HYS}$ | Input voltage rising | 45 | 110 | 175 | mV |
| Current Source to GND | $I_{BAD\_SRC}$ | During bad adapter detection | 15 | 30 | 45 | mA |
| **Input Based Dynamic Power Management** | | | | | | |
| Input Voltage DPM Threshold Programmable Range | $V_{IN\_DPM\_RANGE}$ | | 4.2 | | 4.76 | V |
| $V_{IN\ DPM}$ Threshold Accuracy | $V_{IN\_DPM\_ACC}$ | $V_{IN\_DPM}$ = 4.28V, $I_{CHG}$ = 200mA | -3 | | 3 | % |
| | | $V_{IN\_DPM}$ = 4.52V, $I_{CHG}$ = 200mA | -3 | | 3 | |
| | | $V_{IN\_DPM}$ = 4.76V, $I_{CHG}$ = 200mA | -3 | | 3 | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{VBUS}$ = 5V, HZ_MODE = 0, OPA_MODE = 0 (CD_TS = LOW), $T_J$ = -40℃ to +125℃, typical values are at $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Input Current Limiting** | | | | | | |
| Input Current Limiting Threshold | $I_{IN\_LIMIT}$ | $I_{IN}$ = 500mA | 475 | 500 | 525 | mA |
| **VREF Bias Regulator** | | | | | | |
| Internal Bias Regulator Voltage | $V_{REF}$ | $V_{VBUS}$ > UVLO, $I_{VREF}$ = 1mA, $C_{VREF}$ = 1μF | 4.75 | 5 | 5.25 | V |
| VREF Output Short Current Limit | $I_{REF\_LMT}$ | | | 30 | | mA |
| **Battery Recharge Threshold** | | | | | | |
| Recharge Threshold Voltage Range | $V_{RCH\_RANGE}$ | Below $V_{BAT\_REG}$ | 50 | | 200 | mV |
| Recharge Threshold Voltage | $V_{RCH}$ | Below $V_{BAT\_REG}$, VRCHG[1:0] = 01 | | 100 | | mV |
| **STAT Outputs** | | | | | | |
| Low-Level Output Saturation Voltage, STAT Pin | $V_{OL(STAT)}$ | 10mA sink current | | | 0.4 | V |
| High-Level Leakage Current for STAT | $I_{STAT\_LKG}$ | Voltage on STAT pin is 5V | | | 1 | μA |
| **$I^2C$ Bus Logic Levels and Timing Characteristics** | | | | | | |
| Output Low Threshold Level | $V_{OL}$ | $I_O$ = 10mA, sink current | | | 0.4 | V |
| Input Low Threshold Level | $V_{IL}$ | $V_{PULL-UP}$ = 1.2V, SDA and SCL, I2C_HI_DETC = 0 | | | 0.4 | V |
| Input High Threshold Level | $V_{IH}$ | $V_{PULL-UP}$ = 1.2V, SDA and SCL, I2C_HI_DETC = 1, -40℃ < $T_J$ < +85℃ | 0.84 | | | V |
| | | $V_{PULL-UP}$ = 1.8V, SDA and SCL, I2C_HI_DETC = 0 | 1.1 | | | |
| Input Bias Current | $I_{BIAS}$ | $V_{PULL-UP}$ = 1.2V, SDA and SCL | | | 1 | μA |
| SCL Clock Frequency | $f_{SCL}$ | Range | 10 | | 1000 | kHz |
| $I^2C$ Bus Release Timeout | $t_{I2C\_TIMEOUT}$ | When keep low for SCL or SDA | | 25 | | ms |
| **Battery Detection** | | | | | | |
| Battery Detection Current before Charge Done (Sink Current) | $I_{DETECT}$ | Begins after termination detected, $V_{BAT} \le V_{BAT\_REG}$ | | -0.5 | | mA |
| **Sleep Comparator** | | | | | | |
| Sleep Mode Entry Threshold, $V_{VBUS}$ - $V_{BAT}$ | $V_{SLP}$ | 2.3V ≤ $V_{BAT}$ ≤ $V_{BAT\_REG}$, VBUS falling, internal accuracy | 15 | 40 | 65 | mV |
| Sleep Mode Exit Hysteresis | $V_{SLP\_HYS}$ | 2.3V ≤ $V_{BAT}$ ≤ $V_{BAT\_REG}$, internal accuracy | 120 | 180 | 245 | mV |
| **Under-Voltage Lockout (UVLO)** | | | | | | |
| $V_{VBUS}$ Minimum (as One of the Conditions) to Turn on REGN | UVLO | VBUS rising - exits UVLO | | 3.175 | 3.5 | V |
| $V_{VBUS}$ Hysteresis (as One of the Conditions) to Turn on REGN | $UVLO_{(HYS)}$ | VBUS falling below UVLO - enters UVLO | 20 | 135 | | mV |
| **PWM** | | | | | | |
| Voltage from BOOT Pin to SW Pin | $V_{BOOT}$ | During charge or Boost operation | | | 4 | V |
| Internal Top Reverse Blocking MOSFET On-Resistance | $R_{Q1}$ | $I_{IN\_LIMIT}$ = 500mA, measured from VBUS to PMID | | 30 | | mΩ |
| Internal Top N-Channel Switching MOSFET On-Resistance | $R_{Q2}$ | Measured from PMID to SW, $V_{BOOT}$ - $V_{SW}$ = 4V | | 75 | | mΩ |
| Internal Bottom N-Channel MOSFET On-Resistance | $R_{Q3}$ | Measured from SW to PGND | | 90 | | mΩ |
| Oscillator Frequency | $f_{OSC}$ | | | 1.5 | | MHz |
| Frequency Accuracy | $f_{OSC\_ACC}$ | | -9.5 | | 9.5 | % |
| Maximum Duty Cycle | $D_{MAX}$ | | | 99.5 | | % |
| Synchronous Mode to Non-Synchronous Mode Transition Current Threshold | $I_{SYN\_ASYN}$ | Low-side MOSFET cycle-by-cycle current sensing | | 100 | | mA |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{VBUS}$ = 5V, HZ_MODE = 0, OPA_MODE = 0 (CD_TS = LOW), $T_J$ = -40℃ to +125℃, typical values are at $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Charge Mode Protection** | | | | | | | |
| Input VBUS OVP Threshold Voltage | $V_{OVP\_IN\_USB}$ | VBUS rising threshold to turn off converter during charge | VBUS_OVP = 0 | 6.05 | 6.5 | 6.95 | V |
| | | | VBUS_OVP = 1 | 13.3 | 14 | 14.7 | |
| VBAT OVP Threshold Voltage | $V_{VBAT\_OVP}$ | $V_{BAT}$ threshold over $V_{BAT\_REG}$ to turn off charger during charge | | 113.5 | 117 | 120.5 | $\%V_{BAT\_REG}$ |
| $V_{OVP}$ Hysteresis | | Lower limit for $V_{BAT}$ falling from above $V_{BAT\_OVP}$ | | | 12 | | |
| Cycle-by-Cycle Current Limit for Charge | $I_{ICHG\_LIMIT}$ | Charge mode operation | | | 4 | | A |
| Trickle to Fast Charge Threshold | $V_{SHORT}$ | $V_{BAT}$ rising | | 1.95 | 2.1 | 2.25 | V |
| $V_{SHORT}$ Hysteresis | | $V_{BAT}$ falling below $V_{SHORT}$ | | | 100 | | mV |
| Trickle Charge Charging Current | $I_{SHORT}$ | $V_{BAT} \le V_{SHORT}$ | | 15 | 30 | 45 | mA |
| **Boost Mode Operation for VBUS (OPA_MODE = 1, HZ_MODE = 0)** | | | | | | | |
| Boost Output Voltage (to VBUS Pin) | $V_{VBUS\_B}$ | $V_{BAT}$ = 3.8V, OTG_VOUT[1:0] = 00 | | | 5.05 | | V |
| Boost Output Voltage Accuracy | $V_{VBUS\_B\_ACC}$ | Including line and load regulation, $V_{VBUS\_B}$ = 5.05V or $V_{VBUS\_B}$ = 5.35V | | -2.3 | | 2.3 | % |
| Maximum Output Current for Boost | $I_{BO}$ | $V_{VBUS\_B}$ = 5.05V, $V_{BAT}$ = 3.8V | | 945 | 1400 | | mA |
| Cycle-by-Cycle Current Limit for Boost | $I_{BLIMIT}$ | $V_{VBUS\_B}$ = 5.05V, $V_{BAT}$ = 3.8V | | | 2.9 | | A |
| Over-Voltage Protection Threshold for Boost (VBUS Pin) | $V_{BUSOVP}$ | Threshold over VBUS to turn off converter during boosting | | 5.7 | 6 | 6.3 | V |
| $V_{BUSOVP}$ Hysteresis | | $V_{VBUS}$ falling from above $V_{BUSOVP}$ | | | 100 | | mV |
| Maximum Battery Voltage for Boost (BAT Pin) | $V_{BATMAX}$ | $V_{BAT}$ rising edge during boosting | | 4.65 | 4.9 | 5.15 | V |
| $V_{BATMAX}$ Hysteresis | | $V_{BAT}$ falling from above $V_{BATMAX}$ | | | 200 | | mV |
| Minimum Battery Voltage for Boost (BAT Pin) | $V_{BATMIN}$ | During boosting | | | 2.4 | | V |
| | | Before Boost starts | | | 2.8 | 3 | |
| Boost Output Resistance at High-Impedance Mode (from VBUS to PGND) | $R_{VBUS\_LKG}$ | CD_TS = HIGH or HZ_MODE = 1, 0℃ < $T_J$ < +85℃ | | 200 | | | kΩ |
| **Protection** | | | | | | | |
| Thermal Trip | $T_{SHTDWN}$ | | | | 165 | | ℃ |
| Thermal Hysteresis | $T_{SHTDWN\_HYS}$ | | | | 10 | | ℃ |
| Thermal Regulation Threshold | $T_{CF}$ | Charge current begins to reduce | | | 120 | | ℃ |
| **JEITA Thermistor Comparator (Buck Mode)** | | | | | | | |
| T1 (0℃) Threshold Voltage at CD_TS Pin | $V_{T1}$ | Charge suspended if temperature T is above the threshold, as percentage of $V_{VREF}$ | | | 73.2 | | % |
| | | Falling threshold, as percentage of $V_{VREF}$ | | | 71.2 | | |
| T2 (10℃) Threshold Voltage at CD_TS Pin | $V_{T2}$ | Charge sets to $I_{CHG}$/10 and $V_{BAT\_REG}$ - 100mV, as percentage of $V_{VREF}$ | | | 68.1 | | % |
| | | Falling threshold, as percentage of $V_{VREF}$ | | | 66.7 | | |
| T3 (45℃) Threshold Voltage at CD_TS Pin | $V_{T3}$ | Charge sets to normal $I_{CHG}$ and $V_{BAT\_REG}$ if above the threshold, as percentage of $V_{VREF}$ | | | 45.8 | | % |
| | | Falling threshold, as percentage of $V_{VREF}$ | | | 44.5 | | |
| T4 (60℃) Threshold Voltage at CD_TS Pin | $V_{T4}$ | Charge sets to normal $I_{CHG}$/10 and $V_{BAT\_REG}$ - 100mV if T3 < T <T4, as percentage of $V_{VREF}$ | | | 35.4 | | % |
| | | Falling Threshold, charge suspended if temperature T is below the threshold, as percentage of $V_{VREF}$ | | | 34.0 | | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{VBUS}$ = 5V, HZ_MODE = 0, OPA_MODE = 0 (CD_TS = LOW), $T_J$ = -40℃ to +125℃, typical values are at $T_A$ = +25℃, unless otherwise noted.)

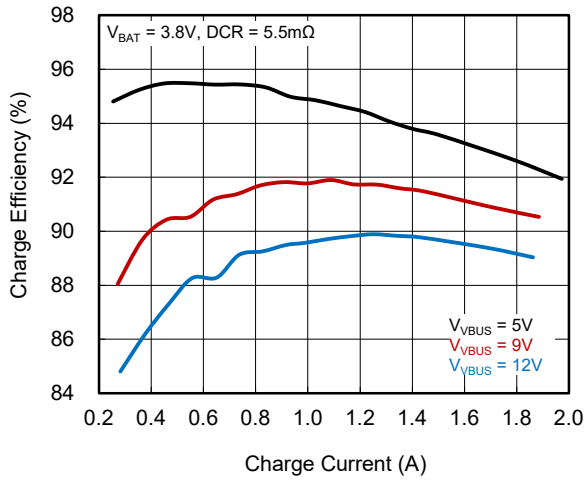
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Cold or Hot Thermistor Comparator (Boost Mode)** | | | | | | |
| Cold Temperature Threshold (CD_TS Pin Voltage Rising Threshold) | $V_{BCOLD}$ | As percentage of $V_{VREF}$ (approx. -20℃ w/ 103AT) | | 80 | | % |
| CD_TS Voltage Falling (Exit from Cold Range to Cool) | | As percentage of $V_{VREF}$ | | 79 | | % |
| Hot Temperature Threshold (CD_TS Pin Voltage Falling Threshold) | $V_{BHOT}$ | As percentage of $V_{VREF}$ (approx. 60℃ w/ 103AT) | | 31.2 | | % |
| CD_TS Voltage Rising (Exit Hot Range to Warm) | | As percentage of $V_{VREF}$ | | 34.5 | | % |

## TIMING REQUIREMENTS

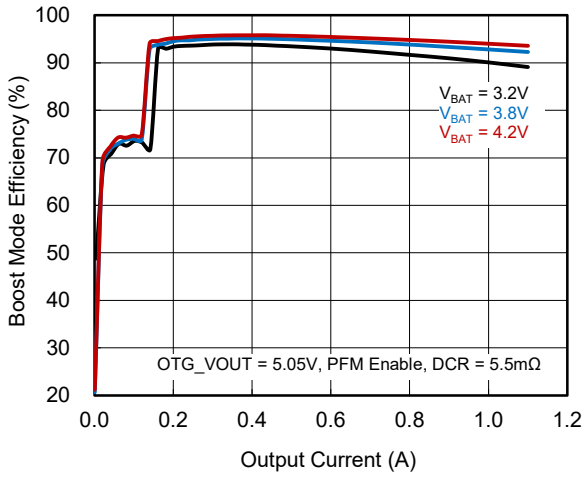
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Weak Battery Detection** | | | | | | |
| Deglitch Time for Weak Battery Threshold | $t_{WEAK\_DGL}$ | Battery detection function: when $V_{BAT} < V_{BAT\_REG} - V_{RCH}$ during $t_{WEAK\_DGL}$, a 128μs pulse is sent to STAT pin | | 100 | | ms |
| **Charge Termination Detection** | | | | | | |
| Deglitch Time for Charge Termination | $t_{TERM\_DGL}$ | TERM_DGL[1:0] = 10 (32ms) | | 30 | | ms |
| **Bad Adapter Detection** | | | | | | |
| Deglitch Time for VBUS Rising above $V_{IN(MIN)}$ | $t_{VBUS\_R\_DGL}$ | | | 30 | | ms |
| $t_{INT}$ Detection Interval | $t_{INT}$ | Input power source detection | | 2 | | s |
| **Battery Recharge Threshold** | | | | | | |
| Deglitch Time | $t_{RECH\_DGL}$ | | | 120 | | ms |
| **Battery Detection** | | | | | | |
| Battery Detection Time | $t_{DETECT}$ | | | 224 | | ms |
| **Sleep Comparator** | | | | | | |
| Deglitch Time for VBUS Rising above $V_{BAT}$ + $V_{SLP\_HYS}$ | $t_{SLEEP\_R\_DGL}$ | | | 30 | | ms |
| **Charge Safety Timer** | | | | | | |
| Charge Safety Timer | $t_{CHG\_SAFE}$ | | 8 | 10 | 12 | h |

## TYPICAL PERFORMANCE CHARACTERISTICS

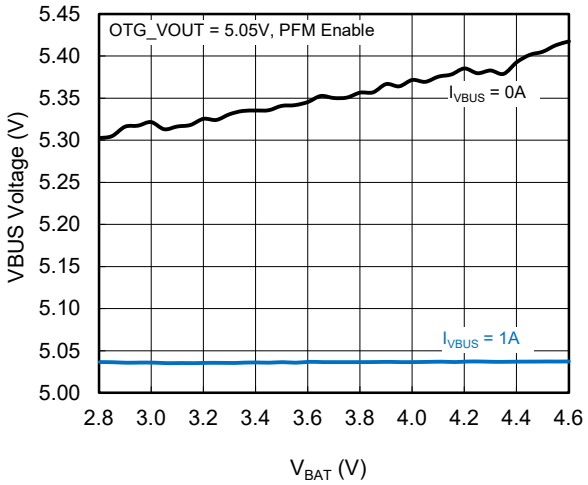
Charge Efficiency vs. Charge Current



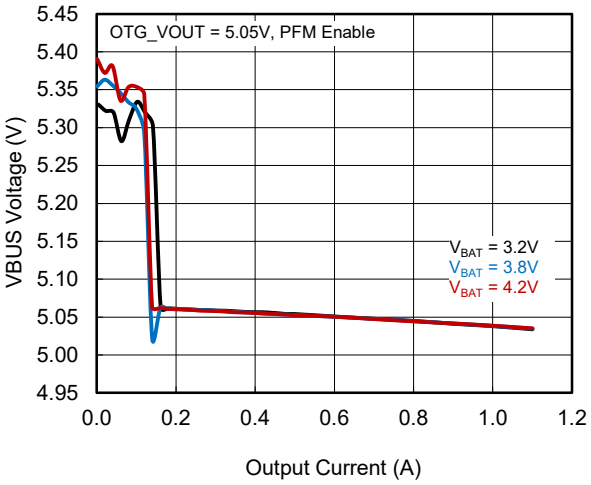

Boost Mode Efficiency vs. Output Current



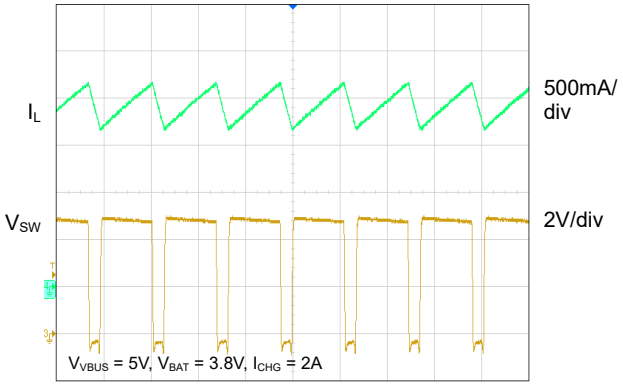

Boost Mode Line Regulation



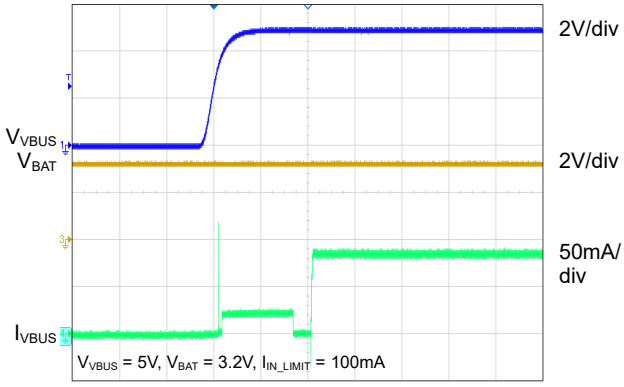

Boost Mode Load Regulation




PWM Charging Waveform

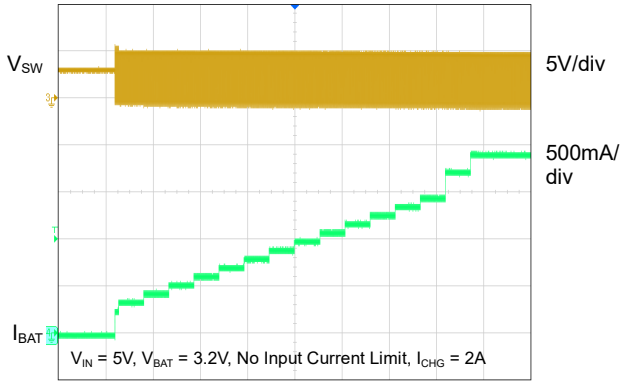



Bad Adapter Detection



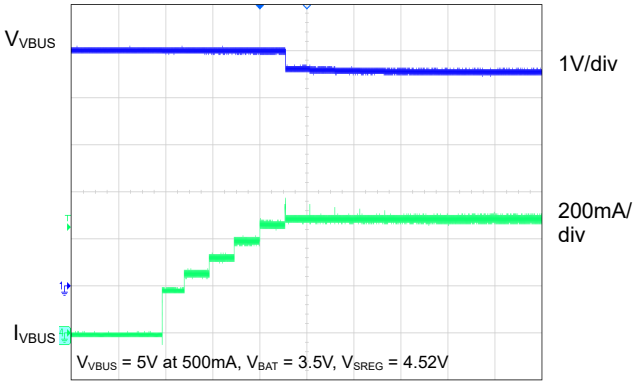
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Charge Current Ramp Up



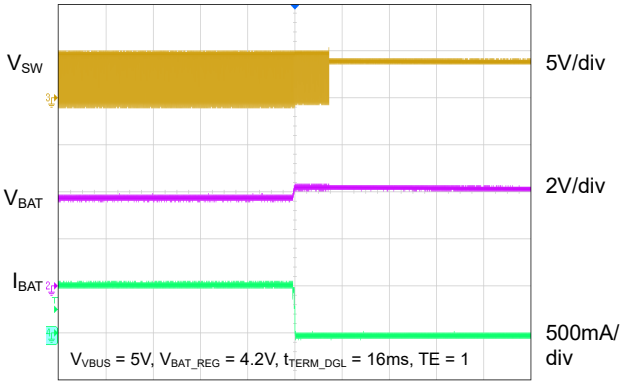

Time (500ms/div)

VIN Based DPM



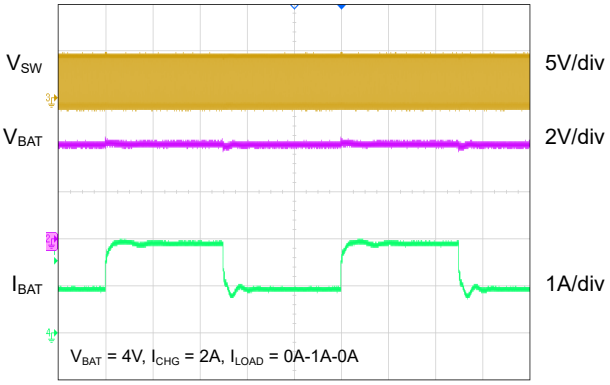

Time (500ms/div)

Charge Termination Detection



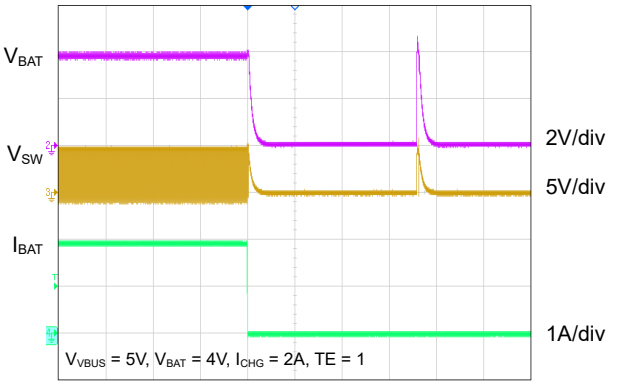

Time (20ms/div)

Load Transient in Charger Mode



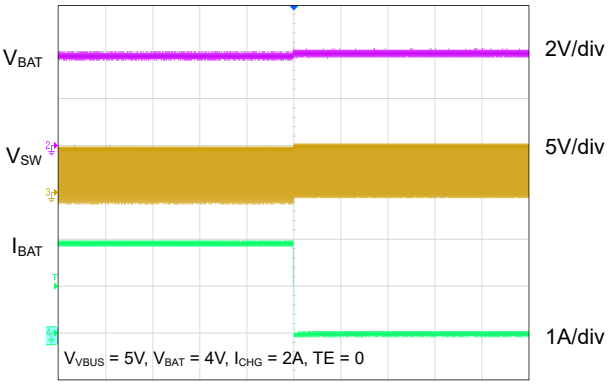

Time (500μs/div)

Battery Removal with TE = 1




Time (500ms/div)

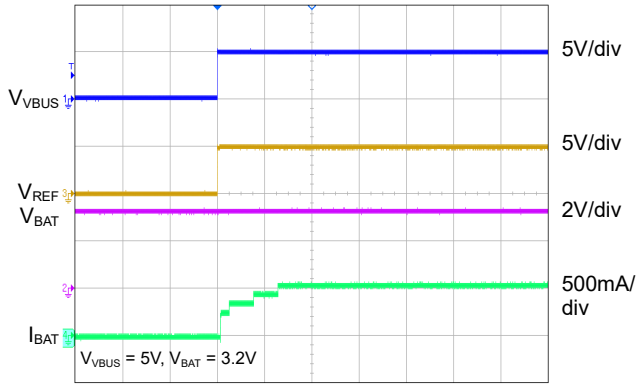
Battery Removal with TE = 0




Time (20ms/div)

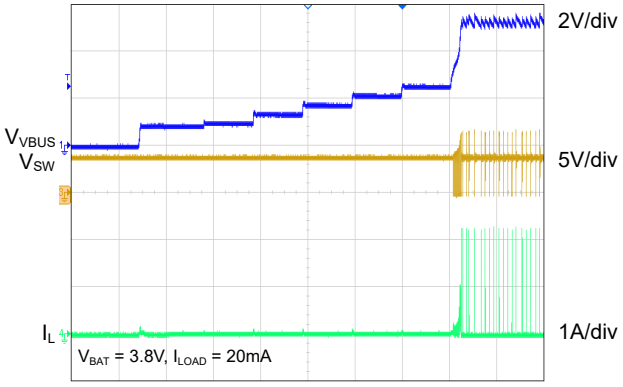
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Charge Startup with Adapter Plug-In



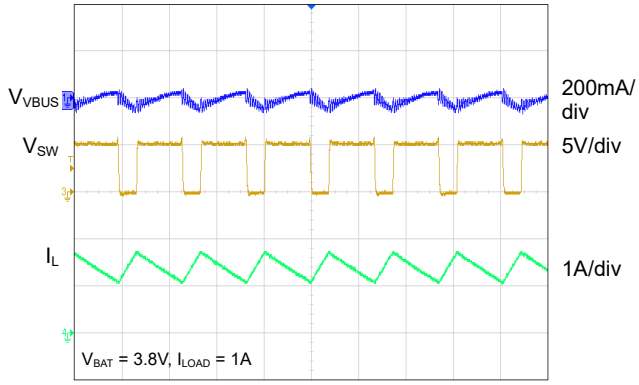

Time (500ms/div)

Boost Startup



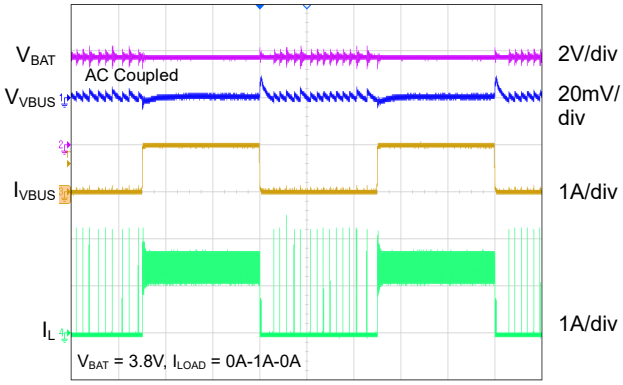

Time (500μs/div)

Boost PWM Waveforms



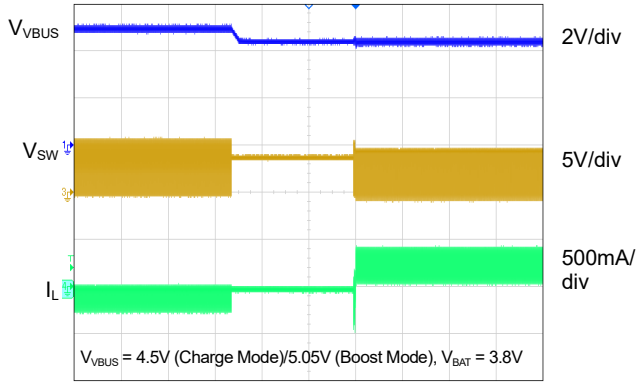

Time (500ns/div)

Boost Mode Load Transient



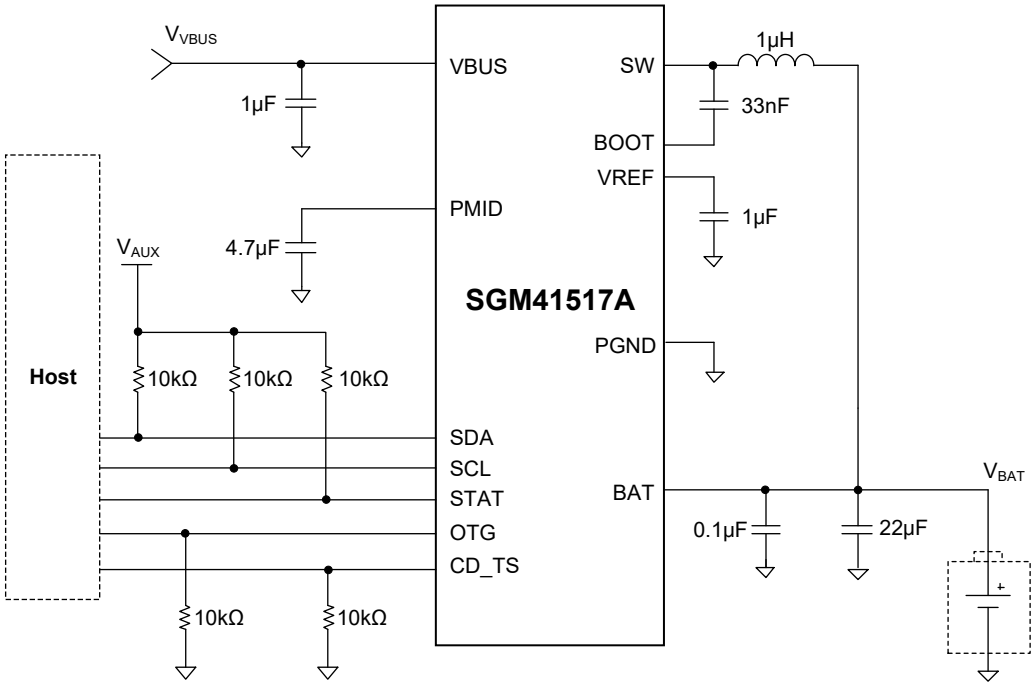

Time (500μs/div)

Boost to Charge Mode Transition




Time (20ms/div)

## TYPICAL APPLICATION CIRCUIT




NOTE: $V_{VBUS}$ = 5V, $I_{CHG}$ = 2000mA, $V_{BAT}$ = 3.5V to 4.6V (adjustable).

**Figure 1. Typical Application Circuit**

## FUNCTIONAL BLOCK DIAGRAM

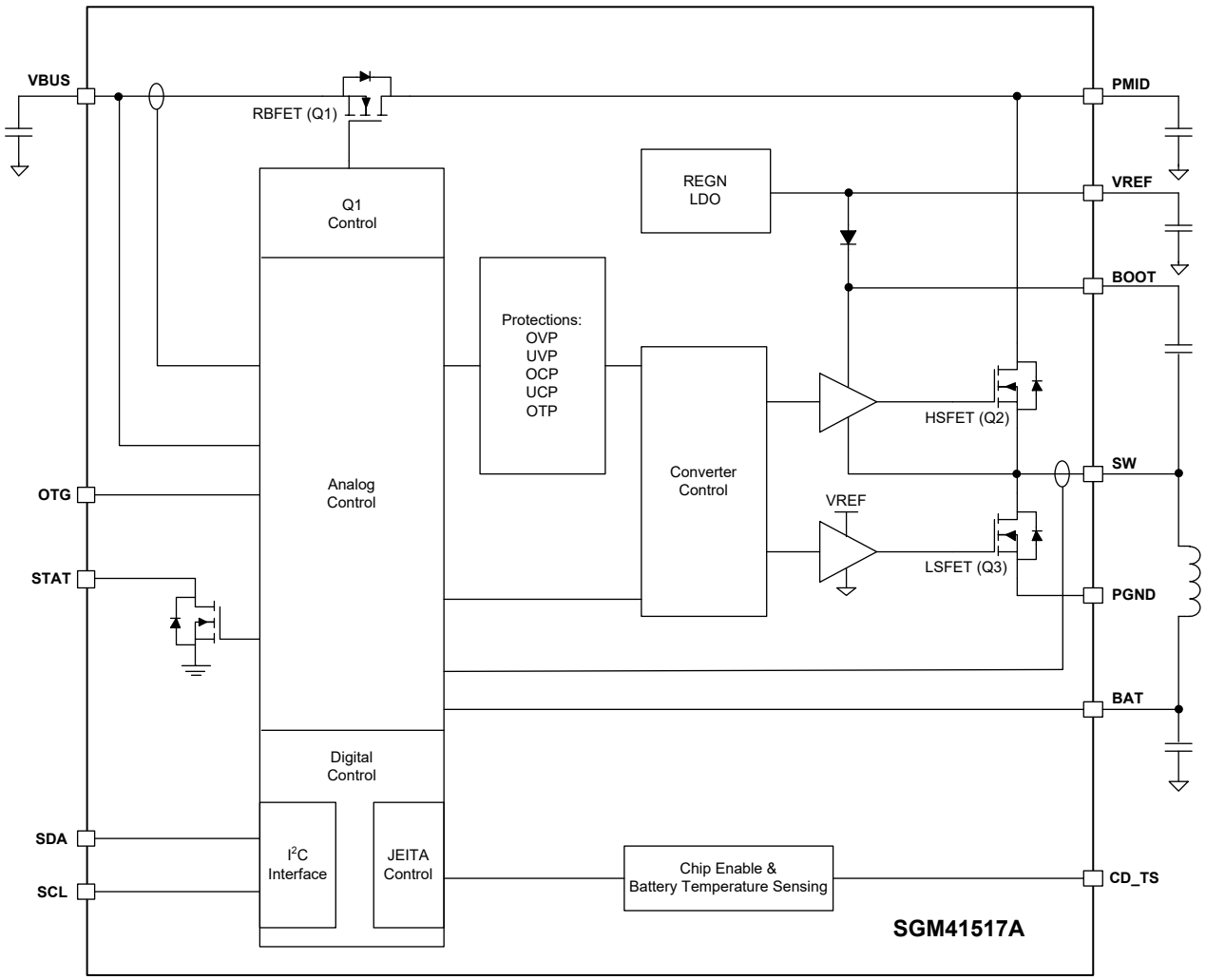



**Figure 2. Block Diagram**

# DETAILED DESCRIPTION

## Overview

For power sources with limited current, such as USB hosts or hubs, efficient converters are crucial for fully use input power capacity to quickly charge batteries. Due to the high-efficiency of switch-mode chargers over a wide input and battery voltage range compared with linear chargers, the switch-mode chargers are a good choice for high-speed charging and better thermal management.

The SGM41517A is a highly integrated synchronous switch-mode charger, which integrates FETs and small external components. The SGM41517A is suitable for portable applications powered by single battery lithium-ion or lithium-polymer battery packs. In addition, the SGM41517A also has bidirectional operation to achieve the Boost function supported by USB OTG.

The SGM41517A has three operating modes: charging mode, Boost mode, and high-impedance mode. In charging mode, the IC supports precision lithium-ion or lithium-polymer charging systems for single battery applications. In Boost mode, the IC boosts the battery voltage to VBUS to supply power to the connected OTG devices. In high-impedance mode, the IC stops charging or boosting and operates in a mode where the current from the VBUS or battery is very low, effectively reducing the power consumption of portable devices in standby mode. Through $I^2C$ communication with the host, i.e. "host" control/mode, the IC achieves smooth transition between different operating modes. Even if there is no available $I^2C$ communication, the IC will start in default mode. During default mode operation, the charger will still charge the battery, but use the default value of registers.

## Operational Flow Chart

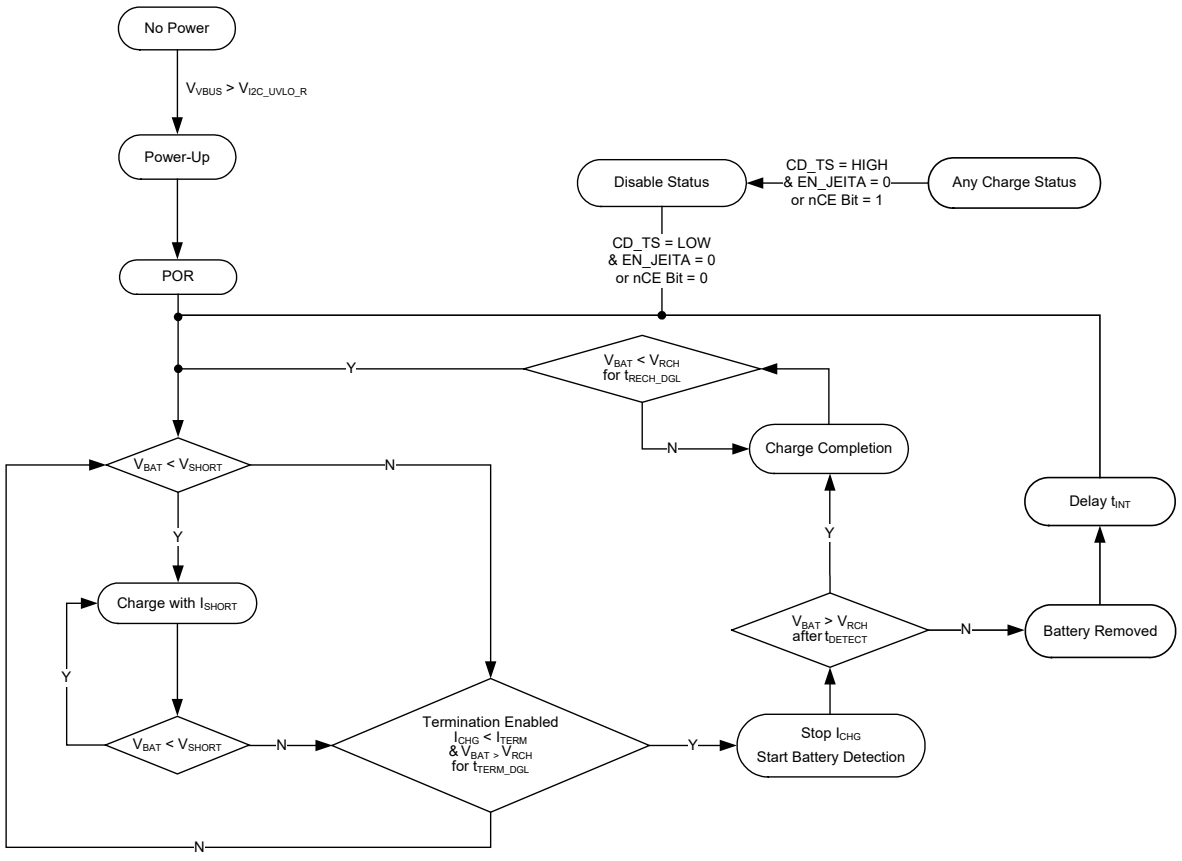



**Figure 3. Operational Flow Chart of SGM41517A in Charge Mode**

# DETAILED DESCRIPTION (continued)

## Input Voltage Protection

### Input Over-Voltage Protection

The IC has built-in input over-voltage protection to protect equipment and other components from damage in the event of high input voltage (voltage from VBUS to PGND). When VBUS OVP is detected, the device turns off the PWM converter and RBFET Q1, sets the fault status bit, and sends a 128μs pulse to the STAT pin. Once $V_{VBUS}$ drops below the input over-voltage exit threshold, the fault will be cleared and the charging process will resume.

### Bad Adapter Detection

When the power-on reset (POR) happens at VBUS pin, the IC performs the bad adapter detection by applying a about 30mA current sink to VBUS. If VBUS is higher than $V_{IN(MIN)}$ for 30ms, the adapter is good and the charging process is started. Otherwise, if VBUS drops below $V_{IN(MIN)}$, a bad adapter is found, and the IC disables the current sink, sends a 128μs low pulse at the STAT pin, and sets the bad adapter flag (FAULT[2:0] = 011 in register REG0x00). After the $t_{INT}$ (2s TYP) delay, the IC restarts the adapter detection process again.

### Sleep Mode

When the VBUS pin voltage falls below the sleep mode entry threshold ($V_{BAT}$ + $V_{SLP}$) and VBUS is higher than the bad adapter detection threshold ($V_{IN(MIN)}$), the SGM41517A enters the low power sleep mode. When adapter is not present, there is no leakage current to from BAT to VBUS. In the sleep mode, both the RBFET Q1 and PWM are turned off.

### Input Voltage Based DPM (Special Charger Voltage Threshold)

In the charging process, if the input power source cannot provide the programmed charging current, the VBUS voltage will drop. Once the VBUS decrease to $V_{IN\_DPM}$ (default 4.52V), the chip begins to decrease the charge current for preventing any further drop of VBUS. The charge current is lower than the set value if the SGM41517A enters this mode. The feature makes the IC has the maximum compatibility with different adapters.

## Battery Protection

### Battery Over-Voltage Protection

The IC integrates a built-in over-voltage protection to protect the device and other components from the over-voltage damage when the battery is suddenly removed. When an over-voltage condition is found, the PWM converter is turned off by the device, the fault status bits can be set, and a fault pulse is sent out to the STAT pin. Once $V_{BAT}$ drops to the battery over-voltage falling threshold, the fault is cleared and charge process is restarted again.

### Battery Short Protection and Charge Timeout

In the normal charging process, if the battery voltage is lower than the short-circuit threshold $V_{SHORT}$, the charger charges the battery with $I_{SHORT}$.

When a charge cycle is started, the internal 10 hours safety timer starts to count. If the charging is not terminated in 10 hours, device will stop the PWM and send 128μs pulse at the STAT pin to notify the AP. Plug out VBUS or set the CD_TS pin to high or set the TMR_RST bit or nCE bit can reset the safety timer.

### Battery Detection in Host Mode

For the applications that need to removable battery pack, once the termination function is enabled, the IC provides a battery presence detection method to detect whether the battery packs is inserted or removed.

During the normal charging process controlled, once the BAT voltage is over the battery recharge threshold $V_{BAT\_REG}$ - $V_{RCH}$, and the termination of charging current is detected, the IC will turn off PWM charging and enable the discharge current $I_{DETECT}$ for $t_{DETECT}$ (224ms, TYP) and check the battery voltage. If the battery voltage remains above the recharge threshold after $t_{DETECT}$, it indicates that the battery is present. On the contrary, if the battery voltage is lower than the battery recharge threshold during $t_{WEAK\_DGL}$ (100ms TYP), the battery does not exist, the FAULT[2:0] bits are set to 111 and a 128μs pulse is sent to STAT pin. In this case, charging will resume after a delay in $t_{INT}$. This function ensures that the charging parameters are reset when replacing the battery.

## Default Mode

The SGM41517A stays in default mode until $I^2C$ communication starts. When the host sends a valid $I^2C$ write command to the SGM41517A, the IC will enter host mode automatically.

## USB Friendly Power-Up

The default control bits set the charging current and regulation voltage low enough to comply with USB spec and avoid over-charging any of the Li-Ion chemistries, while the host has lost communication. The input current limiting is described as follow.

## Input Current Limiting at Power-Up

The SGM41517A integrates the input current sensing circuit and the control loop internally. In default mode, the OTG pin voltage level sets the input current limit to 500mA for low-level and 800mA for high-level. In host mode, the input current limit is set by the programmed control bits in the register REG0x01.

# DETAILED DESCRIPTION (continued)

## Device Functional Modes

### Charge Mode Operation

#### *Charge Profile*

Once a good battery with a voltage lower than the charging threshold is inserted and a good adapter is connected, the SGM41517A will enter charging mode. In charging mode, the device has five control loops to regulate input voltage, input current, charging current, charging voltage, and chip junction temperature. During charging, all five control loops are enabled, one of which is dominant. This IC can charge the Li-Ion or Li-polymer charging systems precisely. Figure 4 shows a typical charging curve without an input current regulation circuit. This is the traditional CC/CV charging curve, and Figure 4 (marked with dashed lines) also shows a typical charging curve when the input current limiting circuit dominates in constant current mode. In this case, the charging current is higher than the input current, so the charging process is faster than a linear charger. The input voltage limit, input current limit, charging current, termination current, and charging voltage can be programmed by the $I^2C$ interface.

### PWM Controller in Charge Mode

The SGM41517A integrates a fixed 1.5MHz or 500kHz frequency voltage-mode controller to regulate charge current or voltage. This controller improves the line transient response, and simplifies the compensation network used for both continuous and discontinuous current mode operation. The elaborate designed controller has enough phase margins for stable operation even use small ceramic capacitors with low ESR.

The IC has integrates three N-FETs: the reverse blocking N-FET (Q1), the high-side N-FET (Q2), and the low-side N-FET (Q3). The reverse blocking N-FET (Q1) prevents the battery discharge when $V_{VBUS}$ is lower than $V_{BAT}$. The high-side N-FET (Q2) is the switching switch. A charge pump circuit is used to turn on the reverse blocking N-FET (Q1), and a bootstrap circuit with an external bootstrap capacitor is used to supply the gate drive circuit for the high-side N-FET (Q2).

The cycle-by-cycle current limit is done by sensing the current through the FETs Q2 and Q3. The limit threshold for Q2 is set to a nominal 4A peak current. The low-side N-FET (Q3) also has the zero crossing detection (ZCD) function, which determines whether the PWM controller will operate in synchronous or non-synchronous mode. If the current of the low-side FET is lower than 100mA, the low-side N-channel FET (Q3) is turned off to prevent the battery from discharging, else synchronous operation is used to minimize power loss.

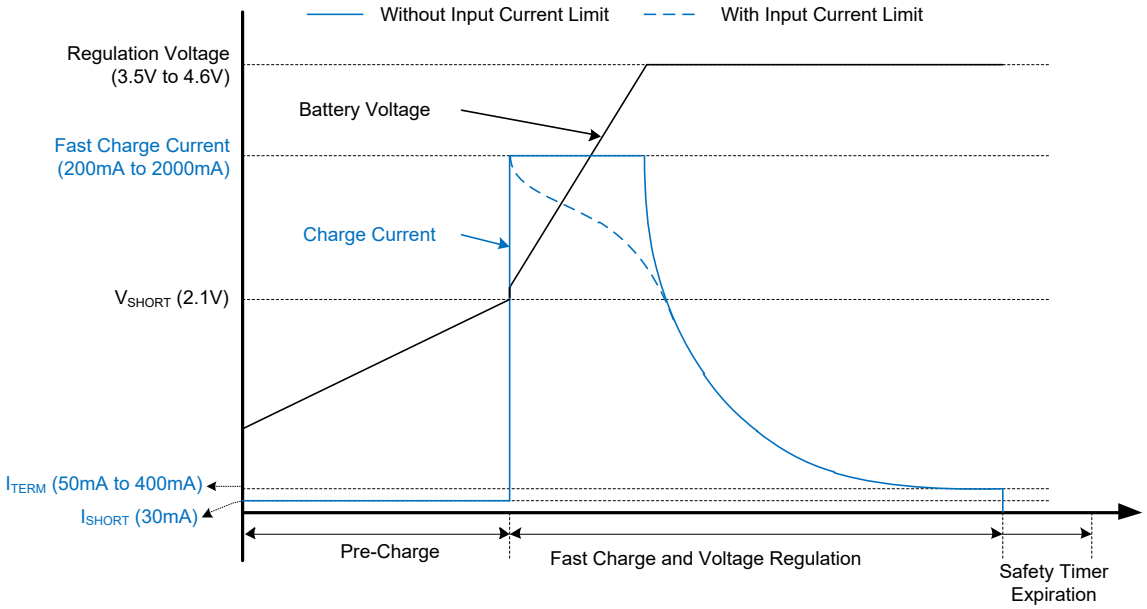



**Figure 4. Typical Charging Profile for without Input Current Limit and with Input Current Limit**

# DETAILED DESCRIPTION (continued)

## Battery Charging Process

At the beginning of pre-charging, when the battery voltage is lower than $V_{SHORT}$, the IC charges the battery with short-circuit current $I_{SHORT}$. When the battery voltage is higher than $V_{SHORT}$ and lower than $V_{BAT\_REG}$, the charging current ramp rises to the fast charging current $I_{CHG}$ or a current decided by input current limit. Controlling the set value of fast charging current can minimize current and voltage overshoot during charging period. The input current limit and the fast charging current $I_{CHG}$ can be set by host. Once the battery voltage reaches the regulated voltage $V_{BAT\_REG}$, the charging current will gradually decrease, as shown in Figure 4. The IC monitors the battery packs voltage by sensing the voltage between the BAT and PGND pin. In host mode, the voltage can be adjusted (3.5V to 4.6V) and programmed through by $I^2C$ interface.

If termination function is enabled, a charge cycle is terminated when the battery voltage is higher than the recharge threshold and the charge current falls below the programmed termination current. TE bit is termination control bit and can be set to 0 to disable termination before it happens.

When one of the following conditions is detected, a new charge cycle is restarted:

- The battery voltage falls below the $V_{BAT\_REG}$ - $V_{RCH}$ threshold.
- nCE bit is toggled or RESET bit is set (host controlled).
- CD_TS pin is toggled from high to low (host controlled).

## Thermal Regulation and Protection

For preventing the chip from overheating during charging, the IC monitors the junction temperature $T_J$ of the die and gradually reduces the charging current when $T_J$ reaches the thermal regulation threshold $T_{CF}$. When the junction temperature rises to about 10℃ above $T_{CF}$, the charging current drops to zero. Whenever $T_J$ exceeds $T_{SHTDWN}$, the IC will stop charging and enter thermal shutdown mode. In the status, PWM is turned off and all timers are frozen. When $T_J$ drops to about 10℃ below $T_{SHTDWN}$, charging resumes.

## Status Outputs Pin (STAT)

The STAT pin is used to indicate the IC status. When EN_STAT bit in control register (REG0x00) is set to 1, the STAT is pulled to low-level during charging. In the other conditions, the STAT pin is used as a high-impedance (open-drain) output. When in the fault conditions, a 128μs pulse is sent out to notify the host. Charging state is indicated with the STAT pin as explained in Table 1. The role of the STAT pin is to drive an LED indicator or send an interrupt to the host processor.

**Table 1. STAT Pin Function**

| Charging State | STAT Indicator |
|---|---|
| Charge in progress and EN_STAT = 1 | Low |
| Other normal conditions | Open-Drain |
| Charge mode faults: Timer fault, sleep mode, VBUS or battery over-voltage, poor input source, VBUS UVLO, no battery, thermal shutdown | 128μs Pulse |
| Boost mode faults: Timer fault, over load, VBUS or battery over-voltage, low battery voltage, thermal shutdown | 128μs Pulse |

## Control Bits in Charge Mode

### *nCE Bit (Charge Mode)*

The nCE bit in the control register is used to disable or enable the charge process. 0 on this bit enables the charge and 1 disables the charge.

### *RESET Bit*

The RESET bit of the control register is used to reset all charge parameters. When the RESET bit is set to 1, all charge parameters will be reset to default values except the safety limit register, and the RESET bit is automatically cleared to 0 once reset action is done. This is designed to reset the charge parameters before the charge starts, it is not recommended to set the RESET bit while charging or boosting are in on-going.

### *OPA_MODE Bit*

The OPA_MODE bit is used as the operation mode control bit. When OPA_MODE = 0 and HZ_MODE = 0, the IC operates in charge mode, and when OPA_MODE = 1 and HZ_MODE = 0, the IC operates in Boost mode. Table 2 shows the detailed operation mode function.

**Table 2. Operation Mode Function**

| OPA_MODE | HZ_MODE | Operation Mode |
|---|---|---|
| 0 | 0 | Charge mode (no fault)<br>Charge configure (fault, $V_{VBUS}$ > UVLO)<br>High-impedance ($V_{VBUS}$ < UVLO) |
| 1 | 0 | Boost mode (no faults)<br>Any fault enters the charge configure mode. |
| X | 1 | High-impedance |

## Control Pins in Charge Mode

### *CD_TS Pin (Charge Disable or JEITA Related Function)*

In the default status, the CD_TS pin is used to enable or disable the charging process. When the CD_TS pin is set to low, the charge is enabled. When the CD_TS pin is set to high, the charge is disabled and the charger goes to high-impedance (Hi-Z) mode.

When EN_JEITA bit is set to 1, CD_TS pin can be used for temperature qualification (support JEITA guideline).

# DETAILED DESCRIPTION (continued)

## Temperature Qualification

The charging current and voltage of the battery must be limited when battery is cold or hot. A thermistor input for battery temperature monitoring is included in the device that can protect the battery based on JEITA guidelines.

## Compliance with JEITA Guideline

JEITA guideline (April 20, 2007 release) is implemented in the device for safe charging of the Li-Ion battery. JEITA highlights the considerations and limits that should be considered for charging at cold or hot battery temperatures. High charge current and voltage must be avoided outside the normal operating temperatures (typically 0℃ and 60℃). This functionality can be disabled if not needed. Four temperature levels are defined by JEITA from T1 (minimum) to T4 (maximum). Outside this range, charging should be stopped. The corresponding voltages sensed by NTC are named $V_{T1}$ to $V_{T4}$. Due to the sensor negative resistance, a higher temperature results in a lower voltage on CD_TS pin. The battery cool range is between T1 and T2, and the warm range is between T3 and T4. Charge must be limited in the cool and warm ranges.

One of the conditions for starting a charge cycle is having the CD_TS voltage within $V_{T1}$ to $V_{T4}$ window limits. If during the charge, battery gets too cold or too hot and CD_TS voltage exceeds the T1 - T4 limits, charging is suspended (zero charge current) and the controller waits for the battery temperature to come back within the T1 to T4 window.

JEITA recommends reducing charge current to 1/2 of fast charging current or lower at cool temperatures (T1 - T2). For warmer temperature (within T3 - T4 range), charge voltage is recommended to be kept below $V_{BAT\_REG}$ - 100mV.

The SGM41517A exceeds the JEITA requirement by its flexible charge parameter settings. At warm temperature range (T3 - T4), the charge voltage is set to the lower of $V_{BAT\_REG}$ - 100mV when JEITA_VSET_H = 0, the charge voltage is set to $V_{BAT\_REG}$ when JEITA_VSET_H = 1, and the charge current can be reduced down to 0%, 10% of fast charging current by the JEITA_ISET_H bit. At cool temperatures (T1 - T2), the current setting can be reduced down to 0% or 10% of fast charging current selectable by the JEITA_ISET_L bit, and the charge voltage is set to $V_{REG}$ - 100mV.

A 103AT-2 type thermistor is recommended for use with the SGM41517A. Other thermistors may be used and bias network (see Figure 5) can be calculated based on the following equations:

$$R_{T2} = \frac{R_{THCOLD} \times R_{THHOT} \times \left(\frac{1}{V_{T1}} - \frac{1}{V_{T4}}\right)}{R_{THHOT} \times \left(\frac{1}{V_{T4}} - 1\right) - R_{THCOLD} \times \left(\frac{1}{V_{T1}} - 1\right)} \quad (1)$$

$$R_{T1} = \frac{\left(\frac{1}{V_{T1}} - 1\right)}{\left(\frac{1}{R_{T2}}\right) + \left(\frac{1}{R_{THCOLD}}\right)} \quad (2)$$

Where, $V_{T1}$ and $V_{T4}$ are $T_{COLD}$ and $T_{HOT}$ thresholds voltage on CD_TS pin as percentage to $V_{VREF}$, $R_{THCOLD}$ and $R_{THHOT}$ are thermistor resistances ($R_{TH}$) at desired T1 (Cold) and T4 (Hot) temperatures. Select $T_{COLD}$ = 0℃ and $T_{HOT}$ = 60℃ for Li-Ion or Li-polymer batteries. For a 103AT-2 type thermistor $R_{THCOLD}$ = 27.28kΩ and $R_{THHOT}$ = 3.02kΩ, the calculation results are: $R_{T1}$ = 5.32kΩ and $R_{T2}$ = 31.09kΩ. The standard value of $R_{T1}$ is 5.23kΩ and that of $R_{T2}$ is 30.9kΩ.

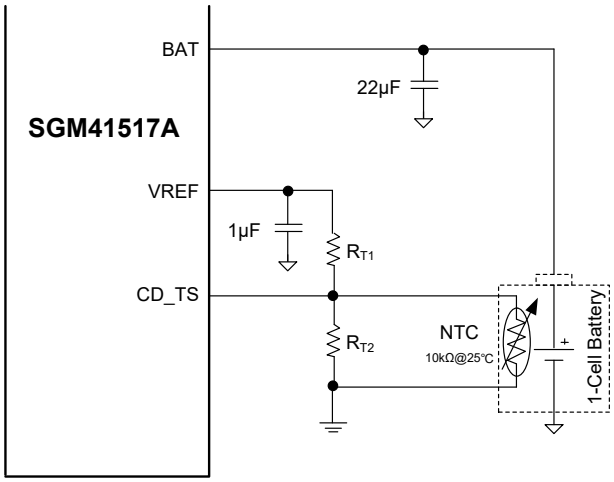



**Figure 5. Battery Thermistor Connection and Bias Network (EN_JEITA = 1)**

**Table 3. Temperature Related Charging Control (EN_JEITA = 1)**

| Temperature Range | Charge Current | Charge Voltage |
|---|---|---|
| Lower than T1 | / | / |
| T1 - T2 | $I_{CHG}$ × 10% (JEITA_ISET_L = 0)<br>$I_{CHG}$ × 0% (JEITA_ISET_L = 1) | $V_{BAT\_REG}$ - 100mV |
| T2 - T3 | $I_{CHG}$ | $V_{BAT\_REG}$ |
| T3 - T4 | $I_{CHG}$ × 10% (JEITA_ISET_H = 0)<br>$I_{CHG}$ × 0% (JEITA_ISET_H = 1) | $V_{BATR\_EG}$ - 100mV (JEITA_VSET_H = 0)<br>$V_{BAT\_REG}$ (JEITA_VSET_H = 1) |
| Higher than T4 | / | / |

# DETAILED DESCRIPTION (continued)

## Boost Mode Temperature Monitoring (Battery Discharge)

The device is capable to monitor the battery temperature for safety during the Boost mode. The temperature must remain within the $V_{BCOLD}$ to $V_{BHOT}$ thresholds otherwise the Boost mode will be suspended. Moreover, NTC_FAULT[2:0] register is updated to report Boost mode cold or hot condition. Once the temperature returns within the window, the Boost mode is resumed and NTC_FAULT[2:0] register is cleared to 000 (normal).

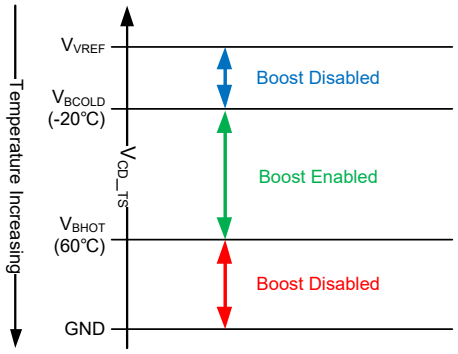



**Figure 6. CD_TS Pin Thermistor Temperature Window Settings in Boost Mode**

## Boost Mode Operation

In host mode, when the OTG pin goes to high or the OPA_MODE bit is set to 1, the SGM41517A operates in Boost mode and delivers the power from the battery to the VBUS. In default condition, the device boosts VBUS to about 5.05V and can delivers a current as much as $I_{BO}$ (1400mA TYP) to power the USB OTG devices.

### *PWM Controller in Boost Mode*

Similar to charge mode operation, in Boost mode, the SGM41517A regulates output voltage at PMID pin ($V_{PMID}$) in voltage mode and with a fixed 1.5MHz frequency. The voltage control loop is internally compensated and provides enough phase margins for stable operation with a wide load range and battery voltage range.

In Boost mode, the N-FET Q1 prevents battery is over discharged when VBUS pin is over loaded. Cycle-by-cycle current limit is done by sensing the current through the N-FET Q3. The cycle-by-cycle current limit threshold of Q3 is set to the nominal 2.9A peak current. Synchronous operation is used in PWM mode to reduce the power losses.

### *Boost Start-Up*

To reduce the inrush current, a soft-start control is performed during the start-up stage in Boost mode.

### *PFM Mode at Light Load*

To minimize the output overshoot in Boost mode, the device starts with PFM first and then switches to PWM. As stated before, PFM can be avoided by using OTG_PFM_DIS bit in Boost mode.

### *Protection in Boost Mode*

The SGM41517A provides an over-voltage protection to protect the device and other components from the damage by too high VBUS voltage. When VBUS OVP happens, the IC turns off the switching and N-FET Q1, resets OPA_MODE bit to 0, sets fault status bits, and sends out a fault pulse at the STAT pin. When the VBUS drops to the normal level, the Boost can be started again after the OPA_MODE bit is set to 1 by host or the OTG pin remains in the active status.

The SGM41517A provides a built-in over-current protection to prevent the device and battery damage when VBUS is over-current. Once an over-current condition is detected, Q1 operates in linear mode, limiting the output current to about 1.4A. If the over-current condition lasts longer than 30ms, the over-current fault is detected. When an over-current is found, the IC sets fault status bits, sends out fault pulse in STAT pin and turns off the PWM converter for 250ms. After 7 times retry (Hiccup), OPA_MODE bit is reset to 0. The 7 times will reset and retime if REG0x00 or REG0x01 is read during Hiccup. If Boost mode is enabled by OTG pin and EN_OTG bit, the Boost will start through reading REG0x00 or REG0x01 when overload is removed.

During boosting period, when the battery voltage is higher than the over-voltage threshold of the battery ($V_{BATMAX}$) or lower than the minimum battery voltage threshold ($V_{BATMIN}$), the switching and N-FET Q1 are turned off by the device, the OPA_MODE bit is reset to 0, the fault status bits are set and the fault pulse is sent out at the STAT pin. When the battery voltage is higher than $V_{BATMIN}$, the Boost can be begun after the OPA_MODE bit is set to 1 by host or the OTG pin remains in the active status.

## High-Impedance (Hi-Z) Mode

In Hi-Z mode, the charger stops charging or boosting and enters a low quiescent current state to save power. Set the CD_TS pin to high level can cause the charger to enter Hi-Z mode. When in default mode and the CD_TS pin is low, the charger automatically enters Hi-Z mode when VBUS falls below UVLO.

When in host mode and the CD_TS is low, the charger can be placed into Hi-Z mode if the HZ_MODE control bit is set to 1 and not in Boost mode enabled by OTG pin and EN_OTG bit.

For exiting Hi-Z mode, the CD_TS pin must go to low, the VBUS must be higher than UVLO, and the HZ_MODE control bit must be written to 0 by host.

# DETAILED DESCRIPTION (continued)

## I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM41517A parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM41517A operates as a slave device that address is 0x6A. It has nine 8-bit registers, numbered from REG0x00 to REG0x08. A register read beyond REG0x08 (0x08) returns 0xFF.

### Physical Layer

The standard I²C interface of SGM41517A supports standard mode and fast mode communication speeds. The frequency of standard mode is up to 100kbits/s, while the fast mode is up to 1Mbits/s. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA pin is open-drain.

## I²C Data Communication

### START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 7. All transactions begin by the master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

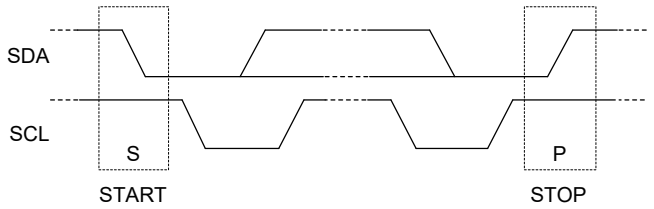



**Figure 7. I²C Bus in START and STOP Conditions**

### Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the high period of the clock. The state of the SDA can only change when the clock (SCL) is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 8.

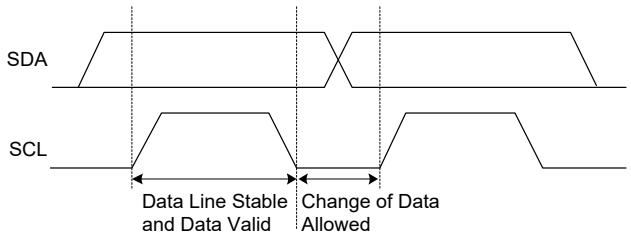



**Figure 8. Bit Transfer**

### Byte Format

The data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. Figure 9 shows the byte transfer process with I²C interface.

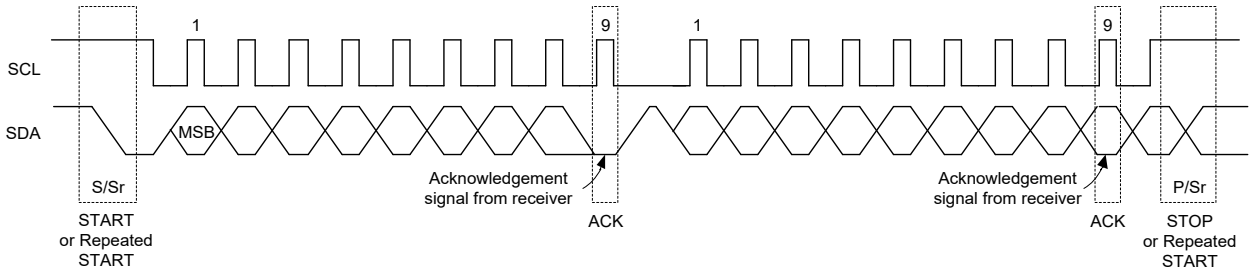



**Figure 9. Byte Transfer Process**

# DETAILED DESCRIPTION (continued)

### Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by the master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

### Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 10.

**WRITE:** If the master wants to write in the register, the third byte can be written directly as shown in Figure 11 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

**READ:** If the master wants to read a single register (Figure 12), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

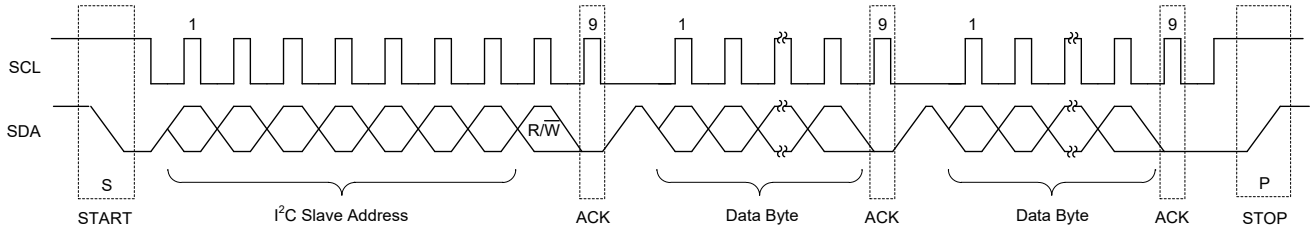



**Figure 10. Data Transfer Transaction**

## DETAILED DESCRIPTION (continued)

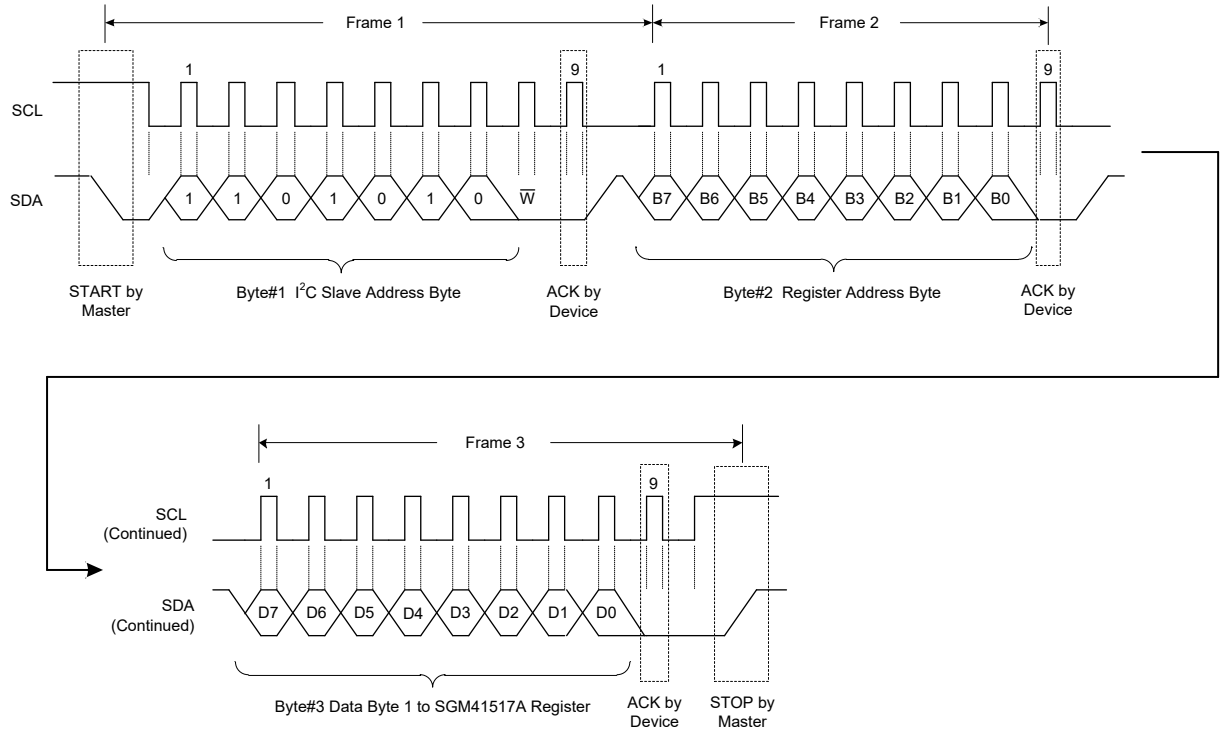



**Figure 11. A Single Write Transaction**

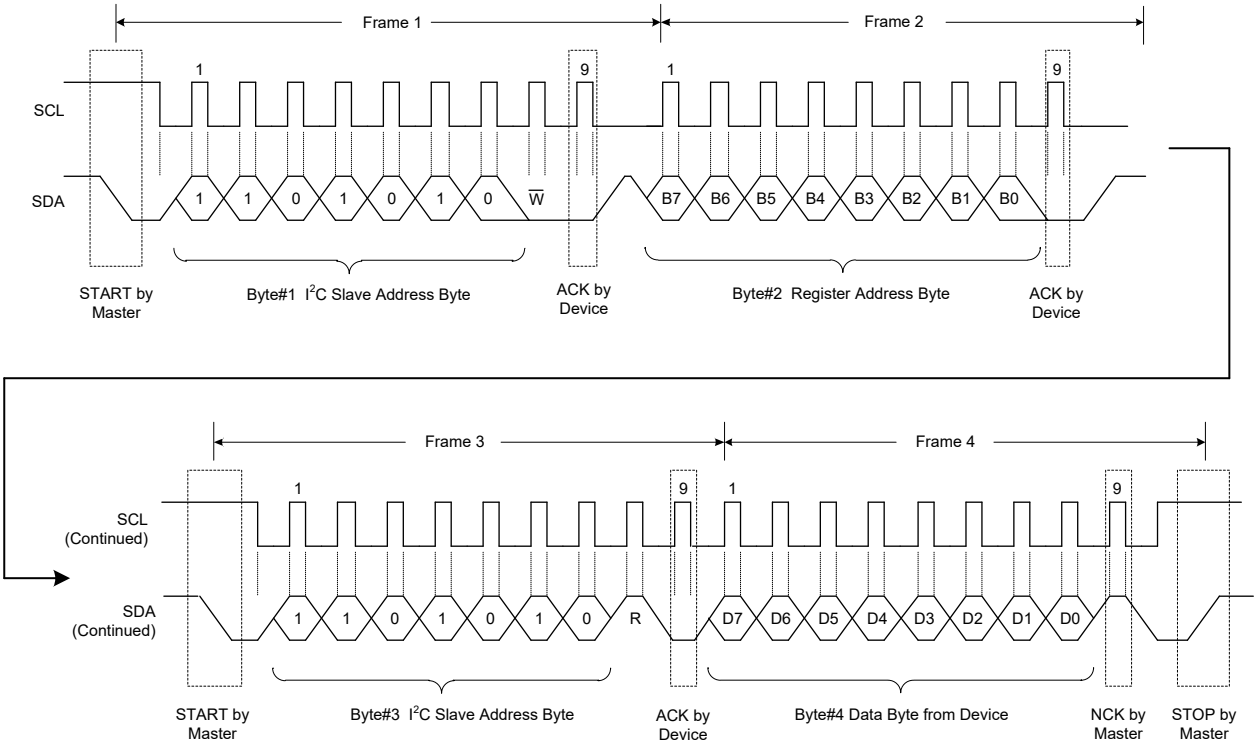



**Figure 12. A Single Read Transaction**

## DETAILED DESCRIPTION (continued)

### Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM41517A for all the registers, as explained in Figure 13 and Figure 14. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

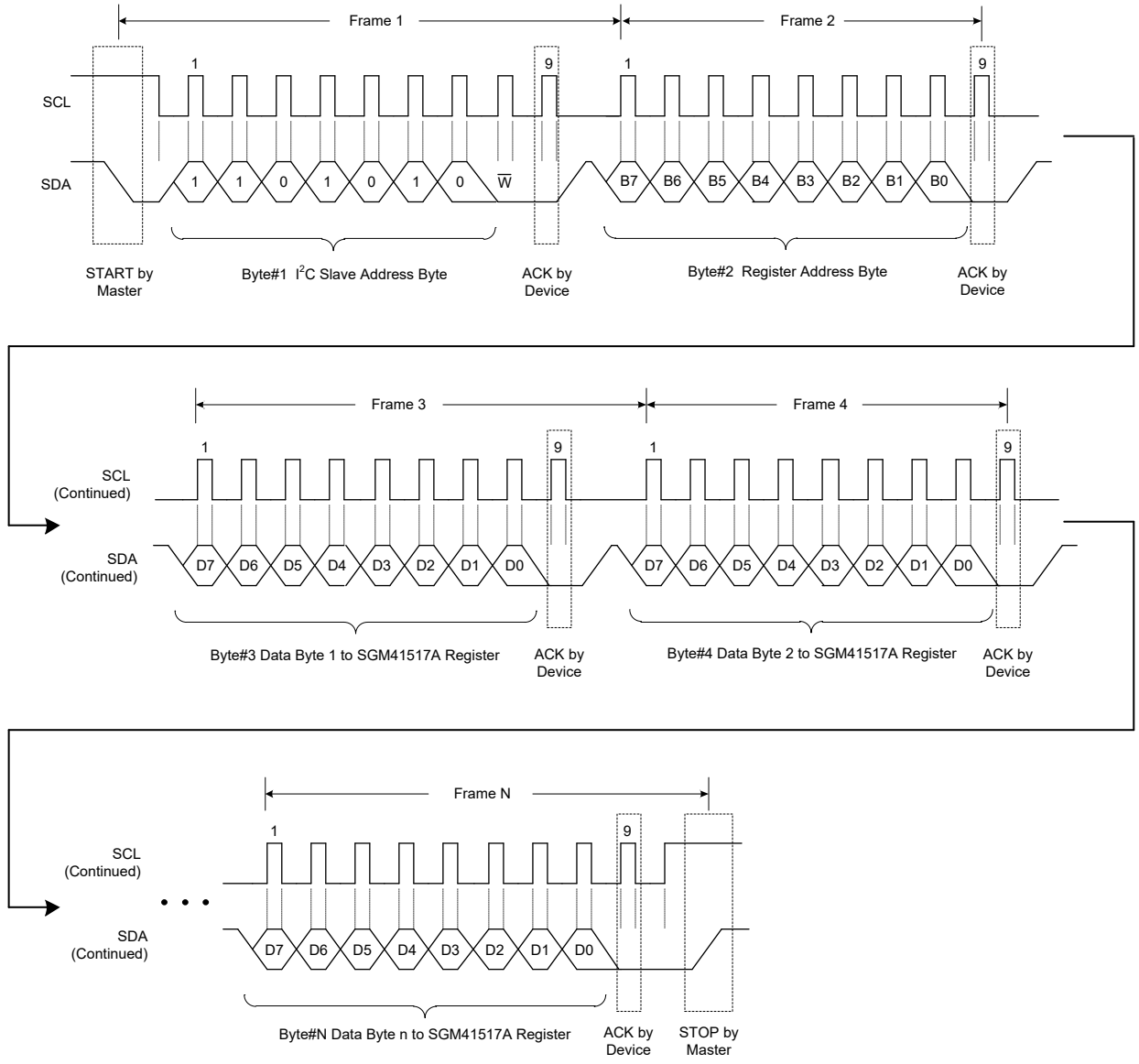



**Figure 13. A Multi-Write Transaction**

## DETAILED DESCRIPTION (continued)

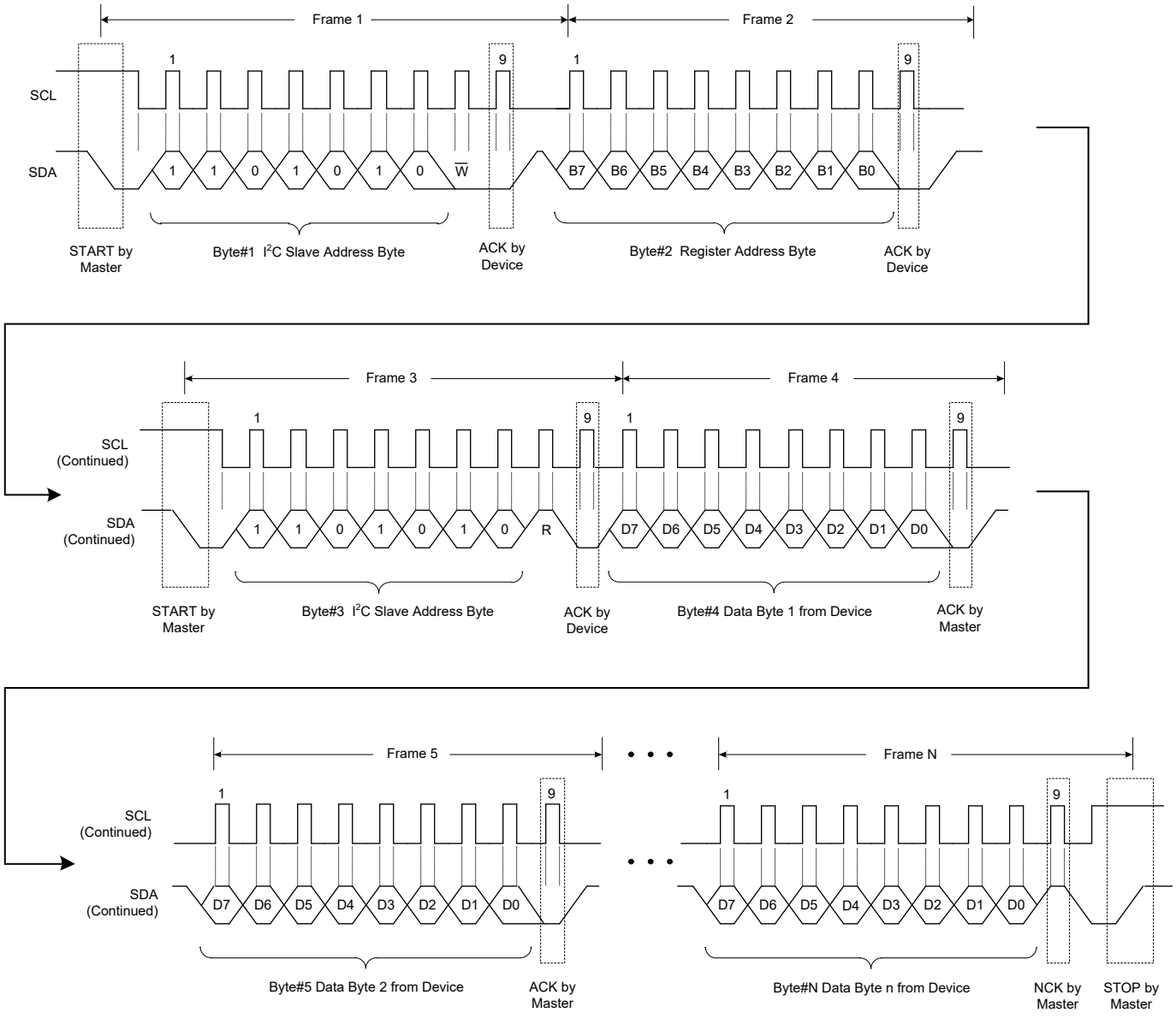



**Figure 14. A Multi-Read Transaction**

## DETAILED DESCRIPTION (continued)

### I2C_25ms Timeout

In $I^2C$ communication, some issues happen sometimes: 1) $I^2C$ device pulls SDA forever to ground caused by ground noise or supply power noise. 2) SCL clock disappear sometimes because of host interrupt or power down. For SGM41517A, $I^2C$ circuit monitor the SCL and SDA line all the time once $I^2C$ interface is alive, when the lasting low level is over 25ms for SCL or SDA, $I^2C$ circuit will return to the idle state and release the SCL & SDA line unconditionally.

#### *Slave Address Byte*

The slave address byte is the first byte received from the master device after the START condition.

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | X |

#### *Register Address Byte*

After successfully confirming the slave address, the bus master sends a byte to the device containing the address of the register to be accessed. The SGM41517A contains nine 8-bit registers that can be accessed via a bidirectional $I^2C$ interface. Eight of the internal registers have read and write access and one has read access only.

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | D2 | D1 | D0 |

# REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

## I²C Register Address Map

| FUNCTION | STAT | FLAG | MASK | THRESHOLD SETTING | ENABLE |
|---|---|---|---|---|---|
| CHARGE | 0x00[5:4] | — | — | — | 0x01[0] + 0x01[2] |
| VBAT_REG | — | — | — | 0x02[7:2] + 0x06[3:0] | — |
| ICHGR | — | — | — | 0x04[6:3] + 0x06[7:4] | — |
| ITERM | — | — | — | 0x04[2:0] | 0x01[3] |
| VRECHG | — | — | — | 0x07[5:4] | — |
| TERM_DGL | — | — | — | 0x07[7:6] | — |
| VINDPM | 0x05[4] | — | — | 0x05[2:0] | — |
| IIN_LIMIT | — | — | — | 0x01[7:6] | 0x01[7:6] |
| STAT_SET | — | — | — | — | 0x00[6] |
| HZ_MODE | — | — | — | — | 0x01[1] |
| OTG | 0x00[3] | — | — | 0x08[5:4] | 0x01[0] + 0x02[1:0] |
| BUCK_FREQ_SET | — | — | — | 0x08[7] | — |
| PFM | — | — | — | — | 0x08[6] |
| JEITA | 0x08[2:0] | — | — | — | 0x07[3] |
| JEITA_VSET_H | — | — | — | 0x07[1] | — |
| JEITA_ISET_L | — | — | — | 0x07[0] | — |
| JEITA_ISET_H | — | — | — | 0x07[2] | — |
| VBUS_OVP | 0x00[2:0] | — | — | 0x08[3] | — |
| CHARGE FAULT | 0x00[2:0] | — | — | — | — |
| BOOST FAULT | 0x00[2:0] | — | — | — | — |
| I2C_HI_DETC | — | — | — | 0x05[6] | — |
| TMR_RST | — | — | — | — | 0x00[7] |
| RESET | — | — | — | — | 0x04[7] |
| SAFETY_TIMER | — | — | — | — | 0x05[5] |
| VENDER | 0x03[7:5] | — | — | — | — |
| PN | 0x03[4:3] | — | — | — | — |
| Revision | 0x03[2:0] | — | — | — | — |

# REGISTER MAPS (continued)

## 7-Bit I²C Slave Device Address of SGM41517A: 0b1101 010 + W/R

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

R/WC: Read/Write bit. Writing a 1 clears the bit. Writing a '0' has no effect.

n: Parameter code formed by the bits as an unsigned binary number.

## REG0x00: Status/Control Register [Reset = 0xXX]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7] | TMR_RST/OTG | x | R/WC | TMR_RST Function (Write)<br>Write 1 to reset the safety timer (auto clear).<br><br>OTG Pin Status (Read)<br>0 = OTG pin at low-level<br>1 = OTG pin at high-level |
| D[6] | EN_STAT | 1 | R/W | 0 = Disable STAT pin function<br>1 = Enable STAT pin function (default) |
| D[5:4] | STAT[1:0] | xx | R | 00 = Ready<br>01 = Charge in progress<br>10 = Charge done<br>11 = Fault |
| D[3] | BOOST | x | R | 0 = Not in Boost mode<br>1 = Boost mode |
| D[2:0] | FAULT[2:0] | xxx | R | Charge Mode:<br>000 = Normal<br>001 = VBUS OVP<br>010 = Sleep mode<br>011 = Bad adapter or $V_{VBUS}$ < $V_{UVLO}$<br>100 = Output OVP<br>101 = Thermal shutdown<br>110 = Timer fault<br>111 = No battery<br><br>Boost Mode:<br>000 = Normal<br>001 = VBUS OVP<br>010 = Overload<br>011 = Battery voltage is too low<br>100 = Battery OVP<br>101 = Thermal shutdown<br>110 = NA<br>111 = NA<br>When fault event happens, the FAULT[2:0] bits are used to record the events. Once the device returns to normal status, the FAULT[2:0] bits can be read clear to 3'b000 by AP. |

# REGISTER MAPS (continued)

## REG0x01: Control Register [Reset = 0x30]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7] | IIN_LIMIT_2 | 0 | R/W | 00 = USB host with 500mA current limit (default)<br>01 = USB host with 100mA current limit<br>10 = USB host/charger with 800mA current limit<br>11 = No input current limit |
| D[6] | IIN_LIMIT_1 | 0 | R/W | |
| D[5:4] | Reserved | 11 | R/W | Reserved |
| D[3] | TE | 0 | R/W | 0 = Disable charge current termination (default)<br>1 = Enable charge current termination |
| D[2] | nCE | 0 | R/W | 0 = Charger enabled (default)<br>1 = Charger is disabled |
| D[1] | HZ_MODE | 0 | R/W | 0 = Not high-impedance mode (default)<br>1 = High-impedance mode |
| D[0] | OPA_MODE | 0 | R/W | 0 = Charger mode (default)<br>1 = Boost mode |

## REG0x02: Control/Battery Voltage Register [Reset = 0x8E]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:2] | VBAT_REG[5:0] | 10 0011 | R/W | Battery Regulation Voltage (n: 6 bits)<br>= 3500 + 20n (mV) if n ≤ 55<br>= 4600mV if n > 55<br><br>Offset: 3.5V<br>Range: 3.5V (000000) - 4.6V (110111)<br>Default: 4.2V (100011) |
| D[1] | OTG_PL | 1 | R/W | 0 = OTG Boost enable with low-level<br>1 = OTG Boost enable with high-level (default)<br>Not applicable to OTG pin control of current limit at POR in default mode. |
| D[0] | EN_OTG | 0 | R/W | 0 = Disable OTG pin in host mode (default)<br>1 = Enable OTG Pin in host mode<br>Not applicable to OTG pin control of current limit at POR in default mode. |

## REG0x03: Vender/Part/Revision Register [Reset = 0x59]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7] | VENDER2 | 0 | R | Vender Code: Bit 2 |
| D[6] | VENDER1 | 1 | R | Vender Code: Bit 1 |
| D[5] | VENDER0 | 0 | R | Vender Code: Bit 0 |
| D[4:3] | PN[1:0] | 11 | R | For $I^2C$ Address 0x6A:<br>01 = NA<br>10 = SGM41517<br>11 = SGM41517A (default) |
| D[2:0] | Revision[2:0] | 001 | R | 011 = Revision 1.0<br>001 = Revision 1.1 (default)<br>100 - 111 = Future revisions |

# REGISTER MAPS (continued)

## REG0x04: Battery Termination/Fast Charge Current Register [Reset = 0x19]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7] | RESET | 0 | R/WC | Write:<br>0 = No effect (default)<br>1 = Charger in reset mode<br>Read: always get "0". Reset the registers to the default value except the REG0x06 and all read only bits when write 1 to RESET bit, and return to 0 automatically. |
| D[6:3] | ICHGR[3:0] | 0011 | R/W | Fast Charge Current Setting<br>n = ICHGR[3:0]<br>$I_{CHG}$ (mA) = 200mA + n × 100mA when n ≤ 13<br>$I_{CHG}$ (mA) = 1800mA when n = 14<br>$I_{CHG}$ (mA) = 2000mA when n = 15<br>$I_{CHG}$ (mA) = 500mA (default) |
| D[2:0] | ITERM[2:0] | 001 | R/W | Termination Current Setting<br>n = ITERM[2:0]<br>$I_{TERM}$ (mA) = 50mA + n × 50mA (1 ≤ n ≤ 7)<br>Range:100mA (001) - 400mA (111)<br>Default: 100mA |

## REG0x05: Special Charger Voltage/Enable Pin Status Register [Reset = 0xXX]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7] | Reserved | 0 | R/W | Reserved |
| D[6] | I2C_HI_DETC | 0 | R/W | $I^2C$ I/O Selection Bit<br>0 = 1.8V (default)<br>1 = 1.2V |
| D[5] | SAFETY_TIMER_DIS | 0 | R/W | 0 = Enable safety timer (default)<br>1 = Disable safety timer |
| D[4] | DPM_STATUS | x | R | VBUS Input Voltage DPM Status Bit<br>0 = DPM mode is not active<br>1 = DPM mode is active |
| D[3] | CD_TS_STATUS | x | R | CD_TS Pin Status Bit, Only Valid when EN_JEITA = 0<br>0 = CD_TS pin at low-level<br>1 = CD_TS pin at high-level |
| D[2:0] | VSREG[2:0] | 100 | R/W | Special Charger Voltage to Set the $V_{IN\_DPM}$ (n: 3 bits)<br>= 4200 + 80n (mV)<br><br>Offset: 4.2V<br>Range: 4.2V (000) - 4.76V (111)<br>Default: 4.52V |

NOTE:

1. It is recommended to set VSREG[2:0] - $V_{BAT}$ > 100mV to avoid Boost-back when plug out adapter.

# REGISTER MAPS (continued)

## REG0x06: Safety Limit Register [Reset = 0xFF]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:4] | MCHRG[3:0] | 1111 | R/W | Maximum Fast Charge Current Setting<br>n = MCHRG[3:0]<br>$I_{CHG}$ (mA) = 200mA + n × 100mA when n ≤ 13<br>$I_{CHG}$ (mA) = 1800mA when n = 14<br>$I_{CHG}$ (mA) = 2000mA when n = 15 (default) |
| D[3:0] | MREG[3:0] | 1111 | R/W | Maximum Battery Safe Regulation Voltages<br>n = MREG [3:0]<br>$V_{SAFE\_REG}$ (mV) = 4200mV + n × 40mV when n ≤ 10<br>$V_{SAFE\_REG}$ (mV) = 4600mV when n > 10 (default) |

NOTES:

1. The safety fast charge current is 2000mA by default and the maximum charge current option is 2A.

2. The safety battery regulation voltage is 4.6V by default and maximum battery regulation voltage option is 4.6V.

3. Memory location REG0x06 resets only when either 1) $V_{BAT}$ < $V_{SHORT}$ threshold (2.1V TYP) if $V_{VBUS}$ > $V_{IN(MIN)}$ and $V_{VBUS}$ - $V_{BAT}$ > $V_{SLP}$ or 2) $V_{VBUS}$ < $V_{IN(MIN)}$ or 3) $V_{VBUS}$ - $V_{BAT}$ < $V_{SLP}$ or 4) $V_{VBUS}$ > UVLO or 5) enter Hi-Z mode. Programmed values in the safety limit register ensure that higher values from REG0x02 (VBAT_REG[5:0]) and from REG0x04 (ICHGR[3:0]) cannot be successfully written.

## REG0x07: JEITA, Recharge and Charge Termination Configure Register [Reset = 0x50]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:6] | TERM_DGL[1:0] | 01 | R/W | Charging Current Termination Deglitch Time<br>00 = 8ms<br>01 = 16ms (default)<br>10 = 32ms<br>11 = 64ms |
| D[5:4] | VRCHG[1:0] | 01 | R/W | Recharge Threshold below Battery Regulation Voltage<br>00 = 50mV<br>01 = 100mV (default)<br>10 = 150mV<br>11 = 200mV |
| D[3] | EN_JEITA | 0 | R/W | JEITA Guideline Enable Bit<br>CD_TS pin is used for sensing battery temperature.<br>0 = Disable (default)<br>1 = Enable |
| D[2] | JEITA_ISET_H | 0 | R/W | Charge current setting when battery temperature is between T3 and T4, only valid when EN_JEITA bit = 1.<br>0 = 10% of $I_{CHG}$ (default)<br>1 = 0% of $I_{CHG}$ |
| D[1] | JEITA_VSET_H | 0 | R/W | JEITA charge voltage when battery temperature is at T3 - T4, only valid when EN_JEITA bit = 1.<br>0 = Set Charge Voltage to $V_{BAT\_REG}$ -100mV (default)<br>1 = Set Charge Voltage to $V_{BAT\_REG}$ |
| D[0] | JEITA_ISET_L | 0 | R/W | JEITA charge current when battery temperature is between T1 and T2, only valid when EN_JEITA bit = 1.<br>0 = 10% of $I_{CHG}$ (default)<br>1 = 0% of $I_{CHG}$ |

## REGISTER MAPS (continued)

### REG0x08: MISC Register [Reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7] | BUCK_FREQ_SET | 0 | R/W | Frequency Setting in Buck mode<br>0 = 1500kHz (default)<br>1 = 500kHz |
| D[6] | OTG_PFM_DIS | 0 | R/W | OTG PFM Mode Disable Bit<br>0 = Enabled (default)<br>1 = Disabled (FCCM mode) |
| D[5:4] | OTG_VOUT[1:0] | 00 | R/W | OTG Output Voltage at VBUS pin<br>00 = 5.05V (default)<br>01 = 5.15V<br>10 = 5.25V<br>11 = 5.35V |
| D[3] | VBUS_OVP | 0 | R/W | VBUS OVP Threshold<br>0 = 6.5V (default)<br>1 = 14V |
| D[2:0] | NTC_FAULT[2:0] | 000 | R | NTC Fault Indication, only Valid When EN_JEITA = 1<br>000 = Normal (default)<br>010 = Warm<br>011 = Cool (Buck mode only)<br>101 = Cold<br>110 = Hot<br>NTC fault bits are updated in real-time and do not need a read to reset. |

# APPLICATION INFORMATION

The SGM41517A is a tiny, high-efficiency, switch-mode charge management solution for single-cell Li-Ion and Li-polymer batteries. The SGM41517A integrates a synchronous PWM controller, power MOSFETs, input current sensing, high-accuracy current and voltage regulation, charging current sense resistor and charge termination and has a small UTQFN-2×2-20L package.

## Design Requirements

Table 4 shows the typical application design specifications, it is used to select external components values for the SGM41517A.

## Detailed Design Procedure

Systems design specifications:

• $V_{VBUS}$ = 5V

• $V_{BAT}$ = 4.2V (1-cell)

• $I_{CHG}$ = 2A

• Inductor ripple current = 30% of fast charge current

## Inductor Design

The inductor value ($L_{OUT}$) is determined for the specified charge current ripple, as shown in the formula below:

$$L_{OUT} = \frac{V_{BAT} \times (V_{VBUS} - V_{BAT})}{V_{VBUS} \times f \times \Delta I_L} \quad (3)$$

The worst case scenario is that the battery voltage is close to half of the input voltage. The detailed calculation is as follows:

$$L_{OUT} = \frac{2.5 \times (5 - 2.5)}{5 \times (1.5 \times 10^6) \times 2 \times 0.3}$$

$L_{OUT}$ = 1.38μH

When the output inductor is determined to be the standard 1μH, the total ripple current is calculated using the 1μH inductance, as shown in the formula below:

$$\Delta I_L = \frac{V_{BAT} \times (V_{VBUS} - V_{BAT})}{V_{VBUS} \times f \times L_{OUT}} \quad (4)$$

The detailed calculation is as follows:

$$\Delta I_L = \frac{2.5 \times (5 - 2.5)}{5 \times (1.5 \times 10^6) \times (1 \times 10^{-6})}$$

$\Delta I_L$ = 0.83A

The maximum output current is calculated as follows:

$$I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (5)$$

The detailed calculation is as follows:

$$I_{LPK} = 2 + \frac{0.83}{2}$$

$I_{LPK}$ = 2.42A

## Output Capacitor Design

The output capacitor value ($C_{OUT}$) is determined by using 40kHz as the resonant frequency, as shown in the formula below:

$$f_O = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (6)$$

The detailed calculation is as follows:

$$C_{OUT} = \frac{1}{4\pi^2 \times f_O^2 \times L_{OUT}}$$

$$C_{OUT} = \frac{1}{4\pi^2 \times (40 \times 10^3)^2 \times (1 \times 10^{-6})}$$

$C_{OUT}$ = 15.8μF

Select two 0603 X5R 6.3V 10μF in parallel or one 0603 X5R 6.3V 22μF ceramic capacitor.

**Table 4. Typical Application Design Specifications**

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input DC Voltage | $V_{IN}$ | Input voltage from AC adapter input | 4 | 5 | 13.2 | V |
| Input Current | | Maximum input current from AC adapter input | 0.1 | 0.5 to 0.8 | | A |
| Charge Current | | Battery charge current | 0.2 | 0.5 | 2 | A |
| Output Regulation Voltage | | Voltage applied at $V_{BAT}$ | 0 | 3 to 4.2 | 4.6 | V |
| Operating Junction Temperature Range | $T_J$ | | 0 | | 125 | ℃ |

# APPLICATION INFORMATION (continued)

## Power Supply Recommendations

### System Load

Figure 15 shows the simple high-efficiency topology for the charging system. The input voltage has been step down to the system voltage with good efficiency by Buck converter. When the input power is present, it powers the system load and charges the battery pack at the same time. As shown in Figure 15, the actual charging current flowing into battery is equal to $I_{CHG}$ - $I_{SYS}$. When the input power is absent, the battery pack directly supplies power to the system.

#### *The Advantages*

1. When the AC adapter is removal, the battery pack powers the system load directly. Therefore, the system's operating time in the battery pack can be maximized.

2. It removes the switch on the power path and offers a lowest-cost solution.

3. Dynamic power management (DPM) feature is also included that automatically reduces the charge current if the input current or voltage limit is reached. Therefore, there is no potential over-current or overheating issues caused by excessive system load requirements.

4. To implement DPM, the device always monitors the input current and voltage to regulate power demand from the source and avoid input adapter overloading or to meet the maximum current limits specified in the USB specs.

5. The supply voltage variation range for the system can be minimized because system is connected with battery directly.

6. The input current soft-start can be achieved by the generic soft-start function.

#### *Design Requirements and Potential Issues*

1. To achieve optimal performance, the power input capacitor connected from the input to the PGND should be as close to the pins as possible. The output inductor should be placed close to the IC, and the output capacitor should be connected between the inductor and PGND, the purpose of which is to minimize the current path loop area from the SW pin through the LC filter and back to PGND pin. To prevent high-frequency oscillation problems, it is important to have an appropriate layout to minimize the high-frequency current path loop (see Figure 16).

2. Place all decoupling capacitors close to their respective pins and close to PGND (do not place components to avoid wiring interruptions to the power stage current). All small control signals should be kept away from high current paths.

3. The PCB should have a grounding plane (circuit) that is directly connected to the circuit of all components through a through hole (two through holes per capacitor for power level capacitors, two through holes for IC PGND, and one through hole per capacitor for small signal components). The star grounding design method is commonly used to maintain current isolation in circuit blocks (high power/low power small signals), which reduces noise coupling and ground bounce issues. This design produces good results with a single grounding plane. Through this small layout and a single grounding plane, there is no issue of grounding rebound, and isolating components can minimize coupling between signals.

4. The size of the high current charging path entering VBUS, PMID, and from SW pins must be suitable for the maximum charging current to avoid voltage drop in these traces. It is recommended that the PGND pin be connected to the ground plane to return current through the N-FET Q3.

5. The 4.7μF PMID capacitor should be placed as close as possible to the PMID pin and PGND pin to minimize the area of the high-frequency current circuit. Add 1μF input capacitor should be placed as close as possible to the VBUS pin and PGND pin to minimize the area of the high-frequency current circuit (see Figure 17).

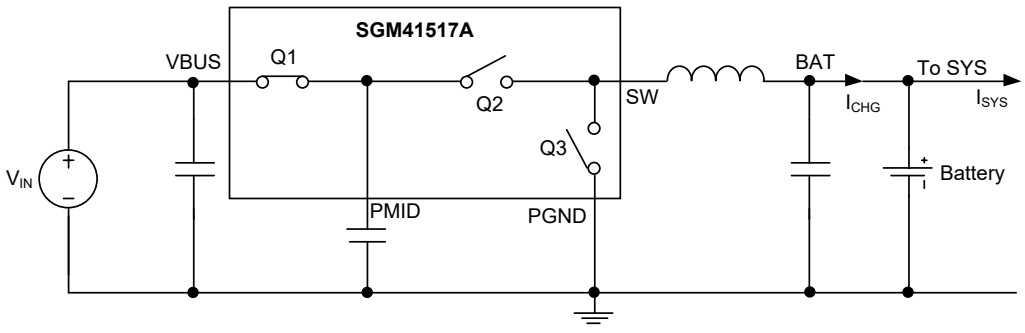



**Figure 15. System Load**

# APPLICATION INFORMATION (continued)

## Layout Guidelines

For PCB layout, the following figure provides some guidelines.

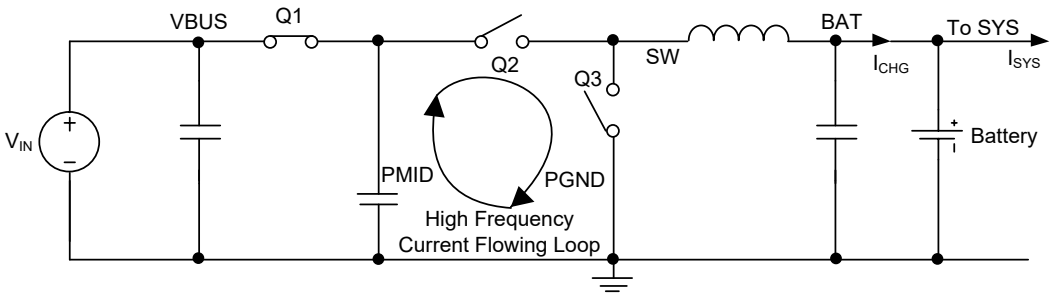



**Figure 16. High Frequency Current Path**

## Layout Example

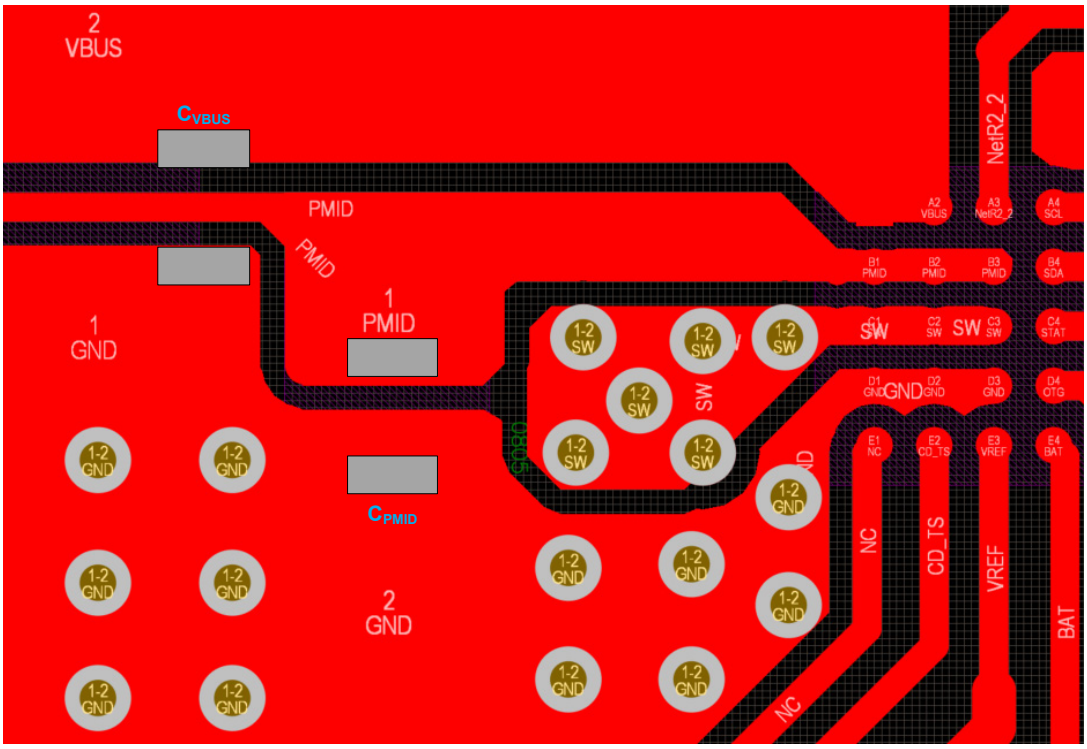



**Figure 17. Layout Example**

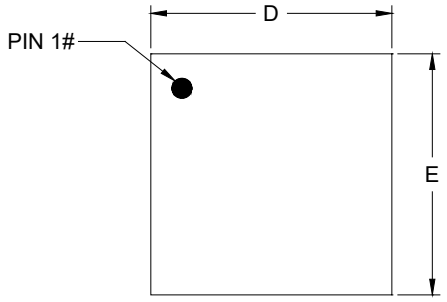
# REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

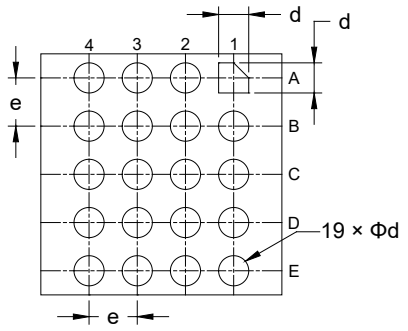
| Changes from Original to REV.A (APRIL 2026) | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

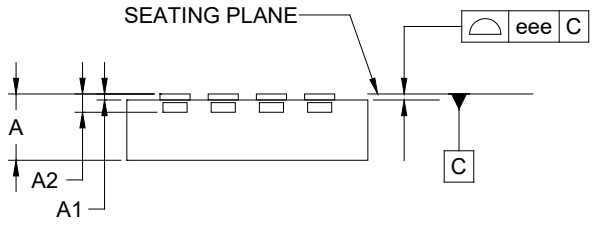
## UTQFN-2×2-20L



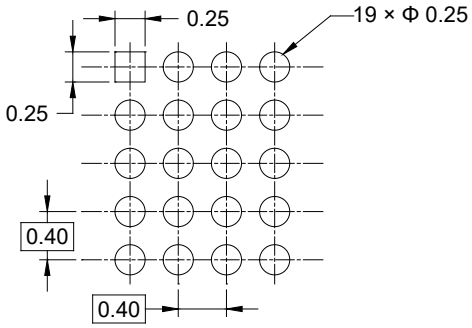

TOP VIEW




BOTTOM VIEW




SIDE VIEW



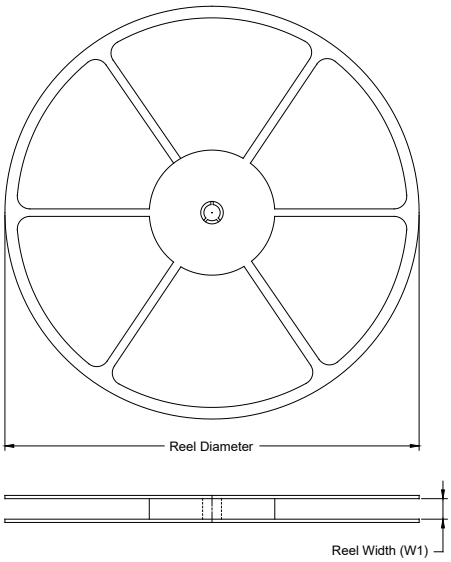

**RECOMMENDED LAND PATTERN** (Unit: mm)

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.500 | - | 0.600 |
| A1 | 0.000 | - | 0.050 |
| A2 | 0.152 REF | | |
| d | 0.200 | - | 0.300 |
| D | 1.900 | - | 2.100 |
| E | 1.900 | - | 2.100 |
| e | 0.400 BSC | | |
| eee | 0.080 | | |

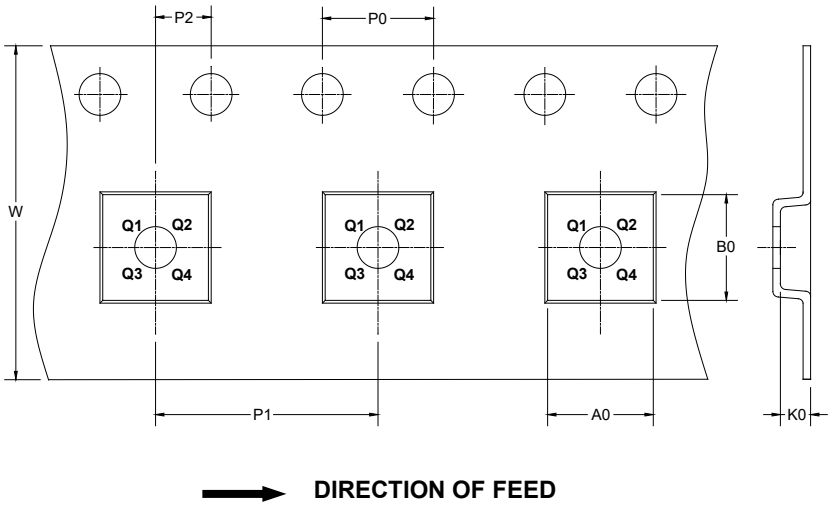
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

## REEL DIMENSIONS




## TAPE DIMENSIONS



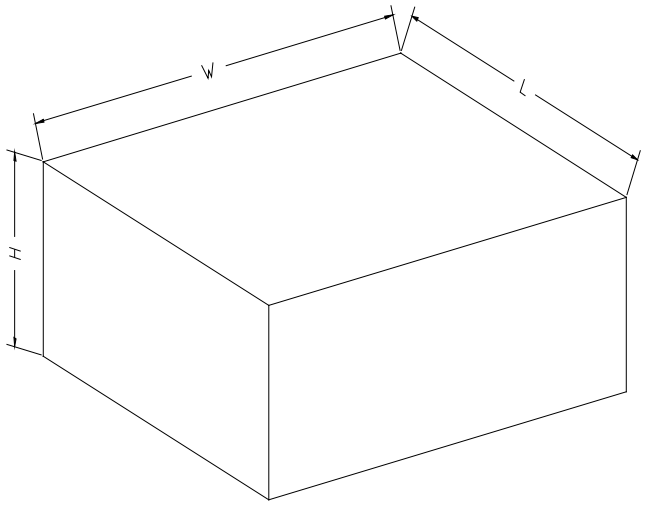

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| UTQFN-2×2-20L | 7″ | 9.5 | 2.30 | 2.30 | 0.75 | 4.0 | 4.0 | 2.0 | 8.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 7″ (Option) | 368 | 227 | 224 | 8 |
| 7″ | 442 | 410 | 224 | 18 |

DD0002