SGM52001-16
16-Bit, 1MSPS, 8-Channel Low Power, Serial Interface ADC

GENERAL DESCRIPTION

The SGM52001-16 is a 16-bit, 8-channel, successive approximation (SAR) analog-to-digital converter (ADC).

The device is powered by a single source VDD (generally is 3.3V).

The device can communicate with 1.8V to 3.6V digital device in which condition the VIO needs to be powered by appropriate voltage accordingly.

The digital interface is compatible to the traditional SPI protocol.

The SGM52001-16 is available in a Green WLCSP-2.39×2.39-20B package. It operates over an ambient temperature range of -40℃ to +125℃.

APPLICATIONS

Process Control
Power Line Monitoring
Battery-Powered Equipment
Instrumentation

FEATURES

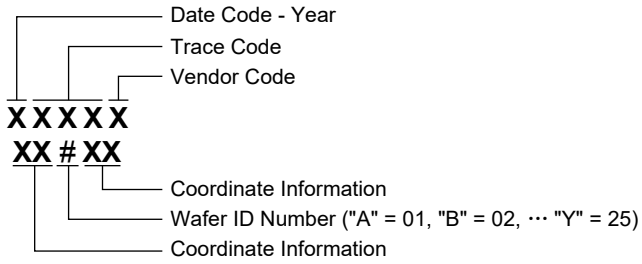
- **16 Bits, 1MSPS SAR ADC**
- **No Missing Codes**
- **8-Channel Multiplexer**
- **Supported Input Types:**
  - **Single-Ended**
  - **Pseudo Differential (Reference to 1/2V_{REF})**
  - **Pseudo Differential (Reference to GND)**
- **Analog Input Range:**
  0V to V_{REF} with V_{REF} up to V_{DD}
- **Supply Voltage Ranges:**
  - **Analog Supply: 3V to 3.6V**
  - **I/O Supply: 1.8V to 3.6V**
- **Integral Nonlinearity (INL): ±1.5LSB (TYP)**
- **Total Harmonic Distortion (THD):**
  -104dB (TYP) at 20kHz
- **Signal-to-Noise + Distortion (SINAD):**
  88.5dBFS (TYP) at 20kHz
- **Power Dissipation**
  - **28mW at 1MSPS**
  - **2.7mW at 100kSPS**
- **Standby Current: 1μA (TYP)**
- **Multiple Reference Type**
  - **External Reference: Up to V_{DD}**
- **Support Channel Sequencer**
- **Support Selectable 1-Pole Filter and Busy Indicator**
- **SPI-Compatible Serial Interface**
- **Available in a Green WLCSP-2.39×2.39-20B Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM52001-16	WLCSP-2.39×2.39-20B	-40℃ to +125℃	SGM52001-16XSG/TR	SGM276 XXXXX XX#XX	Tape and Reel, 500
			SGM52001-16XG/TR	SGM276 XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs
- INx, COM ..... GND - 0.3V to V_{DD} + 0.3V
- REF, REFIN ..... GND - 0.3V to V_{DD} + 0.3V

Supply Voltages
- V_{DD}, V_{IO} to GND ..... -0.3V to 6V
- V_{DD} to V_{IO} ..... ±6V

DIN, CNV, SCLK to GND ..... -0.3V to V_{IO} + 0.3V
SDO to GND ..... -0.3V to V_{IO} + 0.3V
Input Current to Any Pin except Supplies ..... ±10mA
Package Thermal Resistance
- WLCSP-2.39×2.39-20B, θ_{JA} ..... 72℃/W
- WLCSP-2.39×2.39-20B, θ_{JB} ..... 21.4℃/W
- WLCSP-2.39×2.39-20B, θ_{JC} ..... 12℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

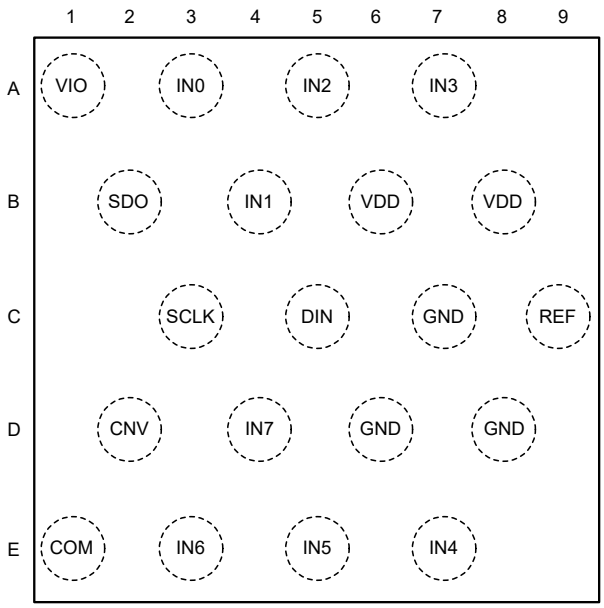
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.39×2.39-20B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	VIO	P	Input/Output Interface Digital Power Supply Pin. Generally, this pin is powered with the same power source of digital controller.
A3, B4, A5, A7	IN0 to IN3	AI	Analog Input Pins, Input Channel 0 to Channel 3.
B2	SDO	DO	Serial Data Output Pin. It is the digital data output pin of serial interface. The SDO will synchronize with the above SCLK and output conversion result. When IN- is connected with GND, the conversion results are straight binary. When IN- is connected with $1/2V_{REF}$, the conversion results are two's complement.
B6, B8	VDD	P	Power Supply Pin. The power supply of this pin must be higher than the voltage potential of reference. 10μF and 100nF decoupling capacitors should be connected here. The range of VDD is from 3V to 3.6V.
C3	SCLK	DI	Serial Data Clock Input Pin. It is the digital clock input pin of serial interface. The SPI data is locked out is in MSB first format.
C5	DIN	DI	Data Input Pin. It is the digital input pin of SPI serial interface.
C9	REF	AI	Reference Input Pin. This pin needs to be decoupled by 10μF capacitors to GND and the capacitor should be installed as close to REF as possible. A precise reference should be directly connected to REF pin for the best drift effect.
D2	CNV	DI	Conversion Input Pin. It is a digital control pin. The rising edge of CNV signal starts the conversion. During conversion, if CNV is held high long enough, the busy indicator is disabled.
C7, D6, D8	GND	P	Power Supply Ground.
E1	COM	AI	Common Input Pin. Common voltage reference of analog input channels. All input channels can be referenced to a common mode point of 0V or $V_{REF}/2V$.
E7, E5, E3, D4	IN4 to IN7	AI	Analog Input Pins, Input Channel 4 to Channel 7.

NOTE: AI = analog input, AI/O = analog input/output, DI = digital input, DO = digital output, P = power.

ELECTRICAL CHARACTERISTICS

(T_A = -40℃ to +125℃, V_{DD} = 3.3V, V_{REF} = 3V, V_{IO} = 3V, all typical values are measured T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution				16			Bits
Analog Input							
Voltage Range	VIN+ - VIN-	Single-ended mode, or differential with COM (INx- = GND), or differential pairs (INx- = GND)		0		$+V_{REF}$	V
		Differential with COM (INx- = $1/2V_{REF}$), or differential pairs (INx- = $1/2V_{REF}$)		$-V_{REF}/2$		$+V_{REF}/2$	
Absolute Input Voltage		Positive input, unipolar and bipolar modes		-0.1		V_{REF} + 0.1	V
		Negative or COM input, unipolar mode		-0.1		+0.1	
		Negative or COM input, bipolar mode			$V_{REF}/2$		
Analog Input CMRR		f_{IN} = 250kHz			60		dB
Leakage Current at +25℃ Input Impedance (1)		Acquisition phase			5		nA
Throughput							
Conversion Rate		Full bandwidth (2)				1000	kSPS
		¼ bandwidth (2)				250	
Transient Response		Full-scale step, full bandwidth				200	ns
		Full-scale step, ¼ bandwidth				800	
Accuracy							
No Missing Codes					16		Bits
Integral Linearity	INL			-6.5	±1.5	5.5	LSB (3)
Differential Linearity	DNL			-0.99999	±0.6	3.5	LSB
Gain Error (4)	E_G			-19	±2	19	LSB
Gain Error Match				-9	±1	9	LSB
Offset Error (4)	E_O	INCC[2:0] = 00X		-19	±2.5	17	LSB
		INCC[2:0] = 010		-26	±4	14	
		INCC[2:0] = 10X		-23	±2	19.5	
		INCC[2:0] = 110		-22.5	±3.5	14	
		INCC[2:0] = 111		-18.5	±2	18.5	
Offset Error Match				-18	±5	18	LSB
Power Supply Sensitivity		V_{DD} = 3.3V			±1.5		LSB
Signal-to-Noise Ratio	SNR	f_{IN} = 20kHz, V_{REF} = 3V	INCC[2:0] = 00X	82.5	89		dBFS (5)
			INCC[2:0] = 010	82.5	89		
			INCC[2:0] = 10X	82.5	89		
			INCC[2:0] = 110	82	89		
			INCC[2:0] = 111	81.5	89		
Signal-to-Noise + Distortion	SINAD	f_{IN} = 20kHz, V_{REF} = 3V	INCC[2:0] = 00X	81.5	88.5		dBFS (5)
			INCC[2:0] = 010	81.5	88.5		
			INCC[2:0] = 10X	81.5	88.5		
			INCC[2:0] = 110	81.5	88.5		
			INCC[2:0] = 111	81	88.5		

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, V_{DD} = 3.3V, V_{REF} = 3V, V_{IO} = 3V, all typical values are measured T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC Accuracy							
Total Harmonic Distortion	THD	f_{IN} = 20kHz, V_{REF} = 3V	INCC[2:0] = 00X		-104	-87	dB
			INCC[2:0] = 010		-104	-87	
			INCC[2:0] = 10X		-104	-85	
			INCC[2:0] = 110		-104	-85	
			INCC[2:0] = 111		-104	-85	
Spurious Free Dynamic Range	SFDR	f_{IN} = 20kHz			107		dB
Channel-to-Channel Crosstalk		f_{IN} = 100kHz on adjacent channel(s)			-85		dB
Sampling Dynamics							
-3dB Input Bandwidth		Full bandwidth			17.5		MHz
		¼ bandwidth			4.4		
External Reference							
Voltage Range		REF input		0.5		V_{DD}	V
Current Drain		1MSPS, V_{REF} = 3V			240		μA
Digital Inputs							
Low Input Voltage	V_{IL}					0.23 × V_{IO}	V
High Input Voltage	V_{IH}			0.7 × V_{IO}			V
Low Input Current	I_{IL}			-1		1	μA
High Input Current	I_{IH}			-1		1	μA
Digital Outputs							
Data Format (6)							
Pipeline Delay (7)							
Low Output Voltage	V_{OL}	I_{SINK} = +500μA				0.4	V
High Output Voltage	V_{OH}	I_{SOURCE} = -500μA		V_{IO} - 0.3			V
Power Requirements							
Analog Supply Voltage	V_{DD}	Specified performance		3	3.3	3.6	V
Digital I/O Supply Voltage	V_{IO}	Specified performance		1.8	3.3	V_{DD}	V
Standby Current (8) (9)		V_{DD} and V_{IO} = 3.3V, at +25℃			1		μA
Power Dissipation		V_{DD} = 3.3V	100kSPS throughput		2.7		mW
			1MSPS throughput		28	72	
Temperature Range							
Specified Performance		T_{MIN} to T_{MAX}		-40		125	℃

NOTES:

1. Refer to the Input Structure section for more details.
2. The bandwidth depends on the configuration register settings.
3. LSB = Least Significant Bit. 1LSB = 45.7μV in the 3V input range.
4. These include the full temperature range variation, but exclude the error contribution from the reference.
5. All those parameters are tested with an input signal at -0.5dB for full-scale, unless otherwise specified. The specifications expressed in dBFS are tested with a -0.5dB signal and are recalculated to a full-scale input signal.
6. Serial 16-bit straight binary in unipolar mode. Serial 16-bit two's complement in bipolar mode.
7. After the conversion is completed, the conversion results are provided immediately.
8. All digital inputs are forced to V_{IO} or GND as required.
9. In the acquisition phase.

TIMING CHARACTERISTICS

(V_{DD} = 3.3V, V_{REF} = 3V, V_{IO} = 1.8V to V_{DD}, T_A = -40℃ to +125℃, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}				890	ns
Acquisition Time	t_{ACQ}		110			ns
Time between Conversions	t_{CYC}		1			μs
CNV Pulse Width	t_1		10			ns
Data Write/Read during Conversion	t_{DATA}				600	ns
SCLK Period (2)	t_2		t_6 + 2			ns
SCLK Low Time	t_3	V_{IO} above 3V	7			ns
		V_{IO} above 1.8V	8			
SCLK High Time	t_4	V_{IO} above 3V	7			ns
		V_{IO} above 1.8V	8			
SCLK Falling Edge to Data Remains Valid	t_5		4			ns
SCLK Falling Edge to Data Valid Delay	t_6	V_{IO} above 3V			14	ns
		V_{IO} above 2.3V			15	
		V_{IO} above 1.8V			17	
CNV Low to SDO D15 MSB Valid	t_7	V_{IO} above 3V			13	ns
		V_{IO} above 2.3V			14	
		V_{IO} above 1.8V			16	
CNV High or Last SCLK Falling Edge to SDO High Impedance	t_8				20	ns
CNV Low to SCLK Rising Edge	t_9		10			ns
Last SCLK Falling Edge to CNV Rising Edge Delay	t_{10}		55			ns
DIN Valid Setup Time from SCLK Rising Edge	t_{11}		5			ns
DIN Valid Hold Time from SCLK Rising Edge	t_{12}		5			ns

NOTES:

1. See Figure 1 and Figure 2.
2. t_2 must be greater than t_3 + t_4.
3. The C_{LOAD} of measuring digital timing is 50pF.

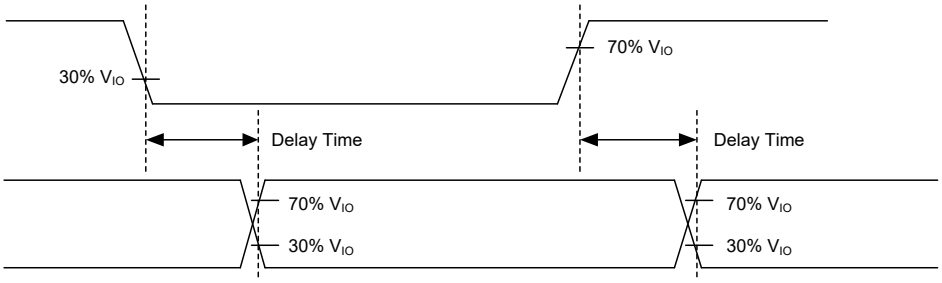
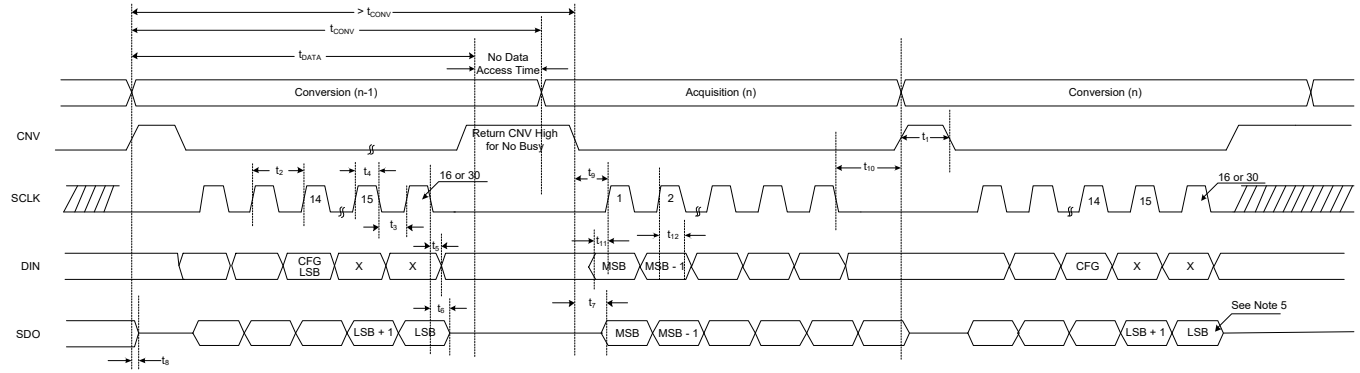


Figure 1. Voltage Levels of Timing Measurement

TIMING DIAGRAMS



NOTES:

1. No data access time is a transition time between t_{CONV} and t_{DATA}. During this time, there should not be any read or write operation.

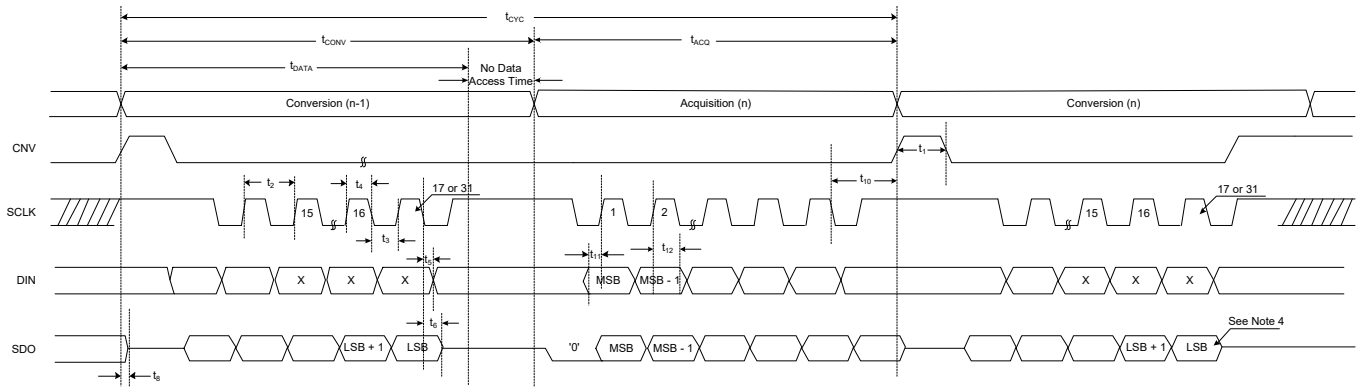
2. The CPOL (clock polarity) bit controls the steady state value of the clock when no data is being transferred.

3. Register Write Operation: The first 14-SCLK rising edges update the configuration of register (CFG). It is in MSB first format. It means that the MSB of the register (Bit[13]) is written at the first SCLK rising edge.

4. Conversion Result Read Operation: The MSB of ADC conversion result is locked out by the falling edge of CNV, and the following ADC data bit is locked out by the subsequent 15-SCLK falling edges. The 16-SCLK falling edge sets the SDO to high impedance status.

5. If CFG readback is disabled, at least 16 SCLKs are needed for the conversion code reading. If CFG readback is enabled, at least 30 SCLKs are needed for both conversion result code and configuration register reading.

Figure 2. Serial Interface Timing without a Busy Indicator (CPOL = 0)



NOTES:

1. No data access time is a transition time between t_{CONV} and t_{DATA}. During this time, there should not be any read or write operation.

2. The CPOL (clock polarity) bit controls the steady state value of the clock when no data is being transferred.

3. Register Write Operation: The first 14-SCLK rising edges update the configuration of register (CFG). It is in MSB first format. It means that the MSB of the register (Bit[13]) is written at the first SCLK rising edge.

4. Conversion Result Read Operation: The BUSY indicate bit '0' on SDO pin is shifted out automatically after the conversion is completed. The subsequent data bit is MSB of ADC conversion result which is locked out by the falling edge of SCLK. To shift out all 16-bit ADC codes, it will take total 16 falling edges of SCLK. And the 17-SCLK falling edge sets the SDO to high impedance status. If CFG readback is disabled, at least 17 SCLK falling edges are needed for the conversion code reading. If CFG readback is enabled, at least 31 SCLK falling edges are needed for both conversion result code and configuration register reading.

Figure 3. Serial Interface Timing with a Busy Indicator (CPOL = 1)

TIMING DIAGRAMS (continued)

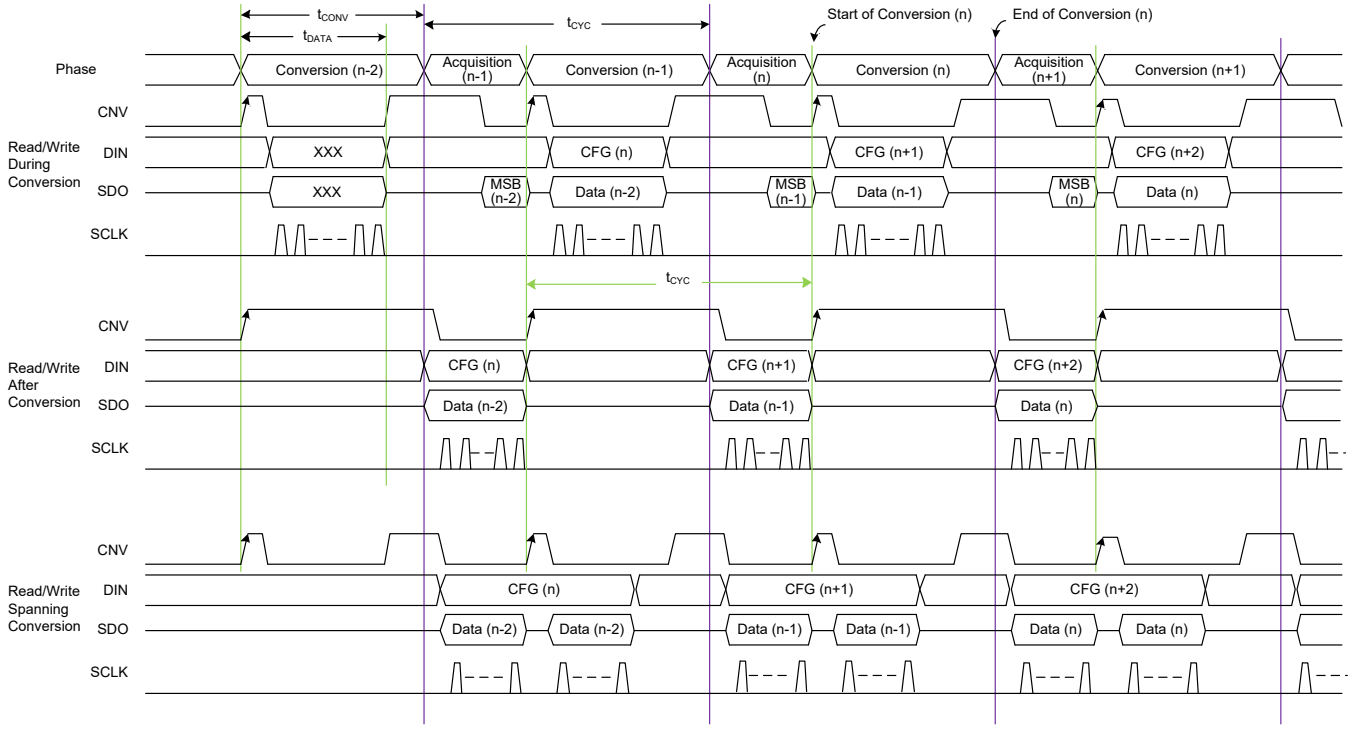


Figure 4. Reading and Writing Sequence without a Busy Indicator (CPOL = 0)

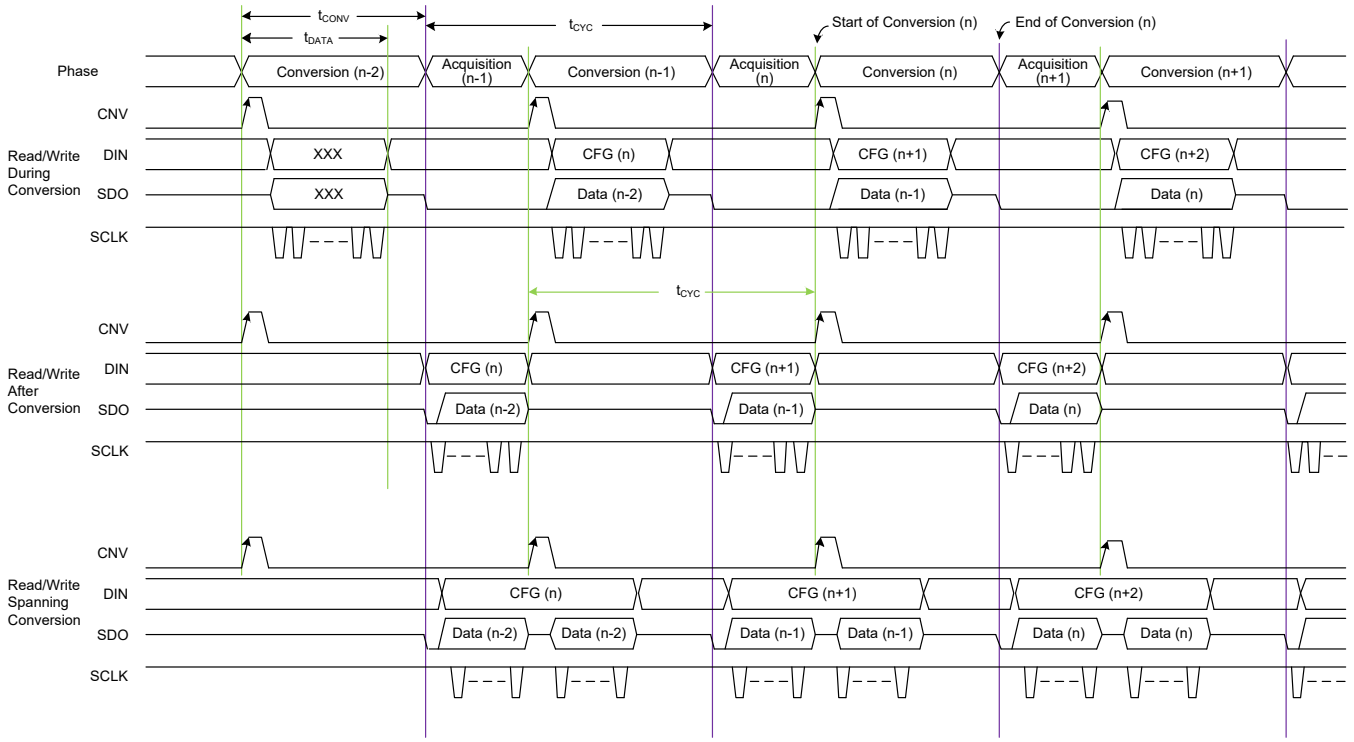


Figure 5. Reading and Writing Sequence with a Busy Indicator (CPOL = 1)

OPERATING TIMING SEQUENCE

The SGM52001-16 can be operated in 3 kinds of timing sequence modes. These modes are not configured by software or hardware. The only difference is that reading/writing time slot is put at different operation timing window.

Reading/Writing during Conversion

As shown in Figure 4 and Figure 5, if the SGM52001-16 is operated in reading (writing) during conversion (cycle #N) mode, the current reading ADC code is the conversion of previous cycle (cycle #N-1). If writing the CFG during conversion (for example, cycle #N+1), the configuration will be effective in next cycle (cycle #N+2).

The transition time is the time between the t_{CONV} and t_{DATA}. It is not recommended to do any operation during this time, because the device does update conversion result during this time. Any operation may cause data corrupted.

The time t_{DATA} is the maximum time which is available for last round conversion result reading.

It is recommended that the host controller should finish reading operation within time of t_{DATA}, in other words, the host controller should read the ADC code as soon as possible, whatever the sampling speed is adopted by the system.

A fast SPI SCLK is recommended in this mode.

If CNV keeps high at the moment of conversion finishing, the device will not output BUSY indicator signal. Otherwise, the device will output BUSY indicator signal as the first output bit on SDO pin.

Reading/Writing after Conversion

As shown in Figure 4 and Figure 5, if the SGM52001-16 is operated in reading (writing) after conversion mode (cycle #N), the reading ADC code is the conversion of last cycle (cycle #N-1). If writing the CFG after conversion (for example, cycle #N+1), the configuration will be effective in next cycle (cycle #N+2).

In this operating mode, all reading (writing) process is issued during acquisition time. As in high speed sampling mode, the minimum acquisition time $t_{ACQ(MIN)}$ is a short time slot, reading (writing) process is compressed to a short time. It is recommended that reading (writing) after conversion mode is used for low speed sampling application.

If CNV keeps high at the moment of conversion finishing, the device will not output BUSY indicator signal. Otherwise, the device will output BUSY indicator signal as the first output bit on SDO pin.

Reading/Writing Spanning Conversion

As shown in Figure 4 and Figure 5, if the SGM52001-16 is operated in reading (writing) spanning conversion mode (cycle #N), the current reading ADC code is the conversion of previous cycle (cycle #N-1). If writing the CFG in the current acquisition and conversion cycle (for example, cycle#N+1), the configuration will be effective in next acquisition and conversion cycle (cycle #N+2).

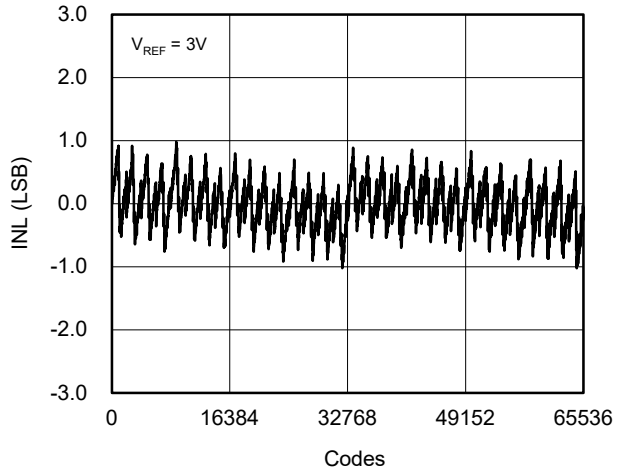
In this mode, the host controller can perform data accessing two times of operation sections to complete one ADC code reading. For these two times of operation sections, it is not necessarily to have to be combined by '8 SCLKs + 8 SCLKs', and it can be any combination, such as '4 SCLKs + 12 SCLKs' or '5 SCLKs + 11 SCLKs'.

There are restrictions for these two times of operation sections. The first operation section must be finished within the acquisition time. The second operation section must be finished within t_{DATA} to prevent data corruption, which is similar to reading/writing during conversion. Data accessing is not allowed when CNV is high. For the maximum throughput, the allocation of SCLKs needs to be carefully considered. Because $t_{ACQ(MIN)}$ is a restricted parameter, it is a better choice to send out less SCLKs in first round and more in second round to achieve maximum sampling rate.

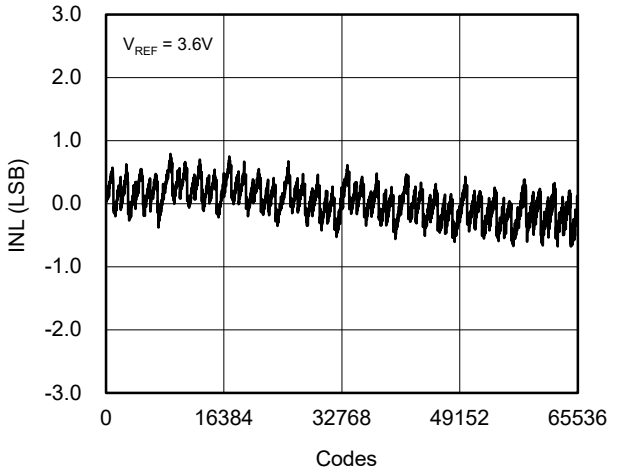
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3V, V_{REF} = 3V, V_{IO} = V_{DD}, unless otherwise noted.

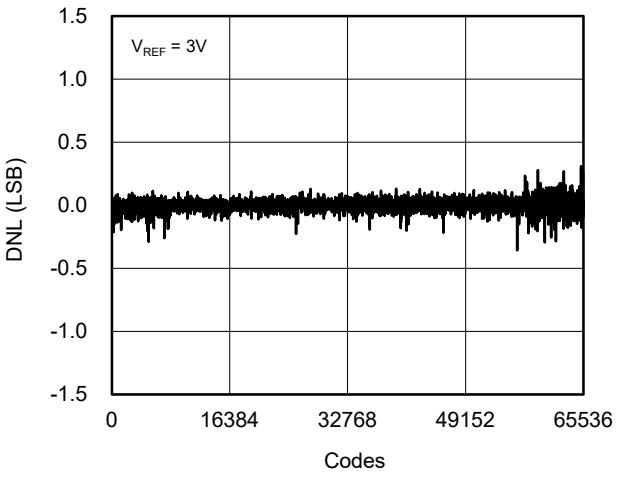
Integral Nonlinearity vs. Code



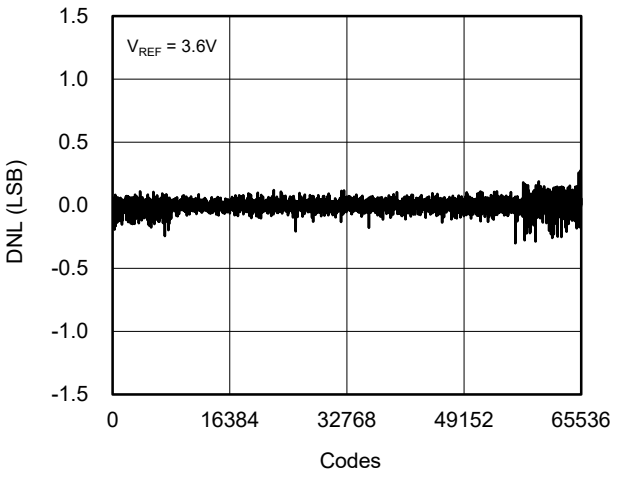
Integral Nonlinearity vs. Code



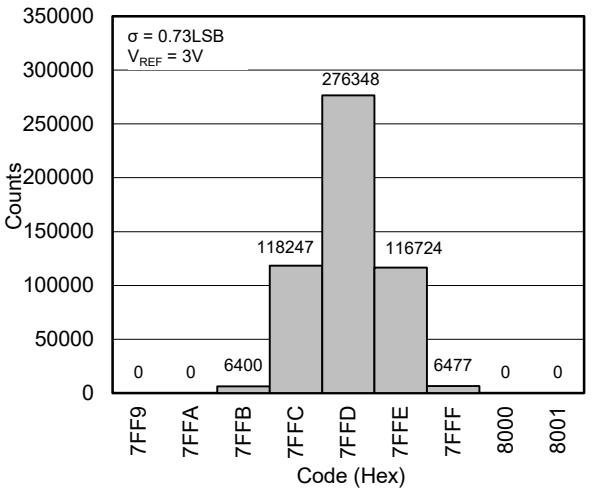
Differential Nonlinearity vs. Code



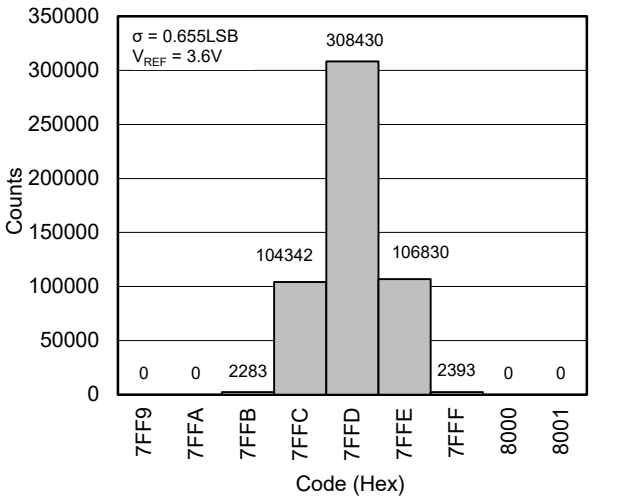
Differential Nonlinearity vs. Code



Histogram of a DC Input at Code Center



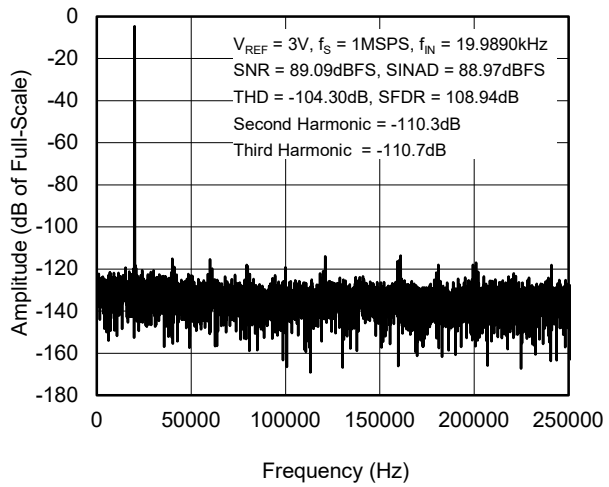
Histogram of a DC Input at Code Center



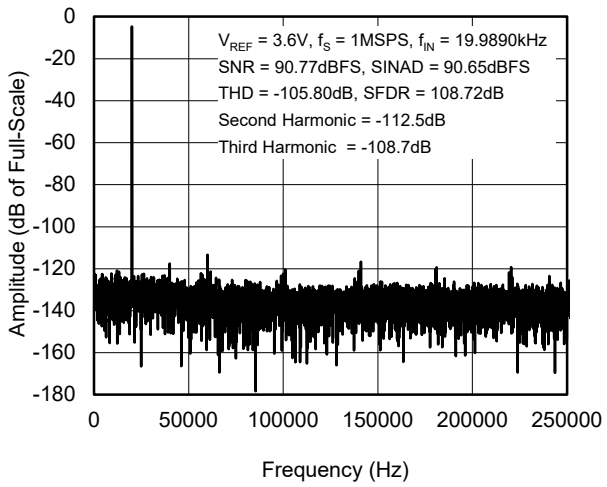
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{DD} = 3.3V, V_{REF} = 3V, V_{IO} = V_{DD}, unless otherwise noted.

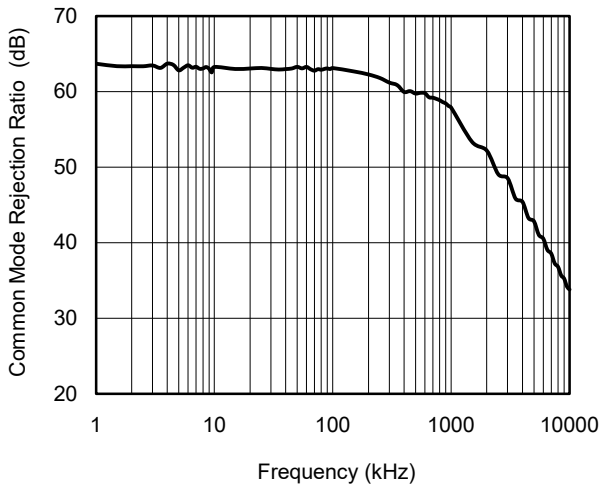
20kHz FFT



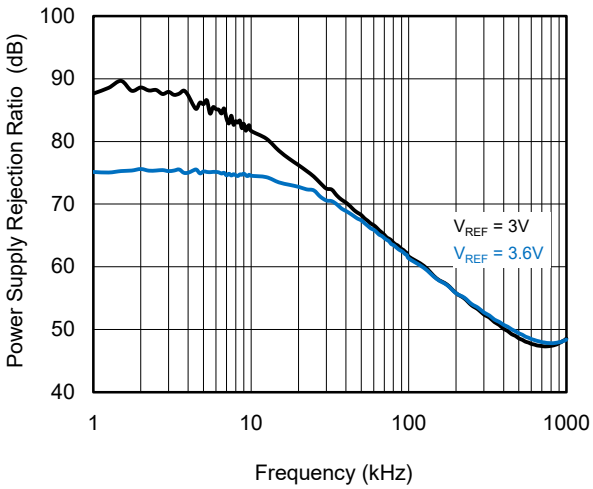
20kHz FFT



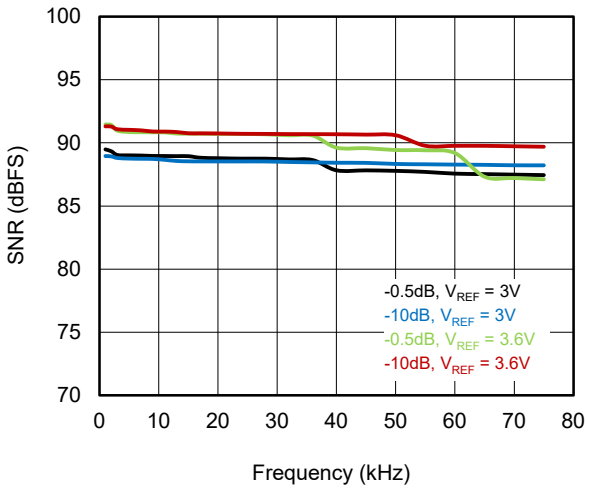
Analog Input CMRR vs. Frequency



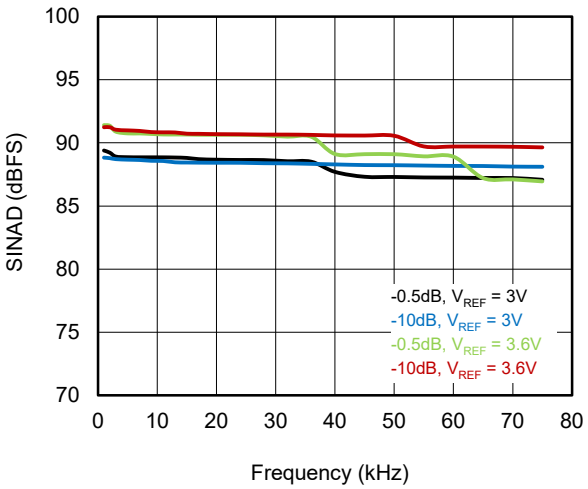
PSRR vs. Frequency



SNR vs. Frequency



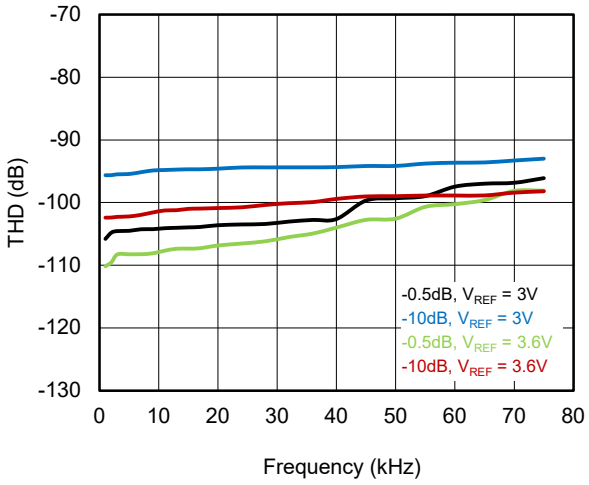
SINAD vs. Frequency



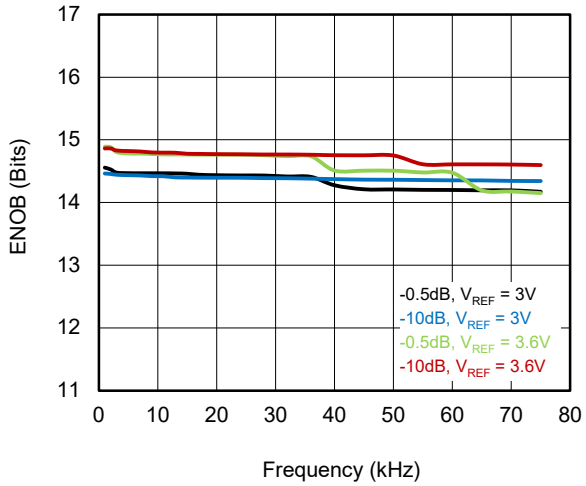
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{DD} = 3.3V, V_{REF} = 3V, V_{IO} = V_{DD}, unless otherwise noted.

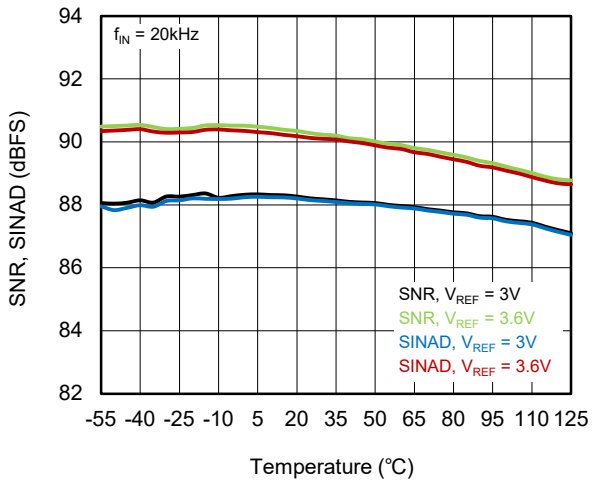
THD vs. Frequency



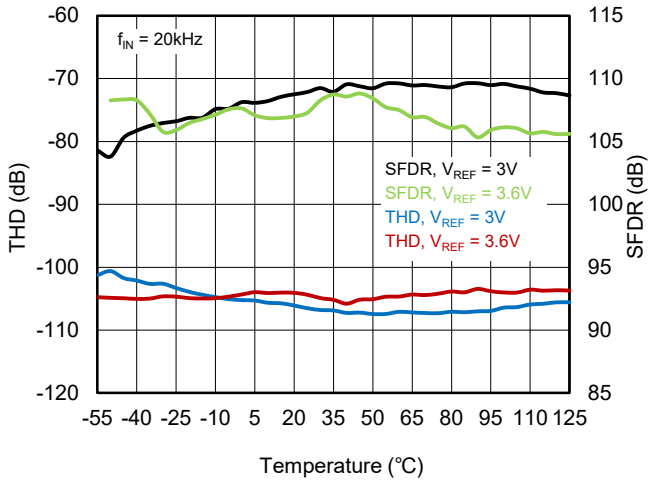
ENOB vs. Frequency



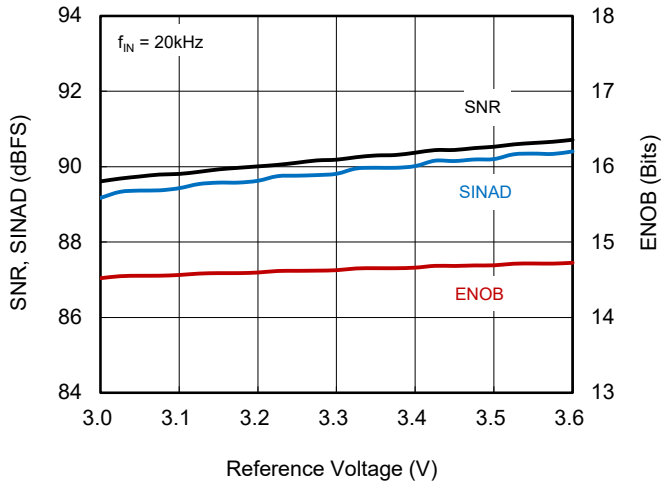
SNR, SINAD vs. Temperature



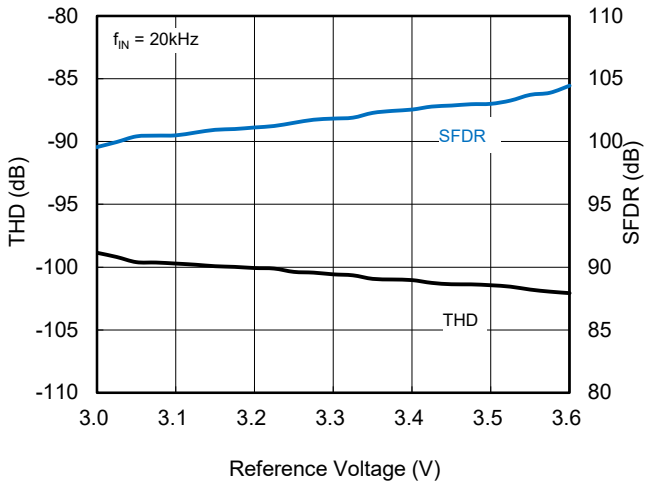
THD, SFDR vs. Temperature



SNR, SINAD, ENOB vs. Reference Voltage



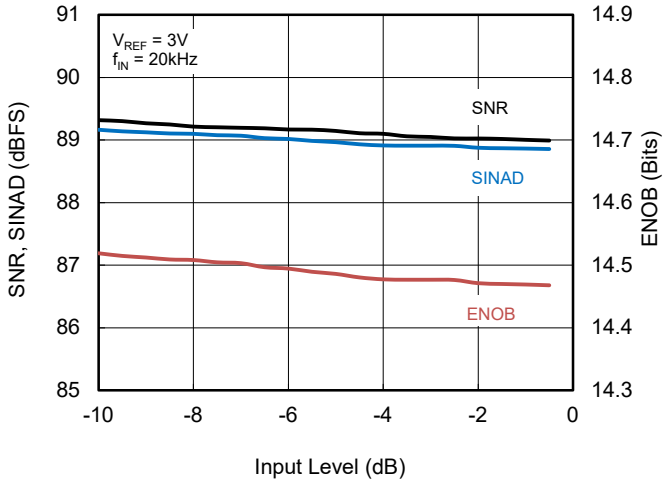
THD, SFDR vs. Reference Voltage



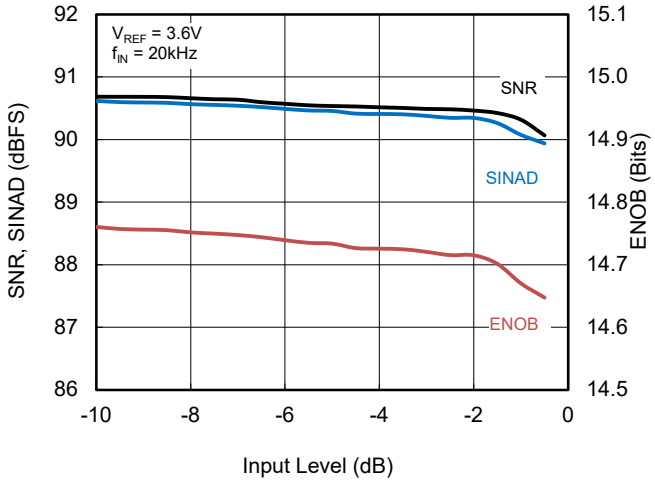
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{DD} = 3.3V, V_{REF} = 3V, V_{IO} = V_{DD}, unless otherwise noted.

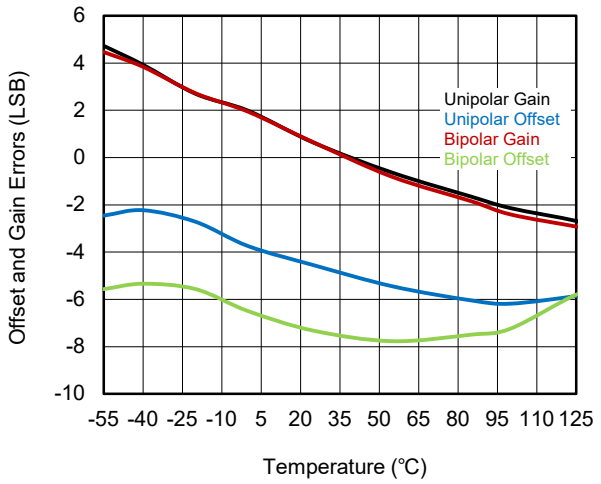
SNR, SINAD, and ENOB vs. Input Level



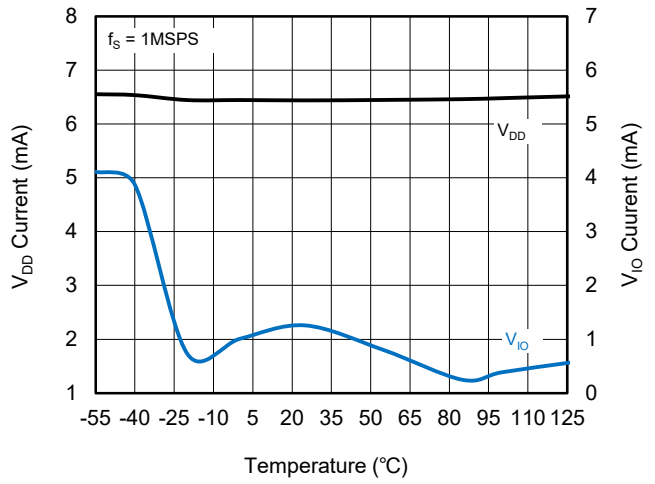
SNR, SINAD, and ENOB vs. Input Level



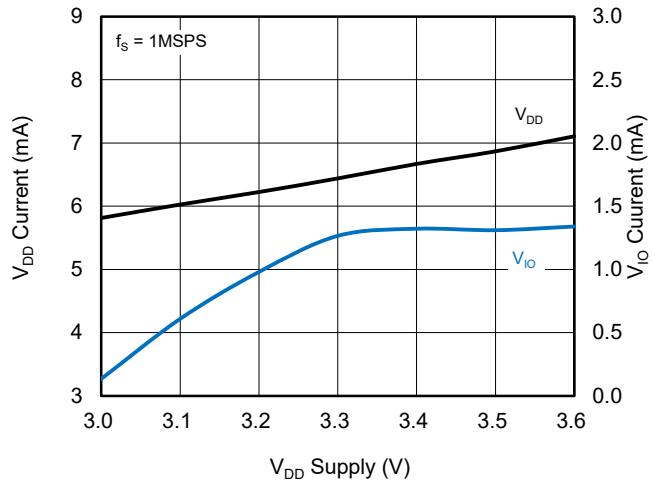
Offset and Gain Errors vs. Temperature, Not Normalized



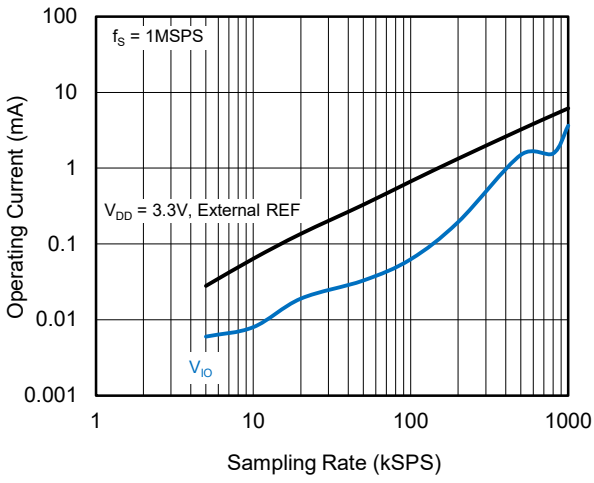
Operating Current vs. Temperature



Operating Current vs. Supply



Operating Current vs. Sampling Rate



FUNCTIONAL BLOCK DIAGRAM

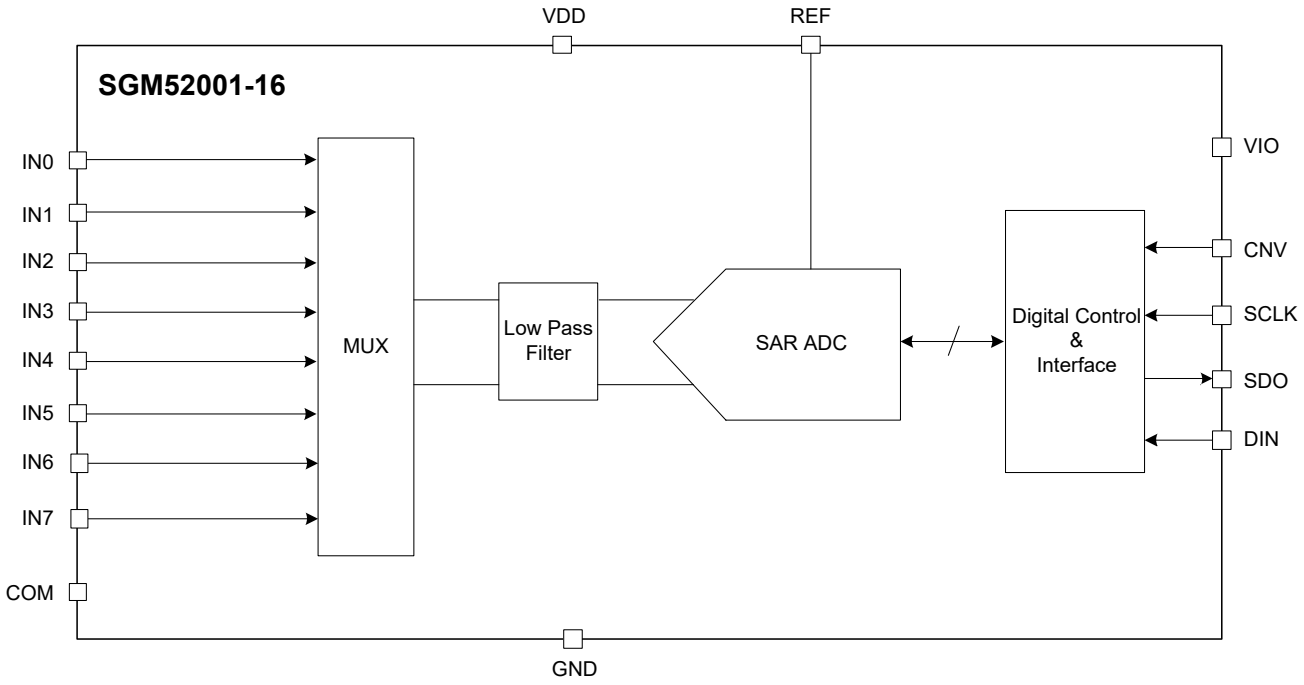


Figure 6. Block Diagram

DETAILED DESCRIPTION

The SGM52001-16 is an 8-channel 16-bit successive approximation ADC, which is based on the switched capacitor array architecture.

The SGM52001-16 has an on-chip internal oscillator which is used to the clock source of internal conversion. The SCLK is not required for the conversion process.

Transfer Functions

The SGM52001-16 supports 5 kinds of input modes, which include single-ended, pseudo differential to COM (referenced to GND or 1/2V_{REF}) and pseudo differential pairs (referenced to GND or 1/2V_{REF}). For the first mode, the inputs are configured as single-ended, all eight channels are referenced to GND, and the data output is a straight binary. For the second and third modes, the inputs are configured as pseudo differential to a common reference (COM). If the COM is connected to GND, then the data output is a straight binary, and if the COM is connected to V_{REF}/2, then the data output is two's complement. For the fourth and fifth modes, the inputs are configured as pseudo differential pairs of two adjacent channels. If the INx- is connected to GND, then the data output is a straight binary, if the INx- is connected to V_{REF}/2, then the data output is two's complement.

Figure 7 shows the ideal transfer characteristic. Table 1 and Table 2 show the correspondence between the input voltage range and the output code.

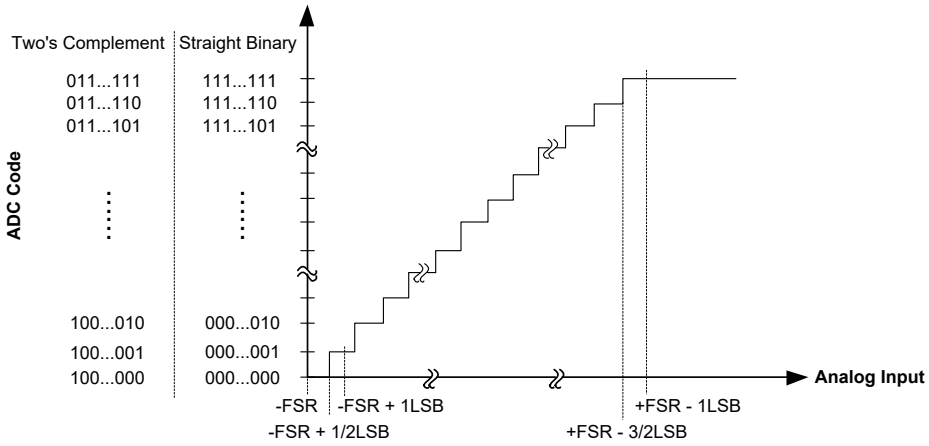


Figure 7. ADC Ideal Transfer Function

Table 1. Theoretical Input Voltages and Output Codes of Unipolar Mode

Description	Digital Output Code (Straight Binary Hex)	Analog Input of Unipolar Mode V_{REF} = 3.3V (1)
FSR - 1LSB	0xFFFF	3.299949V
Mid-scale + 1LSB	0x8001	1.650050V
Mid-scale	0x8000	1.65V
Mid-scale - 1LSB	0x7FFF	1.649949V
-FSR + 1LSB	0x0001	50.35μV
-FSR	0x0000	0V

NOTE: 1. Unipolar Mode: With COM or INx- = 0V or all INx referenced to GND.

Table 2. Theoretical Input Voltages and Output Codes of Bipolar Mode

Description	Digital Output Code (Two's Complement Hex)	Analog Input of Bipolar Mode V_{REF} = 3.3V (1)
FSR - 1LSB	0x7FFF	1.649949V
Mid-scale + 1LSB	0x0001	50.35μV
Mid-scale	0x0000	0V
Mid-scale - 1LSB	0xFFFF	-50.35μV
-FSR + 1LSB	0x8001	-1.649949V
-FSR	0x8000	-1.65V

NOTE: 1. Bipolar Mode: With COM or INx- = V_{REF}/2.

DETAILED DESCRIPTION (continued)

Input Configurations

The SGM52001-16 can be configured as single-ended input or pseudo differential input. In both modes, the positive pin input range is 0V to V_{REF}, and the negative input pin must be GND or $V_{REF}/2$. The selectable configurations are shown in the following 4 conditions:

Configuration A: CFG[12:10] = 111, all 8 channels are single-ended input and referenced to GND pin. In this case, each input channel VIN+ is channel0+ to channel7+, each input channel VIN- is GND.

Configuration B: CFG[12:10] = 010, all 8 channels are pseudo differential to COM pin, and COM pin is connected to $V_{REF}/2$. CFG[12:10] = 110, all 8 channels are pseudo differential to COM pin, and COM pin is connected to GND. In this case, each input channel channelx+ is INx+, and the COM pin is INx-.

Configuration C: CFG[12:10] = 00x, two adjacent channels of all inputs are combined as differential pairs, and the channelx- is referenced to $V_{REF}/2$. CFG[12:10] = 10X, two adjacent channels of all inputs are combined as differential pairs, and the channelx- is referenced to GND. In this case, which channel of these adjacent pairs is channelx+ or channelx- is defined by CFG[9:7]. For example, if CFG[9:7] = 000, the positive pin (channel0+) is IN0, and the negative pin (channel0-) is IN1, vice versa.

Configuration D: The chip supports dynamic combined configuration.

More details of input configuration please refer to Figure 8.

Input Structure

The input signal applied to INx and COM must be limited in the range that is listed in Electrical Characteristics table.

The SGM52001-16 is a capacitor array SAR ADC. During the sampling period, there is an input current flowing into the ADC. The peak input current depends on sampling rate, reference voltage, input voltage and signal source impedance.

A driver amplifier is usually suggested to buffer the signal source. It makes the analog input source to charge the equivalent input capacitor (44pF) to a 16-bit accuracy level in the acquisition time. When the input capacitor is fully charged, no further current flows. An equivalent input circuit is shown in Figure 9.

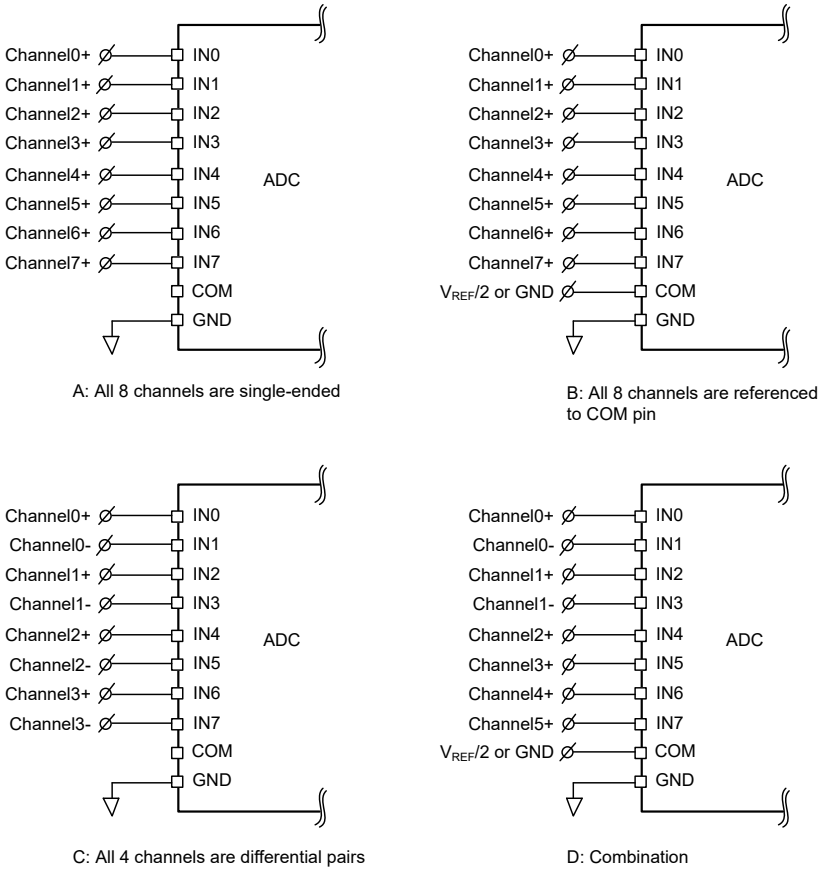
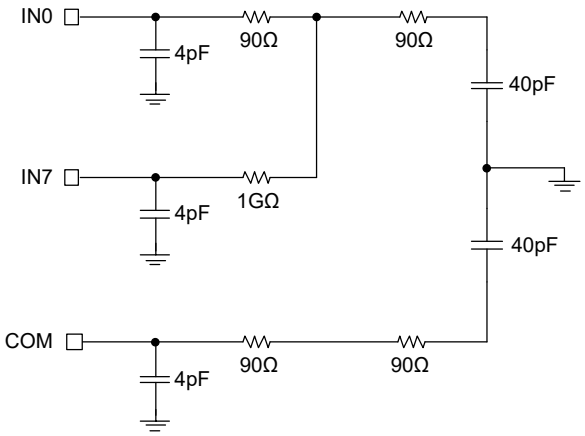


Figure 8. Multiplexed Analog Input Configurations

DETAILED DESCRIPTION (continued)



NOTE: IN0 is assumed to be on, and IN7 is assumed to be off.

Figure 9. Equivalent Analog Input Circuit

Sequencer

The SGM52001-16 supports automatic channel scanning. The channel configuration can be single-ended, pseudo differential to COM or pseudo differential paired.

In the single-ended mode and differential to COM mode, the scan sequence starts at IN0 and ends at the channel which is configured by CFG[9:7].

In the differential paired mode, the scan sequence starts at channel0+ (IN0) and channel0- (IN1), and ends at the paired channel set by CFG[9:7]. In the auto scan mode, the positive input is always the even INx and the negative input is always the odd INx, regardless of the setting of CFG[9:7].

The auto scan sequence is initiated by setting the CFG[2:1]. Once the configuration of CFG[13:0] is uploaded to ADC, the DIN must be held low at least 13 SCLK clocks before the next CFG[13:0] is written to ADC. During these clocks, the ADC data can be read normally.

During the scan sequence, the CFG[13:0] can be updated. Once the CFG[11] or CFG[9:7] is changed, the scan sequence will be restarted from IN0 (or paired with IN1 in pseudo differential mode).

When using the sequencer, the channel number corresponding to the conversion result can be achieved by reading back register configuration. Because the register configuration contains channel information and this information is updated in real time. In other words, the channel number is constantly updated and corresponds one-to-one with the new conversion result. For example, set the sequencer to sample channel Ch0 to Ch5 for one cycle. After reading the conversion result of Ch0, send another 14 SCLKs and read back the register configuration. Bit[9:7] of CFG must be 0. After reading the conversion result of Ch5, send another 14 SCLKs and read back the register configuration. Bit[9:7] of CFG must be 5.

Driver Amplifier Choice

To get the best performance, an input buffer amplifier is recommended. Refer to Figure 10 to Figure 13.

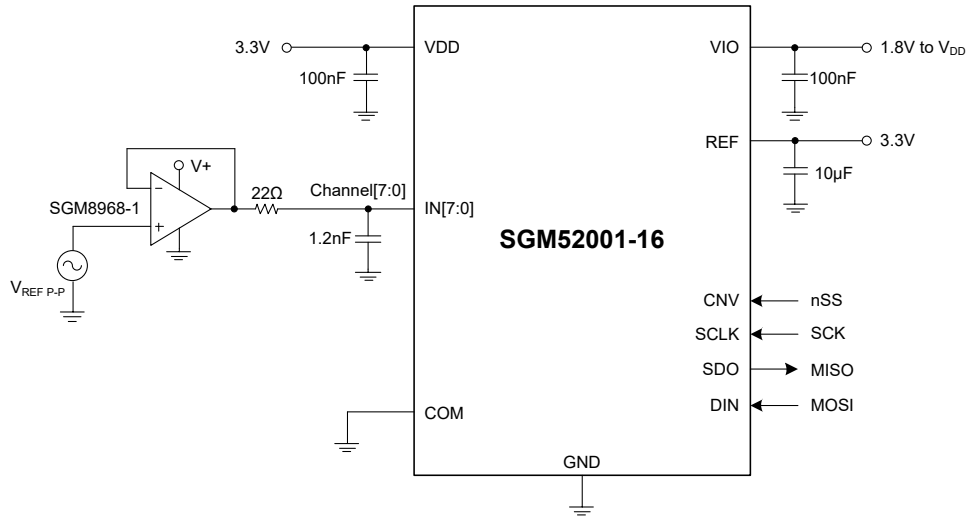


Figure 10. Typical Application with Single-Ended Input or Differential Input to a Common Reference (to GND)

DETAILED DESCRIPTION (continued)

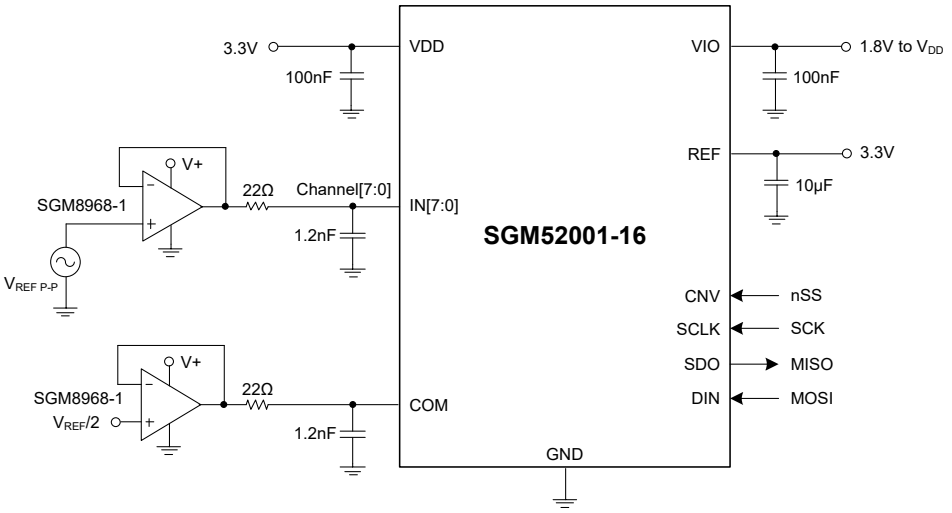


Figure 11. Typical Application with Differential Input to a Common Reference (to 1/2V_{REF})

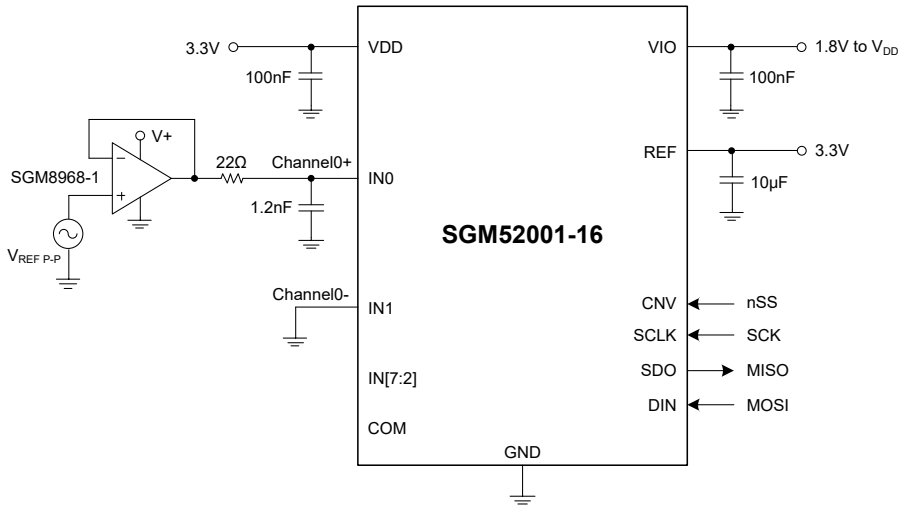


Figure 12. Typical Application with Differential Pairs Input (Reference to GND)

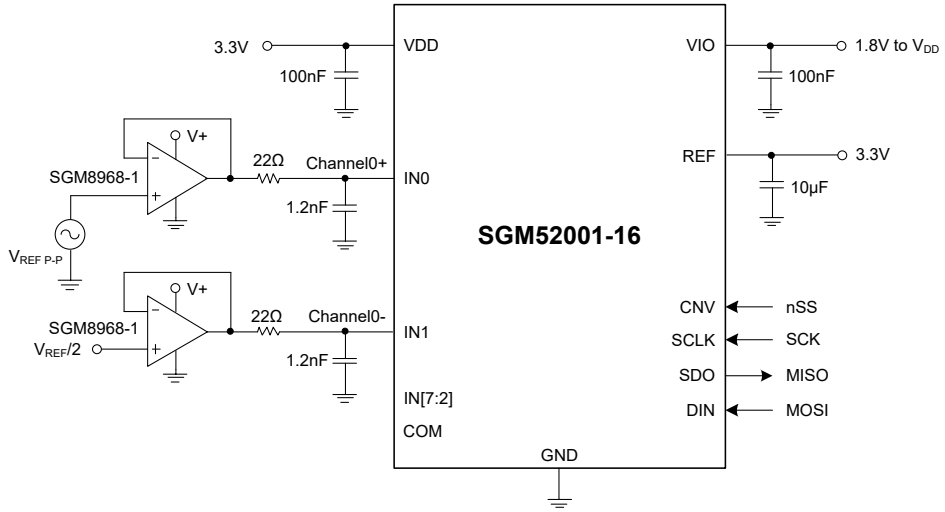


Figure 13. Typical Application with Differential Pairs Input (Reference to 1/2V_{REF})

DETAILED DESCRIPTION (continued)

Voltage Reference

The SGM52001-16 can work with external reference. More details are described in Table 3 and Table 4.

Table 3. Register Content

D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
CFG	INCC[2:0]			INx[2:0]			BW	REF[2:0]			SEQ[1:0]		RB

Table 4. Configuration Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT
D[13]	CFG	Configuration Update 0 = Keep current configuration settings 1 = Overwrite contents of register	The read back value is always 1.
D[12:10]	INCC[2:0]	Input Channel Configuration 00X (1) = Bipolar differential pairs, INx- referenced to V_{REF}/2 ± 0.1V 010 = Bipolar, INx referenced to COM = V_{REF}/2 ± 0.1V 011 = Do not use 10X (1) = Unipolar differential pairs, INx- referenced to GND ± 0.1V 110 = Unipolar, IN0 to IN7 referenced to COM = GND ± 0.1V (GND sense) 111 = Unipolar, IN0 to IN7 referenced to GND	Selection of pseudo bipolar, pseudo differential, pairs, or single-ended. Refer to the Input Configurations section.
D[9:7]	INx[2:0]	Input Channel Selection in Binary Fashion 000 = IN0 001 = IN1 010 = IN2 011 = IN3 100 = IN4 101 = IN5 110 = IN6 111 = IN7	
D[6]	BW	Select Bandwidth for Low-Pass Filter 0 = ¼ of BW, uses an additional series resistor to further bandwidth limit the noise, which can improve SNR and decrease THD slightly. Maximum throughput must also be reduced to ¼ 1 = Full BW	Suggestion: If there are no special requirements, it is recommended to configure BW = 1.
D[5:3]	REF[2:0]	Reference Selection 000 = Do not use 001 = Do not use 010 = Do not use 011 = Do not use 100 = Do not use 101 = Do not use 110 = Use external reference 111 = Do not use	
D[2:1]	SEQ[1:0]	Channel Sequencer 00 = Disable sequencer 01 = Update configuration during sequence 10 = Do not use 11 = Scan IN0 to IN[7:0] (set in CFG[9:7])	Allow scanning channels in an IN0 to IN[7:0] fashion. Refer to the Sequencer section.
D[0]	RB	Read Back the CFG Register 0 = Read back current configuration at end of data 1 = Do not read back contents of configuration	

NOTE:

1. X = Don't care.

REVISION HISTORY

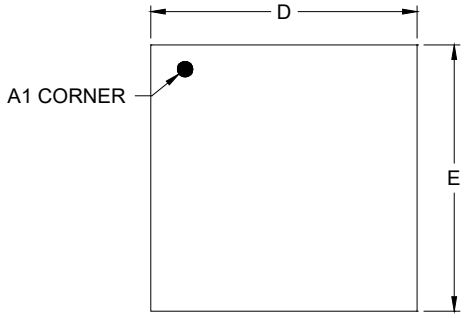
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (OCTOBER 2025) **Page**

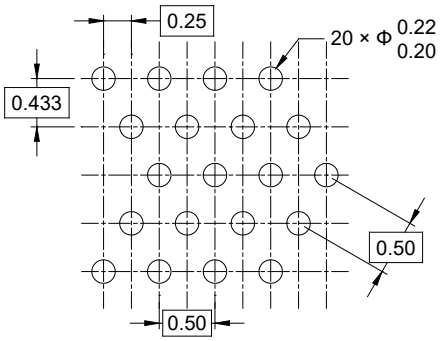
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

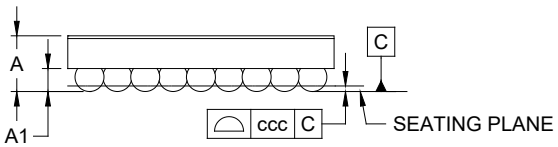
WLCSP-2.39×2.39-20B



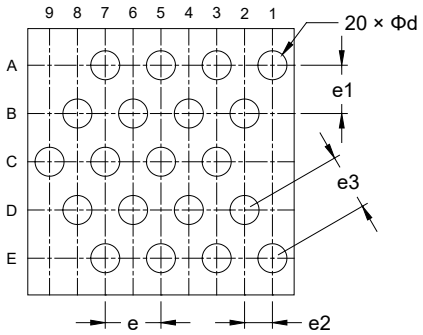
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



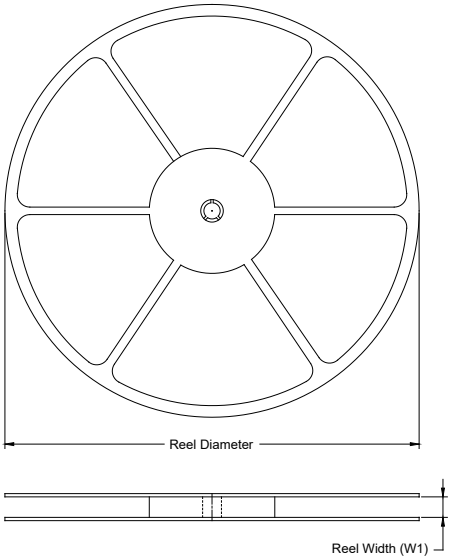
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.538
A1	0.186	-	0.226
D	2.360	-	2.420
E	2.360	-	2.420
d	0.230	-	0.290
e	0.500 BSC		
e1	0.433 BSC		
e2	0.250 BSC		
e3	0.500 BSC		
ccc	0.050		

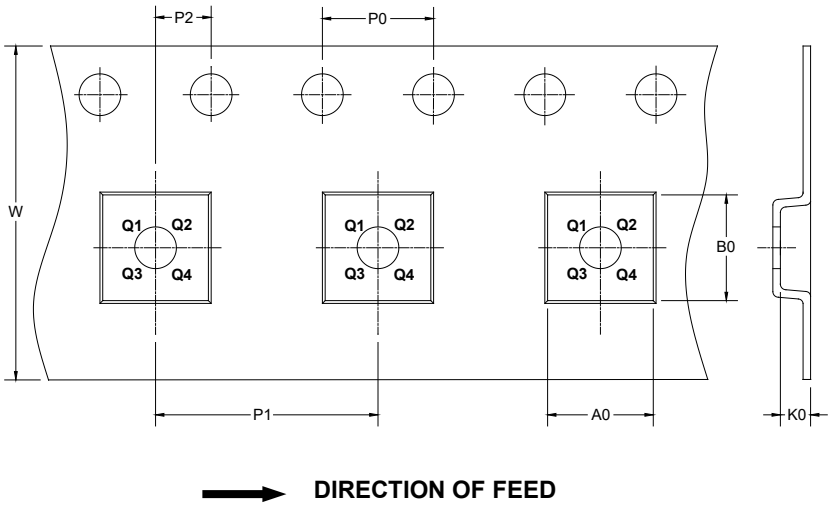
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

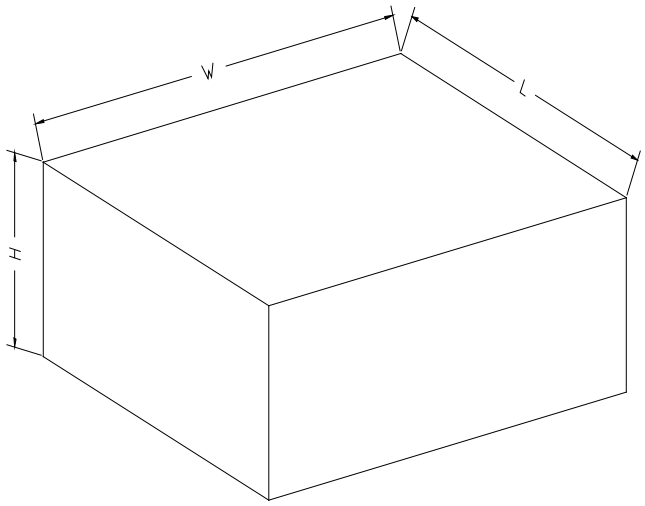
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.39×2.39-20B	7″	9.5	2.52	2.52	0.75	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002