SGM837

High-side or Low-side Measurement Bi-Directional Current and Power Monitor with I²C Compatible Interface

GENERAL DESCRIPTION

The SGM837 is a 16-bit ultra-precision I²C and SMBus compatible interface current, voltage, power monitor with alert function. It operates in a wide common-mode voltage range from 0V to 36V and a single 2.7V to 5.5V power supply.

The device has three operating modes: continuous, triggered and power-down modes that can reduce quiescent current. Programmable averaging and conversion times allow for more flexibly to fit the timing requirements in a variety of applications. It also integrates alert functions with configured priority.

Considering the low input bias current feature, the device is capable of applying a larger sensing resistor, so as to ensure the accuracy of current detection within micro-amp range.

The SGM837 is available in a Green MSOP-10 package. It is specified over the operating temperature range of -40℃ to +125℃.

FEATURES

- **2.7V to 5.5V Supply Voltage Range**
- **0V to 36V Senses Bus Voltages**
- **High-side or Low-side Sensing**
- **Current, Voltage and Power Monitor**
- **Low Gain Error: 0.25% (MAX)**
- **Low Input Offset Voltage: 20μV (MAX)**
- **Programmable Averaging and Conversion Times**
- **16 Programmable Addresses**
- **Available in a Green MSOP-10 Package**

APPLICATIONS

Communication Equipment
Servers
Battery Chargers
Power Management
Test Equipment
Power Supplies
Notebook Computers

TYPICAL APPLICATION

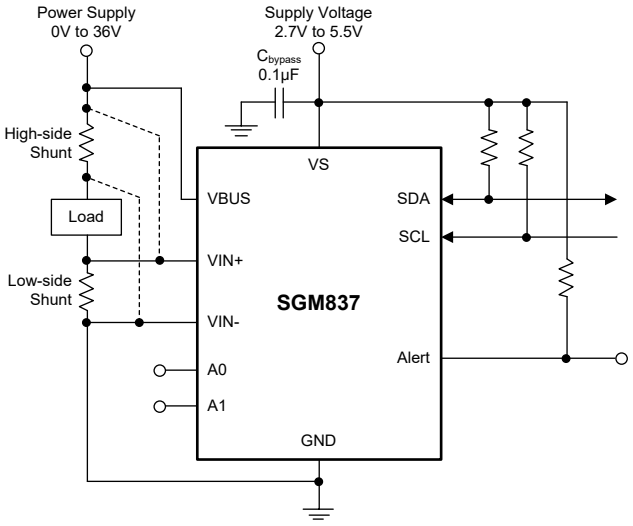


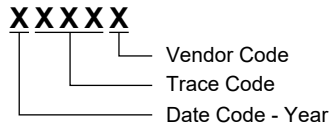
Figure 1. High-side/Low-side Sensing Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM837	MSOP-10	-40℃ to +125℃	SGM837XMS10G/TR	SGM837 XMS10 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{VS} 6V
Analog Inputs, IN+, IN-
Differential (V_{IN+} - V_{IN-}) (1) ..... -26V to 26V
Common-Mode (V_{IN+} + V_{IN-})/2 ..... -0.3V to 40V
V_{VBUS} ..... -0.3V to 40V
V_{SDA} ..... GND - 0.3V to 6V
V_{SCL} ..... GND - 0.3V to V_{VS} + 0.3V
Input Current into Any Pin, I_{IN} 5mA
Open-Drain Digital Output Current, I_{OUT} 10mA
Package Thermal Resistance
MSOP-10, θ_{JA} ..... 128.6℃/W
MSOP-10, θ_{JB} ..... 80.7℃/W
MSOP-10, θ_{JC} ..... 42.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (2) (3)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. There may exist a differential voltage from -26V to 26V of IN+ and IN-. And the voltages of these pins should be in the range of -0.3V to 40V.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Common-Mode Input Voltage, V_{CM} 12V
Operating Supply Voltage, V_{VS} 3.3V

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

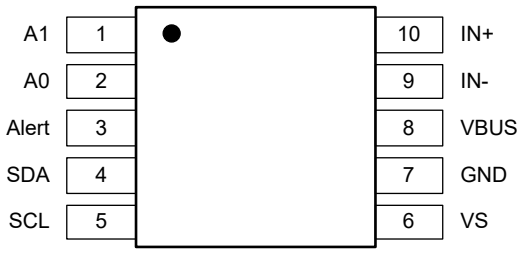
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



MSOP-10

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	A1	DI	Address Pin. Four options: GND, SCL, SDA, or VS with corresponding addresses.
2	A0	DI	Address Pin. Four options: GND, SCL, SDA, or VS with corresponding addresses.
3	Alert	DO	Multi-Functional Alert Pin.
4	SDA	DI/DO	Data Input/Output Pin.
5	SCL	DI	Clock Input Pin.
6	VS	A	Power Supply Pin.
7	GND	A	Ground.
8	VBUS	AI	Bus Voltage Input.
9	IN-	AI	Load-Side Connection Pin.
10	IN+	AI	Power-Side Connection Pin.

NOTE: A: analog, AI: analog input, DI: digital input, DO: digital output, DI/DO: digital input/digital output.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_{VS} = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} - V_{IN-}) = 0mV and V_{VBUS} = 12V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input						
Shunt Voltage Input Range	V_{SHUNT}		-81.92		81.9175	mV
Bus Voltage Input Range (1)	V_{BUS}		0		36	V
Common-Mode Rejection	CMRR	0V ≤ V_{IN+} ≤ 36V	120	145		dB
Shunt Offset Voltage, RTI (2)	V_{OS}			±2.5	±20	μV
		vs. temperature, T_A = -40℃ to +125℃		0.1	0.3	μV/℃
	PSRR	vs. power supply, V_{VS} = 2.7V to 5.5V, V_{IN+} = 1V		3		μV/V
Bus Offset Voltage, RTI (2)	V_{OS}			±1.25	±10	mV
		vs. temperature, T_A = -40℃ to +125℃		20	80	μV/℃
	PSRR	vs. power supply, V_{VS} = 2.7V to 5.5V, V_{IN+} = 1V		0.3		mV/V
Input Bias Current (IN+, IN- Pins)	I_B			0.01		μA
VBUS Input Impedance				850		kΩ
Input Leakage (3)		(IN+ pin) + (IN- pin), power-down mode		0.005	0.2	μA
DC Accuracy						
ADC Native Resolution				16		Bits
1 LSB Step Size		Shunt voltage		2.5		μV
		Bus voltage		1.25		mV
Shunt Voltage Gain Error				±0.03	±0.25	%
		vs. temperature, T_A = -40℃ to +125℃		10	50	ppm/℃
Bus Voltage Gain Error				±0.03	±0.25	%
		vs. temperature, T_A = -40℃ to +125℃		10	50	ppm/℃
ADC Conversion Time	t_{CT}	CT bit = 000		160	180	μs
		CT bit = 001		220	250	
		CT bit = 010		350	390	
		CT bit = 011		550	600	
		CT bit = 100		1.10	1.30	ms
		CT bit = 101		2.10	2.40	
		CT bit = 110		4.10	4.70	
		CT bit = 111		8.30	9.10	
SMBus						
SMBus Timeout (4)				28	35	ms

NOTES:

1. The 36V input voltage corresponds to the full range of the ADC scaling of 40.96V. Do not exceed 36V.

2. RTI = Referred-to-Input.

3. The leakage current that defined as the current flowing into the pin in this table is positive. And in the other input conditions, the negative leakage current may occur.

4. Once SCL keeps low for more than 28ms, the SMBus timeout of SGM837 will reset.

ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25℃, V_{VS} = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} - V_{IN-}) = 0mV and V_{VBUS} = 12V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input/Output						
Input Capacitance				6		pF
Leakage Input Current		0V ≤ V_{IN} ≤ V_{VS}		0.05	0.2	μA
High-Level Input Voltage	V_{IH}		0.7 × V_{VS}			V
Low-Level Input Voltage	V_{IL}				0.3 × V_{VS}	V
Low-Level Output Voltage, SDA, Alert	V_{OL}	I_{OL} = 3mA		0.2	0.4	V
Hysteresis				500		mV
Power Supply						
Quiescent Current	I_Q			1000	1500	μA
		Power-down (shutdown) mode		0.95	2.0	μA
Power-On Reset Threshold	V_{POR}			2.2		V

TIMING REQUIREMENTS

PARAMETER	SYMBOL	FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL Operating Frequency	f_{SCL}	0.001	0.4	0.001	3.4	MHz
Bus Free Time between STOP and START Condition	t_{BUF}	1300		160		ns
Hold Time after Repeated START Condition (After this period, the first clock is generated.)	t_{HDSTA}	600		160		ns
Repeated START Condition Setup Time	t_{SUSTA}	600		160		ns
STOP Condition Setup Time	t_{SUSTO}	600		160		ns
Data Hold Time	t_{HDDAT}	0	900	20	100	ns
Data Setup Time	t_{SUDAT}	100		20		ns
SCL Clock Low Period	t_{LOW}	1300		160		ns
SCL Clock High Period	t_{HIGH}	600		60		ns
Data Fall Time	t_F		300		80	ns
Clock Fall Time	t_F		300		40	ns
Clock Rise Time	t_R		300		40	ns
Data Rise Time	t_R		300		40	ns
Clock/Data Rise Time for SCL ≤ 100kHz	t_R		1000			ns

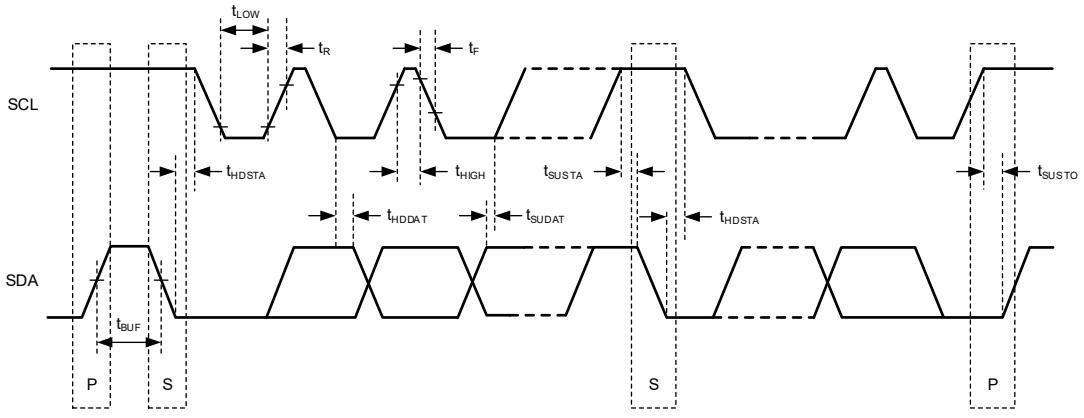
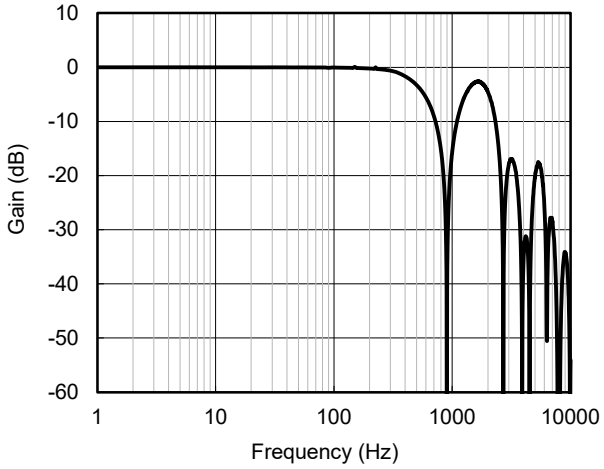


Figure 2. Bus Timing Diagram

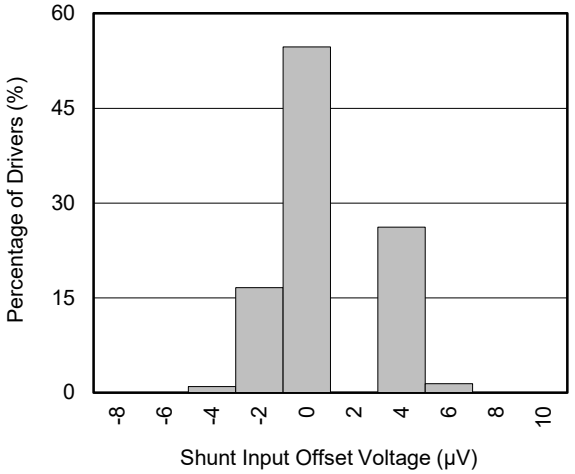
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{VS} = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} - V_{IN-}) = 0mV and V_{VBUS} = 12V, unless otherwise noted.

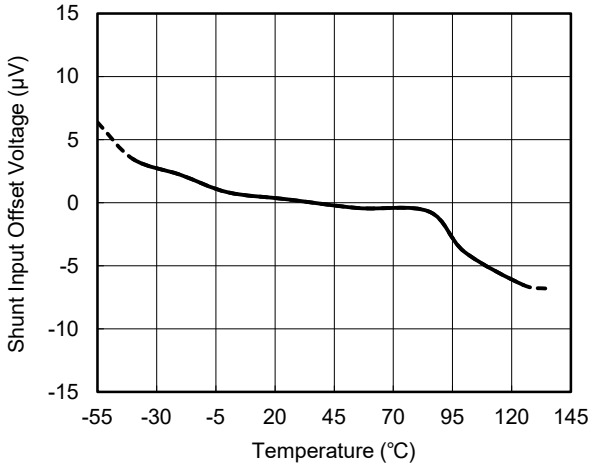
Frequency Response (Shunt Only)



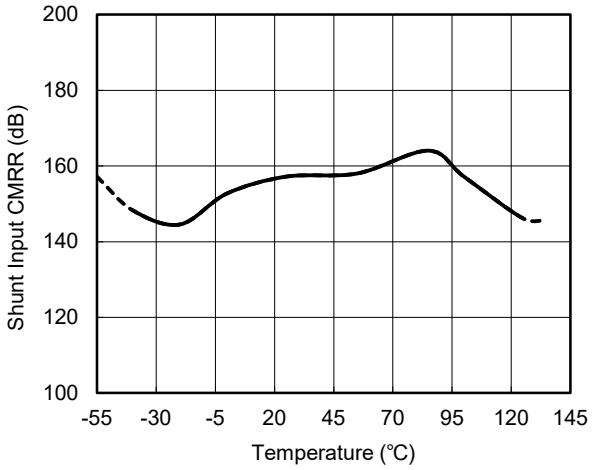
Shunt Input Offset Voltage Production Distribution



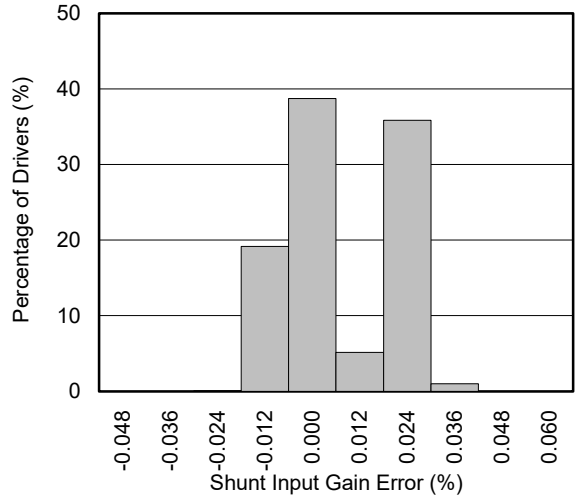
Shunt Input Offset Voltage vs. Temperature



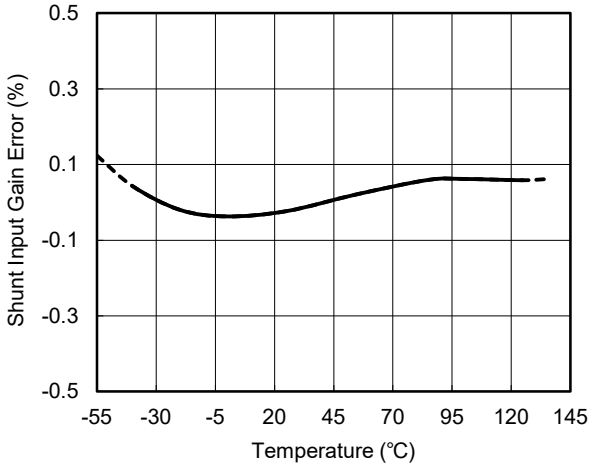
Shunt Input Common-Mode Rejection Ratio vs. Temperature



Shunt Input Gain Error Production Distribution



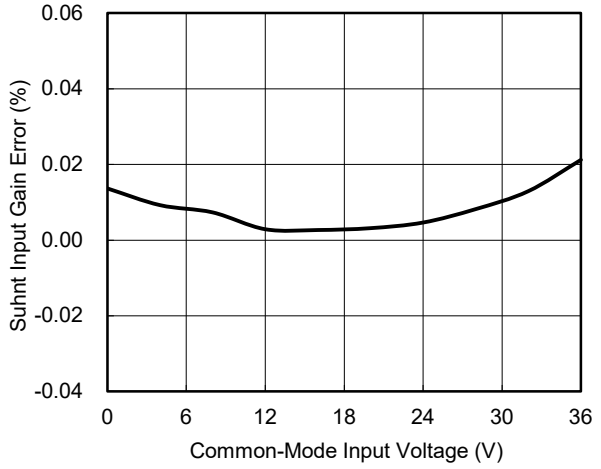
Shunt Input Gain Error vs. Temperature



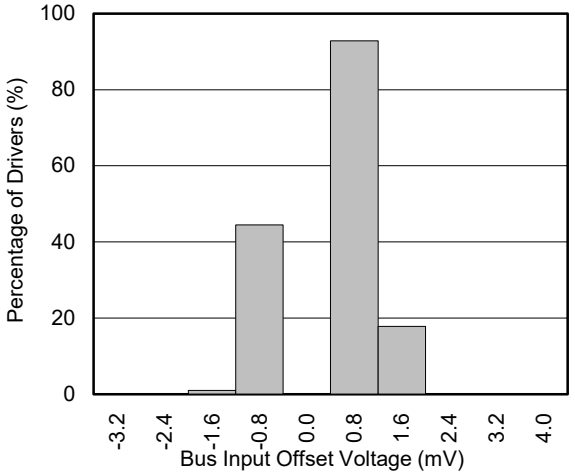
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{VS} = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} - V_{IN-}) = 0mV and V_{VBUS} = 12V, unless otherwise noted.

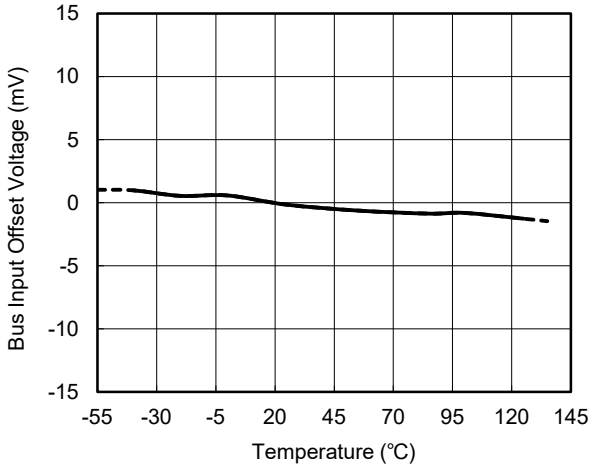
Shunt Input Gain Error vs. Common-Mode Input Voltage



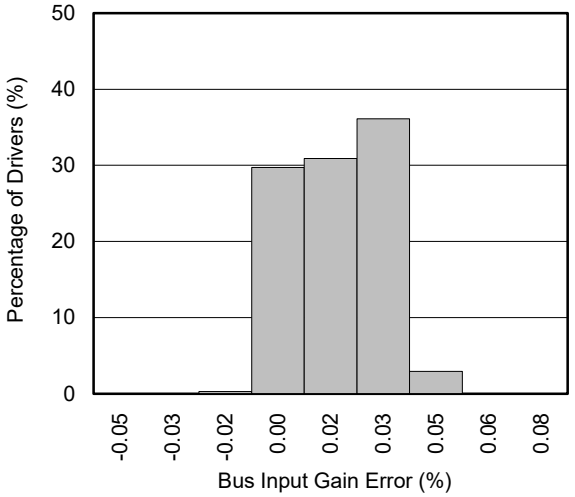
Bus Input Offset Voltage Production Distribution



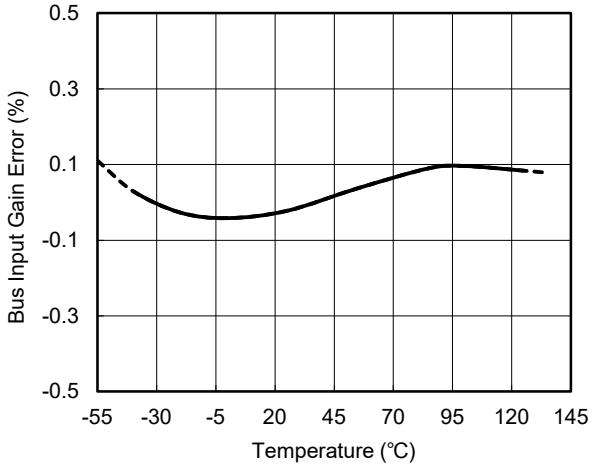
Bus Input Offset Voltage vs. Temperature



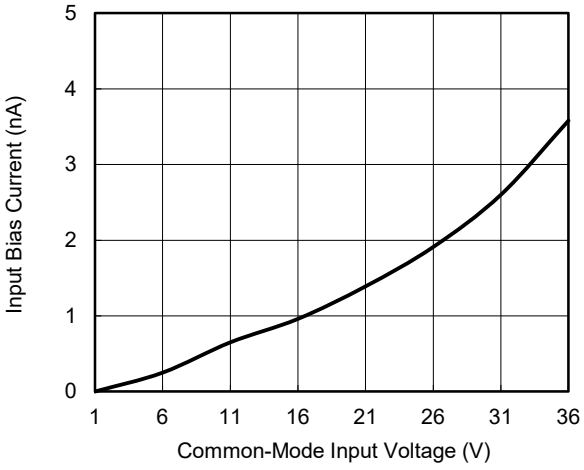
Bus Input Gain Error Production Distribution



Bus Input Gain Error vs. Temperature



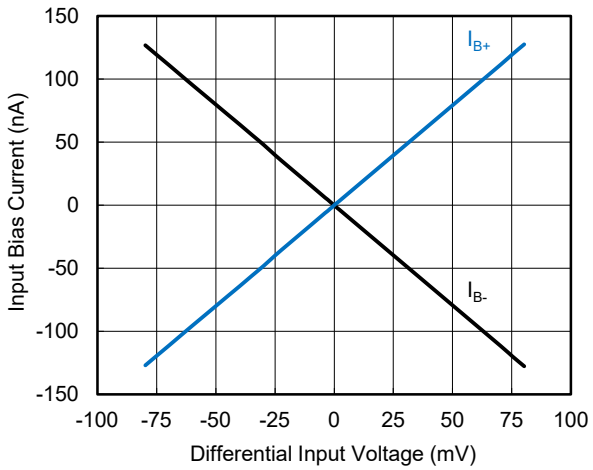
Input Bias Current vs. Common-Mode Voltage



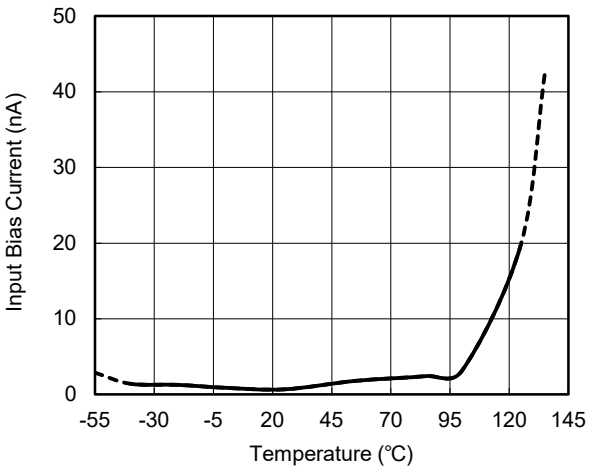
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{VS} = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} - V_{IN-}) = 0mV and V_{VBUS} = 12V, unless otherwise noted.

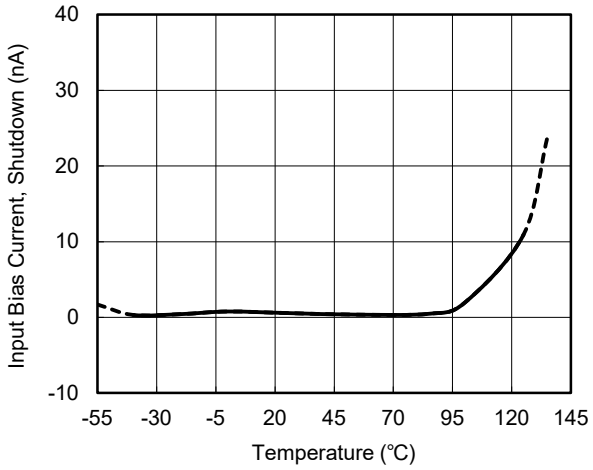
Input Bias Current vs. Differential Input Voltage



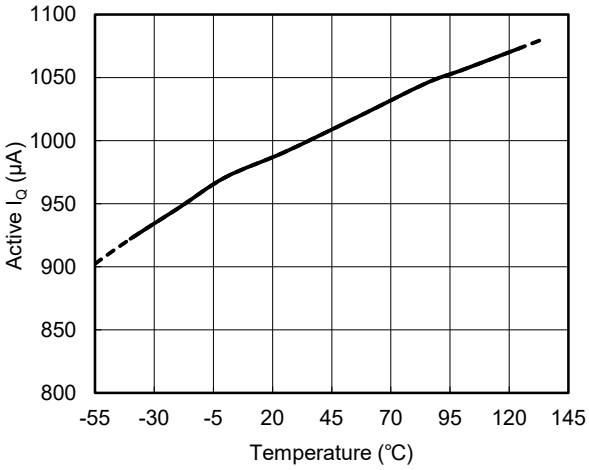
Input Bias Current vs. Temperature



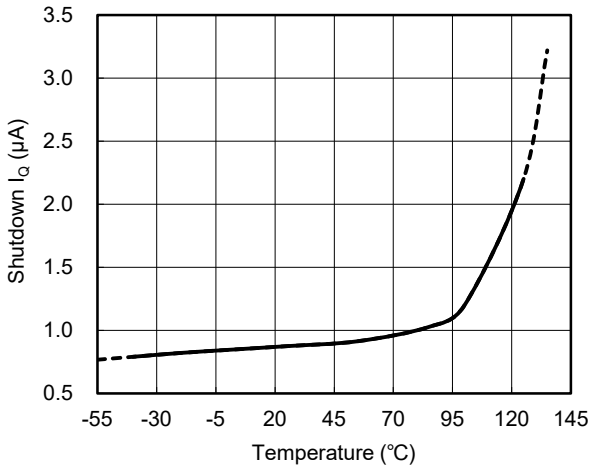
Input Bias Current vs. Temperature, Shutdown



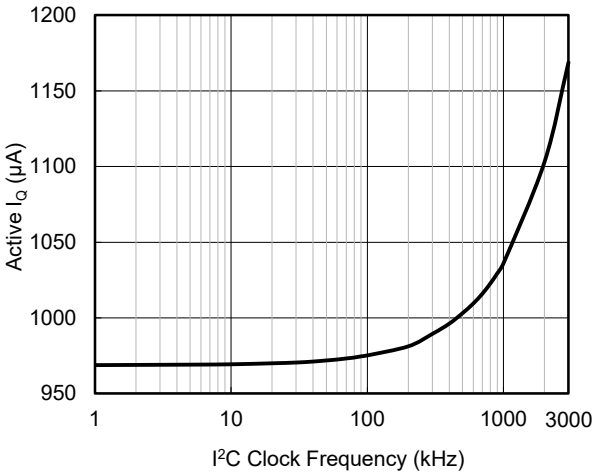
Active I_Q vs. Temperature



Shutdown I_Q vs. Temperature

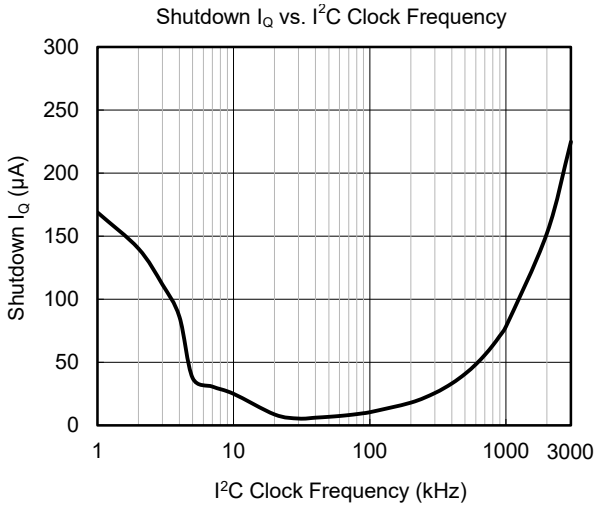


Active I_Q vs. I^2C Clock Frequency



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{VS} = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} - V_{IN-}) = 0mV and V_{VBUS} = 12V, unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

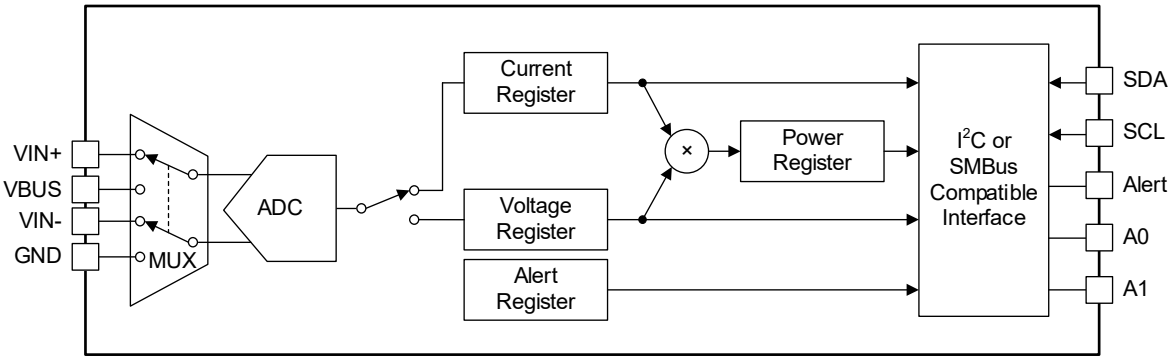


Figure 3. Functional Block Diagram

DETAILED DESCRIPTION

Overview

The SGM837 is a 16-bit ultra-precision I²C and SMBus compatible interface current, voltage, power monitor. The device senses both shunt and bus voltages, and provides digital voltages, current and power readings in the data registers. In addition, it provides programmable registers to flexibly configure the device such as operating modes, conversion time, averaging times and alert functions.

Basic ADC Functions

The SGM837 measures two voltages at the input terminals, namely the voltage between the IN+ and IN- pins, and the voltage between VBUS and GND pins. In typical applications, a current sense resistor (shunt resistor) is connected to the IN+ and IN- pins. When load current flows through the resistor, the shunt voltage developed is measured. The bus voltage with respect to the ground is measured by connecting to the VBUS pin.

The power supply voltage of the device ranges from 2.7V to 5.5V. The voltage monitored on the VBUS pin (typically the bus voltage) ranges from 0V to 36V. The fixed LSB of the bus voltage measurement is 1.25mV, and therefore the full-scale range of SGM837 is 40.96V. Please note that the voltage applied on the VBUS pin should not exceed 36V.

Since the power supply of the device is independent of the input voltage, the power-up sequence does not need special attention. Therefore, the bus and shunt voltages can be applied on the input pins when the device is power-off.

The SGM837 measures two voltages, shunt voltage and bus voltage. The measured shunt voltage is converted to current according to the value programmed into the Calibration Register (05h). Then, the power is calculated based on the calculated current and the measured bus voltage.

Continuous mode and triggered mode are two operating modes of the device. For the continuous mode (default, set MODE[2:0] bits of the Configuration Register (00h) to '111'), the device continuously measures and converts the shunt voltage followed by the bus voltage. The current can be calculated after shunt voltage conversion. Then, the calculated current value along with the converted bus voltage value are used to calculate the power. See Programming the Calibration Register section for more detailes. The values of shunt voltage, bus voltage, current and power are subsequently stored in an internal accumulator, and then repeat the above steps until the repeat times reach the average value set in the Configuration Register. Following each sequence, the measured and calculated values are added to the previously accumulated values. When the number of sequence reaches the averages, the average calculations are performed on all the accumulated values, and the final average value of shunt voltage, bus voltage, current and power are updated in the corresponding data registers which can be read. These values in the data registers remain readable until the next fully conversion cycle is completed. The ongoing conversion is not affected by the data registers reading.

Besides converting both the shunt voltage and bus voltage, the device can also be configured to convert only the shunt voltage or the bus voltage by setting the mode control bits in the Configuration Register. This design provides more application flexibility to the users.

Please note that all the current and power calculations are performed in the background and they do not take up the conversion time.

For the triggered mode, the device is triggered to perform a single-shot measurement/conversion by writing any of the triggered control modes to the Configuration Register (set the MODE[2:0] bits to '001', '010' or '011'). This action controls the device to perform a single measurement/conversion. Therefore, to trigger another single conversion, the Configuration Register must be written again, even though the operation mode does not change.

Besides the continuous and triggered modes, the power-down mode of the device can decrease the quiescent current and block current into the inputs. In this mode, the registers of the device can still be written and read. Until one of the active modes is written into the Configuration Register, the device stays in power-down mode.

DETAILED DESCRIPTION (Continued)

The device provides a conversion ready flag bit (Mask/Enable Register, CVRF bit) to help coordinate one-shot or trigger conversions. The CVRF bit is set after all the conversions, multiplication and averaging are completed.

The CVRF bit clears under the conditions of writing to the Configuration Register (the MODE[2:0] bits is not in power-down mode), and reading the Mask/Enable Register (06h).

Power Calculation

Following each shunt voltage and bus voltage measurement, the current and power are calculated, as shown in Figure 4. Following a shunt voltage measurement, the current is calculated according to the value set in the Calibration Register. If no value is written to the Calibration Register, the current value in the output register (Current Register, 04h) is '0'. Following a bus voltage measurement, the power is calculated based on the measured bus voltage and the calculated current value. Also, if no value is written to the Calibration Resister, the power value in the register (Power Register, 03h) is '0'. The current and power values are regarded as intermediate results (unless the average time is set to '1'), and are stored in an accumulator rather than the output data registers. Following each conversion sequence, the calculated current and power values are added to the previously accumulated values until the number of sequence reaches the average times. After that, the accumulated values are averaged, and the final current and power values are updated in the corresponding registers.

Similar to the current and power values, the shunt and bus voltage values are also collected and accumulated following each measurement sequence. After the number of sequence reaches the averages, the accumulated values are averaged and the final shunt and bus voltage values are updated in the corresponding registers.

Low Bias Current

The SGM837 has a very low input bias current, which is beneficial for reducing power loss of the device in both active and shutdown states. Another advantage brought by low input bias current is that filters can be used to the front end of the digital current sensing amplifier, where the filters can filter out high-frequency noise and minimize the accuracy reduction. Besides, the low input bias current makes the device capable of applying a larger sensing resistor, so as to ensure the accuracy of current detection within sub-mA range. When the sensed current is zero, the input bias current of SGM837 is the smallest. When the detection current increases and the differential voltage drop on the sense resistor becomes larger, the input bias current will gradually increase.

Alert Pin

The SGM837 provides an Alert pin to respond to one of the five available alert functions or to a conversion ready event. They are shunt voltage over-limit (SOL), shunt voltage under-limit (SUL), bus voltage over-limit (BOL), bus voltage under-limit (BUL) and power over-limit (POL). The alert functions and the conversion ready event can be enabled through the Mask/Enable Register. The device provides an Alert Limit Register (07h) to set limit value for comparison. By writing a value into the Alert Limit Register and enable the alert function through the Mask/Enable Register, the Alert pin is asserted when the alert event occurs.

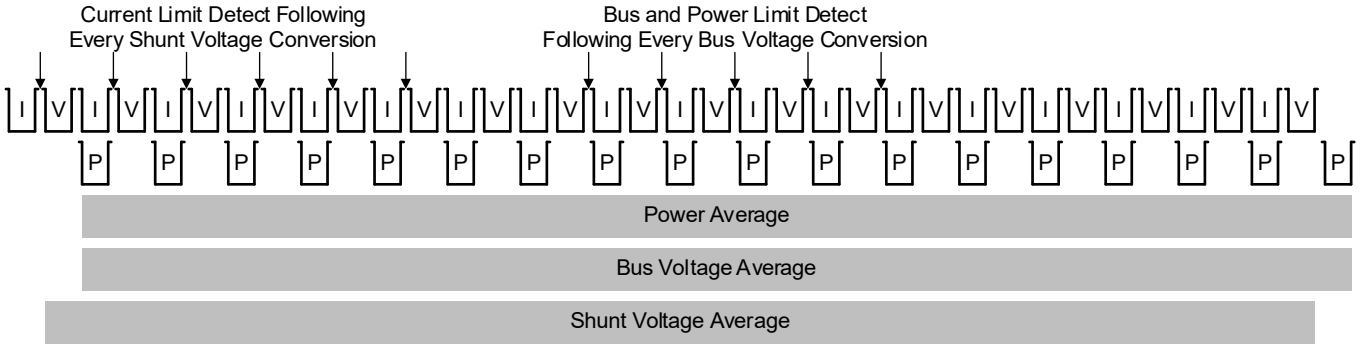


Figure 4. Power Calculation Scheme

DETAILED DESCRIPTION (Continued)

The Alert pin is an open-drain structure. It will be asserted if the alert function selected in the Mask/Enable Register is above the alert limit value set in the Alert Limit Register.

Correspondingly, the alert function flag (AFF bit, 4-bit) in the Mask/Enable Register is set when the selected alert event occurs. Among the five available alert functions, only one can be enabled. If multiple alert function bits in the Mask/Enable Register are selected, only the alert function with the highest significant bit will be successfully enabled and monitored. For example, if both the shunt voltage over-limit (SOL bit, 15-bit) and the shunt voltage under-limit (SUL bit, 14-bit) functions are selected, only the shunt voltage over-limit function will be successfully enabled, and the Alert pin is asserted when the value in the Shunt Voltage Register exceeds the value in the Alert Limit Register.

The Alert pin can also be configured to monitor the conversion ready state through setting the CNVR bit (10-bit) of the Mask/Enable Register. The Alert pin is asserted when the device has finished the previous conversions and the conversion ready flag (CVRF bit, 3-bit) is set. If both the conversion ready and an alert function are enabled, the Mask/Enable Register must be read to determine if the selected alert event occurs. Since the CVRF bit is set when the conversion ready event occurs, and the alert function flag (AFF bit, 4-bit) is set when the selected alert event occurs, by reading the CVRF and AFF bits in the Mask/Enable Register, the alert event can be determined. If the conversion ready is not desired to be monitored at the Alert pin, by clearing the CNVR bit, the Alert pin would respond to the selected alert function.

Leave the Alert pin floating if not use it to monitor the conversion ready state or any alert function.

Figure 4 shows the relative timing of the conversion and alert detection. Take the SOL function as an example, following each shunt voltage conversion, the shunt voltage value is compared with the limit value programmed into the Alert Limit Register to determine whether the selected alert event occurs. The AFF bit of the Mask/Enable Register is asserted (set to high) when the converted value exceeds the limit value. When the AFF bit is asserted, the Alert pin is asserted and its polarity is decided by the alert polarity bit (APOL bit, 1-bit) of the Mask/Enable Register. If the Alert pin is latched by asserting the alert latch enable bit (LEN bit, 0-bit), the AFF bit along with the Alert pin remain asserted until reading the Mask/Enable Register.

The BOL converted bus voltage value with the limit value following each bus voltage conversion and asserts the AFF bit and Alert pin once the converted value exceeds the limit value.

The POL alert function compares the calculated power value with the limit value following each bus voltage conversion and asserts the AFF bit and Alert pin once the converted value exceeds the limit value.

Device Functional Modes

Averaging and Conversion Times Considerations

The averaging and conversion times are programmed by the Configuration Register. Eight levels of conversion time from 160μs to 8.30ms are available. The programmable conversion and average times allow the device to match different time requirements in real applications. For example, if a system requires reading the shunt voltage and bus voltage every 10ms, the conversion time for shunt and bus voltage measurement can be set to 1.10ms, with the average time set to 4. With this configuration, the shunt and voltage values are updated approximately every 8.8ms. Also, the conversion time for shunt and voltage measurement can be different, which allows the device to focus on one of the two voltages. Suppose the system desires more conversion time for shunt voltage, a 8.30ms conversion time can be set for shunt voltage, with 1.10ms of conversion time for bus voltage and single conversion (average time set to ‘1’). With this configuration, the shunt and bus voltage values are updated approximately every 9.40ms.

There are trade-offs between the conversion and average times used. The averaging can filter the input signal, thus effectively improving the measurement accuracy. With more average times, the device would reduce the noise of the input signal more effectively.

DETAILED DESCRIPTION (Continued)

Similarly, the conversion time also affects the measurement accuracy. A longer conversion time results in better measurement accuracy. Therefore, to achieve the highest measurement accuracy, use the longest conversion time with the most average times, provided that the time requirements of the system are met.

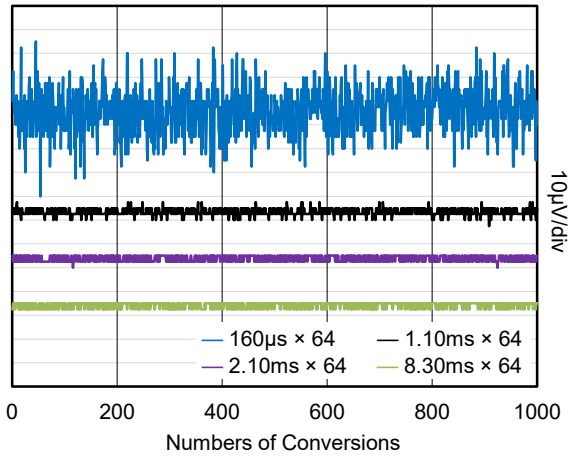


Figure 5. Noise vs. Conversion Time

Filtering and Input Considerations

In real applications, the current measurement usually introduces undesirable noise. The SGM837 provides different noise filtering capabilities by configuring the conversion and average times independently in the Configuration Register. The conversion time for shunt and bus voltage can be set independently, while the average times are the same.

The ADC of SGM837 is a sigma-delta (Σ-Δ) structure with typical sampling rates of 500kHz and 1MHz. The delta-sigma structure has good noise suppression capability. However, if there are transients at or near the sampling frequency (greater than 1.06MHz), it will affect the measurement accuracy which needs to be handled. By placing low-value resistors in series with a ceramic capacitor at the IN+ and IN- pins, this high frequency signals can be effectively filtered. Figure 6 shows the filter setup, where the recommended resistor value is less than 100Ω and the recommended capacitor value is between 0.1μF and 1μF. Both resistor values should be consistent to avoid offset due to I_{BIAS}.

Besides the transients, the input overload conditions should also be well addressed. The inputs of the device can tolerate 40V voltage. During a load short-circuit, the load current flows the shunt resistor increases sharply. When the short-circuit fault is removed, the parasitic inductance in the power loop could induce kickback voltages on the inputs which may exceed the voltage ratings. Such kickback voltages can be well suppressed using zener-type devices.

In some applications, an over-stress condition may occur as a result of an excessive dV/dt caused by event such as input hard short. The over-stress occurs due to the activation of the internal ESD protection with large available currents. The test results show that adding the 100Ω resistors at the inputs can sufficiently protect the devices from dV/dt induced fault event.

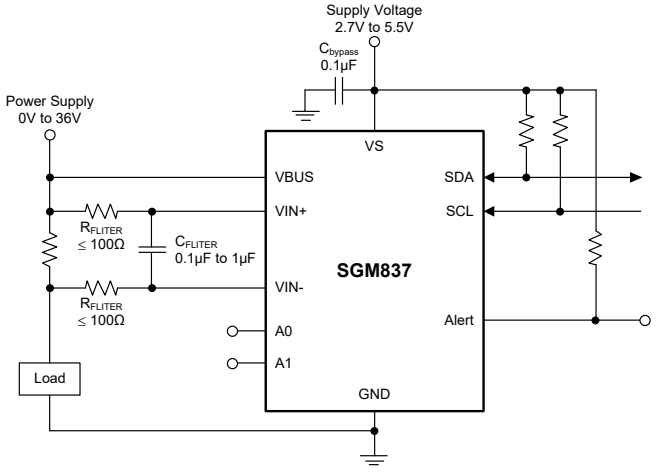


Figure 6. Input Filtering

PROGRAMMING

The SGM837 does not need to measure current and power directly, it realizes the calculation of current and power by measuring the differential voltage between IN+ and IN- pins and the voltage on VBUS pin. To obtain the correct current and power values, users need to program the resolution of the Current Register (Current_LSB) and the value of the sampling resistor applied between the IN+ and IN- pins. The resolution of the Power Register is set to be 25 times the programmed Current_LSB internally. The Calibration Register is used to calculate the corresponding current and power through the values of measured shunt and bus voltages. The determination of the Calibration Register value requires the value of Current_LSB and the sampling resistor.

As shown in Equation 1, the value of Calibration Register is determined by Current_LSB and the sampling resistor (R_{SHUNT}). Users can convert the value in Current Register to the actual current value in amperes through Current_LSB. According to Equation 2, the minimum Current_LSB can be obtained to realize the highest resolution of the Current Register, which needs to determine an estimated maximum current first. In order to simplify the calculation process of converting the Current Register and Power Register into the corresponding amperes and watts, the smallest Current_LSB is generally rounded up to an integer.

$$CAL = \frac{0.00512}{Current\_LSB \times R_{SHUNT}} \quad (1)$$

And 0.00512 is an internal fixed value to guarantee calibration accuracy.

$$Current\_LSB = \frac{Maximum\ Expected\ Current}{2^{15}} \quad (2)$$

After setting the value of Calibration Register, the Current Register and Power Register will be calculated and updated according to the measured shunt and bus voltages. Before the Calibration Register is programmed, both registers stay at 0.

Programming the Calibration Register

As shown in Figure 11, a nominal 10A load will result in a 20mV differential voltage across the 2mΩ shunt resistor. The VBUS pin of the SGM837 is used to measure the bus voltage, while in this example, it measures the voltage on the load by connecting to the IN- pin. And due to the 20mV drop across R_{SHUNT}, the voltage on the IN- and the VBUS pin is 11.98V.

For this example, assuming that the maximum expected current is 15A, the value of the Current_LSB can be calculated according to Equation 2 to be 457.8μA/bit. In order to simplify the calculation process of converting the Current Register and the Power Register into the corresponding amperes and watts, choose the value of Current_LSB as 500μA/bit or 1mA/bit. A value of 1mA/bit is chosen as Current_LSB, which is a trade-off between resolution and ease of conversion process for the user. After the above parameters are selected, the value of Calibration Register can be calculated according to Equation 1 to be 2560, or A00h.

The value in the Current Register is then obtained by multiplying the decimal value in the Calibration Register by the decimal value in the Shunt Voltage Register (01h), and then dividing by 2048, as shown in Equation 3. In this example, 8000 is obtained from the Shunt Voltage Register, which means the shunt voltage is 20mV, and the decimal value in the Current Register is 10000 or 2710h through Equation 3. Multiply this value by 1mA/bit to get a load current of 10A through R_{SHUNT}.

$$Current = \frac{Shunt\ Voltage \times Calibration\ Register}{2048} \quad (3)$$

The LSB of the Bus Voltage Register (02h) is fixed at 1.25mV/bit, so 11.98V at the VBUS pin has a value of 9584 or 2570h in the register. Since the VBUS cannot measure negative voltages, the MSB of the Bus Voltage Register is always 0.

PROGRAMMING (continued)

Multiply the decimal value of the Current Register, 10000 and the decimal value of the Bus Voltage Register, 9584 together, and then divide by 20000 to calculate the decimal value of the Power Register using Equation 4.

$$\text{Power} = \frac{\text{Current} \times \text{Bus Voltage}}{20000} \quad (4)$$

For this example, the Power Register calculates to 4792, or 12B8h. Multiply this value by the power LSB to yield a power of 119.8W. As mentioned earlier, there is a ratio of 25 between the LSB of the power and the Current_LSB, which ensures that the calculated power is within an acceptable range. By manually calculating the power of the load, the bus voltage of 11.98V is multiplied by the load current of 10A, and the result is 119.8W.

The MSB of the Power Register is always 0, even if the current is negative, and the final calculated power is also positive.

Table 1 shows the steps to configure registers, measure shunt and bus voltages, and calculate current and power for this device under the conditions of load = 10A, V_{CM} = 12V, R_{SHUNT} = 2mΩ and V_{VBUS} = 11.98V.

Programming the Power Measurement Engine

Calibration Register and Scaling

The Calibration Register allows the user to set the range of the Current Register and Power Register within the most appropriate range for a specific application scenario. For example, set the value of the Calibration Register so that the value in the Current Register and Power Register is as close as possible to the full-scale point under the maximum current or power condition, so as to improve the current and power resolution. After Calibration Register is configured, the Current Register and Power Register will generate corresponding values. Users can calculate the actual current and power values equivalently by multiplying these values of registers by the corresponding LSB. In addition, in order to avoid other errors in the system, system-level calibration can be realized through an external ammeter and SGM837. The specific principle is shown in Equation 5. The value inside the Calibration Register is adjusted by the current value measured by the external ammeter and the measured value of SGM837.

$$\text{Corrected\_Full\_Scale\_Cal} = \text{trunc}\left(\frac{\text{Cal} \times \text{Meas Shunt Current}}{\text{SGM837\_Current}}\right) \quad (5)$$

Simple Current Shunt Detection Application (No Programming Necessary)

If the device only needs to read the shunt and bus voltage under the POR default configuration, where the conversion of shunt and bus voltages is continuous, the chip does not need other redundant programming. Without programming the Calibration Register of the device, the device will not provide current and power values (both remain at 0).

Default Settings

The default values of the registers after power-on are shown in the Register Maps section. These registers are volatile, so if the values in the registers are programmed to non-default values, the registers will need to be reprogrammed each time power is cycled. Specific information for programming the calibration register is given in the programming section, and the calculation process is based on Equation 1.

Table 1. Calculating Current and Power

Step	Register Name	Address	Contents	Dec.	LSB	Value
1	Configuration Register	00h	476Fh	—	—	—
2	Shunt Register	01h	1F40h	8000	2.5μV	20mV
3	Bus Voltage Register	02h	2570h	9584	1.25mV	11.98V
4	Calibration Register	05h	A00h	2560	—	—
5	Current Register	04h	2710	10000	1mA	10A
6	Power Register	03h	12B8h	4792	25mW	119.8W

PROGRAMMING (continued)

Bus Overview

The SGM837 provides compatibility with I²C and SMBus interfaces. I²C and SMBus are essentially compatible. In this manual, the I²C interface is used as an example, and the SMBus interface will only be mentioned unless there is a difference between the SMBus interface and the I²C interface. SCL and SDA connect the device to the bus, and they are both open-drain connections.

The device which can send the command to the target register is called master and the device which can be controlled by the master is called slave. The master device can generate the clock signal to the slave in order to control it with SCL and SDA lines.

Send a specific address to start the slave, the SDA signal will be pulled from high to low while SCL is still in high state. For the slaves connected to the bus, at the CLK rising edge, the slaves start to be addressed by the master, and followed by a READ or WRITE bit. For the ninth bit of the transmission signal, if SDA is pulled low, the slave acknowledges the transmission, in which case the slave is being addressed.

In one word, for the data transfer process, the initial signal will indicate a start state, and then followed by eight clock pulsed and an acknowledge signal. However, the stability of SDA signal should be guaranteed when SCL is high, otherwise it will be mistaken for START or STOP mode. After the transmission completes, the signal of SDA will change from low to high when SCL is high. The device provides a 28ms timeout action logic on its interface to avoid the bus being locked up.

Serial Bus Address

For the definition of I²C communication, before sending data, the master device should address the specified slave device. There are seven bits for the address of the slave device and another one bit is for the command of reading or writing.

A0 and A1 are used to determine the address of the device. As shown in Table 2, if these two pins are at different logic levels, the device will have different addresses. The device will sample the state of A0 and A1 pins before each communication, so it is necessary to ensure the stability of the states of A0 and A1 pins before any actions taken on the interface.

Serial Interface

On the I²C bus or SMBus, the SGM837 can be operated as a slave device, which is controlled by the master. When connecting to the bus, both SDA and SCL pins are connected through the topology of open-drain. In addition, in order to improve the performance of slave devices under the condition of input spikes and noise bus, filter and Schmitt flip-flop are adopted. Although the device has integrated tip suppression in the digital I/O lines, it is recommended that proper layout be used to minimize coupling in the communication lines. Noise in communication lines mainly comes from two sources: capacitive coupling generated at the signal edges between two communication lines, or switching noise generated by other parts of the system. Keeping lines parallel to ground when routing can reduce coupling effects between communication lines. In addition, shielded signal lines reduce the possibility of unintended noise coupling into digital I/O lines that could be misinterpreted as a START or STOP command.

There are two modes of transmission protocol: fast mode (1kHz to 400kHz) and high-speed mode (1kHz to 3.4MHz). MSB is the first bit to be transferred when transmitting a byte.

Table 2. Different Slave Addresses

A1	A0	Slave Address
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

PROGRAMMING (continued)

Writing and Reading Operation

In order to access the specified pointer register of SGM837, it is necessary to send the values of the desired pointer register after addressing the slave device. As already illustrated in Figure 7, the values of pointer register are required after each write command.

The first byte written to a register is the address of the slave device, and R/$\overline{W}$ bit is low, then the device acknowledges receipt of a valid address. The second byte sent by the host is the address of the register to be written, which updates the register pointer to the desired register. The following two bytes are written to the register addressed by the register pointer, and the device then acknowledges receipt of each byte. Finally, the master generates a START or STOP condition to terminate data transfer (Figure 8).

If the master device desires to read the information of the specified register, a write command must be send by the master at first to indicate which pointer register is needed. First, the slave address should be sent with the low state of R/$\overline{W}$, followed by the address of the pointer address (Figure 7). Second, the START command should be sent by the master, the slave address of the specified SGM837, and then followed with the high state of R/$\overline{W}$ to indicate a read command (Figure 9). The slave transmits the next byte, which is the most significant byte of the register indicated by the register pointer. For the condition of repeated reading, it is not required for sending the bytes of pointer register again, unless the device is reset or the address of pointer register is altered by the write command.

High-Speed (HS) I²C Mode

The SGM837 also supports high-speed (HS) I²C mode whose data rate speeds up to 3.4MHz. To enable this mode, the master device sends a START condition. After the START, a master code is transmitted '00001XXX', followed by a mandatory Not Acknowledge (NACK) condition. Note that the master code is sent in Fast-mode or Standard-mode, which is at most 400kHz.

The three lowest bits of the master code are used to identify different I²C masters on the same bus. The user should guarantee that each master device has its unique identifier.

After the NACK condition, the high-speed transfer begins. At the master device side, the master device sends a REPEATED START condition followed by the slave address and the remaining data, the same as the frame in Fast-mode or Standard mode, just higher speed. At the slave device side, the SGM837 switches the internal circuit to support HS mode. To keep the bus in HS mode, the user should avoid using the STOP condition and use the REPEATED START condition instead. A STOP condition make the SGM837 switch back to support Fast-mode or Standard-mode.

SMBus Alert Response

The SGM837 has the ability to respond to the SMBus alert response that has the ability to identify a quick fault for simple slaves. The master broadcasts the alert response slave address (0001100) and the R/$\overline{W}$ bit is high. The slave that generates the ALERT signal will send its own address through the bus after recognizing the alert response. The host can identify the slave that generates the alert after receiving the slave address (Figure 10).

The alert response is similar to the I²C broadcast call, which may cause multiple slave devices to respond at the same time, and the bus arbitration rules is applied at this time. The losing device will not generate an Acknowledge but continue to pull the Alert line low until it is the device's turn to complete the Acknowledge. Cleared Alert pin asserts again until alert event removes.

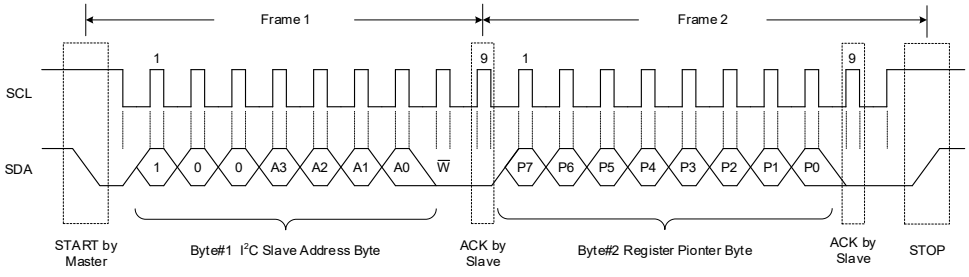


Figure 7. Typical Register Pointer Set

PROGRAMMING (continued)

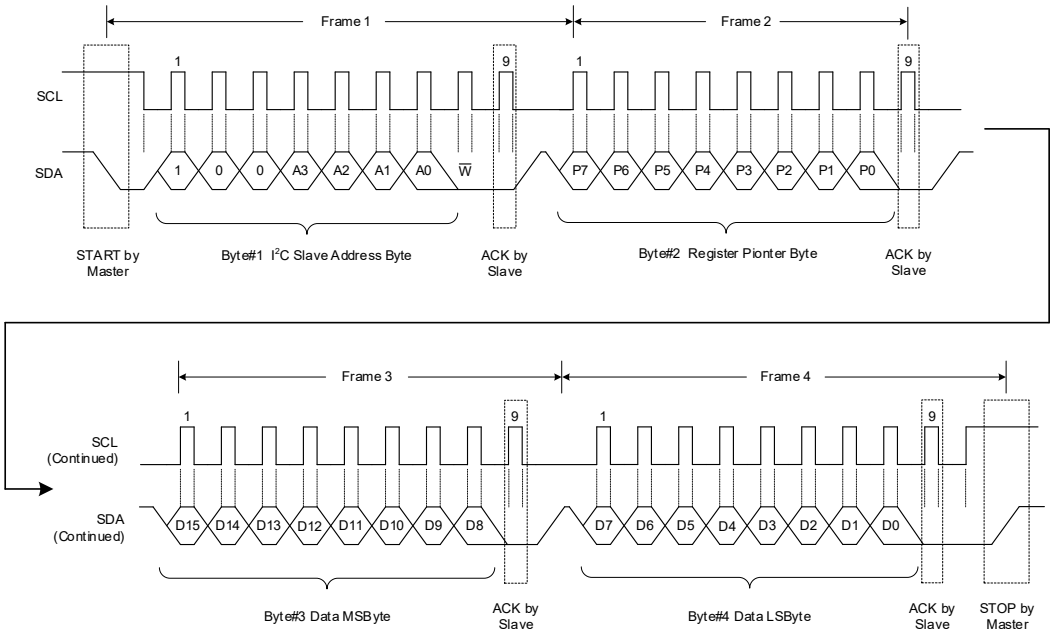


Figure 8. Register Write Word Format

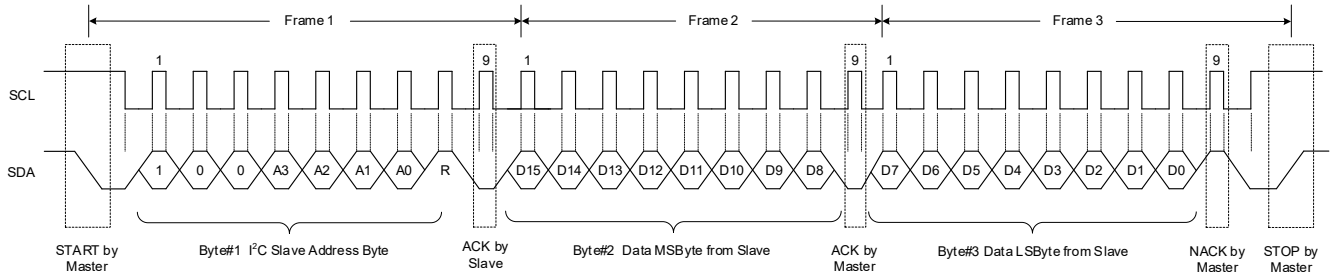


Figure 9. Register Read Word Format

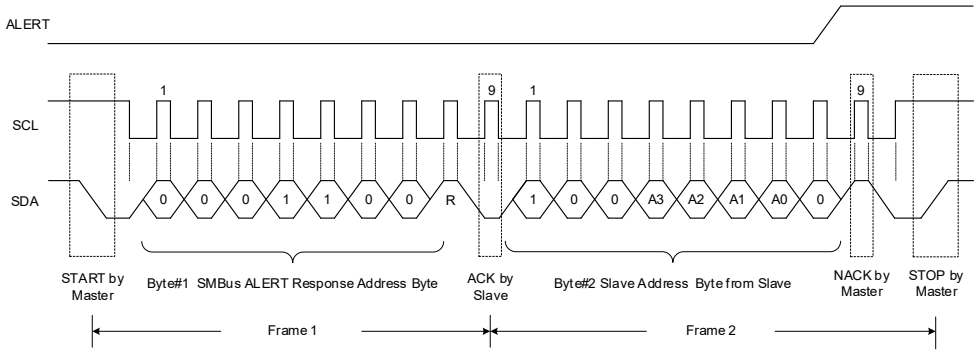


Figure 10. SMBus Alert Format

REGISTER MAPS

I²C Register Set Summary

The SGM837 uses multiple registers to hold configuration information, test results, threshold settings and status information. All device registers are 16 bits, 2 bytes, and communicate through the I²C interface.

POINTER ADDRESS	REGISTER NAME	FUNCTION	POWER-ON RESET		TYPE (1)
HEX			BINARY	HEX	
00h	Configuration Register	Configure ADC averaging, conversion times and operating mode of shunt voltage and bus voltage, reset function.	0100000100100111	4127	R/$\overline{W}$
01h	Shunt Voltage Register	Output data of shunt voltage.	0000000000000000	0000	R
02h	Bus Voltage Register	Output data of bus voltage.	0000000000000000	0000	R
03h	Power Register (2)	Output data of power through internal multiplier.	0000000000000000	0000	R
04h	Current Register (2)	Output data of current through internal multiplier.	0000000000000000	0000	R
05h	Calibration Register	Configures LSB and full-scale range of current.	0000000000000000	0000	R/$\overline{W}$
06h	Mask/Enable Register	Sets alert mode and ready indication.	0000000000000000	0000	R/$\overline{W}$
07h	Alert Limit Register	Sets limit data of one alert function.	0000000000000000	0000	R/$\overline{W}$
FEh	Manufacturer ID Register	ID data of manufacturer.	0101010001001001	5449	R
FFh	Die ID Register	ID data of die.	0010001001100000	2260	R

NOTES:

1. Type: R = Read-Only, R/$\overline{W}$ = Read/Write.
2. The Current Register and Power Register default to ‘0’ because the Calibration register defaults to ‘0’, yielding zero current and power values until the Calibration register is programmed.

REGISTER MAPS (Continued)

Configuration Register (Address = 00h)

The Configuration Register is used to configure the operating mode of the device. This register can not only control the conversion time and averaging mode of both shunt and bus voltages, but also control what signals are selected to be measured.

The Configuration Register can be read without affecting device configuration and ongoing conversion. Writing to the Configuration Register suspends ongoing conversion until the write process is completed, and then the device will begin a new conversion process with the new configuration. The purpose is to avoid any uncertainty about the conditions under which a new conversion process will be started.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	RST	0	R/$\overline{W}$	Reset Bit. When this bit is set to '1', the system will be reset as the power-on reset. It means that all registers are set to their default values. This bit self-clears.
D[14:12]	RESERVED	100	R/$\overline{W}$	Reserved
D[11:9]	AVG[2:0]	000	R/$\overline{W}$	Averaging Mode. Determine the number of samples collected and averaged. 000 = 1 (Default) 001 = 4 010 = 16 011 = 64 100 = 128 101 = 256 110 = 512 111 = 1024
D[8:6]	VBUSCT[2:0]	100	R/$\overline{W}$	Bus Voltage Conversion Time. Set the conversion time for the bus voltage measurement. 000 = 160μs 001 = 220μs 010 = 350μs 011 = 550μs 100 = 1.10ms (Default) 101 = 2.10ms 110 = 4.10ms 111 = 8.30ms
D[5:3]	VSHCT[2:0]	100	R/$\overline{W}$	Shunt Voltage Conversion Time. Set the conversion time for the shunt voltage measurement. 000 = 160μs 001 = 220μs 010 = 350μs 011 = 550μs 100 = 1.10ms (Default) 101 = 2.10ms 110 = 4.10ms 111 = 8.30ms
D[2:0]	MODE[2:0]	111	R/$\overline{W}$	Operating Mode. Select the operation modes, continuous, triggered or power-down. These bits default to continuous shunt and bus measurement mode. 000 = Power-Down or Shutdown 001 = Shunt Voltage, Triggered 010 = Bus Voltage, Triggered 011 = Shunt and Bus, Triggered 100 = Power-Down or Shutdown 101 = Shunt Voltage, Continuous 110 = Bus Voltage, Continuous 111 = Shunt and Bus, Continuous (Default)

REGISTER MAPS (Continued)

Shunt Voltage Register (Address = 01h)

The Shunt Voltage Register is used to store the shunt voltage reading, V_{SHUNT}. Positive numbers are directly displayed in binary format, while negative numbers are displayed in two's complement format. The two's complement of the negative number can be obtained by taking the binary complement of the absolute value of the negative number and adding one. An MSB = '1' indicates it is a negative number.

For example: assuming V_{SHUNT} = -80mV:
Convert the absolute value (80mV) to a decimal integer in LSBs (80mV/2.5μV) = 32000
Convert this number to binary = 0111110100000000
Complement this binary = 1000001011111111
Add '1' to the complement to get the two's complement = 1000001100000000 = 8300h.

The register will display the averaged value if averaging enabled.
Full-scale range of shunt voltage = 81.9175mV (decimal = 7FFF). LSB: 2.5μV.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	SIGN	0	R	
D[14:0]	SD[14:0]	000000000000000	R	

Bus Voltage Register (Address = 02h)

The Bus Voltage Register is used to store the bus voltage reading, V_{BUS}.

The register will display the averaged value if averaging enabled.

Full-scale range of bus voltage = 40.96V (decimal = 7FFF). LSB: 1.25mV.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	RESERVED	0	R	Reserved. This bit is always '0' because bus voltage can only be positive.
D[14:0]	BD[14:0]	000000000000000	R	

Power Register (Address = 03h)

The register will display the averaged power value if averaging enabled.

Set the resolution of the Power Register (03h) to 25 times the programmed Current_LSB internally.

Multiply the decimal value of the Current Register and the decimal value of the Bus Voltage Register together, and then divide by 20000 to caculate the decimal value of the Power Register using Equation 4.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15:0]	PD[15:0]	0000000000000000	R	

Current Register (Address = 04h)

The register will display the averaged current value if averaging enabled.

Multiply the decimal value of the Current Register and the decimal value of the Shunt Voltage Register together, and then divide by 2048 to caculate the decimal value of the Current Register using Equation 3.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	CSIGN	0	R	
D[14:0]	CD[14:0]	000000000000000	R	

REGISTER MAPS (Continued)

Calibration Register (Address = 05h)

This register provides the value of the shunt resistor to the device and sets the resolution of the Current Register. Then Current_LSB and Power_LSB are also determined. This register can also be used for system current calibration. Please see the Programming the Calibration Register section for specific information.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	RESERVED	0	R/$\overline{W}$	Reserved.
D[14:0]	FS[14:0]	000000000000000	R/$\overline{W}$	

Mask/Enable Register (Address = 06h)

The Mask/Enable Register can choose different logic to control Alert, as well as how that pin functions. If more than one function is enabled, the highest significant bit in the alert function (D[15] to D[11]) takes precedence and responds to the Alert Limit Register (07h).

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	SOL	0	R/$\overline{W}$	Over-Voltage Alert Function of Shunt Voltage. If the shunt voltage ADC output exceeds the set value in 07h register, set this bit high to assert the Alert pin.
D[14]	SUL	0	R/$\overline{W}$	Under-Voltage Alert Function of Shunt Voltage. If the shunt voltage ADC output is lower than the set value in 07h register, set this bit high to assert the Alert pin.
D[13]	BOL	0	R/$\overline{W}$	Over-Voltage Alert Function of Bus Voltage. If the bus voltage ADC output exceeds the set value in 07h register, set this bit high to assert the Alert pin.
D[12]	BUL	0	R/$\overline{W}$	Under-Voltage Alert Function of Bus Voltage. If the bus voltage ADC output is lower than the set value in 07h register, set this bit high to assert the Alert pin.
D[11]	POL	0	R/$\overline{W}$	Over Power Alert Function. If the internal multiplier calculated power ADC output exceeds the set value in 07h register, set this bit high to assert the Alert pin high.
D[10]	CNVR	0	R/$\overline{W}$	Conversion Ready Function. Set it high to assert the Alert pin high when the CVRF bit is asserted high.
D[9:5]	RESERVED	00000	R/$\overline{W}$	Reserved.
D[4]	AFF	0	R/$\overline{W}$	Alert Function Flag. Set it high to indicate any one of alert functions actives. Clarify the source of Alert pin.
D[3]	CVRF	0	R/$\overline{W}$	Conversion Ready Flag. Setting it high indicates that all the measurements are finished. The bit can be cleared under two conditions: 1. Configure Register writing (except for power-down mode). 2. Mask/Enable Register reading.
D[2]	OVF	0	R/$\overline{W}$	Math Overflow Flag. Setting it high indicates math overflow error. Output datum is invalid.
D[1]	APOL	0	R/$\overline{W}$	Alert Polarity bit. Setting it low indicates normal operation: active low output. Setting it high indicates inverted operation: active high output.
D[0]	LEN	0	R/$\overline{W}$	Alert Latch Enable Bit. Latch the Alert pin and Alert Flag bits. 1 = Latch enabled 0 = Transparent (default) Setting it low indicates that the Alert pin and Flag bit is reset when the limit state is cleared. Setting it high indicates that the Alert pin and Flag bit keeps high until reading Mask/Enable Register.

REGISTER MAPS (Continued)

Alert Limit Register (Address = 07h)

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15:0]	AUL[15:0]	0000000000000000	R/$\overline{W}$	The Alert Limit Register is used to provide a limit threshold for the register selected by the Mask/Enable Register to determine whether it exceeds or falls below the threshold.

Manufacturer ID Register (Address = FEh)

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15:0]	ID[15:0]	0101010001001001	R	Manufacturer ID Bits. Store the manufacturer identification bits.

Die ID Register (Address = FFh)

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15:4]	DID[11:0]	001000100110	R	Device ID Bits. Store the device identification bits.
D[3:0]	RID[3:0]	0000	R	Die Revision ID Bits. Store the device revision identification bits.

APPLICATION INFORMATION

The SGM837 is a current and power monitor with an I²C and SMBus compatible interface. Since the device can monitor the shunt and bus voltages, the current in amperes and power in watts readings can be directly obtained through the internal multiplier by setting the correct calibration value, conversion time and average mode.

Typical Applications

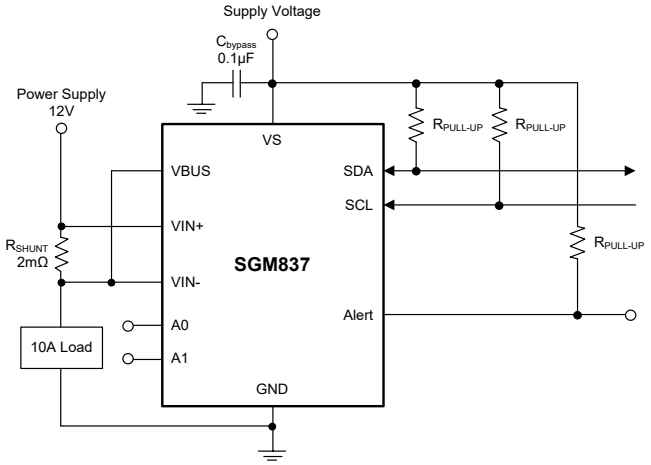


Figure 11. High-Side Sensing Circuit

Design Requirements

The SGM837 characterizes current by the voltage drop across the shunt resistor. The device can also measure the bus voltage, and then calculate the corresponding power by programming the Calibration Register. It has a programmable alert function, which can respond to user-defined fault or conversion completion events. In addition, users can also customize the specific threshold that triggers alert.

Detailed Design Procedure

The Configuration Register is set according to the required conversion time and averaging mode. There are five alert response logics in the Mask/Enable Register, and the user selects the required alert function. The Alert pin should be pulled up to V_{VS} via the pull-up resistor. With the comparison threshold set in the Alert Limit Register, the device determines whether the alert pin responds to the selected alert function.

Figure 12 shows that the alert pin responds to the shunt voltage over-limit when the threshold is set to 80mV, the conversion time (t_{CT}) is 1.10ms and averaging is set to 1. Figure 13 shows the response of reducing the conversion time from 1.10ms to 160μs under the same conditions.

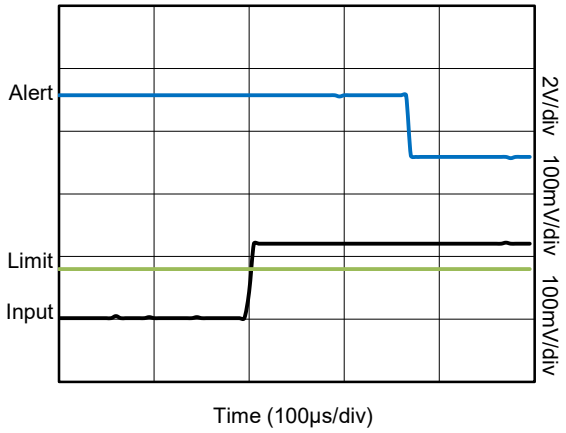


Figure 12. Alert Response (t_{CT} = 1.10ms)

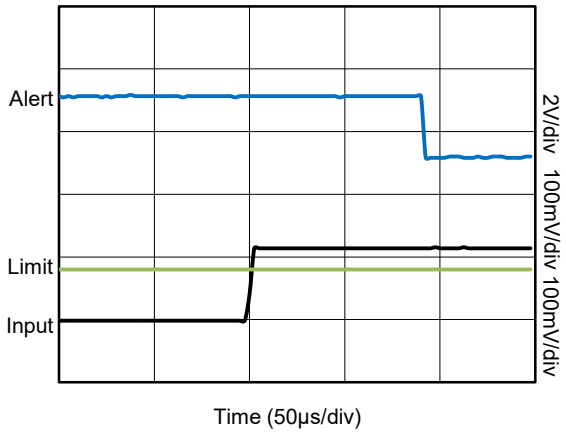


Figure 13. Alert Response (t_{CT} = 160μs)

Table 3. Configuration Register Settings for Figure 12 (Value = 4025h)

BITS	BIT NAME	POR
D[15]	RST	0
D[14:12]	RESERVED	100
D[11:9]	AVG[2:0]	000
D[8:6]	VBUSCT[2:0]	000
D[5:3]	VSHCT[2:0]	100
D[2:0]	MODE[2:0]	101

APPLICATION INFORMATION (Continued)

Table 4. Configuration Register Settings for Figure 13 (Value = 4005h)

BITS	BIT NAME	POR
D[15]	RST	0
D[14:12]	RESERVED	100
D[11:9]	AVG[2:0]	000
D[8:6]	VBUSCT[2:0]	000
D[5:3]	VSHCT[2:0]	000
D[2:0]	MODE[2:0]	101

Table 5. Mask/Enable Register Settings for Figure 12 and Figure 13 (Value = 8000h)

BITS	BIT NAME	POR
D[15]	SOL	1
D[14]	SUL	0
D[13]	BOL	0
D[12]	BUL	0
D[11]	POL	0
D[10]	CNVR	0
D[9:5]	RESERVED	00000
D[4]	AFF	0
D[3]	CVRF	0
D[2]	OVF	0
D[1]	APOL	0
D[0]	LEN	0

Table 6. Alert Limit Register Settings for Figure 12 and Figure 13 (Value = 7D00h)

BITS	BIT NAME	POR
D[15:0]	AUL[15:0]	0111110100000000

Power Supply Recommendations

The device can accurately measure the common-mode voltages applied to power supply terminals, which may be beyond its supply voltage V_{VS}. For example, the device power supply voltage V_{VS} is 5V, but the monitored load voltage can be as high as 36V. Regardless of whether the device is powered or not, the input terminal of the device can withstand a voltage of 0V to 36V.

The bypass capacitors should be placed as close to input and GND pins of the device as possible to ensure the stability of the power supply. A bypass capacitor of 0.1μF is recommended. For noisy or high-impedance power supplies, the device requires additional decoupling capacitors to filter power supply noise.

Layout Guidelines

A Kelvin connection or a 4-wire connection is recommended to be made between the input pins (IN+ and IN-) and the sensing resistor. These connection techniques avoid introducing additional impedance between the input pins. Considering that the resistance of the sensing resistor is very small, the additional high current-carrying impedance will result in considerable measurement errors.

REVISION HISTORY

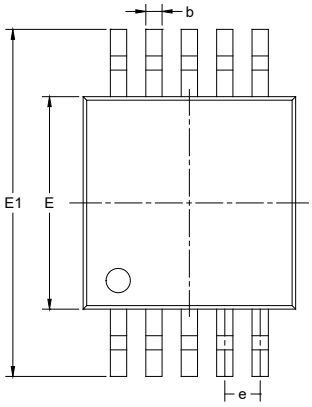
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

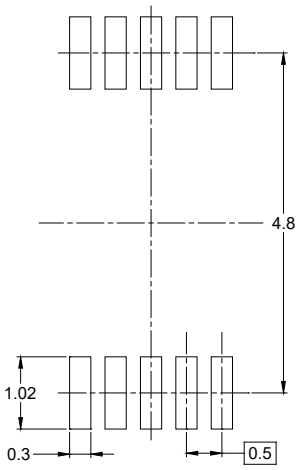
JANUARY 2025 – REV.A to REV.A.1	Page
Updated Typical Performance Characteristics section	6

Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

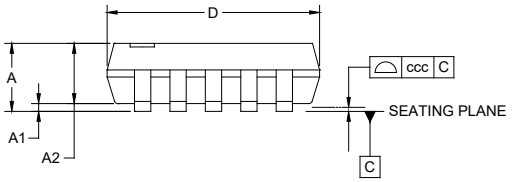
PACKAGE OUTLINE DIMENSIONS

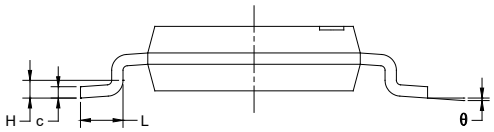
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)



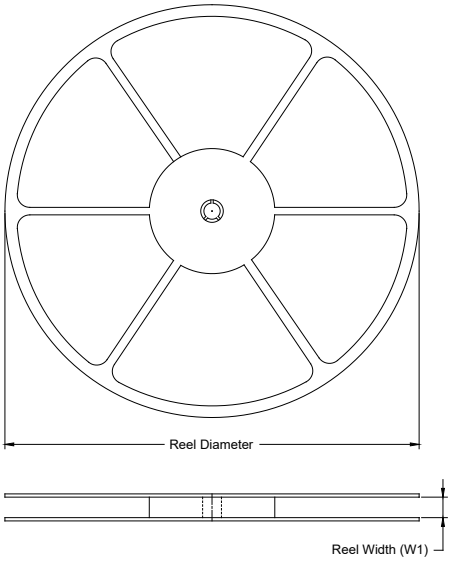


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.170	-	0.330
c	0.080	-	0.230
D	2.900	-	3.100
E	2.900	-	3.100
E1	4.750	-	5.050
e	0.500 BSC		
H	0.250 TYP		
L	0.400	-	0.800
θ	0°	-	8°
ccc	0.100		

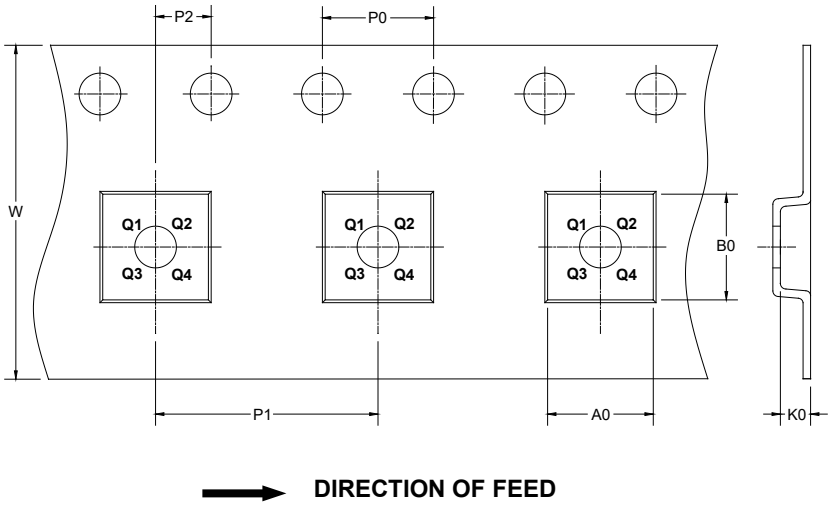
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

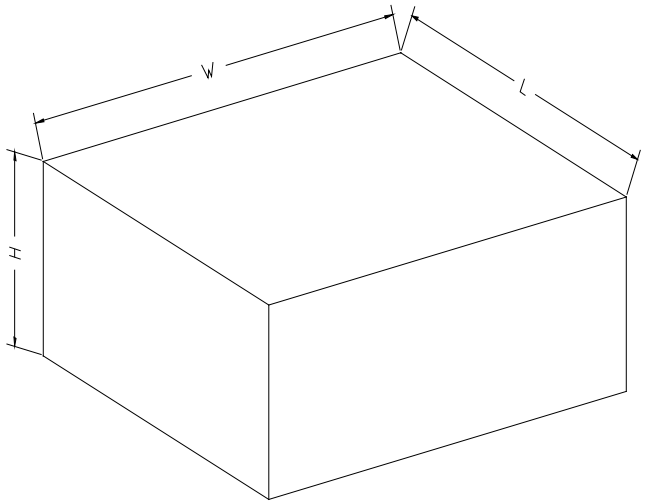
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002