SGM6614
18V Output, 15A, Fully Integrated Synchronous Boost Converter

GENERAL DESCRIPTION

The SGM6614 is a 15A switch current, fully integrated synchronous Boost converter. The integrated switch FET and rectifier switch with an 8.8mΩ low-side on-resistance and a 12.2mΩ high-side on-resistance respectively provide high conversion efficiency for portable applications. The wide input voltage range of 2.17V to 18V offers flexibility to various input supplies such as single-cell to multi-cell Lithium batteries. The device can support up to 18V output.

The SGM6614 adopts the fixed frequency peak current mode control topology for main switch FET PWM duty cycle control. The device operates in pulse width modulation (PWM) mode at medium and heavy loads, where two power FETs are alternately turned on in one switching cycle. It automatically switches to pulse frequency modulation (PFM) mode at light loads. PWM mode adopts 500kHz switching frequency.

The SGM6614 offers various protection features to improve device robustness, such as over-voltage protection, over-current protection and thermal shutdown.

The SGM6614 is available in a Green TQFN-3×2.5-11L package.

FEATURES

- **2.17V to 18V Input Voltage Range**
- **4.5V to 18V Output Voltage Range**
- **2.4V Minimum Input Voltage for Startup**
- **15A (TYP) Peak Switch Current Limit**
- **8.8mΩ Low-side and 12.2mΩ High-side MOSFETs**
- **Fixed 500kHz Switching Frequency**
- **High Efficiency**
  - **Up to 94.42% Efficiency at V_{IN} = 3.6V, V_{OUT} = 13V, and I_{OUT} = 2A**
  - **Up to 97.07% Efficiency at V_{IN} = 7.2V, V_{OUT} = 16V, and I_{OUT} = 2.5A**
- **85μA (TYP) Quiescent Current into VOUT Pin**
- **Less than 1.5μA Shutdown Current**
- **Auto PFM at Light Loads**
- **19V Output Over-Voltage Protection**
- **Cycle-by-Cycle Over-Current Protection**
- **Thermal Shutdown**
- **Available in a Green TQFN-3×2.5-11L Package**

APPLICATIONS

Smart Speaker
Portable POS
Power Bank

TYPICAL APPLICAITION

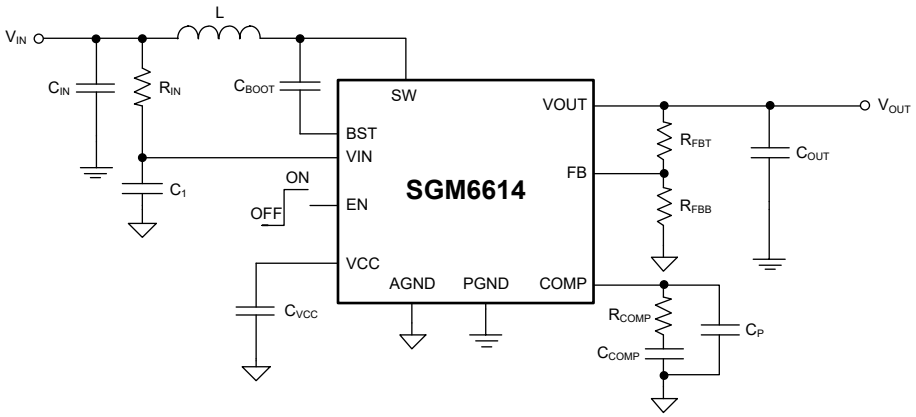


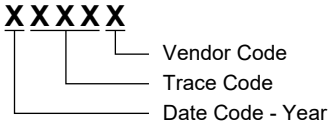
Figure 1. Typical Application

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6614	TQFN-3×2.5-11L	-40℃ to +125℃	SGM6614XTSL11G/TR	SGMMEV XXXXX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

BST Voltage ..... -0.3V to V_{SW} + 5.5V
VIN, EN, VOUT, SW Voltages ..... -0.3V to 20V
Other Pin Voltages ..... -0.3V to 6V
Package Thermal Resistance
TQFN-3×2.5-11L, θ_{JA} ..... 63℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 2.17V to 18V
Output Voltage Range, V_{OUT} ..... 4.5V to 18V
Effective Inductance Range, L ..... 0.8μH to 5.6μH
Effective Input Capacitance Range, C_{IN} ..... 10μF (TYP)
Effective Output Capacitance Range, C_{OUT} .. 10μF to 1000μF
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

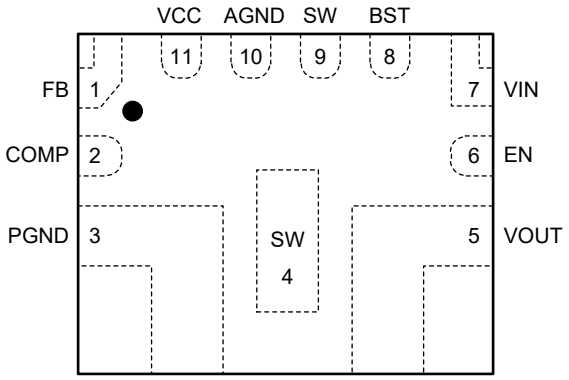
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×2.5-11L

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	FB	I	Inverting Input of the Error Amplifier. Connect it to the midpoint of a resistor divider to set the Boost output voltage.
2	COMP	O	Internal Error Amplifier Output. Connect the loop compensation components between the COMP and AGND pins.
3	PGND	P	Power Ground Pin. Source connection of the internal N-channel low-side MOSFET.
4, 9	SW	P	Switching Node. Drain connection of the internal N-channel low-side MOSFET.
5	VOUT	P	The Boost Output Pin.
6	EN	I	Enable Pin. Logic high turns the converter on. Logic low turns the converter off.
7	VIN	I	Input Power Supply Pin.
8	BST	O	N-Channel Rectify Switch Power Supply Pin. Connect a 0.1μF ceramic capacitor between the BST and SW pins.
10	AGND	-	Signal Ground Pin.
11	VCC	O	Internal Regulator Output Pin. Connect a ceramic capacitor greater than 1.0μF between the VCC and the ground.

NOTE: I = input, O = output, P = power supply.

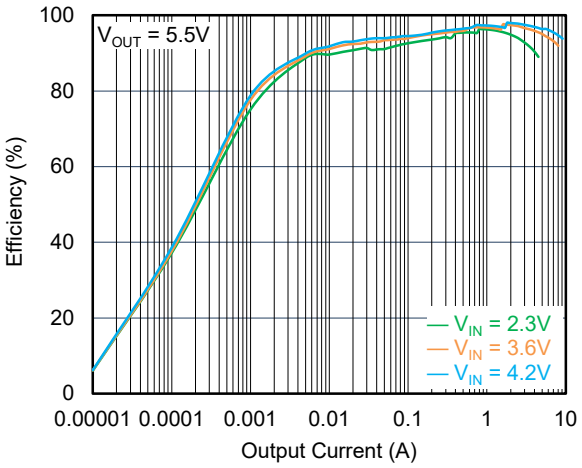
ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.7V to 9V, V_{OUT} = 16V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

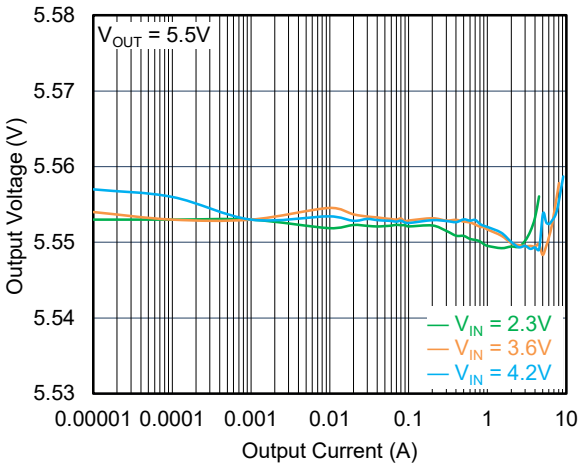
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Input Voltage Under-Voltage Lockout (UVLO) Threshold	V_{UVLO}	V_{IN} rising		2.3	2.63	V
		V_{IN} falling, V_{OUT} > 3V	1.55	1.9	2.17	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}	V_{UVLO} rising - V_{UVLO} falling		400		mV
VCC Regulated Voltage	V_{CC}	I_{CC} = 5mA, V_{IN} = 9V		4.96		V
VCC Falling Threshold	V_{CC_UVLO}	V_{CC} falling		2		V
Quiescent Current into VIN Pin	I_{Q_IN}	EN = high, no switching, 2.7V < V_{IN} < 16V, V_{OUT} > 1.1V_{IN}, T_J = -40℃ to +85℃		0.34	1.4	μA
Quiescent Current into VOUT Pin	I_{Q_OUT}	EN = high, no switching, 2.7V < V_{OUT} < 16V, V_{OUT} > 1.1V_{IN}, T_J = -40℃ to +85℃		85	220	μA
Shutdown Current into VIN Pin	I_{SD}	EN = low, no switching, 2.7V < V_{IN} < 18V, V_{OUT} > 1.1V_{IN}, T_J = -40℃ to +85℃			1.5	μA
Reverse Leakage Current into SW Pin	I_{SD_SW}	EN = low, no switching, V_{SW} = 0V, 4.5V < V_{OUT} < 18V, T_J = -40℃ to +85℃			1.2	μA
Output						
Feedback Regulation Reference Voltage	V_{REF}	PWM Operation	0.565	0.598	0.628	V
Feedback Input Bias Current	I_{FB}				20	nA
Over-Voltage Protection	V_{OVP}	Rising threshold	18.1	19	20	V
Over-Voltage Protection Hysteresis	V_{OVP_HYS}			570		mV
Power Switch						
High-side FET On-Resistance	R_{DSON}	V_{CC} = 5V		12.2		mΩ
Low-side FET On-Resistance	R_{DSON}	V_{CC} = 5V		8.8		mΩ
Current Limit						
Switching Peak Current Limit	I_{LIM}	V_{IN} = 7.2V, V_{OUT} = 16V, L = 2.2μH, T_J = -20℃ to +125℃	10.9	15	17	A
Logic Interface						
EN High-Level Input Voltage	V_{IH}				1.18	V
EN Low-Level Input Voltage	V_{IL}		0.46			V
Hysteresis of The Control Logic	V_{HYS}		50			mV
Pull-Down Resistor for Control Pin	R_{EN}			850	1140	kΩ
Error Amplifier						
COMP Pin Output High Voltage	V_{COMP_H}	V_{FB} = V_{REF} - 50mV		1.92		V
COMP Pin Output Low Voltage	V_{COMP_L}	V_{FB} = V_{REF} + 50mV		0.54		V
Error Amplifier Transconductance	G_{EA}			160		μS
Power Stage Transconductance (Inductor Peak Current/Comp Voltage)	K_{COMP}			12		A/V
COMP Pin Sink Current	I_{SINK}	V_{FB} = V_{REF} + 200mV, V_{COMP} = 1.5V		27		μA
COMP Pin Source Current	I_{SOURCE}	V_{FB} = V_{REF} + 200mV, V_{COMP} = 1.5V		27		μA
Switching Time						
Soft-Start Time	t_{SS}	V_{IN} = 7.2V, V_{OUT} = 16V, L = 2.2μH, $C_{OUT(EFF)}$ = 50μF		3		ms
Switching Frequency	f_{SW}	V_{IN} = 7.2V, V_{OUT} = 16V, V_{IN} = 3.6V, V_{OUT} = 13V	400	500	600	kHz
Minimum On-Time	t_{ON_MIN}			120		ns
Protection						
Thermal Shutdown	T_{SD}	Junction temperature rising		160		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}			20		℃

TYPICAL PERFORMANCE CHARACTERISTICS

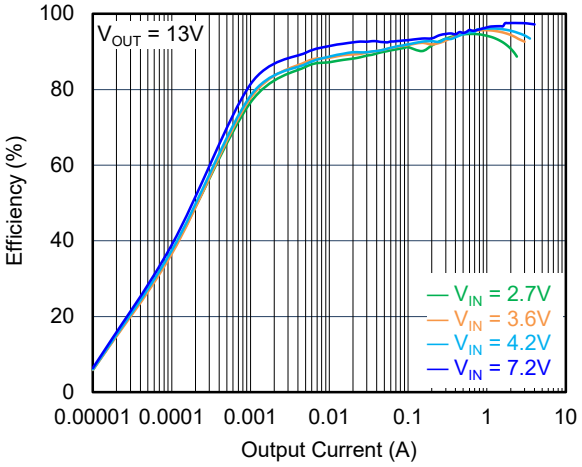
Efficiency vs. Output Current



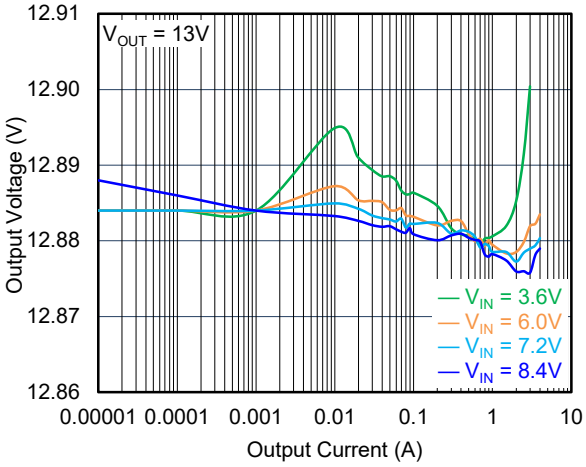
Output Voltage vs. Output Current



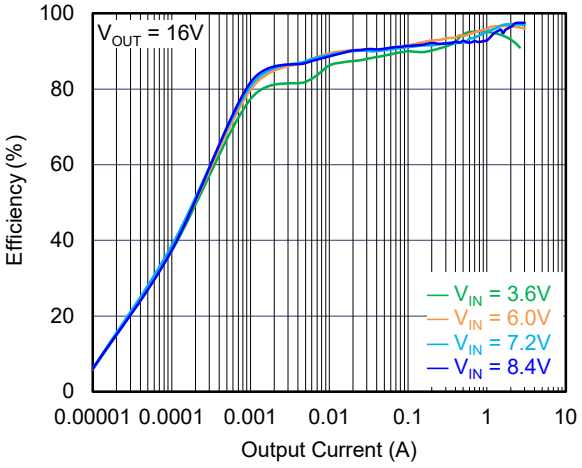
Efficiency vs. Output Current



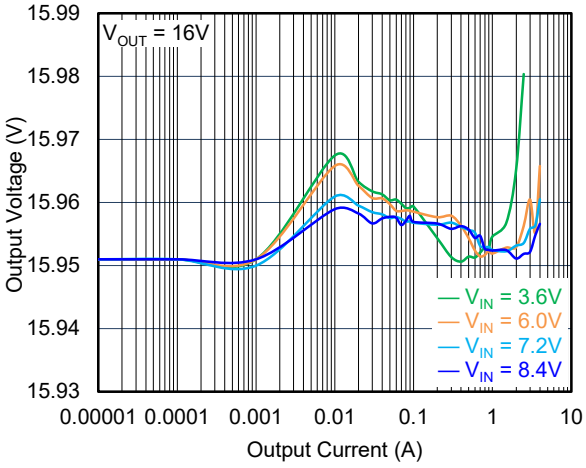
Output Voltage vs. Output Current



Efficiency vs. Output Current

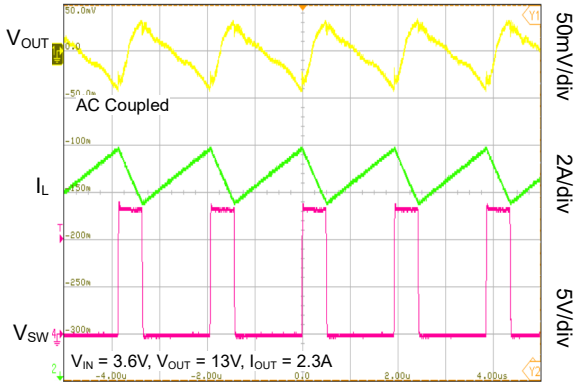


Output Voltage vs. Output Current



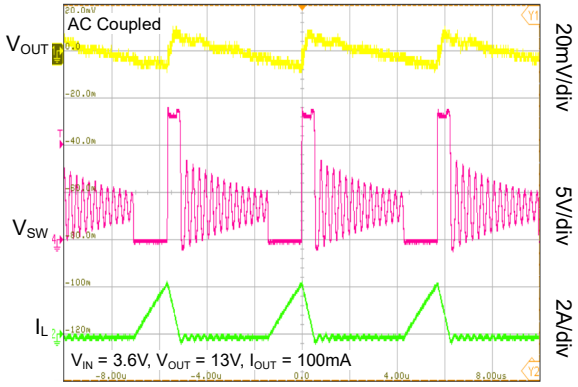
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Switching Waveforms in CCM



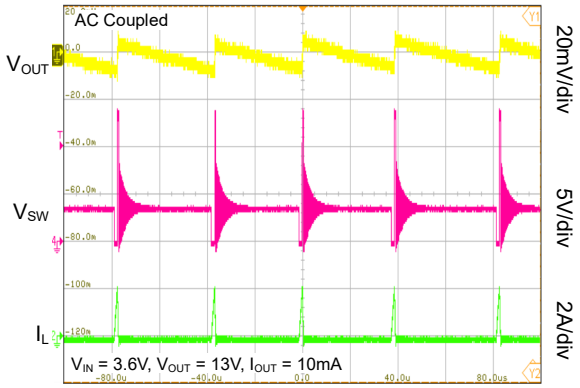
Time (1μs/div)

Switching Waveforms in 100mA load



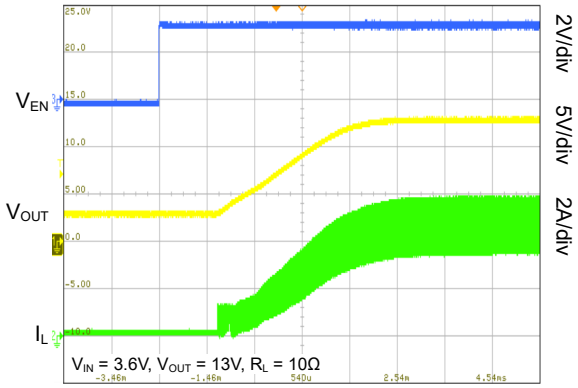
Time (2μs/div)

Switching Waveforms in 10mA load



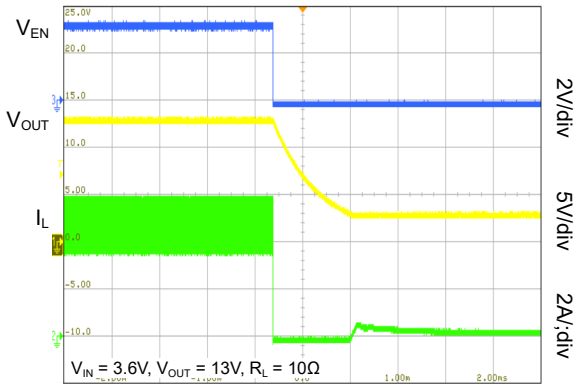
Time (20μs/div)

Startup Waveforms



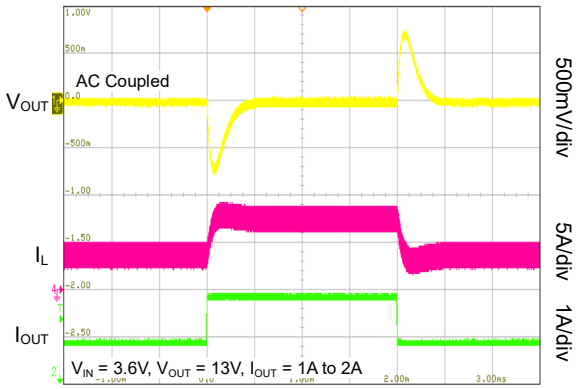
Time (1ms/div)

Shutdown Waveforms



Time (500μs/div)

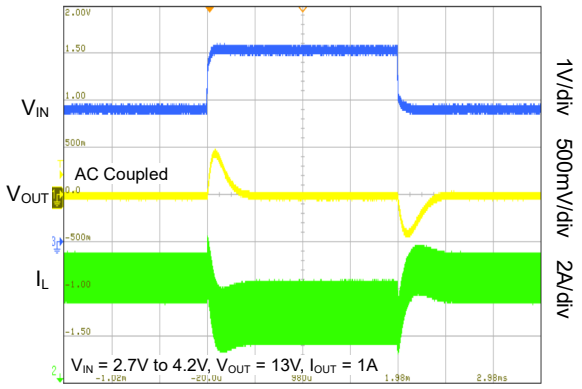
Load Transient



Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Line Transient



Time (500μs/div)

FUNCTIONAL BLOCK DIAGRAM

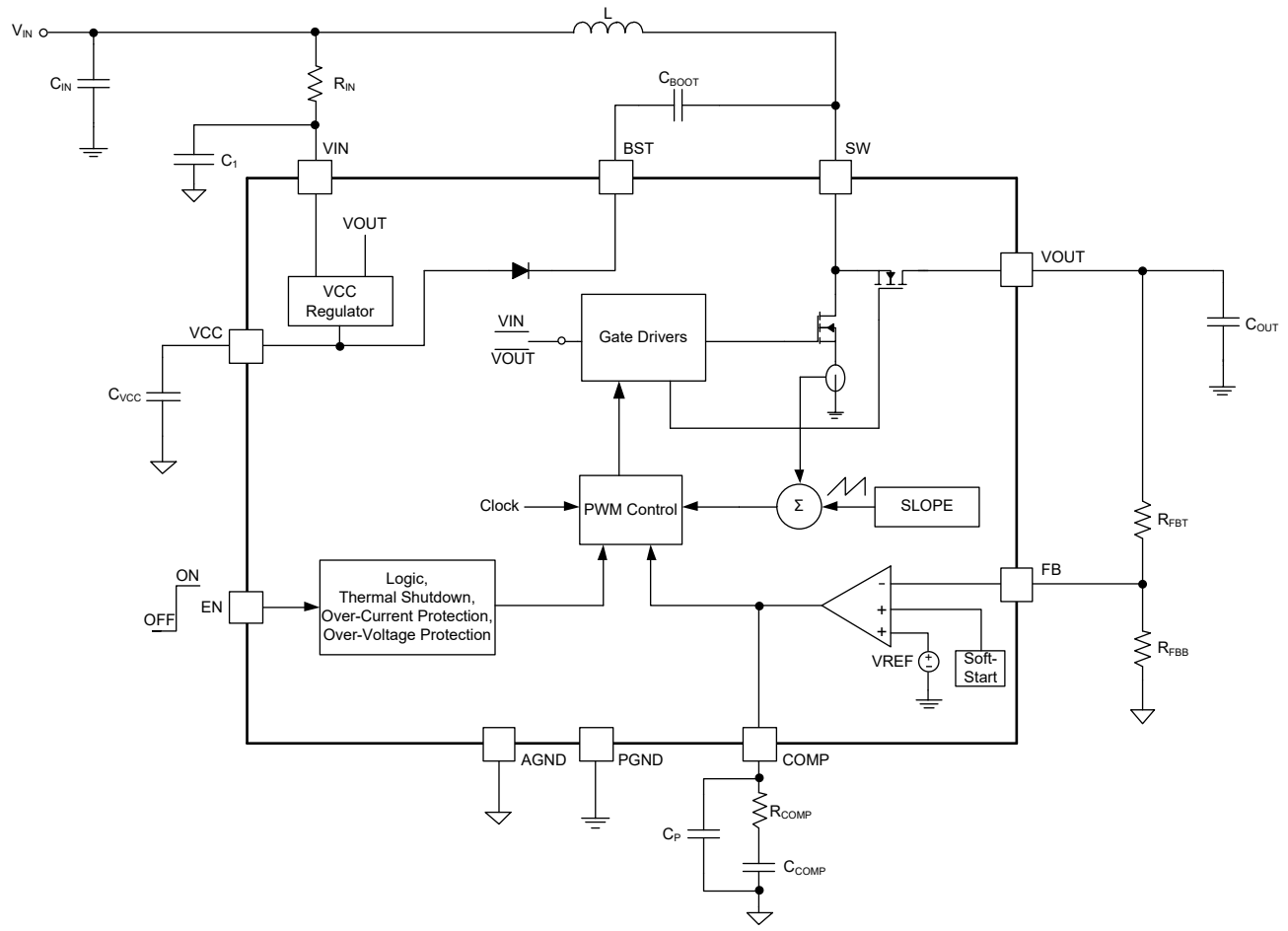


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Overview

The SGM6614 is a high power density synchronous Boost converter with 15A (TYP) switch current limit. The device integrates 8.8mΩ low-side (LS) and 12.2mΩ high-side (HS) power FETs to support the high power output. The wide input voltage operates from 2.17V to 18V, which supports wide range of input sources, while the maximum output voltage is up to 18V, and the device sources up to 2.5A load current from a two-cell Lithium battery.

The SGM6614 adopts 500kHz fixed frequency peak current mode control to regulate the output voltage. The device automatically implements PFM mode at light loads. In moderate to heavy loads, the device automatically switches to PWM operation to reduce the output ripple.

The SGM6614 integrates various protection features such as cycle-by-cycle current limit in overload conditions, and thermal shutdown to prevent the device from overheating.

An external loop compensation network improves the flexibility of the device to work with different combination of inductor and output capacitor selection, and the loop response can be optimized based on the application that needs to achieve excellent line and load transient responses.

Under-Voltage Lockout (UVLO)

The SGM6614 provides UVLO function at the VIN pin to prevent undesired input source conditions, such as excessive discharge of input battery. When V_{IN} drops below 1.9V (TYP), the device stops operation. The VCC pin also implements UVLO function. The device is disabled when V_{CC} drops below 2V (TYP).

Enable and Startup

The SGM6614 provides internal soft-start (SS) function to prevent output voltage overshoot and to reduce inrush current at startup. When V_{IN} exceeds the V_{UVLO} rising threshold and EN pin is toggled to logic high, the internal SS circuit will regulate the SS voltage to the reference voltage in 3ms. The SS voltage is fed to the inverting input of the error amplifier to compare with the reference voltage. After t_{SS} time expires, the inverting input is switched to the FB pin to regulate the output voltage. SS sequence occurs when the EN pin logic toggles.

PWM Mode

The SGM6614 adopts fixed frequency peak current mode architecture to regulate the output voltage. In PWM mode, the LS FET is turned on to ramp up the inductor current. When the inductor current reaches the threshold that depends on the error amplifier output, the LS FET is turned on. After a short deadtime, the HS FET is turned on to deliver the inductor current to the output capacitor. When the next clock pulse arrives, after a short deadtime, the LS FET is turned on again, and this cycle repeats. The internal error amplifier adjusts duty cycle of the LS FET on-time to regulate the output voltage.

PFM Mode

The SGM6614 provides auto PFM operation to improve the efficiency at light loads. As the load current decreases in PWM mode, the output of the error amplifier decreases accordingly to reduce the peak inductor current, and thus it delivers less current to the load. As the load decreases further, the inductor current reaches 0A during the HS FET on-time, the internal zero cross detect comparator triggers to turn off the HS FET to prevent negative current flow, and waits for the next clock pulse to turn on the LS FET. As the load current continues decreasing, the output of the error amplifier drops to the PFM threshold voltage and is clamped at this voltage, then the SGM6614 operates in PFM mode. In PFM operation, the device skips pulses to deliver just enough power to the load and to maintain the output voltage in regulation.

The output voltage remains constant across various operation modes, as shown in Figure 3.

DETAILED DESCRIPTION (continued)

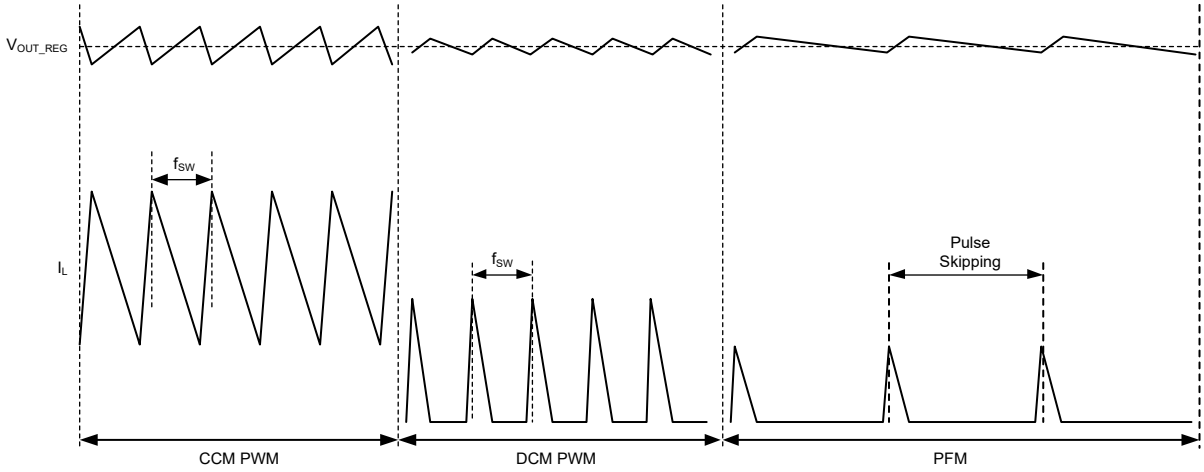


Figure 3. PFM Mode Diagram

Switching Peak Current Limit

The SGM6614 has cycle-by-cycle peak switch current limit to prevent output overload condition. As soon as the inductor current reaches 15A (TYP), the SGM6614 turns off the LS FET immediately to prevent the inductor current from ramping up.

Over-Voltage Protection

The SGM6614 has output over-voltage protection to prevent the device from damaging. When V_{OUT} reaches 19V (TYP), the device stops switching. The device resumes normal operation when V_{OUT} drops below 18.43V (TYP).

Thermal Shutdown

The SGM6614 includes thermal shutdown function to protect the die against overheating damage. When the junction temperature (T_J) exceeds +160℃ (TYP), the device stops switching. The device operation will resume when T_J is cooled down by 20℃.

APPLICATION INFORMATION

The SGM6614 is a high power density synchronous Boost converter with 15A (TYP) switch current limit, and is capable of supporting up to 18V output voltage. The device implements the fixed frequency peak current mode architecture to regulate the output voltage. The device automatically enters the PFM mode operation at light loads to maximize the efficiency. At medium to heavy load range, the device automatically enters the CCM operation with minimal output voltage ripple. The external compensation network offers flexibility to adopt in various application needs and the combinations of external inductor and output capacitor.

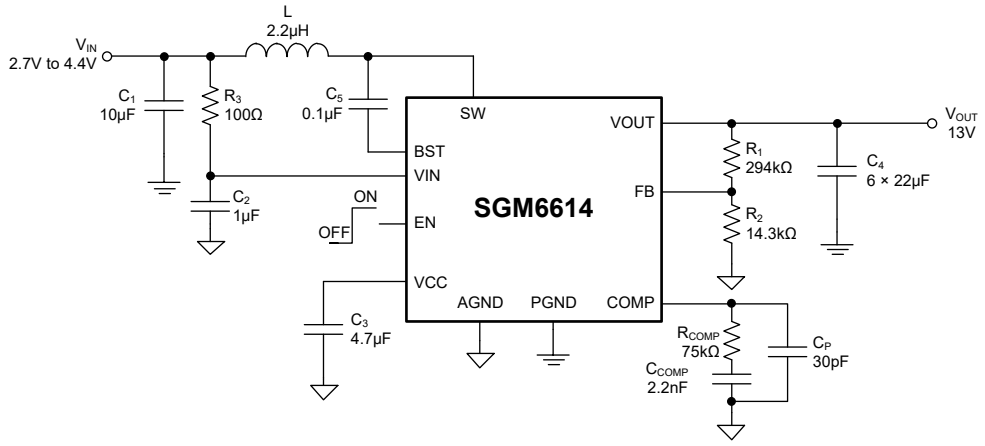


Figure 4. 3.6V to 13V/2.3A Output Converter

Design Requirements

Table 1. Design Requirements

Design Parameters	Example Values
Input Voltage Range	2.7V to 4.4V
Output Voltage	13V
Output Voltage Ripple	100mV$_{PP}$
Output Current Rating	2.3A

Setting Output Voltage

A resistor divider connected between VOUT and FB pins programs the output voltage. In order to achieve best output voltage accuracy, the recommended value for R_2 resistor should be less than 300kΩ to ensure that the current flowing through R_2 is 100 times larger than the leakage current flowing into the FB pin. Lower R_2 resistance also improves the device noise immunity. Use equation below to calculate the R_1 resistance.

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \quad (1)$$

Input Capacitor

It is recommended to connect a 0.1μF ceramic bypass capacitor as close to the input pin of SGM6614 as possible, since the VIN pin serves as the power supply for the device. The VCC pin is the output of the internal LDO regulator. A 1μF or higher ceramic capacitor is recommended to place as close to the VCC pin as possible to ensure the stable operation of the LDO.

A 10μF or higher ceramic capacitor is recommended to place at the power stage input to filter out any parasitic inductance from the input supply to the SGM6614.

Due to the DC derating effect of the ceramic capacitor, the selected capacitor should have higher voltage rating than the maximum voltage expected at the power stage input, VCC pin, and VIN pin.

APPLICATION INFORMATION (continued)

Inductor

Inductor is an essential element for today's DC/DC switch mode power supplies regardless of topology. Inductor serves as an energy storage element for power conversion. Inductance and inductor's saturation current are two most important criterions for inductor selection.

The SGM6614 is optimized to operate with inductance ranges from 1.0μH to 4.7μH. A typical 2.2μH inductor meets the requirements of most applications.

Saturation current and DCR are the key selection criterions for a power inductor. The minimal saturation current rating of the selector inductor should be higher than the worst-case peak current of the application.

Equations 2 to 4 show the calculated key parameters for selecting the inductor. Worst case occurs at minimum input voltage, maximum output voltage, maximum load current, and minimal switching frequency. A -30% inductance tolerance should be considered for the calculation as well.

Equation 2 calculates the DC current going through the inductor.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (2)$$

where V_{OUT} is the output voltage, I_{OUT} is the load current, V_{IN} is the input voltage, and η is the conversion efficiency.

Use Equation 3 to calculate the peak-to-peak ripple current going through the inductor.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times f_{SW}} \quad (3)$$

where I_{PP} is the peak-to-peak ripple current of the inductor, L is the inductance, f_{SW} is the switching frequency, V_{OUT} is the output voltage, and V_{IN} is the input voltage.

Based on Equations 2 and 3, the peak current is the sum of DC average current plus half of the ripple current as shown in Equation 4.

$$I_{LPEAK} = I_{DC} + \frac{I_{PP}}{2} \quad (4)$$

Use the value calculated in Equation 4 to select the inductor with proper saturation current rating.

Lower DCR inductor is recommended to improve the conversion efficiency of the device, especially for large load current applications. As shown in Equation 3, smaller inductance increases the peak-to-peak current, which results in higher AC core loss of the inductor. However, the tradeoff of smaller inductance parts comes with smaller footprint and larger inductance parts with same saturation current rating generally comes with a larger footprint. For SGM6614, Table 2 lists the recommended inductors from various manufacturers.

Table 2. Recommended Inductor Selection

L (μH)	DCR MAX (mΩ)	Saturation Current/ Heat Rating Current (A)	Size MAX (L × W × H mm^3)	Part Number	Manufacturer
2.2	4.5	26.0/19.5	10.3 × 11.5 × 5.0	CMLE105T-2R2MS-99	Cyntec
1.0	2.5	36.0/25.5	10.3 × 11.5 × 5.0	CMLE105T-1R0MS-99	Cyntec
2.2	4.95	32.0/20.0	10.0 × 11.3 × 6.0	XAL1060-222ME	Coilcraft
2.2	7.0	18.0/15.0	11.5 × 10.3 × 4.0	104CDMCCDS-2R2MC	Sumida

APPLICATION INFORMATION (continued)

Output Capacitor

The output capacitors of Boost converter dictate the output voltage ripple and load transient response. Equation 5 is used to estimate the output voltage ripple based on the designed output capacitance.

The DC derating effect of the ceramic capacitor should be considered when selecting the capacitors. The voltage rating of the selected capacitor should be higher than maximum operation output voltage with >30% margin.

$$V_{RIPPLE\_DIS} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \quad (5)$$

ESR of the output capacitor affects the output ripple. Use Equation 6 to calculate the output ripple due to ESR.

$$V_{RIPPLE\_ESR} = I_{LPEAK} \times R_{C\_ESR} \quad (6)$$

Loop Stability

The compensation network of SGM6614 is implemented externally to improve design flexibility. The SGM6614 implements a transconductance error amplifier, where the COMP pin is the output of the internal error amplifier. A Type-II compensation network consisting of R_{COMP}, C_{COMP}, and C_P connected on COMP pin is used to configure the loop response of SGM6614.

The power stage small signal loop response of peak current control can be modeled by Equation 7.

$$G_{PS}(S) = K_{COMP} \times \frac{R_O \times (1-D)}{2} \times \frac{(1+\frac{S}{2\pi f_{ESRZ}}) \times (1-\frac{S}{2\pi f_{RHPZ}})}{1+\frac{S}{2\pi f_P}} \quad (7)$$

where R_O is the output load resistance, D is the switching duty cycle, K_{COMP} is power stage transconductance (inductor peak current/comp voltage), which is 12A/V, f_P is the pole's frequency, f_{ESRZ} is the zero's frequency, and f_{RHPZ} is the right-half-plane-zero's frequency.

$$f_P = \frac{2}{2\pi \times R_O \times C_{OUT}} \quad (8)$$

where C_{OUT} is effective capacitance of the output capacitor.

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (9)$$

where R_{ESR} is the equivalent series resistance of the output capacitor.

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L} \quad (10)$$

Equation 11 shows the small signal transfer function of compensation network.

$$G_C(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{(1+\frac{S}{2\pi f_{COMZ}})}{(1+\frac{S}{2\pi f_{COMP1}})(1+\frac{S}{2\pi f_{COMP2}})} \quad (11)$$

where G_{EA} is the amplifier's transconductance, R_{EA} is the amplifier's output resistance, V_{REF} is the FB reference voltage, V_{OUT} is the output voltage, f_{COMP1} and f_{COMP2} are the pole's frequency of the compensation network, and f_{COMZ} = the zero's frequency of the compensation network.

Once the error amplifier and power stage's poles and zeros are determined, the component value of compensation network can be designed. The designed loop crossover frequency f_C should be within 1/5 of the RHPZ frequency (f_{RHPZ}) or 1/10 of the switching frequency. Higher crossover frequency could improve the transient response. However, the crossover frequency should be designed to avoid instability.

With a selected f_C, use Equation 12 to calculate the required R_{COMP}.

$$R_{COMP} = \frac{2\pi \times V_{OUT} \times C_{OUT} \times f_C}{(1-D) \times V_{REF} \times G_{EA} \times K_{COMP}} \quad (12)$$

The value of C_{COMP} can be calculated by:

$$C_{COMP} = \frac{R_O \times C_{OUT}}{2R_{COMP}} \quad (13)$$

The value of C_P can be calculated by:

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_{COMP}} \quad (14)$$

For application with only ceramic capacitor, or if the calculated value of C_P is less than 10pF, C_P is not needed.

To measure good loop compensation design, greater than 45° of phase margin and greater than 10dB gain margin could provide good loop stability and avoid output voltage ringing during load and line transient.

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The SGM6614 operates from a wide 2.17V to 18V input voltage. If the input supply source is located far away from the device, an electrolytic or tantalum capacitor of 47μF is recommended to damp the wiring inductance.

Layout Considerations

In addition to component selection, layout is a critical step to ensure the performance of switch mode power supplies. Poor layout could result in system instability, EMI failure, and device damage. Thus, place the inductor, input and output capacitors as close to the IC as possible, and use wide and short traces for current carrying traces to minimize PCB inductance.

For Boost converter, the current loop of output capacitor from VOUT pin back to the GND pin of the device should be as small as possible. The traces connected to SW node should be as short as possible. A ground plane underneath the SGM6614 is recommended to minimize interplane coupling.

Due to the high power density of SGM6614, the current-carrying SW, VOUT and PGND pins should be connected with large copper polygon pour to ensure good thermal performance, and thermal vias on these nodes are recommended.

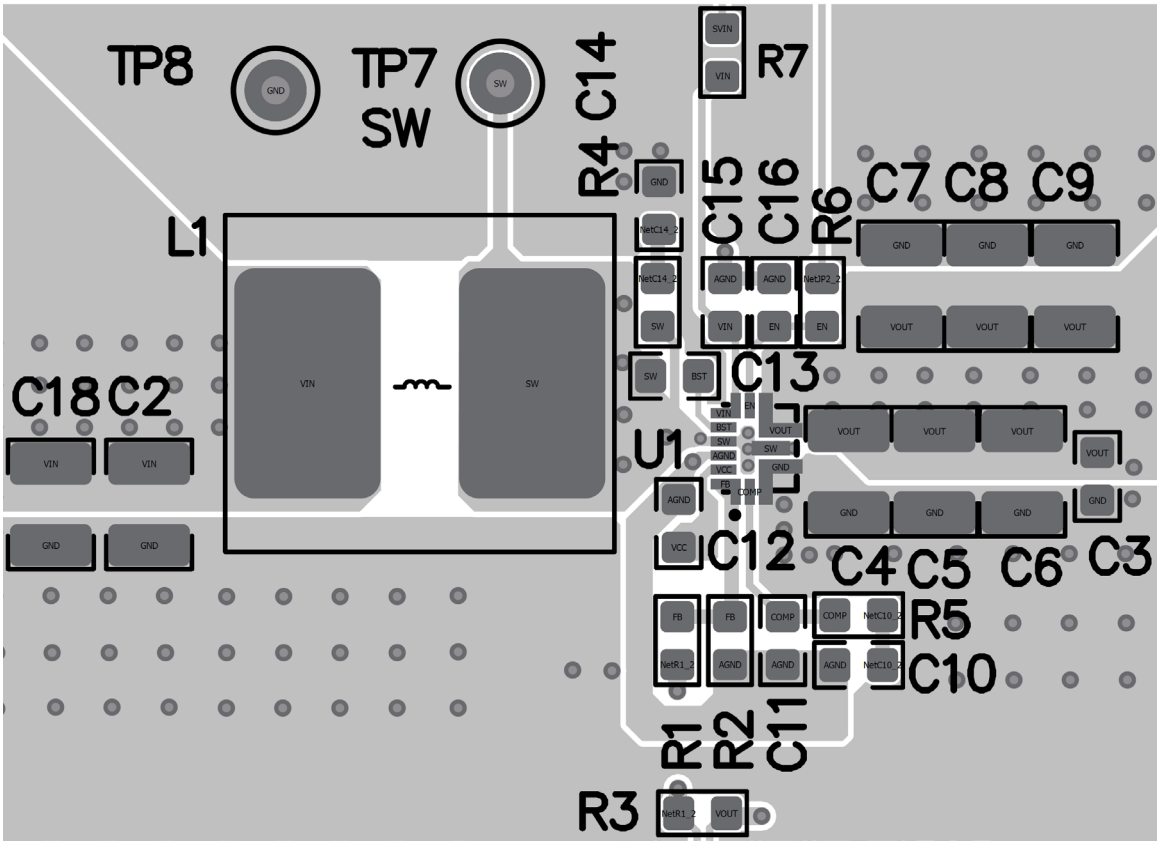


Figure 5. PCB Layout Reference

REVISION HISTORY

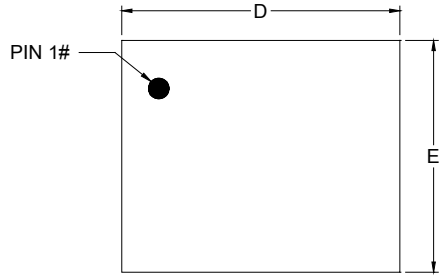
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

AUGUST 2024 – REV.A to REV.A.1	Page
Changed V_{IN} conditions of Output Voltage vs. Output Current curves from 3.0V to 3.6V	5

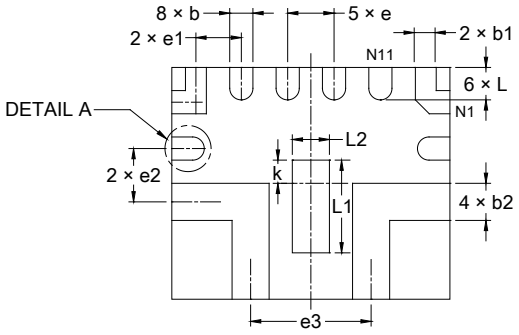
Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

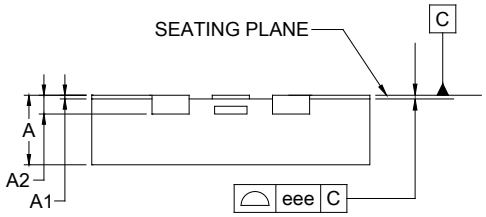
TQFN-3×2.5-11L



TOP VIEW

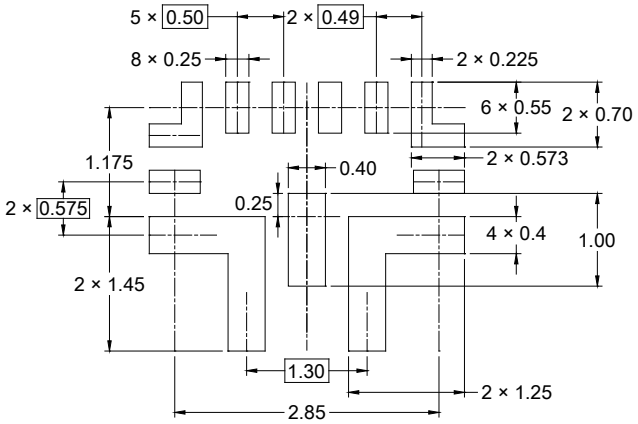


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



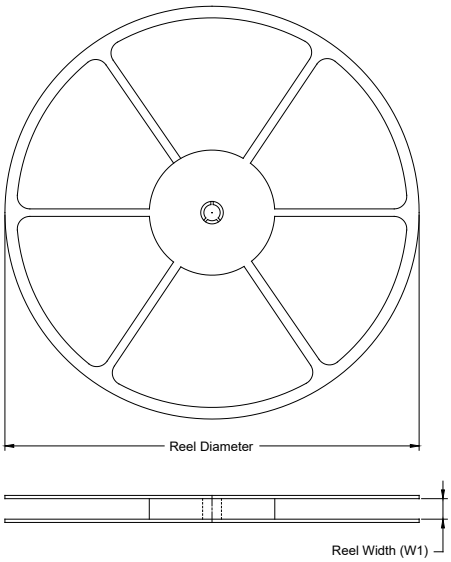
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
b1	0.175	-	0.275
b2	0.350	-	0.450
D	2.900	-	3.100
E	2.400	-	2.600
e		0.500 BSC	
e1		0.490 BSC	
e2		0.575 BSC	
e3		1.300 BSC	
k		0.250 REF	
L	0.250	-	0.450
L1	0.900	-	1.100
L2	0.300	-	0.500
eee		0.080	

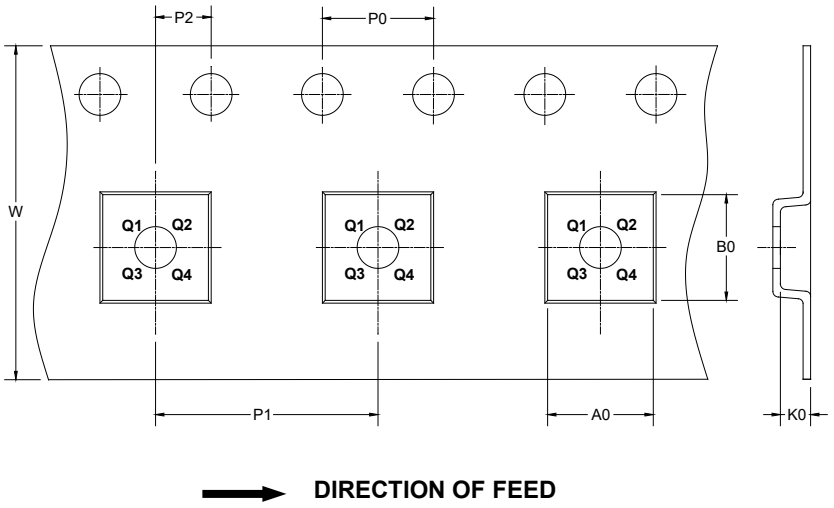
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



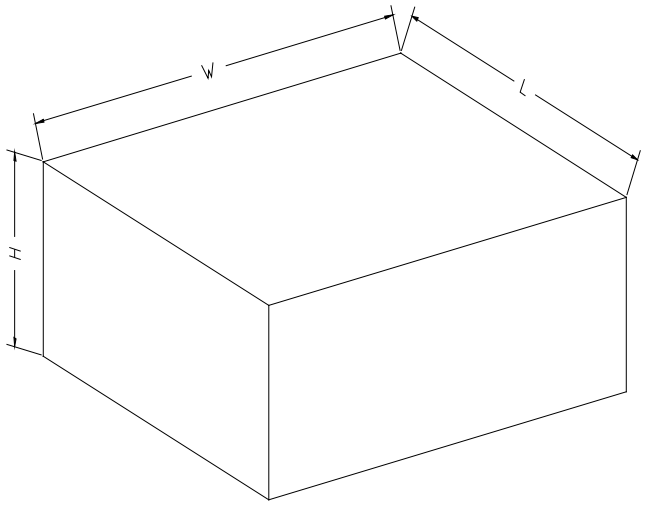
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×2.5-11L	13"	12.4	2.80	3.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002