SGM2535
2.7V to 18V eFuse with True Reverse Blocking and Multiple Protection Modes

GENERAL DESCRIPTION

The SGM2535 is a compact and rich power management eFuse power switch with a full range of protection functions. SGM2535A/AL has a low power sleep mode in compliance with the SATA device sleep standard. SGM2535B/BL provides a Diode Mode which is useful for ORing operation. Due to the wide device operating range, numerous basic DC bus voltages can be controlled by the device. Since integrated back-to-back FETs enable bidirectional current regulation, the device is highly suitable for systems whose load side hold-up energy must not flow reversely to the failed power side.

Many programmed features like load, source, and device safety are included, such as over-current, SS ramp, and over-voltage and under-voltage thresholds. PG, nFAULT, and precise current monitor output are provided by the device for system status monitoring and downstream load control. SSD power management design is simplified by precise programmable under-voltage, over-voltage thresholds and the low I_Q device sleep mode (SGM2535A/AL).

The device monitors V_{IN} and V_{OUT} to provide true reverse current blocking when V_{IN} < V_{OUT} - 10mV. In systems where the backup voltage is higher than the bus voltage, this function enables faster change to a boosted voltage rail.

The SGM2535 is available in a Green TQFN-3×4-20L package.

TYPICAL APPLICATION

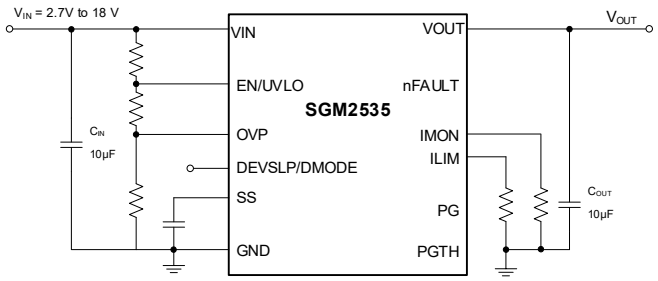


Figure 1. Typical Application Circuit

FEATURES

- **Wide Input Voltage Range from 2.7V to 18V with Surge up to 20V**
- **Low On-Resistance: 34mΩ (TYP)**
- **Adjustable Current Limit from 0.6A to 5.3A (±9%)**
- **Current Monitor (IMON) Output (±8%)**
- **Operating I_Q: 133µA (TYP)**
- **Device Sleep Mode I_Q (SGM2535A/AL Only): 103µA (TYP)**
- **Disabled I_Q: 3.9µA (TYP)**
- **±2.3% Over-Voltage, Under-Voltage Threshold**
- **Reverse Current Blocking**
- **1.8µs Reverse Voltage Shut-Off**
- **Programmable SS Control**
- **State Indicators: Power Good and Fault**
- **Options:**
  - **SGM2535A: Auto-Retry (Device Sleep Mode)**
  - **SGM2535AL: Latch-Off (Device Sleep Mode)**
  - **SGM2535B: Auto-Retry (Diode Mode)**
  - **SGM2535BL: Latch-Off (Diode Mode)**
- **Available in a Green TQFN-3×4-20L Package**

APPLICATIONS

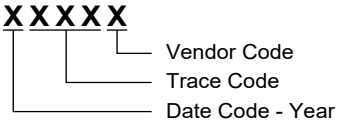
PCI-E/SATA/SAS HDD and SSD Drives
Enterprise and Micro Servers
Smart Load Switch
Set-Top-Box (STB), DTVs and Game Consoles
RAID Cards – Hold-up Power Management
Telecom Switches and Routers
Adapter Powered Devices

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2535A	TQFN-3×4-20L	-40℃ to +125℃	SGM2535AXTSF20G/TR	SGM 2535ATSF XXXXX	Tape and Reel, 4000
SGM2535AL	TQFN-3×4-20L	-40℃ to +125℃	SGM2535ALXTSF20G/TR	SGM 08ZTSF XXXXX	Tape and Reel, 4000
SGM2535B	TQFN-3×4-20L	-40℃ to +125℃	SGM2535BXTSF20G/TR	SGM 2535BTSF XXXXX	Tape and Reel, 4000
SGM2535BL	TQFN-3×4-20L	-40℃ to +125℃	SGM2535BLXTSF20G/TR	SGM 1HITSF XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range
- PG, PGTH, VOUT, VIN, EN/UVLO ..... -0.3V to 20V
- OVP, DEVSLP/DOMDE, nFAULT ..... -0.3V to 20V
- VIN (10ms Transient) 22V
- SS, ILIM ..... Internally Limited
- IMON ..... -0.3V to 7V

Sink Current, PG, nFAULT, SS 10mA
Source Current, SS, ILIM, IMON ..... Internally Limited
Package Thermal Resistance
- TQFN-3×4-20L, θ_{JA} ..... 38.8℃/W
- TQFN-3×4-20L, θ_{JB} ..... 13.3℃/W
- TQFN-3×4-20L, $\theta_{JC\ (TOP)}$ ..... 38℃/W
- TQFN-3×4-20L, $\theta_{JC\ (BOT)}$ ..... 5.5℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range
- VIN ..... 2.7V to 18V
- EN/UVLO, OVP, DEVSLP/DMODE ..... 0V to 18V
- VOUT, PGTH, PG, nFAULT ..... 0V to 18V
- SS, ILIM ..... Internally Limited
- IMON ..... 0V to 4.5V

Resistance
- ILIM ..... 16.9kΩ to 150kΩ
- IMON ..... > 1kΩ

External Capacitance
- OUT ..... > 10μF
- SS ..... < 470nF

Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

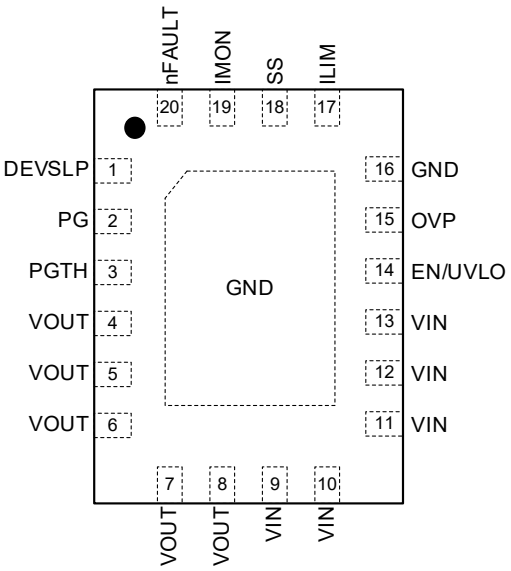
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

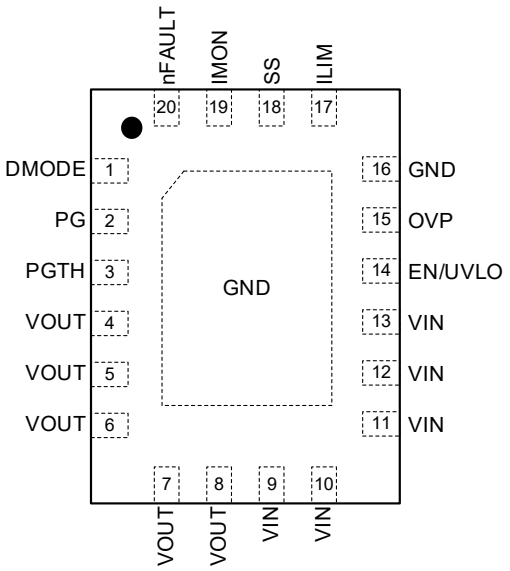
PIN CONFIGURATIONS

SGM2535A/AL (TOP VIEW)



TQFN-3×4-20L

SGM2535B/BL (TOP VIEW)



TQFN-3×4-20L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	DEVSLP	SGM2535A/AL: Active-High Device Sleep Mode Control. Setting this pin high activates the device sleep mode (low power mode).
	DMODE	SGM2535B/BL: Diode Mode Control Pin. Set this pin high to activate the non-ideal diode mode.
2	PG	Open-Drain Output Pin. Active-High. Setting this pin high indicates PGTH has crossed the threshold value.
3	PGTH	PG Comparator Positive Input Pin.
4, 5, 6, 7, 8	VOUT	Power Output Pin.
9, 10, 11, 12, 13	VIN	Power Input and Supply Voltage Pin.
14	EN/UVLO	Input for setting the Under-Voltage Lockout Threshold. An under-voltage event will turn off the internal FET and assert nFAULT to signal power-failure. When pull this pin to GND, the fault latched in the device is reset. Do not leave this pin floating.
15	OVP	Input for Setting Programmable Over-Voltage Protection Threshold. An over-voltage event will turn off the internal FET and assert nFAULT to signal over-voltage.
16	GND	Ground.
17	ILIM	Current Limit Programming Pin. Overload and short-circuit current limit are set by the resistor from this pin to GND.
18	SS	Soft-Start Pin. The output slew rate is set by the capacitor from this pin to GND.
19	IMON	Current Monitor pin. The sourcing current of this pin is proportional to the FET current. Placing a resistor from this pin to GND transforms the current to voltage signal.
20	nFAULT	Open-Drain Output Pin. This pin functions as a fault event indicator which goes low to indicate fault condition because of under-voltage, over-voltage, reverse voltage and thermal shutdown.
Exposed Pad	GND	The GND terminal must be connected to the exposed pad, which needs to be connected through numerous vias to a PCB ground plane for effective thermal performance.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 2.7V to 18V, $V_{EN/UVLO}$ = 2V, V_{OVP} = V_{DEVSLP} = V_{PGTH} = V_{DMODE} = 0V, R_{ILIM} = 150kΩ, C_{OUT} = 1μF, C_{SS} = open, PG = nFAULT = IMON = open. Positive current into terminals, all voltages are referenced to GND, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage and Internal Under-Voltage Lockout							
Operating Input Voltage	V_{IN}			2.7		18	V
Internal UVLO Threshold, Rising	V_{UVR}				2.4	2.5	V
Internal UVLO Hysteresis	V_{UVR_HYS}	SGM2535A/AL			186	250	mV
		SGM2535B/BL			186	251	
Supply Current, Enabled	I_{Q_ON}	$V_{EN/UVLO}$ = 2V, V_{IN} = 2.7V	SGM2535A/AL	70	120	170	μA
			SGM2535B/BL	77	120	163	
		$V_{EN/UVLO}$ = 2V, V_{IN} = 12V	SGM2535A/AL	80	133	190	
			SGM2535B/BL	84	133	181	
		$V_{EN/UVLO}$ = 2V, V_{IN} = 18V	SGM2535A/AL	80	135	190	
			SGM2535B/BL	85	135	184	
Supply Current, Disabled	I_{Q_OFF}	$V_{EN/UVLO}$ = 0V	V_{IN} = 2.7V		1.0	3.0	μA
			V_{IN} = 12V		3.9	8.5	
			V_{IN} = 18V		5.7	12.5	
Supply Current, Device Sleep Mode	I_{Q_DEVSLP}	V_{DEVSLP} = 0V, V_{IN} = 2.7V to 18V, SGM2535A/AL		50	103	155	μA
Enable and Under-Voltage Lockout (EN/UVLO) Input							
EN/UVLO Threshold Voltage, Rising	V_{ENR}			0.965	0.990	1.015	V
EN/UVLO Threshold Voltage, Falling	V_{ENF}			0.895	0.920	0.940	V
EN Threshold Voltage for Low I_Q Shutdown, Falling	V_{SHUTF}			0.29	0.46	0.62	V
EN Hysteresis for Low I_Q Shutdown, Hysteresis (1)	V_{SHUTF_HYS}				41		mV
EN Input Leakage Current	I_{EN}	$V_{EN/UVLO}$ = 0V to 12V		-100	0	100	nA
Over-Voltage Protection (OVP) Input							
Over-Voltage Threshold Voltage, Rising	V_{OVPR}			0.965	0.990	1.015	V
Over-Voltage Threshold Voltage, Falling	V_{OVPF}			0.880	0.920	0.960	V
OVP Input Leakage Current	I_{OVP}	V_{OVP} = 0V to 5V		-150	0	150	nA
Device Sleep Mode Input (DEVSLP): Active-High (SGM253A/AL)							
DEVSLP Threshold Voltage, Rising	$V_{DEVSLPR}$			1.75	1.82	1.89	V
DEVSLP Threshold Voltage, Falling	$V_{DEVSLPF}$			0.93	0.99	1.04	V
DEVSLP Input Leakage Current	I_{DEVSLP}	V_{DEVSLP} = 12V		0.51	1	1.75	μA
Diode Mode Input (DMODE): Active-High (SGM253B/BL)							
DMODE Threshold Voltage, Rising	V_{DMODER}			1.75	1.82	1.89	V
DMODE Threshold Voltage, Falling	V_{DMODEF}			0.93	0.99	1.04	V
DMODE Input Leakage Current	I_{DMODE}	V_{DMODE} = 12V		0.51	1	1.75	μA
Output Ramp Control (SS)							
SS Charging Current	I_{SS}	V_{SS} = 0V, V_{IN} = 12V		0.7	1	1.2	μA
SS Discharging Resistance	R_{SS}	$V_{EN/UVLO}$ = 0V, I_{SS} = 10mA sinking			20	42	Ω
SS Maximum Capacitor Voltage	V_{SS_MAX}			2.52	2.64	2.77	V
SS to VOUT Gain	$GAIN_{SS}$	V_{IN} = 12V, $\Delta V_{OUT}/\Delta V_{SS}$		11.90	12.08	12.27	V/V
Current Limit Programming (ILIM)							
ILIM Bias Voltage	V_{ILIM}				0.89		V

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 2.7V to 18V, $V_{EN/UVLO}$ = 2V, V_{OVP} = V_{DEVSLP} = V_{PGTH} = 0V, R_{ILIM} = 150kΩ, C_{OUT} = 1μF, C_{SS} = open, PG = nFAULT = IMON = open. Positive current into terminals, all voltages are referenced to GND, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current Limit (2)	I_{LIM}	V_{IN} - V_{OUT} = 1V	R_{ILIM} = 150kΩ	0.53	0.59	0.63	A
			R_{ILIM} = 88.7kΩ	0.89	0.98	1.07	
			R_{ILIM} = 42.2kΩ	1.91	2.06	2.25	
			R_{ILIM} = 24.9kΩ	3.25	3.50	3.81	
			R_{ILIM} = 16.9kΩ	4.78	5.17	5.62	
		R_{ILIM} = open, open resistor current limit (Single Point Failure Test: UL60950)		0.3	0.44	0.57	
		R_{ILIM} = short, shorted resistor current limit (Single Point Failure Test: UL60950)		0.44	0.60	0.76	
Device Sleep Mode Current Limit	I_{DEVSLP_LIM}	SGM2535A/AL		0.43	0.60	0.76	A
DMODE Current Limit	I_{DMODE_LIM}	DMODE = high, non-ideal diode mode, SGM2535B/BL		0.47 × I_{LIM}			A
Short-Circuit Current Limit (2)	I_{OS}	V_{IN} = 12V, V_{IN} - V_{OUT} = 5V, R_{ILIM} = 42.2kΩ		1.79	2.05	2.32	A
		V_{IN} = 12V, V_{IN} - V_{OUT} = 5V, T_J = -40℃ to +85℃	R_{ILIM} = 24.9kΩ	3.08	3.45	3.81	
			R_{ILIM} = 16.9kΩ	4.66	5.09	5.52	
Fast-Trip Comparator Threshold (1) (2)	I_{FAST_TRIP}			1.5 × I_{LIM} + 0.3			A
Current Monitor Output (IMON)							
Gain Factor I_{IMON}: I_{OUT}	$GAIN_{IMON}$	I_{OUT} = 1A to 4A		48.1	52.3	57.2	μA/A
Power Switch							
On-Resistance	R_{ON}	I_{OUT} = 1A to 4A	T_J = +25℃	28	34	40	mΩ
			T_J = -40℃ to +85℃	19	34	50	
			T_J = -40℃ to +125℃		34	56	
Pass FET Output (OUT)							
OUT Leakage Current in Off-State	I_{LKG_OUT}	V_{IN} = 18V, $V_{EN/UVLO}$ = 0V, V_{OUT} = 0V sourcing		-9	-2	-1	μA
		V_{IN} = 2.7V, $V_{EN/UVLO}$ = 0V, V_{OUT} = 18V sinking		6	16	26	
V_{IN} - V_{OUT} Threshold for Reverse Protection Comparator, Falling	V_{REVTH}			-19	-11	-2	mV
V_{IN} - V_{OUT} Threshold for Reverse Protection Comparator, Rising	V_{FWDTH}			46	105	164	mV
Fault Flag (nFAULT): Active-Low							
nFAULT Internal Pull-Down Resistance	R_{nFAULT}	V_{OVP} = 2V, I_{nFAULT} = 5mA sinking			20	48	Ω
nFAULT Input Leakage Current	I_{nFAULT}	V_{nFAULT} = 0V to 18V		-200	0	200	nA
Positive Input for Power Good Comparator (PGTH)							
PGTH Threshold Voltage, Rising	V_{PGTHR}			0.965	0.990	1.015	V
PGTH Threshold Voltage, Falling	V_{PGTHF}			0.895	0.920	0.940	V
PGTH Input Leakage Current	I_{PGTH}	V_{PGTH} = 0V to 18V		-200	0	200	nA
Power Good Comparator Output (PG): Active-High							
PG Internal Pull-Down Resistance	R_{PG}	V_{PGTH} = 0V, I_{PG} = 5mA sinking			20	48	Ω
PG Input Leakage Current	I_{PG}	V_{PG} = 0V to 18V		-100	0	100	nA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 2.7V to 18V, $V_{EN/UVLO}$ = 2V, V_{OVP} = V_{DEVSLP} = V_{PGTH} = 0V, R_{ILIM} = 150kΩ, C_{OUT} = 1μF, C_{SS} = open, PG = nFAULT = IMON = open. Positive current into terminals, all voltages are referenced to GND, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown (TSD)						
TSD Threshold (1)	T_{SD}			160		℃
TSD Hysteresis (1)	T_{HYS}			20		℃

NOTES:

1. These parameters are given as a reference and are not considered part of SGMICRO's official device specifications for warranty purposes.
2. Pulse-testing methods ensure that the junction temperature remains near the ambient temperature. Thermal impacts should be considered independently.

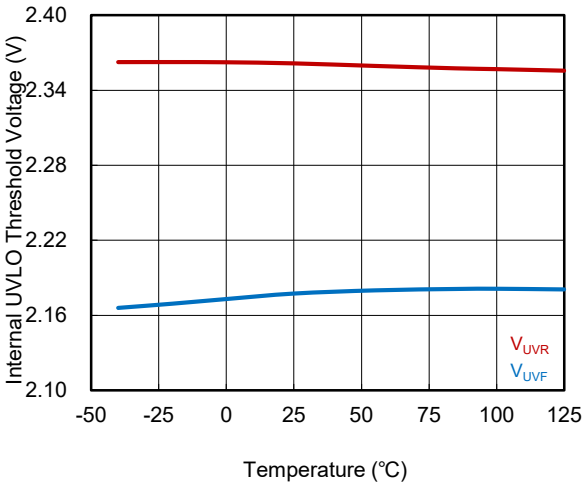
TIMING REQUIREMENTS

(T_J = -40℃ to +125℃, V_{IN} = 2.7V to 18V, $V_{EN/UVLO}$ = 2V, V_{OVP} = V_{DEVSLP} = V_{PGTH} = 0V, R_{ILIM} = 150kΩ, C_{OUT} = 1μF, C_{SS} = open, PG = nFAULT = IMON = open. Positive current into terminals, all voltages are referenced to GND, typical values are at T_J = +25℃, unless otherwise noted.)

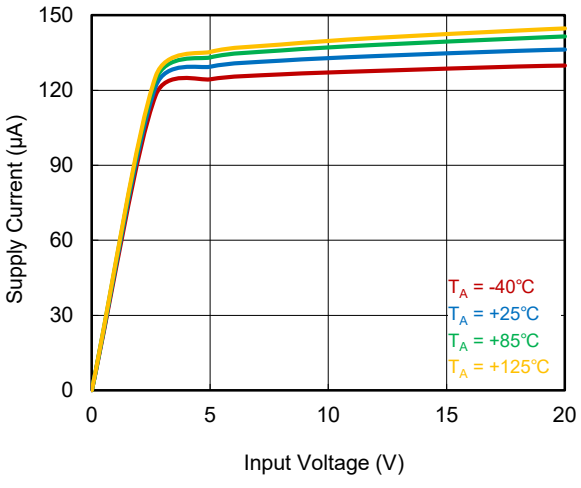
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Enable and UVLO Input							
EN Turn-On Delay	t_{ON_DLY}	EN/UVLO↑ (100mV above V_{ENR}) to V_{OUT} = 100mV, C_{SS} < 0.8nF	SGM2535A/AL		262		μs
			SGM2535B/BL		273.4		
		EN/UVLO↑ (100mV above V_{ENR}) to V_{OUT} = 100mV, C_{SS} ≥ 0.8nF, [C_{SS} in nF]		200 + 160 × C_{SS}			μs
EN Turn-Off Delay	t_{OFF_DLY}	EN/UVLO↓ (100mV below V_{ENF}) to nFAULT↓	SGM2535A/AL		1.24		μs
			SGM2535B/BL		1.3		
Over-Voltage Protection Input (OVP)							
OVP Disable Delay	t_{OVP_DLY}	OVP↑ (100mV above V_{OVPR}) to nFAULT↓			1.0		μs
Diode Mode Input: Active-High (DMODE)							
DMODE Turn-On Delay	t_{DMODE}	DMODE↓ to (V_{IN} - V_{OUT}) ≤ 200mV, with 1A resistive load at VOUT			87		μs
DMODE Turn-Off Delay		DMODE↑ to (V_{IN} - V_{OUT}) > 200mV, 1A resistive load at VOUT			11.0		
Output Ramp Control (SS)							
Output Ramp Time	t_{SS}	EN/UVLO↑ to V_{OUT} = 4.5V, with C_{SS} = open			0.36		ms
		EN/UVLO↑ to V_{OUT} = 11V, with C_{SS} = open		0.23	0.39	0.56	
		EN/UVLO↑ to V_{OUT} = 11V, with C_{SS} = 1nF			1.40		
Current Limit							
Fast-Trip Comparator Delay	$t_{FASTRIP\_DLY}$	I_{OUT} > I_{FAST_TRIP}			300		ns
Reverse Protection Comparator							
Reverse Protection Comparator Delay	t_{REV_DLY}	(V_{IN} - V_{OUT})↓ (10mV overdrive below V_{REVTH}) to nFAULT↓			1.8		μs
	t_{FWD_DLY}	(V_{IN} - V_{OUT})↑ (10mV overdrive above V_{FWDTH}) to nFAULT↑			3.7		
Power Good Comparator Output (PG): Active High							
PG Delay (De-Glitch) Time	t_{PG_R}	Rising edge, all models		0.43	0.66	0.89	ms
	t_{PG_F}	Falling edge (SGM2535A/AL)		0.43	0.66	0.89	ms
	t_{PG_F}	Falling edge (SGM2535B/BL)			2.59		ms
Thermal Shutdown (TSD)							
Retry Delay in TSD		SGM2535A/B Only			160		ms

TYPICAL PERFORMANCE CHARACTERISTICS

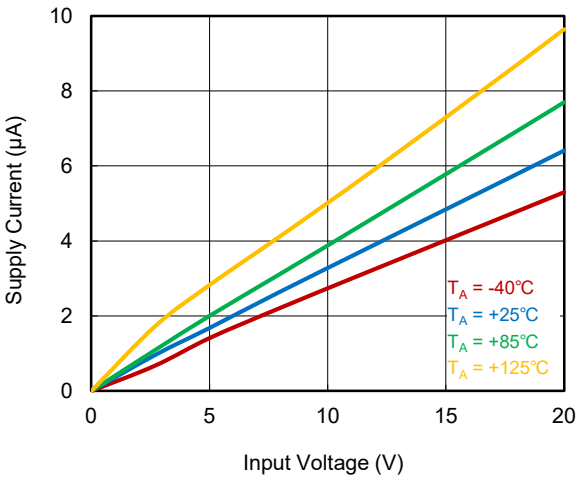
Internal UVLO Threshold Voltage vs. Temperature



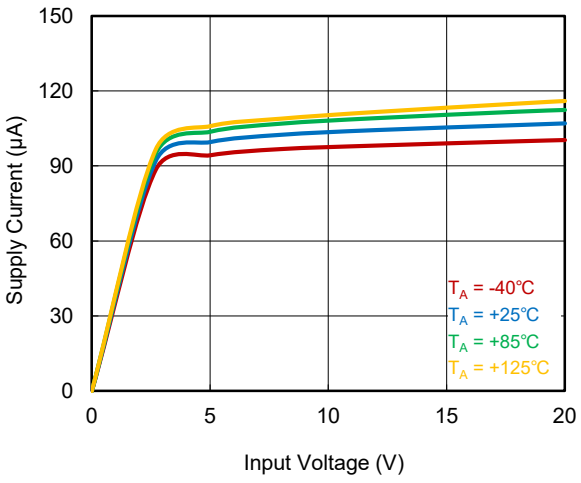
Supply Current vs. Input Voltage during Normal Operation



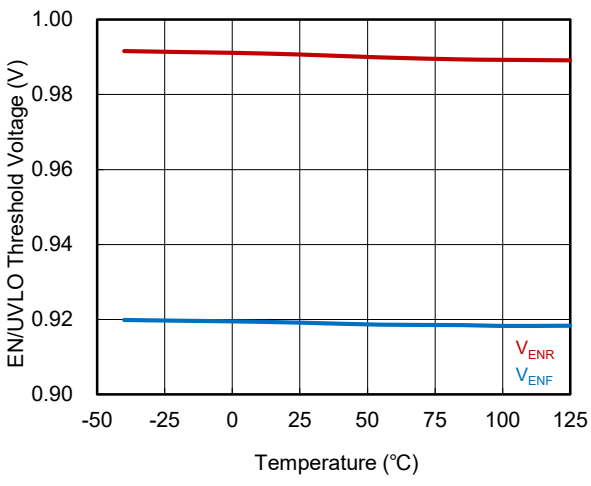
Supply Current vs. Input Voltage at Shutdown



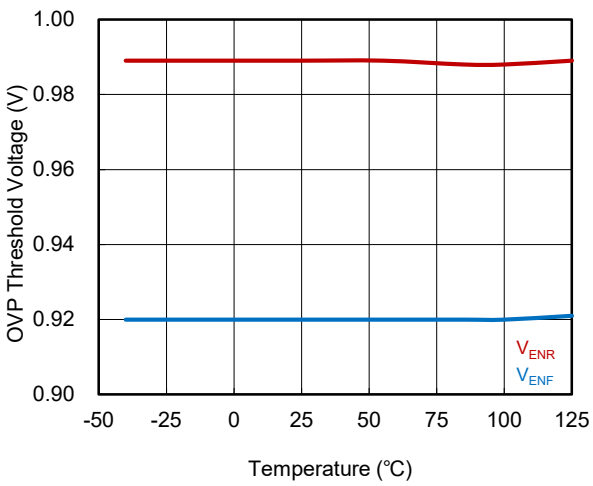
Supply Current vs. Input Voltage in DEVSLP Mode



EN/UVLO Threshold Voltage vs. Temperature

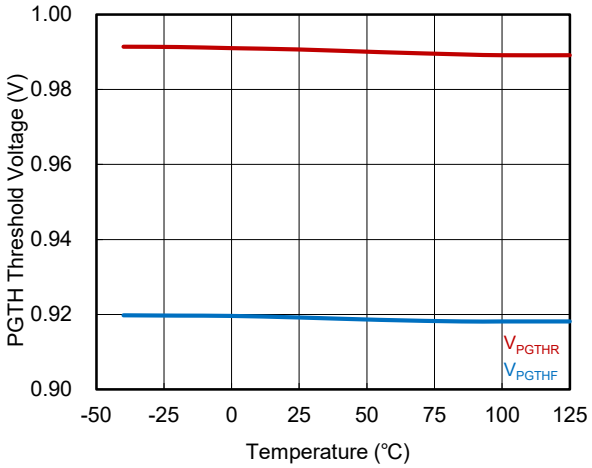


OVP Threshold Voltage vs. Temperature

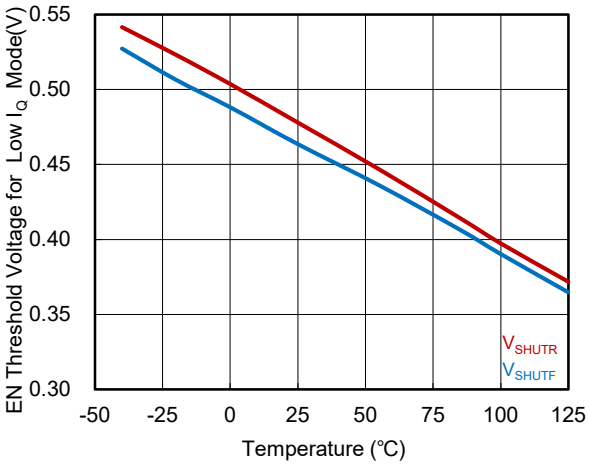


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

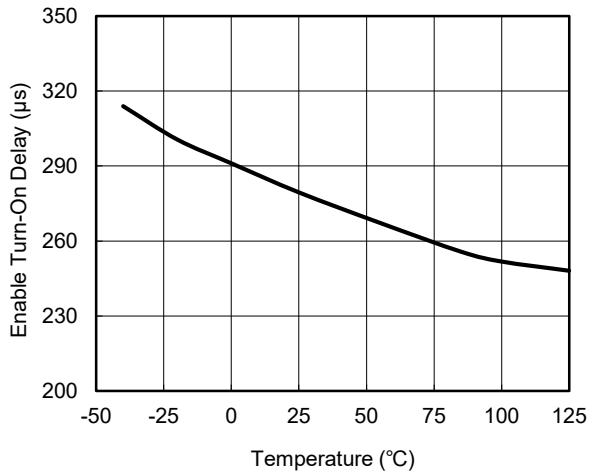
PGTH Threshold Voltage vs. Temperature



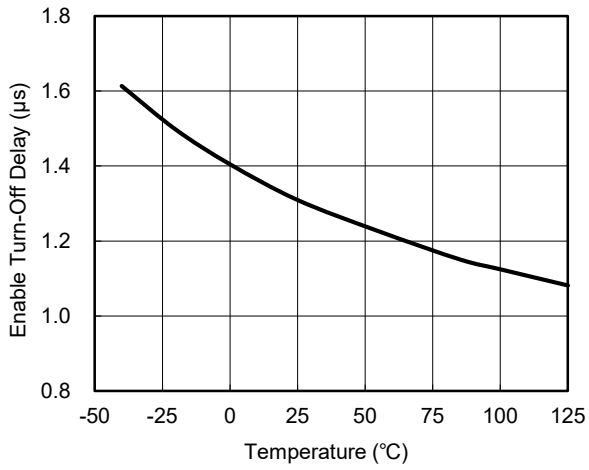
EN Threshold Voltage for Low I_Q Mode vs. Temperature



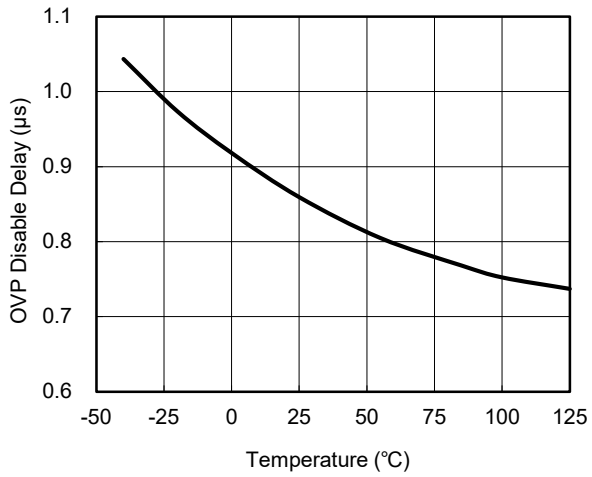
Enable Turn-On Delay vs. Temperature



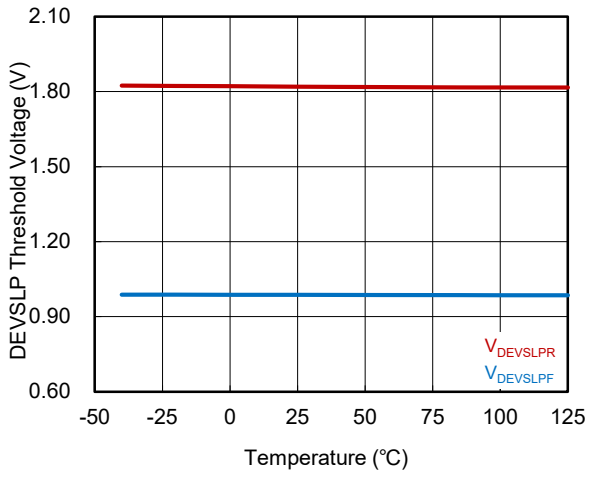
Enable Turn-Off Delay vs. Temperature



OVP Disable Delay vs. Temperature

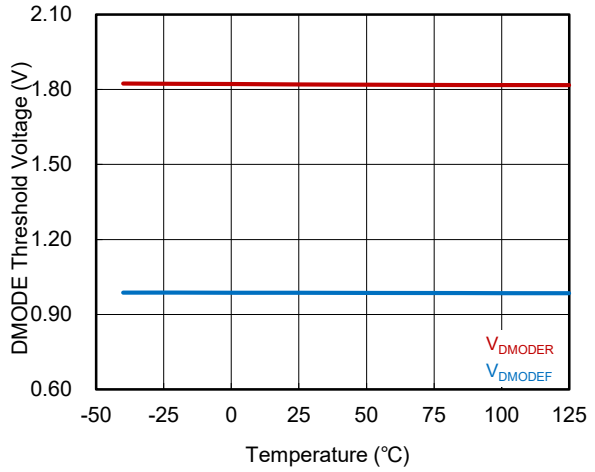


DEVSLP Threshold Voltage vs. Temperature (SGM2535A/AL)

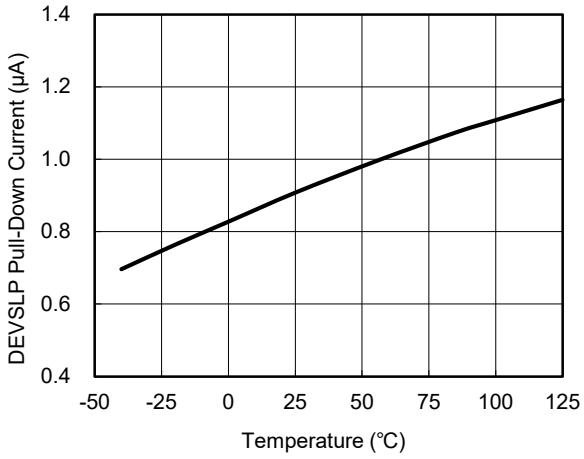


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

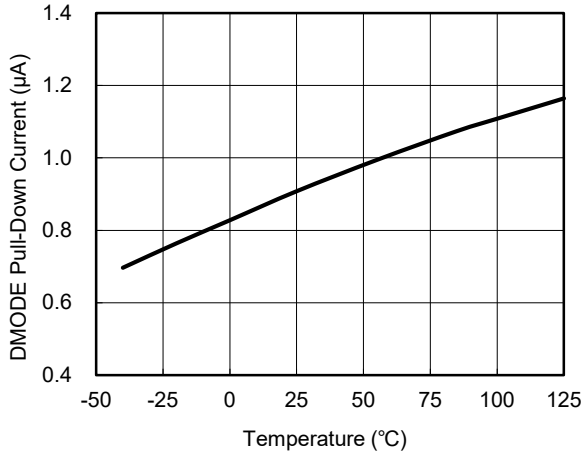
DMODE Threshold Voltage vs. Temperature (SGM2535B/BL)



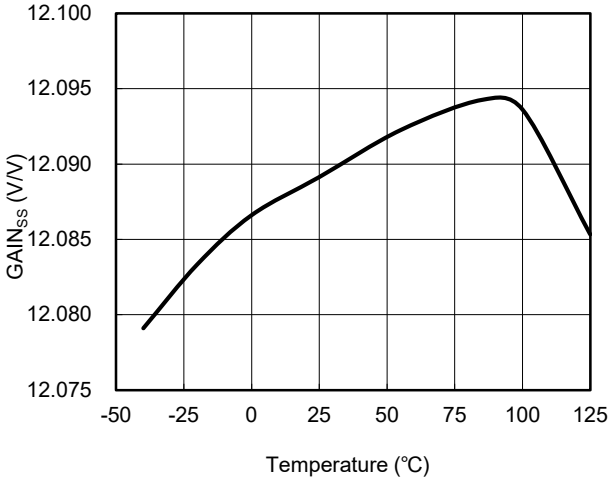
DEVSLP Pull-Down Current vs. Temperature (SGM2535A/AL)



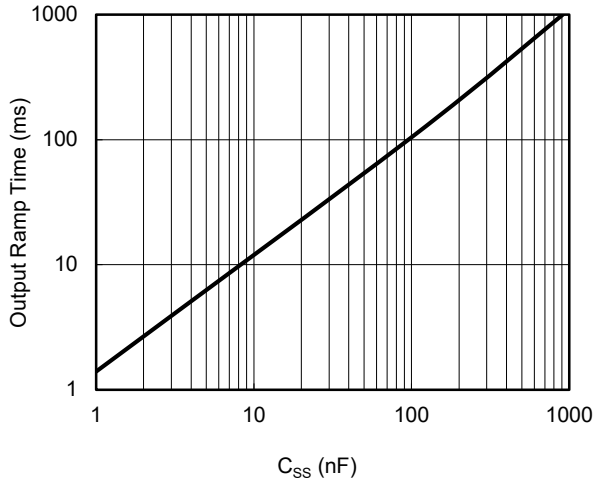
DMODE Pull-Down Current vs. Temperature (SGM2535B/BL)



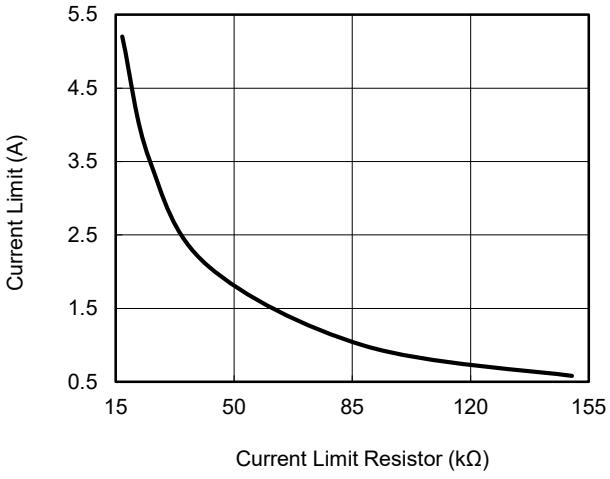
$GAIN_{SS}$ vs. Temperature



Output Ramp Time vs. C_{SS}

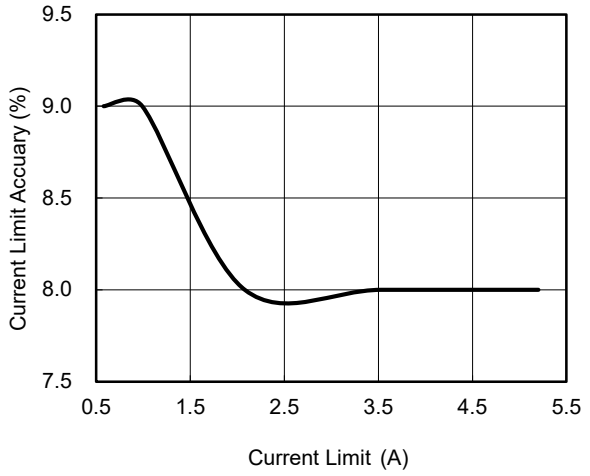


Current Limit vs. Current Limit Resistor

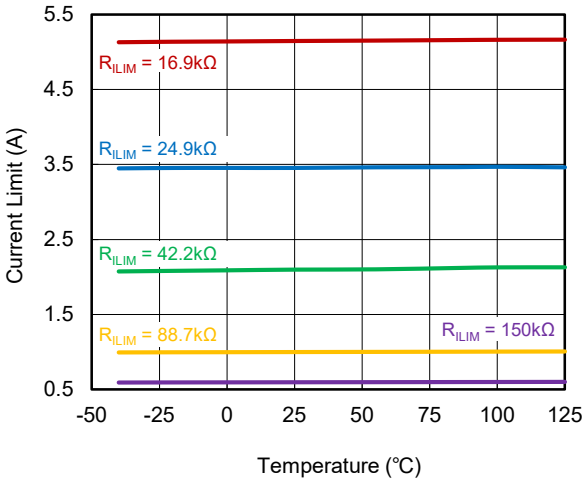


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

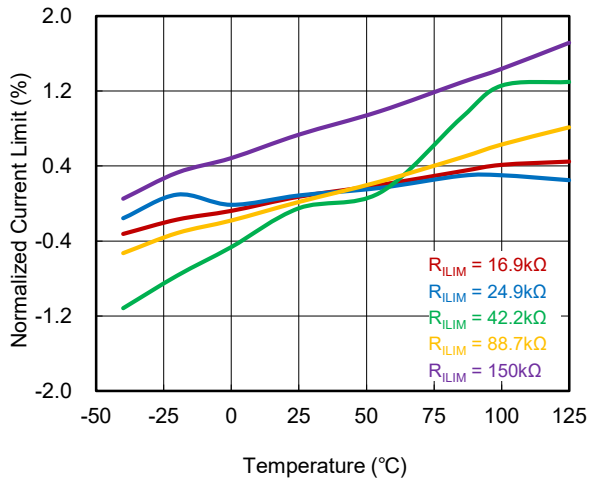
Current Limit Accuracy vs. Current Limit



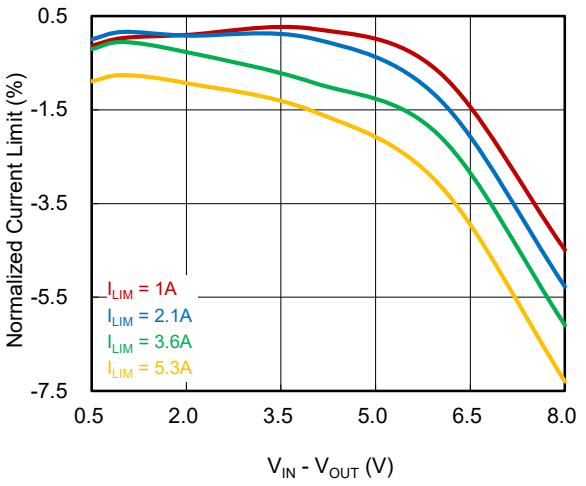
Current Limit vs. Temperature across R_{ILIM}



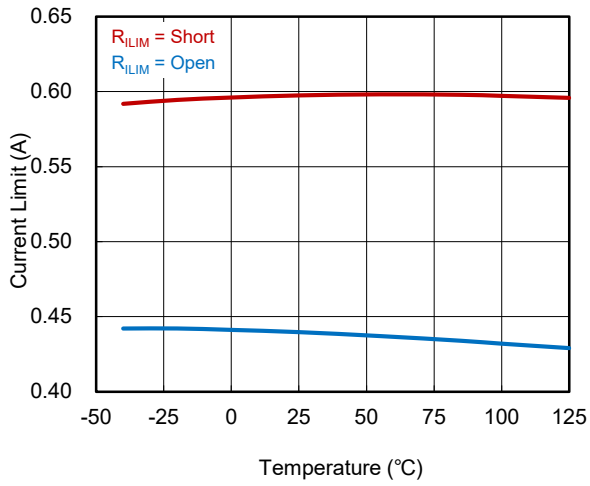
Normalized Current Limit vs. Temperature across R_{ILIM}



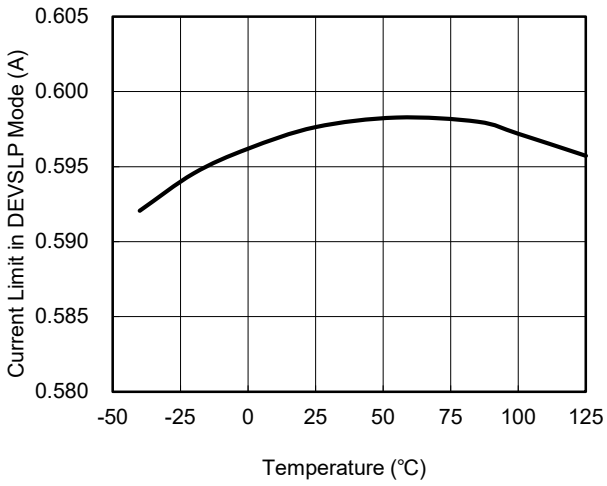
Normalized Current Limit vs. V_{IN} - V_{OUT}



Current Limit vs. Temperature

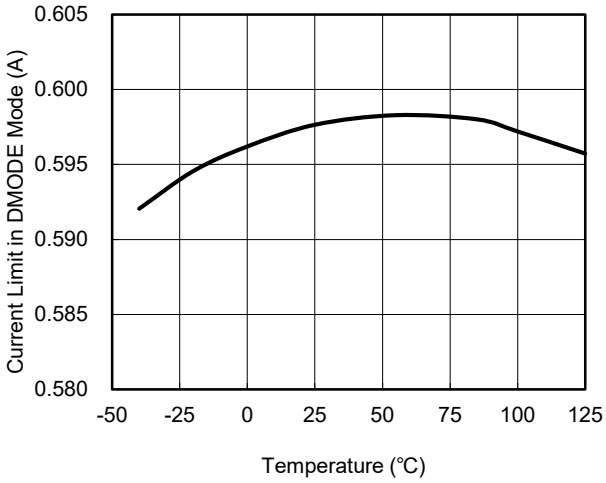


Current Limit in DEVSLP Mode vs. Temperature (SGM2535A/AL)

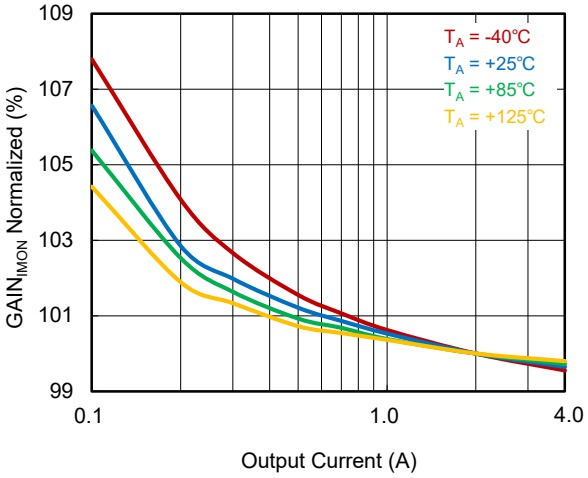


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

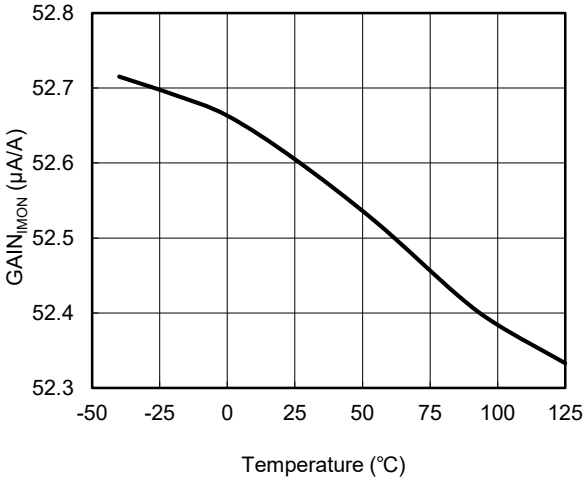
Current Limit in DMODE Mode vs. Temperature (SGM2535B/BL)



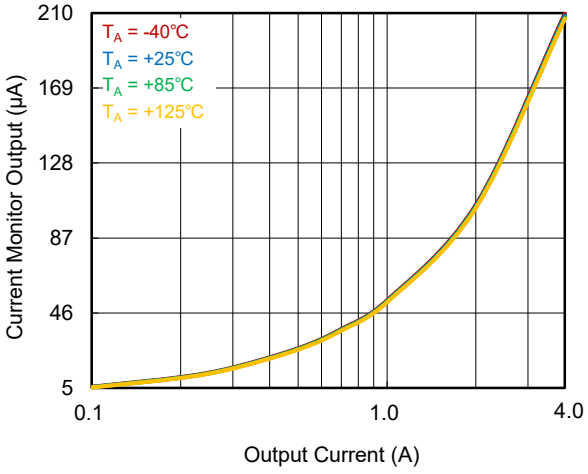
$GAIN_{IMON}$ (%) Normalized vs. Output Current



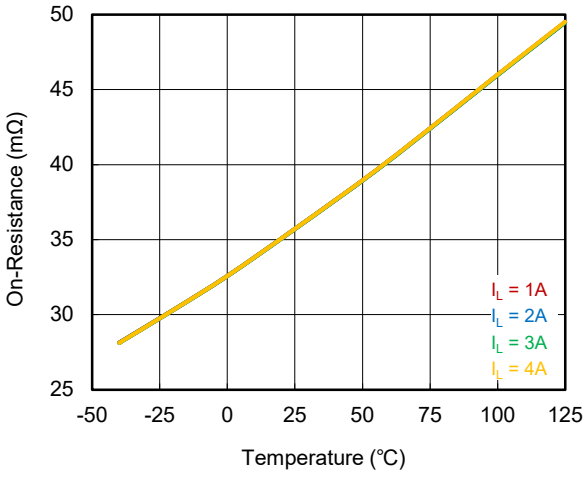
$GAIN_{IMON}$ vs. Temperature



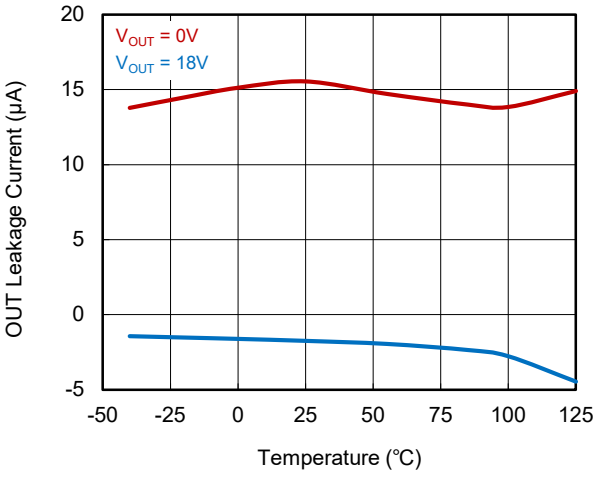
Current Monitor Output vs. Output Current



On-Resistance vs. Temperature across Load Current

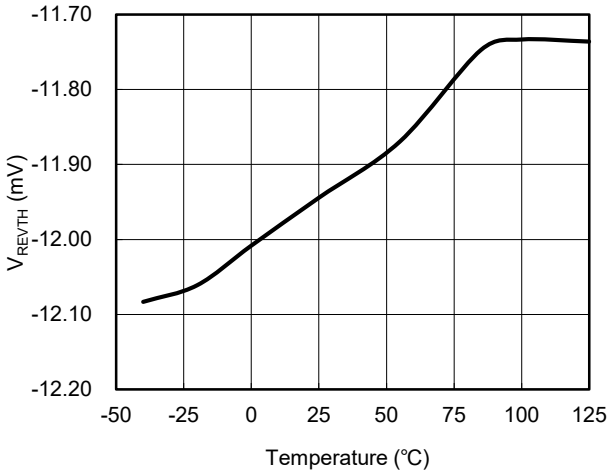


OUT Leakage Current in Off-State vs. Temperature

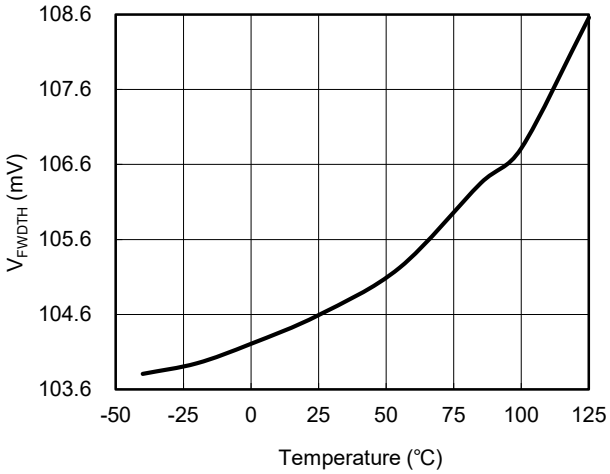


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

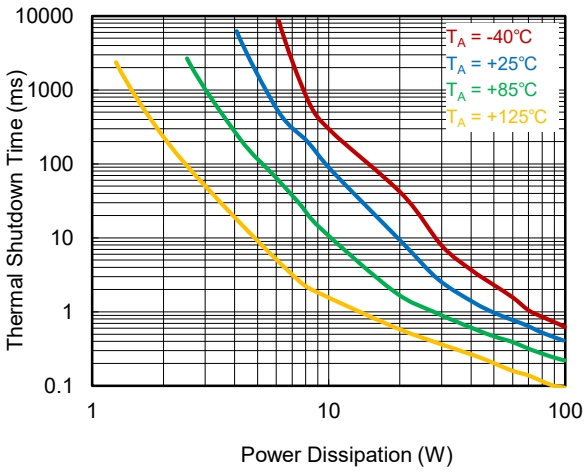
V_{REVTH} vs. Temperature



V_{FWDTH} vs. Temperature



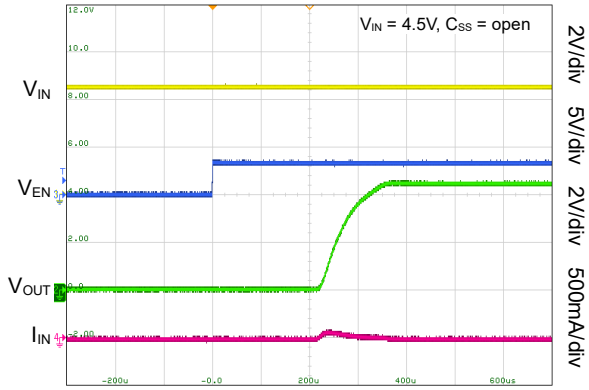
Thermal Shutdown Time vs. Power Dissipation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

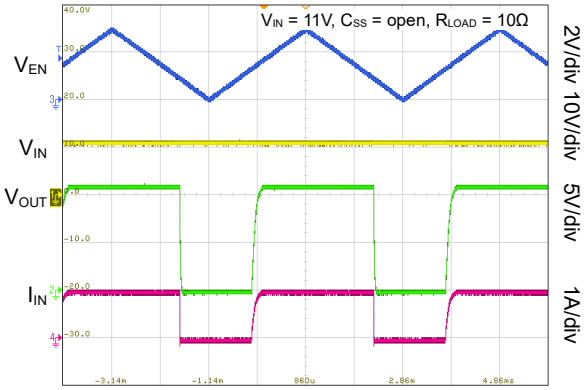
V_{IN} = 12V, C_{OUT} = 1μF, PG and nFAULT are pulled up through a 100kΩ resistor, unless otherwise noted.

Turn-On with Enable



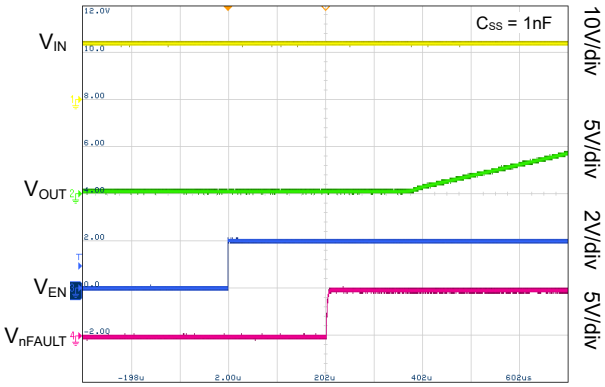
Time (100μs/div)

Turn-On and Off with Enable



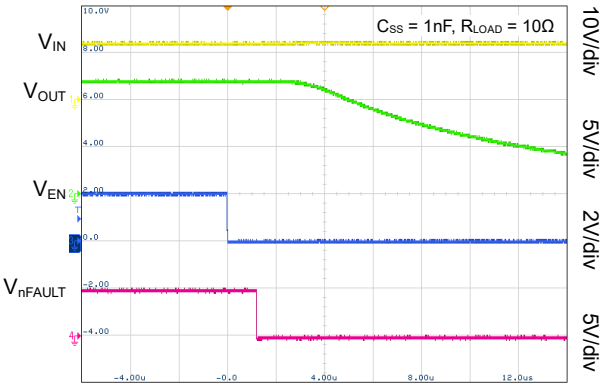
Time (1ms/div)

EN Turn-On Delay: EN↑ to Output Ramp↑



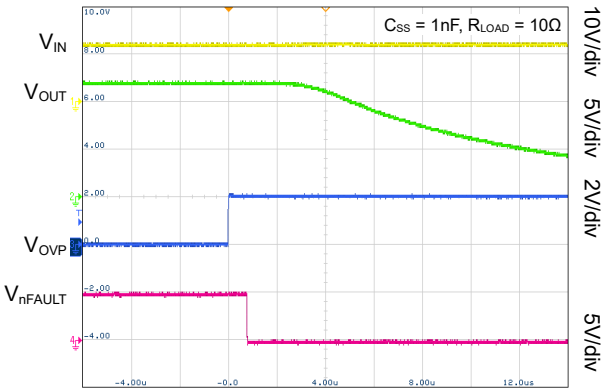
Time (100μs/div)

EN Turn-Off Delay: EN↓ to nFAULT↓



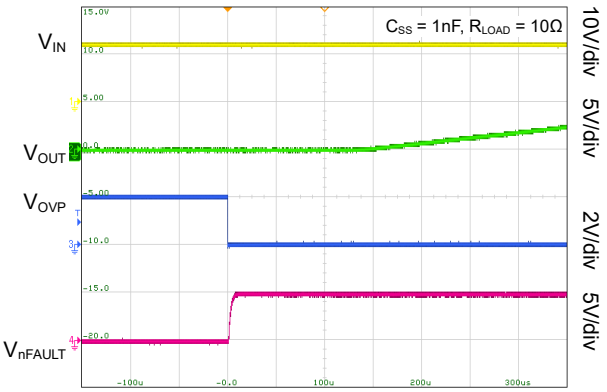
Time (2μs/div)

OVP Turn-Off Delay: OVP↑ to Fault↓



Time (2μs/div)

OVP Turn-On Delay: OVP↓ to Output Ramp↑

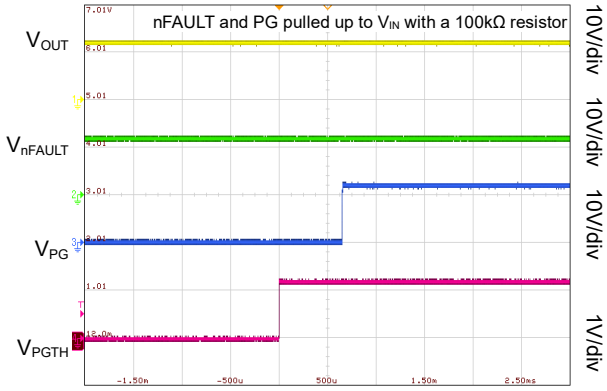


Time (50μs/div)

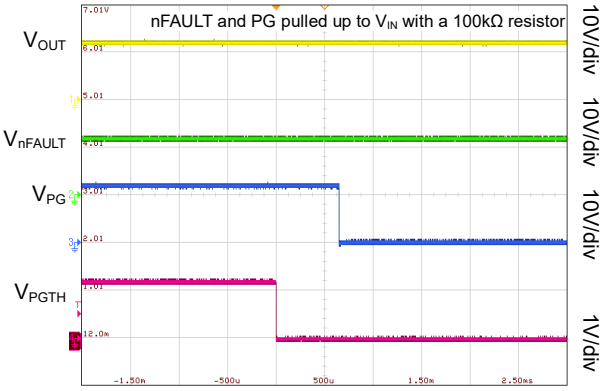
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, C_{OUT} = 1μF, PG and nFAULT are pulled up through a 100kΩ resistor, unless otherwise noted.

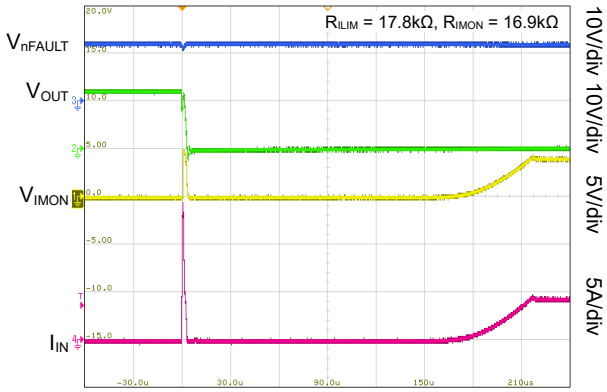
Power Good Delay (Rising)



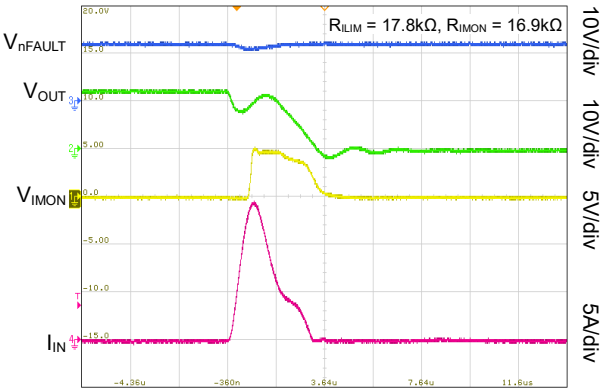
Power Good Delay (Falling)



Hot-Short: Fast-Trip Response and Current Regulation



Hot-Short: Fast-Trip Response (Zoomed)



FUNCTIONAL BLOCK DIAGRAM

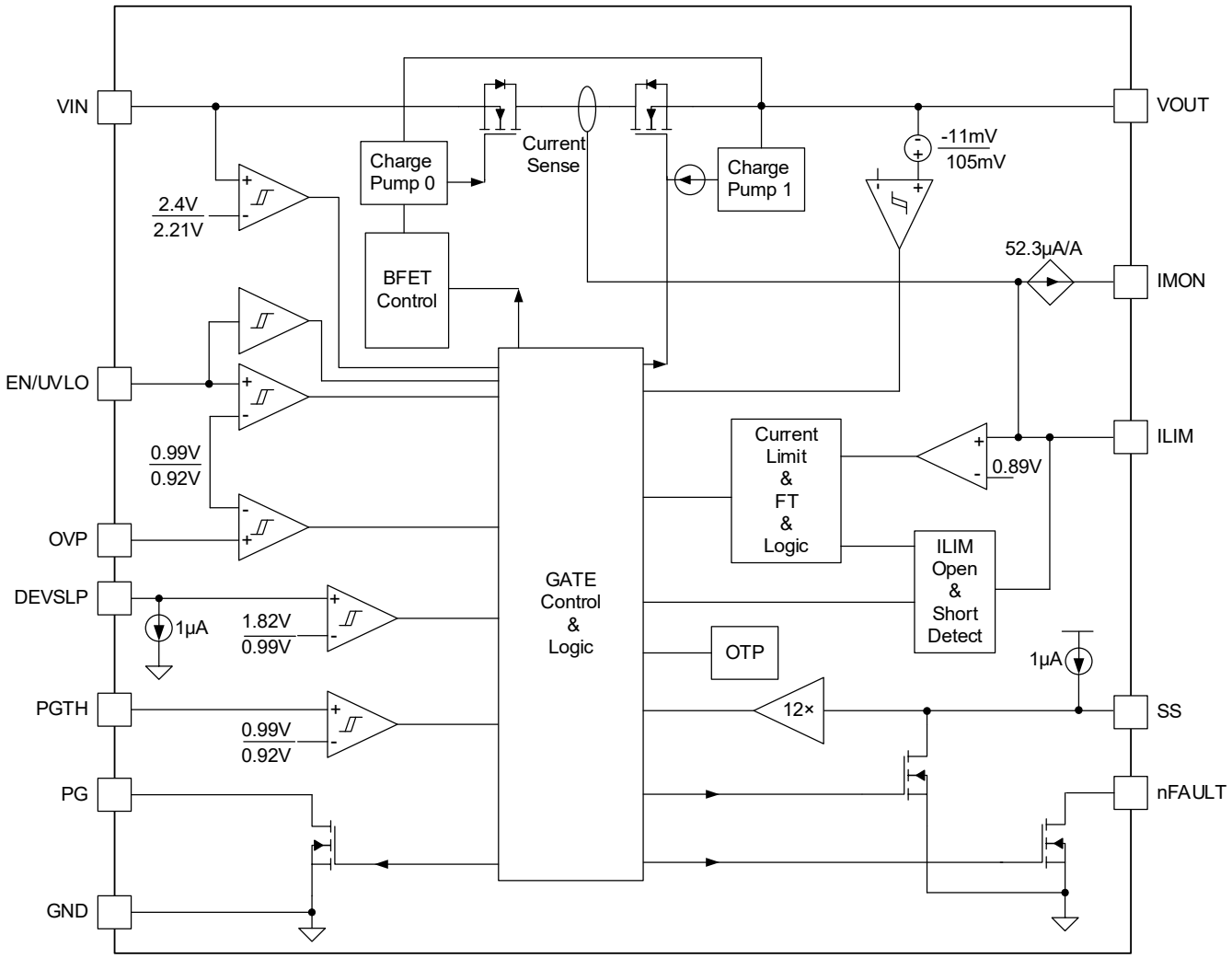


Figure 2. Block Diagram-SGM2535A/AL

FUNCTIONAL BLOCK DIAGRAM

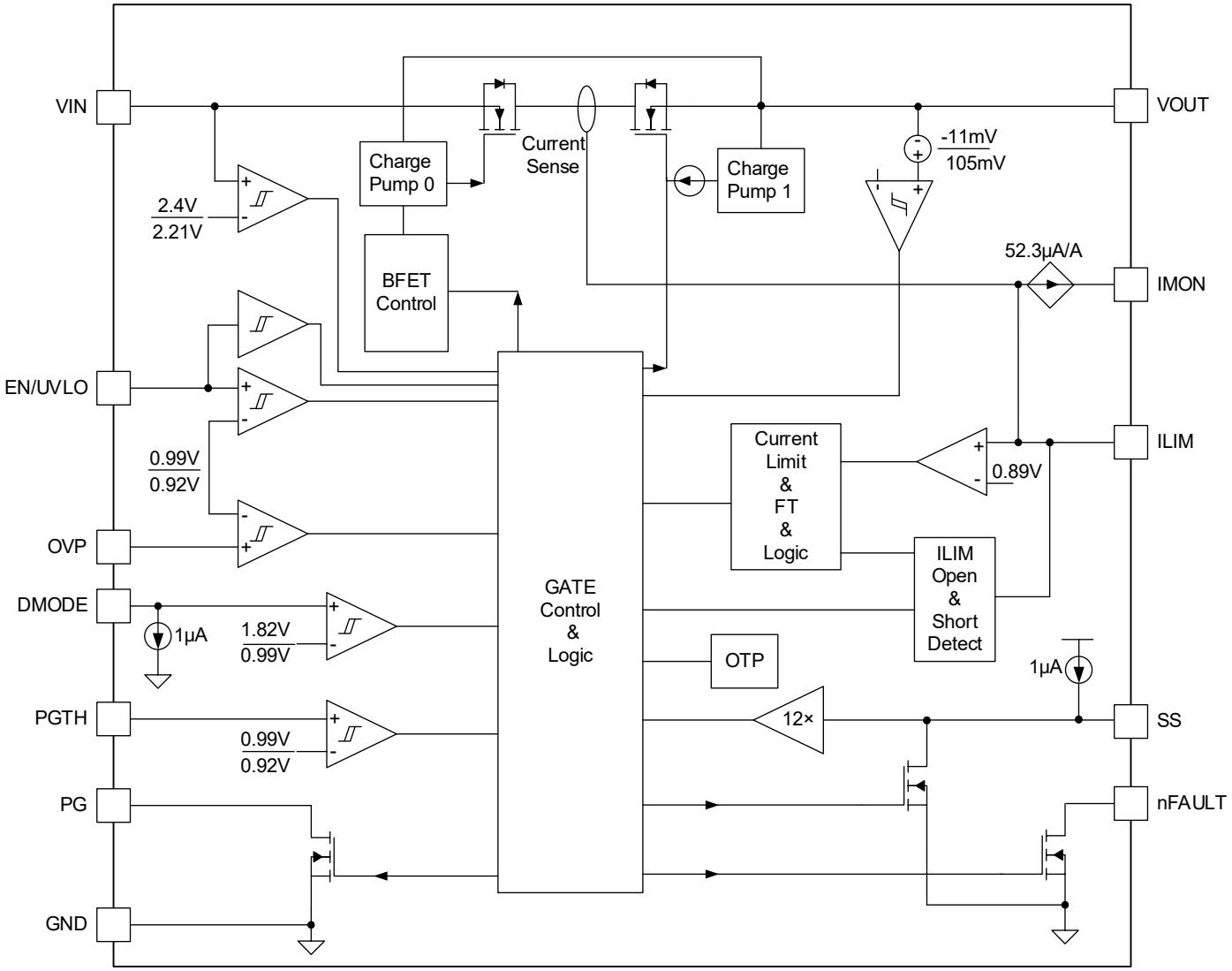


Figure 3. Block Diagram-SGM2535B/BL

DETAILED DESCRIPTION

Overview

The SGM2535 is an eFuse integrated with back-to-back FETs and a full range of protection functions. It is suitable for 2.7V to 18V power system protection applications.

For hot plug-in applications, the SGM2535 provides inrush current control through adjustable output slew rate. Besides, the part also provides over-current protection and short-circuit protection. Specifically, the adjustable over-current limit simplifies design of the power supply, and the short-circuit protection with fast response can cut off the load current rapidly once output short-circuit event is detected. The over-current limit threshold can be reset to 0.6A to 5.3A through external resistor on the ILIM pin.

The device monitors the input voltage to provide under-voltage protection and over-voltage protection. The voltage protection threshold is up to 2% which helps to supervise the bus voltage well without the need for additional voltage supervisor chip.

The device is suitable for power system protections such as Solid-State Disk (SSD) drives to avoid immediate power loss fault. The device monitors the voltage difference between input and output, namely V_{IN} - V_{OUT}, to provide reverse blocking protection against reverse current from output or input power loss condition. Besides, the part signals the controller through the state indicator pin to control power and the hold-up capacitor for data hardening.

Besides the above features, the additional features of SGM2535 include:

- Precise load current monitor.
- Power Good (PG) indicator for power rail voltage (input voltage, output voltage or any other) monitoring through the integrated comparator with precise reference.
- Over-temperature protection with thermal shutdown.
- Input power supply under-voltage and over-voltage fault reports with deglitch time.
- Available latch-off and auto-retry versions after thermal shutdown.

Feature Description

Enable and Adjusting Under-Voltage Lockout

The internal FETs of SGM2535 can be controlled by the EN/UVLO pin. When $V_{EN/UVLO}$ < V_{ENF}, the internal FETs will be turned off, and the OUT is disconnected from IN. When $V_{EN/UVLO}$ is below the shutdown threshold voltage V_{SHUTF}, the device will enter shutdown mode with the supply current I_Q less than 3.9μA to minimize power loss. Setting the EN/UVLO low and high again resets the SGM2535AL when the part is latched off due to fault.

The EN/UVLO pin has low internal deglitch delay on the falling edge to fast detect power loss fault. A higher deglitch delay can be achieved by placing an external capacitor on the EN/UVLO pin to GND.

The SGM2535 provides programmable input under-voltage lockout (UVLO) threshold on the EN/UVLO pin by placing a resistor divider from the VIN to EN/UVLO pin to GND. Once the UVLO condition is detected, the internal FETs are turned off quickly with the nFAULT pin asserted. If the UVLO function is not needed, this pin can be tied to the IN pin. Note that the EN/UVLO pin should not be left floating.

The device also provides fixed UVLO protection on the supply VIN terminal. The device is disabled when V_{IN} is below the internal UVLO threshold V_{UVF}. The internal UVLO hysteresis is 186mV.

Over-Voltage Protection (OVP)

The SGM2535 provides input over-voltage lockout (OVLO) protection. The OVLO threshold can be programmed by placing a resistor divider from the VIN to OVP pin to GND. When the voltage on the OVP pin V_{OVP} is greater than the internal reference V_{OVPR}, the internal FETs will be turned off. The OVP pin should be tied to GND if the protection is not needed.

Hot Plug-in and Inrush Current Control

The SGM2535 is designed to provide hot plug-in power management by controlling the inrush current as well as the output slew rate. This design helps eliminate the voltage drop and avoid undesired power reset. The output ramp rate is set by the capacitor from the SS pin to GND, as shown in Figure 4. The slew rate can be calculated using Equation 1.

DETAILED DESCRIPTION (continued)

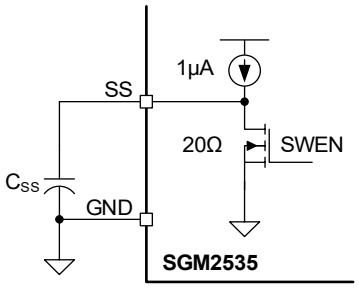


Figure 4. Output Ramp-up Time t_{SS} is Set by C_{SS}

$$I_{SS} = (\frac{C_{SS}}{GAIN_{SS}}) \times (\frac{dV_{OUT}}{dt}) \quad (1)$$

where,

I_{SS} = 1μA (TYP).

$\frac{dV_{OUT}}{dt}$ = Desired output slew rate.

$GAIN_{SS}$ = SS to output slew rate = 12.08.

$$t_{SS}(ms) = 8.28 \times 10^{-2} \times V_{IN}\ (V) \times C_{SS}\ (nF) \quad (2)$$

The SS pin can be floated to obtain a fastest output slew rate.

For startup with load, the load current is controlled within the over-current limit set by the resistor R_{ILIM} on the ILIM pin.

Overload and Short-Circuit Protection

The load current is continuously sensed and monitored. When over-current occurs, the current is precisely limited to the current limit I_{LIM} set by the R_{ILIM} resistor.

$$I_{LIM} = \frac{87.5}{R_{ILIM}(k\Omega)} \quad (3)$$

where, I_{LIM} is the over-current limit in Ampere, R_{ILIM} is the current limit resistor on the ILIM pin.

The SGM2535 is designed with two different limit levels: a current limit level (I_{LIM}) and a fast-trip threshold I_{FAST_TRIP}.

Note that the current limit performance is directly determined by the bias current on the ILIM pin. When routing the PCB, the I_{LIM} node must be kept away from any noisy signals.

Overload Protection

When overload occurs, the internal current limit amplifier of the device regulates the load current to the current limit threshold I_{LIM}. The output voltage would drop under regulation, which leads to increased power dissipation of the device. Once the junction temperature T_J reaches the over-temperature protection threshold T_{SD}, the internal FETs would be turned off. During thermal shutdown, the SGM2535AL version remains latched-off, while the SGM2535A version would perform auto-restart with 160ms cycle when T_J falls below T_{SD} - 20℃. During thermal shutdown, the nFAULT pin is asserted to indicate fault condition.

Short-Circuit Protection

When the output short-circuit occurs, the current from VIN to VOUT rises very rapidly. Due to limited bandwidth, the current limit amplifier is unable to respond quickly to this condition. To solve this, the SGM2535 integrates with a fast-trip comparator which could shut down the internal FETs within 1μs. The fast-trip comparator works and cuts off the short-circuit current when the current through the device I_{OUT} exceeds the fast-trip threshold I_{FAST_TRIP}. The fast-trip threshold is designed to be greater than 50% of the I_{LIM} (I_{FAST_TRIP} = 1.5 × I_{LIM} + 0.3). The internal FETs would remain off-state for only a few ms following by soft-restart in a current limit manner where current through the device is regulated to I_{LIM} under the regulation of current limit amplifier. Then, the device behaves the same as the overload condition. The fast-trip short-circuit protection is shown in Figure 5.

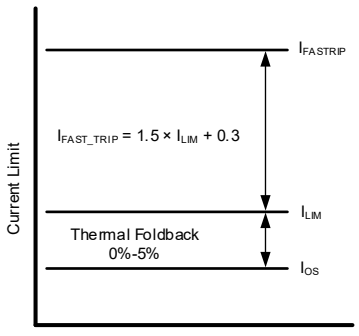


Figure 5. Fast-Trip Current

DETAILED DESCRIPTION (continued)

FAULT Response

The SGM2535 provides an nFAULT pin for fault indicator. The open-drain nFAULT pin is asserted under over-voltage, under-voltage, and reverse current and thermal shutdown conditions. The nFAULT pin remains active-low until the above fault is removed and the device operates normally. To avoid false trigger of fault, the device is integrated with a deglitch delay for over-voltage and under-voltage (1.24μs TYP for SGM2535A/AL, and 1.3μs TYP for SGM2535B/BL) conditions. This design ensures that transient fluctuation on the bus would not false assert the nFAULT pin.

The nFAULT pin can be pulled up through a resistor to input, output or other voltage rail. This pin can be left floating or tied to GND if not used. The nFAULT pin would be reset when the input voltage is below V_{UVF}.

Current Monitoring

The SGM2535 has a current monitoring function at the IMON pin. The sourcing current of this pin is proportional to the current of internal FETs. By placing a resistor R_{IMON} from this pin to GND, this monitored current is transformed to voltage as calculated in Equation 4.

The maximum voltage on the IMON pin is internally limited to minimum (V_{IN} - 0.5V, 4.5V). With this limitation, the maximum value of R_{IMON} can be determined using Equation 4.

$$R_{IMON\_MAX} = \frac{\text{minimum } (V_{IN} - 0.5,\ 4.5)}{1.6 \times I_{LIM} \times GAIN_{IMON}} \quad (4)$$

The voltage on the IMON pin, V_{IMON}, is calculated using Equation 5.

$$V_{IMON} = R_{IMON} \times (I_{OUT} \times GAIN_{IMON}) \quad (5)$$

where,

$GAIN_{IMON}$ is the gain factor I_{MON}: I_{OUT} (52.3μA/A TYP).

I_{OUT} is the current from VIN to VOUT.

The analog IMON voltage can be converted to digital data using an ADC (such as SGM58031) for current read through IC interface bus.

Power Good Comparator

The SGM2535 provides a power good indicator through the PG pin. The open-drain active-high PG pin is controlled by the PGTH pin which incorporates a voltage comparator. The positive terminal of the comparator is the PGTH pin, and the negative terminal is tied to the internal reference V_{PGTHR} (0.99V TYP). The PG pin would be asserted when the internal FETs are fully turned on and the PGTH voltage is greater than the V_{PGTHR}.

The PG pin incorporates an internal deglitch delay to ensure that the internal FETs is fully turned on and the device startup is completed before the downstream load is connected.

The PG pin can be pulled up through resistor to input, output or other power supply rail. This pin can be left floating or tied to GND if not used.

VIN, VOUT and GND Pins

The SGM2535 has multiple IN and OUT pins.

All VIN pins should be connected together to the power supply. It is recommended to place a ceramic input capacitor between VIN and GND. The capacitor should be close to the terminal for better transient suppression. The recommended input voltage is 2.7V to 18V.

Thermal Shutdown

The SGM2535 incorporates over-temperature protection with thermal shutdown function. The internal FETs would be turned-off when the internal temperature $T_J > T_{SD}$ (+160℃ TYP). For the auto-retry version, the part will continuously attempt to restart with a 160ms cycle after T_J drops below T_{SD} - 20℃. During thermal shutdown, the nFAULT pin is asserted to indicate fault condition.

DETAILED DESCRIPTION (continued)

Device Functional Modes

Device Sleep Mode for SATA® Interface Devices SGM2535A/AL Only

Device Sleep is a new state introduced by SATA®, which needs a low power level operation for SATA storage systems. In the Device Sleep mode, the power consumption is limited to 5mW or less for SSDs.

The SGM2535 incorporates a Device Sleep operation mode (DEVSLP) specifically used for driving SATA device in low power level. The DEVSLP pin is compatible with standard signal levels of controller. In the Device Sleep mode, the over-current limit threshold is set to I_{DEVSLP_LIM} and the reverse current/voltage protection as well as the current monitor function are disabled. The other functions remain active and behave the same as the normal operation mode.

When the device enters into Device Sleep mode, ensure that the load current is limited to less than I_{DEVSLP_LIM}. Also, when back to normal operation mode, the device should be sequenced before the downstream load. Otherwise, the load current could exceed the over-current limit which causes current limit operation and further lead to thermal shutdown. Figure 7 to Figure 10 illustrate the behavior of the system in DEVSLP mode.

Diode Mode SGM2535B/BL Only

The device provides a Diode Mode through the DMODE pin. This pin is active high with internal pull down. Under this mode, the device acts as a non-ideal diode rather than a MOSFET as shown in Figure 6, and the over-current limit is set to 50% of normal mode by RLIM resistor. The Diode Mode is useful for Power MUX applications to switch from the main power supply to the auxiliary power and vice-versa smoothly when the two supplies are within a diode drop pf each other.

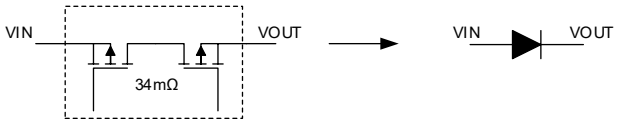


Figure 6. Diode Mode: VIN to VOUT Power Path

Shutdown Control

The internal FETs of SGM2535 can be remotely turned off by pulling the EN/UVLO pin below 0.6V through an open-drain (collector) transistor. The supply current I_Q is reduced to less than 12μA in the shutdown mode. Once the UVLO pin is released, the device restarts with the programmed output slew rate.

DETAILED DESCRIPTION (continued)

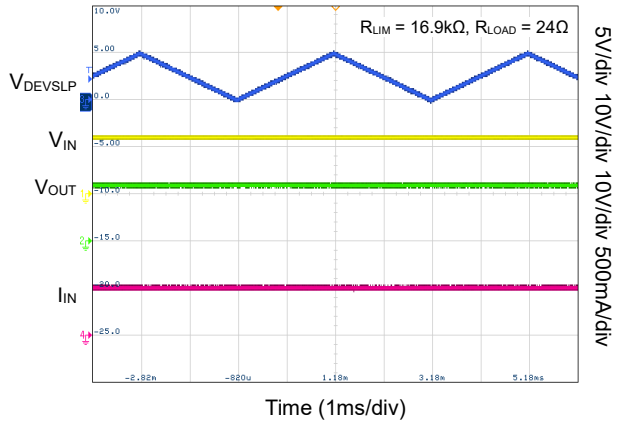


Figure 7. In and Out of DEVSLP Mode with 500mA Load

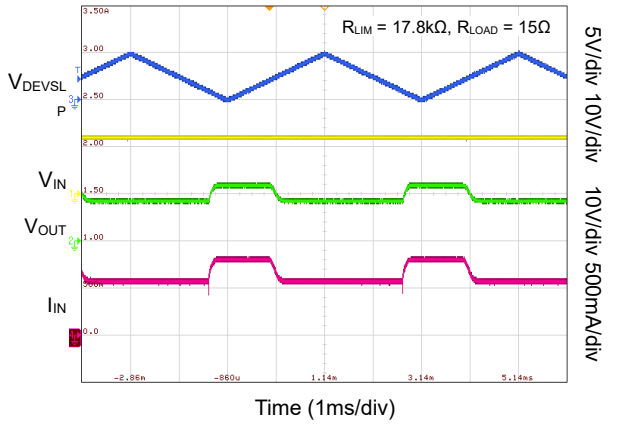


Figure 8. In and Out of DEVSLP Mode with 800mA Load

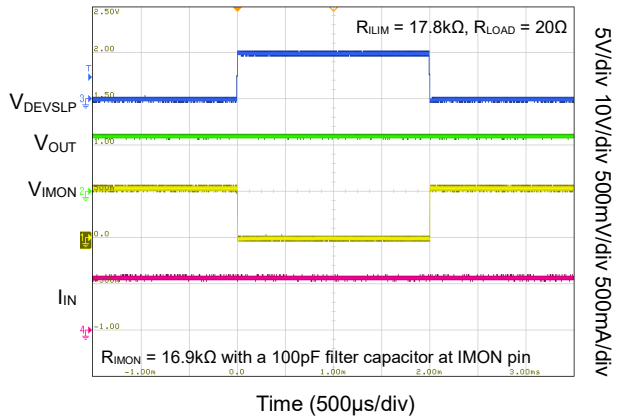


Figure 9. IMON Disabled in DEVSLP Mode

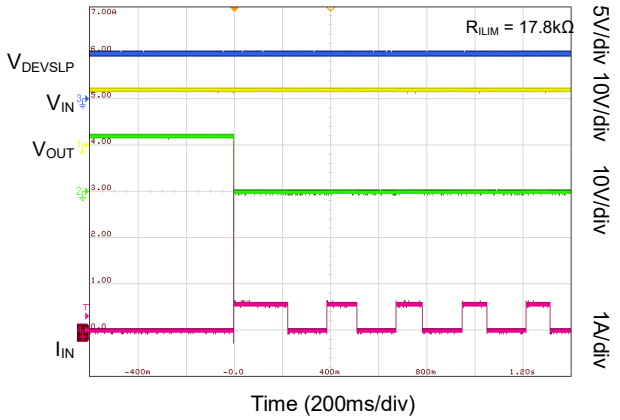


Figure 10. Hot-Short and Retry in DEVSLP Mode

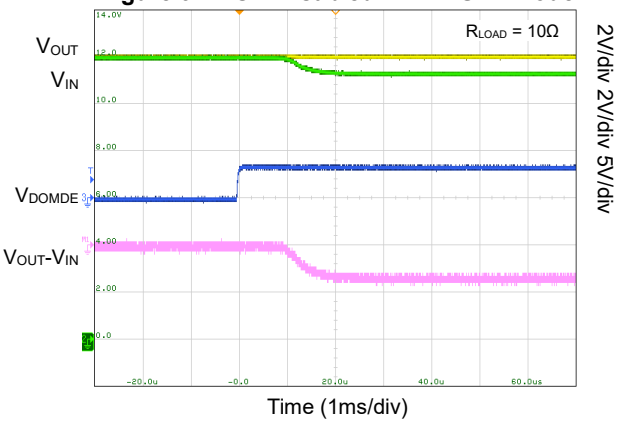


Figure 11. Transition from Normal Mode to Non-Ideal Diode

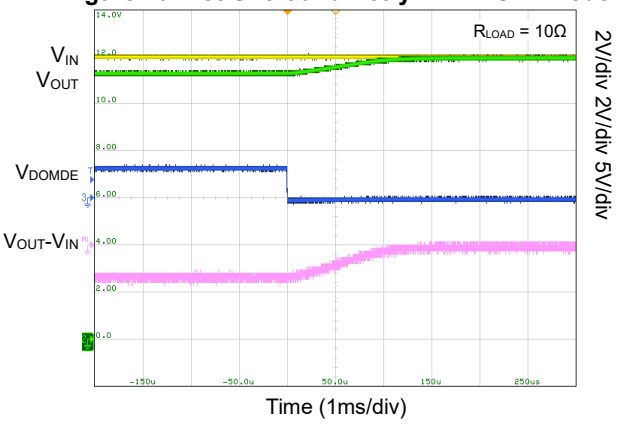
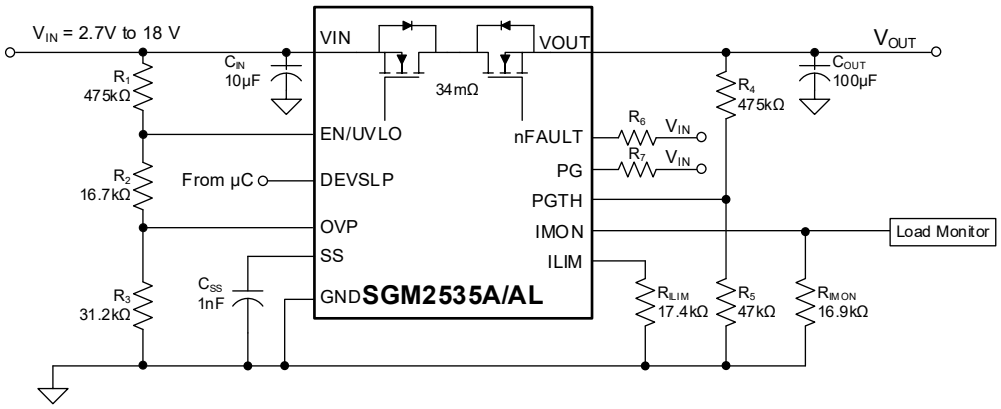


Figure 12. Transition from Non-Ideal Diode Mode to Normal Mode

APPLICATION INFORMATION

Typical Application



NOTE: 1. C_{IN}: Suggest using 10µF to suppress transients caused by PCB wiring inductance or input wiring.

Figure 13. Typical Application Schematics: eFuse for Enterprise SSDs-SGM2535A/AL

Design Requirements

Table 1. Design Parameters

Design Parameter	Example Value
Input voltage range	12V
Under-voltage lockout set point	10.8V
Over-voltage protection set point	16.5V
Load at startup	4.8Ω
Current limit	5A
Load capacitance	100µF
Ambient temperature	+85℃

Detailed Design Procedure

Step by Step Design Procedure

The following parameters must be decided by the designer previously:

- Normal input operation voltage.
- Maximum output capacitance.
- Maximum current limit level.
- Load during startup.
- Maximum ambient temperature during operation.

The below design procedure aims to control the device junction temperature under both steady and transient condition with appropriate output slew rate and other components. The design procedure is for reference and the designer could adjust according to actual criteria.

Programming the Current limit Threshold: R_{ILIM} Selection

The over-current limit threshold is set by the resistor R_{ILIM} at the ILIM pin using Equation 6.

$$R_{ILIM} = \frac{87.5}{5} = 17.5k\Omega \quad (6)$$

Using the nearest standard 1% resistor values, R_{ILIM} = 17.4kΩ is chosen.

Under-Voltage Lockout and Over-Voltage Set Point

The under-voltage lockout (UVLO) and the over-voltage lockout (OVLO) thresholds can be adjusted through the resistor divider network R_1, R_2 and R_3 connected from among VIN, EN/UVLO, OVP and GND pins. The resistor values are calculated using Equation 7 and Equation 8.

$$V_{OVPR} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{OV} \quad (7)$$

$$V_{ENR} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{UV} \quad (8)$$

For minimizing the current drawn by the resistors, use higher values of resistance for R_1, R_2 and R_3.

However, the internal leakage current of the device pins would introduce errors to the calculations. Therefore, the current flows through the resistors current, I_{R123} must be chosen to be 20x greater than the leakage current expected.

From the EC table, V_{OVPR} = 0.99V and V_{ENR} = 0.99V. For design requirements, V_{OV} = 16.5V and V_{UV} = 10.8V. First choose the value of R_3 = 31.2kΩ. Then use Equation 7, which gives (R_1 + R_2) = 488.8kΩ, and combine this with Equation 8, which gives R_2 = 16.47kΩ. Finally, R_1 = 472.33kΩ.

Using the closest standard 1% resistor values: R_1 = 475kΩ, R_2 = 16.7kΩ, and R_3 = 31.2kΩ.

APPLICATION INFORMATION (continued)

The input power failure is detected on the falling edge of V_{IN}, and the threshold is 7% lower than the rising threshold, V_{UV} as shown in Equation 9.

$$V_{PFAIL} = 0.93 \times V_{UV} \quad (9)$$

Programming Current Monitoring Resistor - R_{IMON}

V_{IMON} is proportional to the load current, which can be read through an ADC for system state monitoring. The R_{IMON} should be selected based on the maximum voltage at IMON pin. Equation 10 gives the calculation.

$$R_{IMON} = \frac{V_{IMON\_MAX}}{I_{LIM} \times 52.3 \times 10^{-6}} \quad (10)$$

For I_{LIM} = 5A, suppose the voltage range of ADC is 0V to 5V, V_{IMON_MAX} is 4.5V and R_{IMON} is calculated by:

$$R_{IMON} = \frac{4.5}{5 \times 52.3 \times 10^{-6}} = 17.2k\Omega \quad (11)$$

Select R_{IMON} less than the calculated value to ensure that ADC is within the operation range for maximum load current.

Choose closest 1 % standard value: 16.9kΩ.

If current monitoring up to I_{FAST_TRIP} is desired, R_{IMON} can be reduced by a factor of 1.6.

Setting Output Voltage Ramp Time (t_{SS})

During startup and steady state operation, the device temperature should be well designed below the upper limit to avoid thermal shutdown. Since transient power dissipation are often much greater than the steady state, it is necessary to design the proper startup time and inrush current for the given output capacitance to prevent the device from thermal shutdown.

Considering the two possible cases, the soft-start capacitor C_{SS} is determined:

Case1: Startup without Load: Only Output Capacitance C_{OUT} Draws Current during Startup

During startup, the voltage difference on the internal FETs (V_{IN}/V_{OUT}) as well as the power dissipation decrease. The average power dissipation during startup is equal to the area of the red curve averaged over startup time t_{SS}. See Figure 14 and Figure 15.

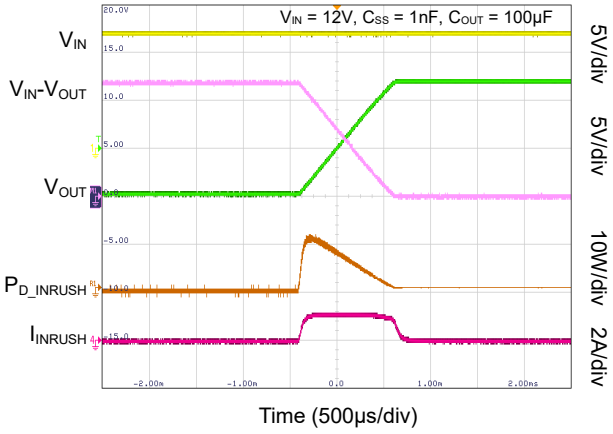


Figure 14. Startup without Load

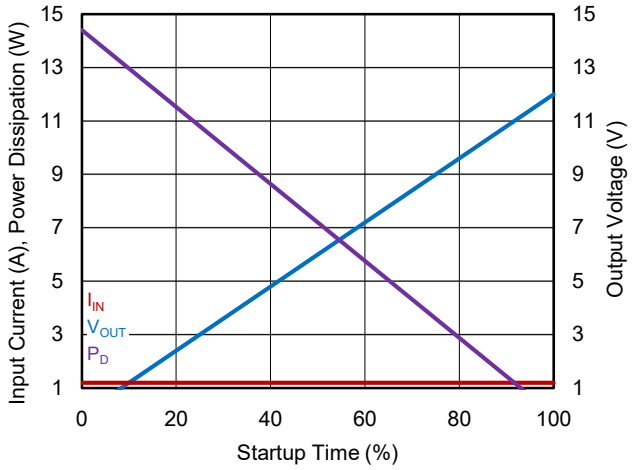


Figure 15. P_{D_INRUSH} due to Inrush Current

For SGM2535, the inrush current is calculated by:

$$I = C \times \frac{dV}{dt} \Rightarrow I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{t_{SS}} \quad (12)$$

The power dissipation of the device during startup is:

$$P_{D\_INRUSH} = 0.5 \times V_{IN} \times I_{INRUSH} \quad (13)$$

Note that Equation 13 is only applicable for startup without any load drawing current.

APPLICATION INFORMATION (continued)

Case2: Startup with Load: Output Capacitance C_{OUT} and Load Draws Current during Startup

When both the output capacitance and the load draw current during the startup process, the device will have additional power dissipation. Suppose a resistor load R_{L_SU} is driven during startup, the current flows through the resistor load ramps up proportional to the output voltage. See Figure 16 and Figure 17.

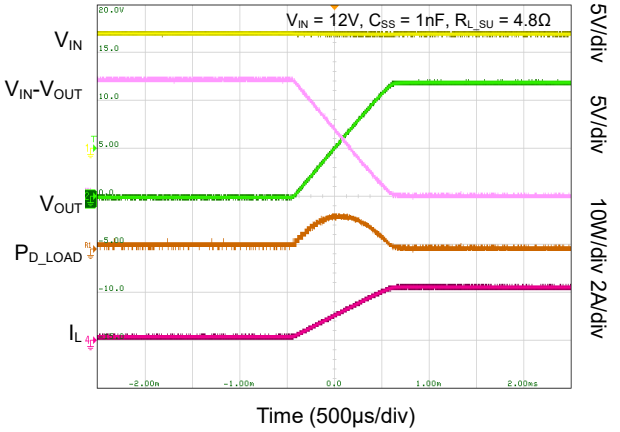


Figure 16. Startup with Load

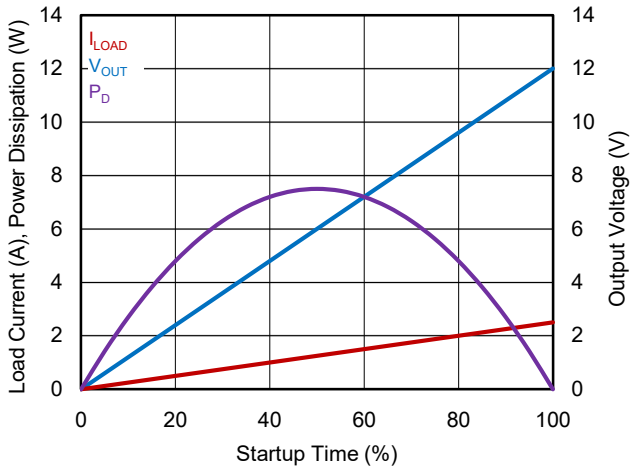


Figure 17. P_{D_LOAD} in Load during Startup

The additional power dissipation introduced by the resistor load is:

$$(V_I - V_O) \times t = V_{IN} \times (1 - \frac{t}{t_{SS}}) \quad (14)$$

$$I_L(t) = \left(\frac{V_{IN}}{R_{L\_SU}}\right) \times \frac{t}{t_{SS}} \quad (15)$$

The total energy loss of the device introduced by the resistor load during startup is:

$$W_t = \int_0^{t_{SS}} V_{IN} \times \left(1 - \frac{t}{t_{SS}}\right) \times \left(\frac{V_{IN}}{R_{L\_SU}} \times \frac{t}{t_{SS}}\right) dt \quad (16)$$

Using Equation 17, the average power loss of the device introduced by the load during startup is given by:

$$P_{D\_LOAD} = \left(\frac{1}{6}\right) \times \frac{V_{IN}^2}{R_{L\_SU}} \quad (17)$$

Therefore, the total power loss of the device during startup is:

$$P_{D\_STARTUP} = P_{D\_INRUSH} + P_{D\_LOAD} \quad (18)$$

Therefore, the total current during startup is:

$$I_{STARTUP} = I_{INRUSH} + I_L(t) \quad (19)$$

If $I_{STARTUP}$ > I_{LIM}, the device limits the current to I_{LIM} and the current limited charging time is:

$$t_{SS\_CURRENT\ LIMIT} = C_{OUT} \times \frac{V_{IN}}{I_{LIM}} \quad (20)$$

For the above design, using Equation 21, the soft-start capacitor C_{SS} is selected as 1nF.

$$t_{SS} = 8.28 \times 10^{-2} \times 12 = 0.994ms \approx 1ms \quad (21)$$

Using Equation 22, the inrush current drawn by the output capacitance C_{OUT} during startup is:

$$I_{INRUSH} = (100 \times 10^{-6}) \times \left(\frac{12}{1 \times 10^{-3}}\right) = 1.2A \quad (22)$$

Using Equation 23, the power dissipation introduced by C_{OUT} is:

$$P_{D\_INRUSH} = 0.5 \times 12 \times 1.2 = 7.2W \quad (23)$$

For $P_{DINRUSH}$ = 7.2W, the thermal shutdown time should be greater than the soft-start time t_{SS}. The thermal shutdown time is about 30ms for T_A = +85℃, P_D = 7.2W. Therefore, it is safe to use 1ms soft-start time with only output capacitance and without load.

Furthermore, considering the 4.8Ω of startup load, the additional power dissipation during startup is:

$$P_{D\_LOAD} = \left(\frac{1}{6}\right) \times \frac{12 \times 12}{4.8} = 5W \quad (24)$$

The total power dissipation during startup is:

$$P_{D\_STARTUP} = (7.2 + 5) = 12.2W \quad (25)$$

APPLICATION INFORMATION (continued)

For P_D = 12.2W, the thermal shutdown time is about 7ms for T_A = +85℃, see Thermal Shutdown Time vs. Power Dissipation figure in TYPICAL PERFORMANCE CHARACTERISTICS section. Therefore, it is safe to use 1ms soft-start time with a 4.8Ω of startup load.

If lower power loss during startup is needed, the soft-start capacitor C_{SS} can be increased to meet this requirement.

Programing the Power Good Set Point

R_4 and R_5 set the PG signal threshold. For this design, the PG threshold is 11V and the values of R_4 and R_5 are calculated using Equation 25.

$$V_{PGTH} = 0.99 \times \left(1 + \frac{R_4}{R_5}\right) \quad (26)$$

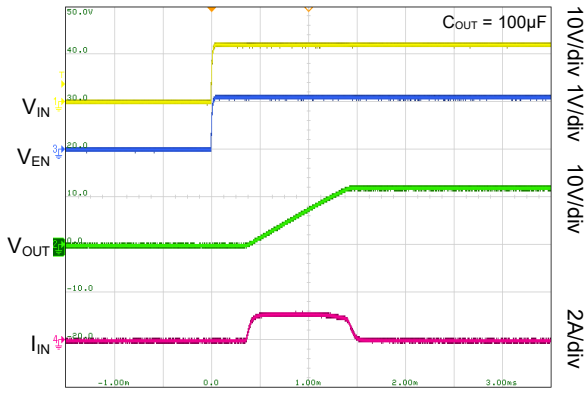
For lower current consumed, it is recommended to use high values of resistors. For example, choose R_4 = 475kΩ, R_5 = 47kΩ and V_{PGTH} = 11V.

Support Component Selections - R_6, R_7 and C_{IN}

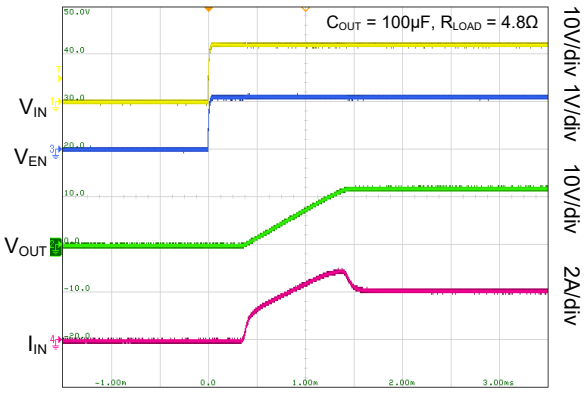
R_6 and R_7 are required only if the state indictor function PG and nFAULT are used. These resistors are used for pulling up the open-drain transistors. The current flows through these pins should not exceed 10mA. The capacitor placed at VIN terminal is used to suppress transient voltages and noise. If acceptable, it is recommended to use a range of 0.1μF to 10μF for C_{IN}.

Application Curves

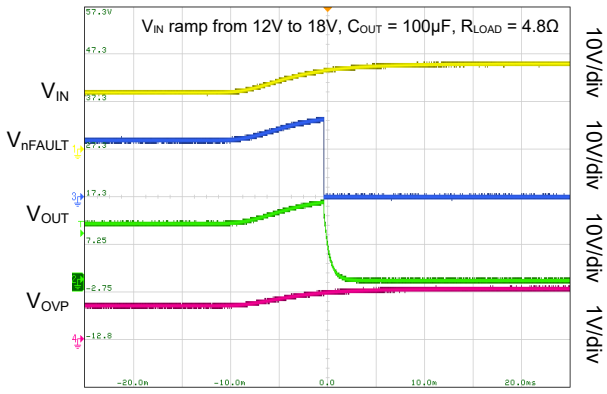
Hot-Plug Startup: Output Ramp without Load on Output



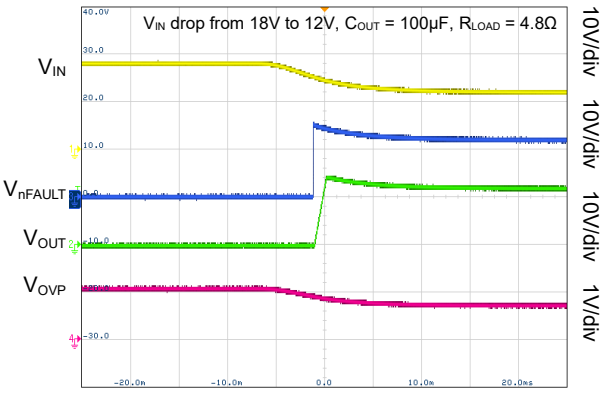
Hot-Plug Startup: Output Ramp with Startup Load of 4.8Ω



Over-Voltage Shutdown

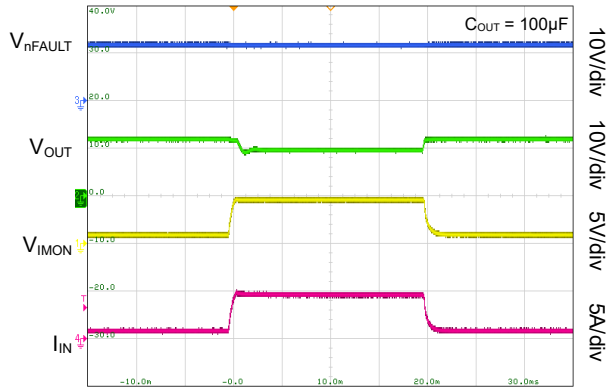


Over-Voltage Recovery



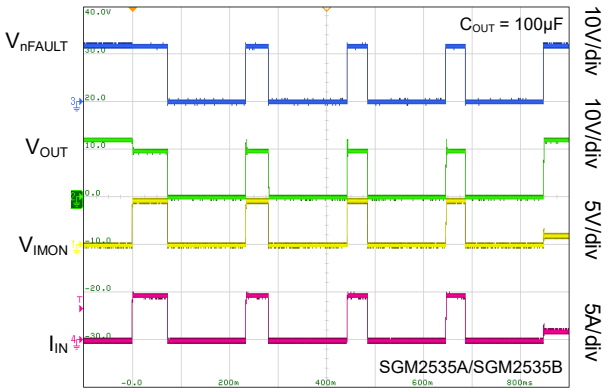
APPLICATION INFORMATION (continued)

Overload: Step Change in Load from 12Ω to 2Ω and Back



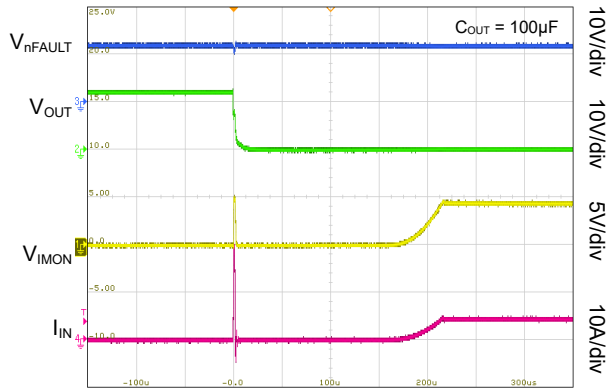
Time (5ms/div)

Overload Condition: Auto-Retry and Recovery



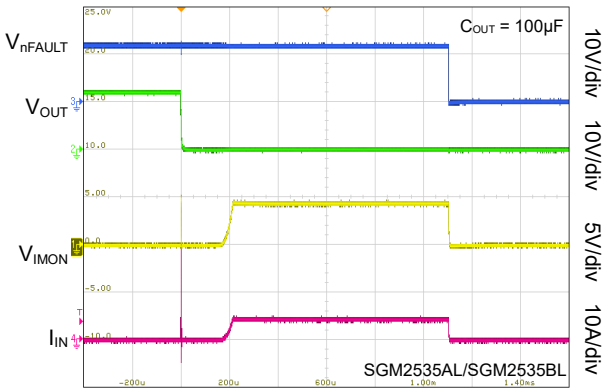
Time (100ms/div)

Hot-Short: Fast-Trip and Current Regulation



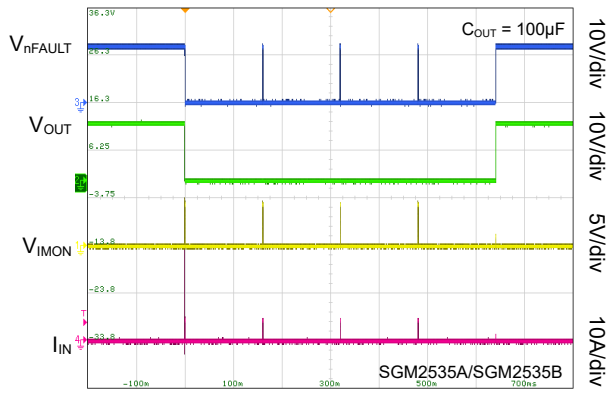
Time (50μs/div)

Hot-Short: Latched



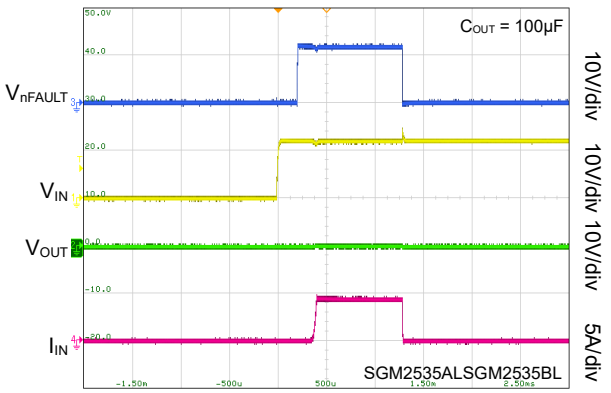
Time (200μs/div)

Hot-Short: Auto-Retry and Recovery from Short-Circuit



Time (100ms/div)

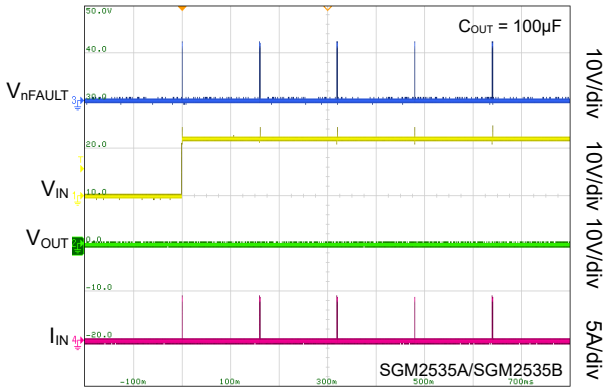
Hot Plug-In with Short on Output: Latched



Time (500μs/div)

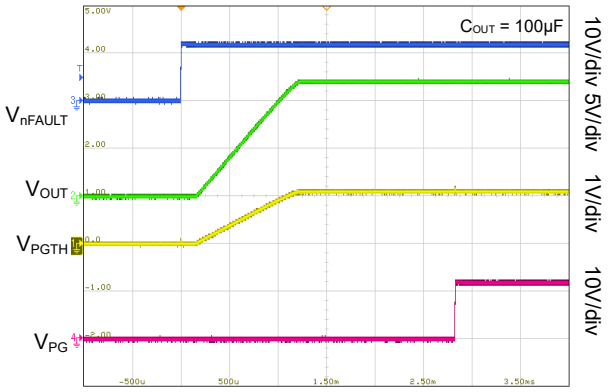
APPLICATION INFORMATION (continued)

Hot Plug-In with Short on Output: Auto-Retry



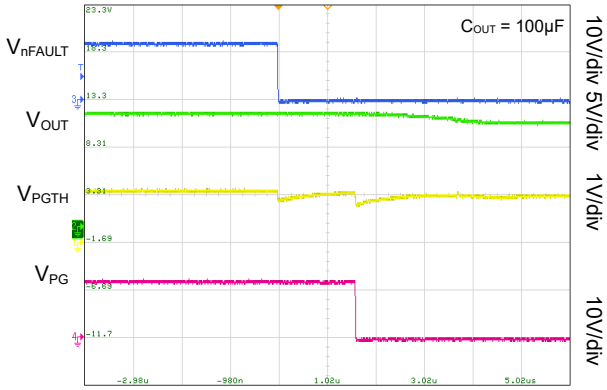
Time (100ms/div)

Power Good Response during Turn-On



Time (500μs/div)

Power Good Response during Turn-Off



Time (1μs/div)

System Examples for SGM2535A/AL

Power Failure Protection and Data Retention in SSDs

For enterprise and industrial SSD applications, the hold-up capacitor bank is needed to prevent data loss during power failure fault. The power-failure fault could happen due to power supply hot plug-out or input transient brown out.

The SGM2535 detects the input voltage at EN/UVLO pin and turns off the device when V_{IN} drops below the preset UVLO threshold. The device also monitors the voltage between input and output V_{IN} - V_{OUT} and cuts off the reverse current when V_{IN} - V_{OUT} exceeds -10mV. Besides, the device has a fault indicator pin nFAULT to signal the SSD controller for initialing the date hardening.

The typical block diagram and application schematic of SGM2535 implementation for enterprise SSD are shown in Figure 18 and Figure 19.

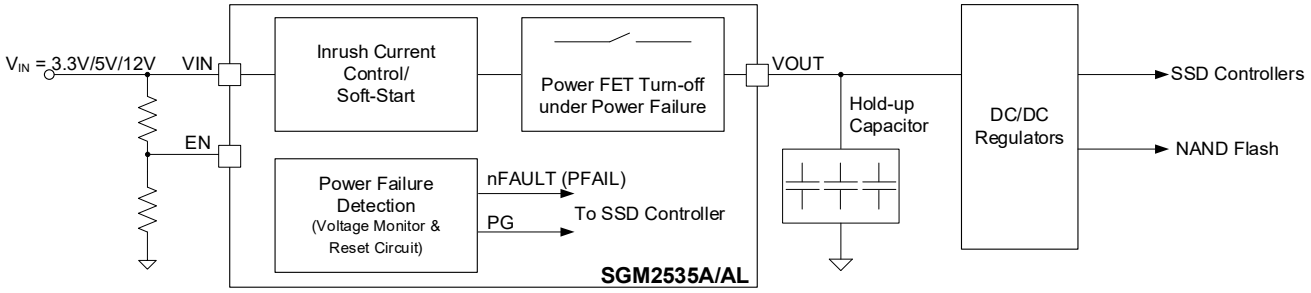


Figure 18. Power Circuit Block Diagram of Enterprise and Industrial SSDs

APPLICATION INFORMATION (continued)

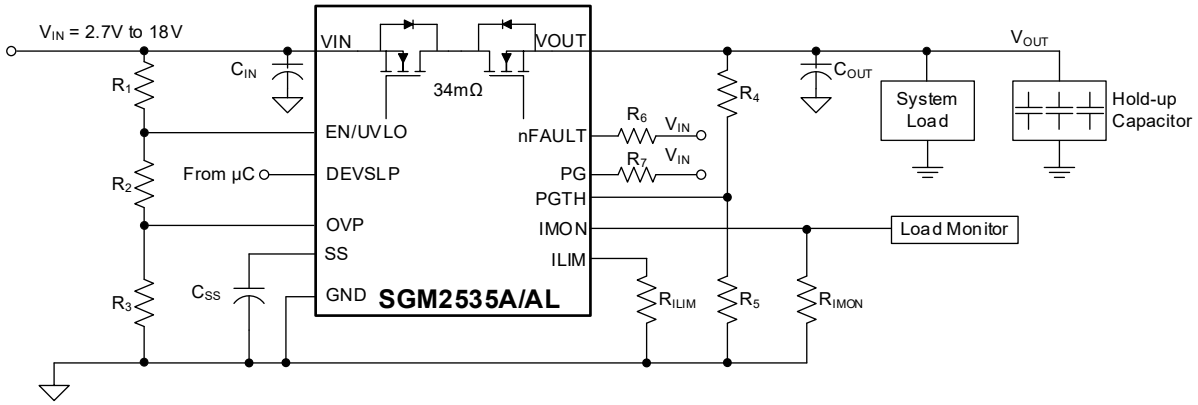
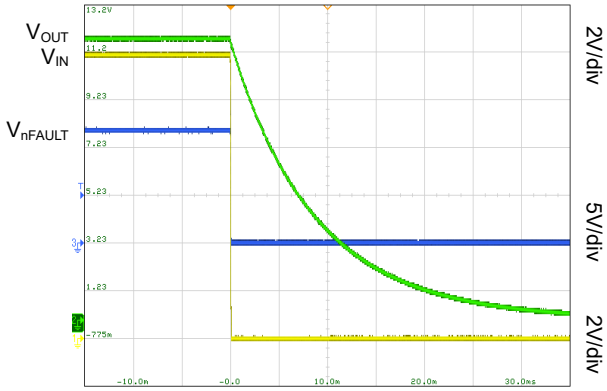


Figure 19. Enterprise SSD – Hold-up Capacitor Implementation using SGM2535A/AL

Application Curves

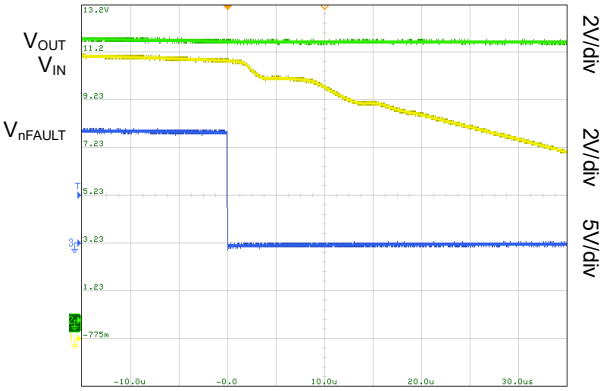
C_{OUT} = 1500µF, R_{LOAD} = 5.6Ω, unless otherwise noted.

Hot Plug-Out Condition



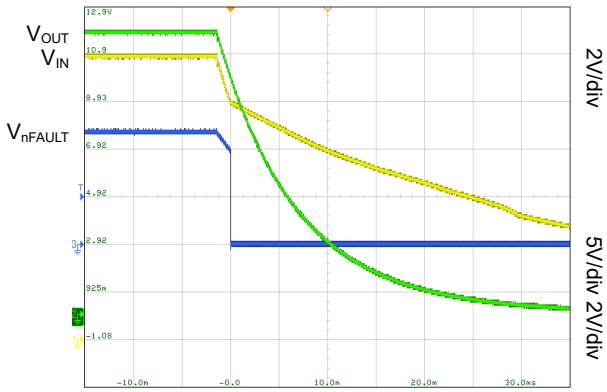
Time (5ms/div)

Hot Plug-Out Condition: nFAULT Delay



Time (5µs/div)

Standard Power Shutdown or Brownout Conditions



Time (5ms/div)

APPLICATION INFORMATION (continued)

System Examples for SGM2535B/BL

Active ORing (Auto-Power Multiplexer) Operation

For redundant power supply (ORing) applications shown in Figure 20, Schottky diodes are usually used for connecting parallel power sources, such as a battery source paralleled with a hold-up capacitor bank. Besides, additional eFuses are needed to provide protections which increase system complexity. With the integrated diode mode and multiple protection modes, the SGM2535B provide a simple solution. The ORing power system using SGM2535B is shown in Figure 20.

The SGM2535B integrates with a fast reverse comparator to provide reverse current blocking protection as shown in Figure 21. The internal FET is turned off within 3.7μs (TYP) when the voltage difference between VIN and VOUT (V_{IN} - V_{OUT}) drops below -10mV, and is turned on within 1.8μs (TYP) when V_{IN} - V_{OUT} exceeds 100mV. Besides, both the device can operate in Diode Mode through controlling the DMODE pin separately.

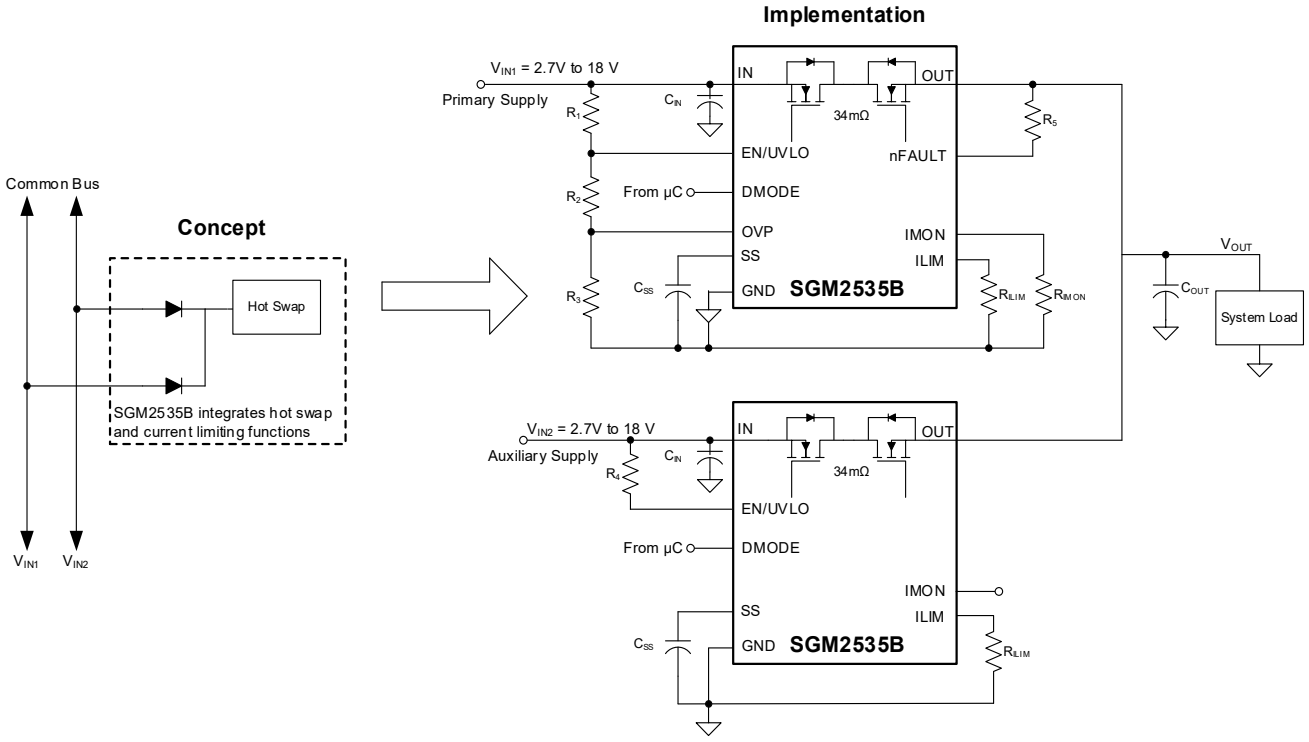


Figure 20. Active ORing Implementation

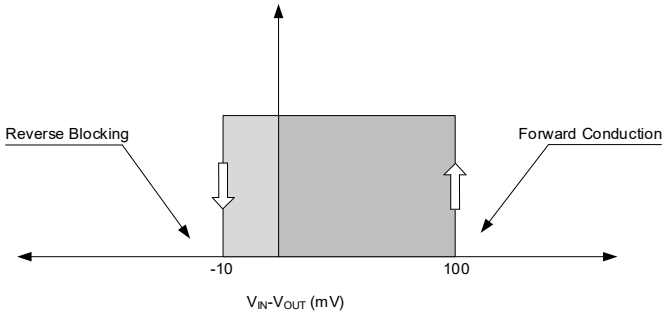


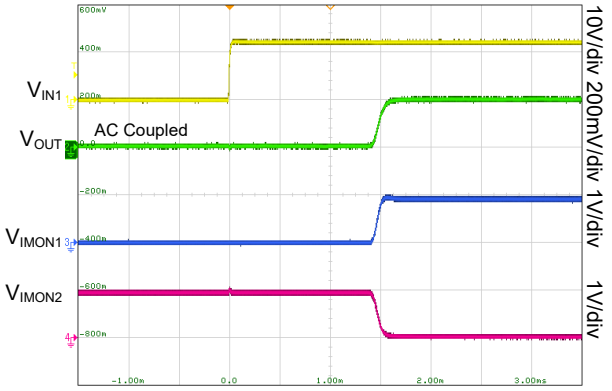
Figure 21. Active ORing Thresholds

APPLICATION INFORMATION (continued)

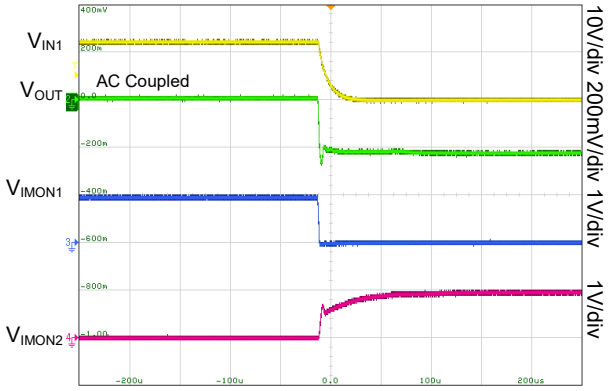
Application Curves

V_{IN1} = 12.2V, V_{IN2} = 12V, C_{OUT} = 100μF, C_{SS} = 1nF, and R_{LOAD} = 12Ω, unless otherwise noted.

IN1 Power Recovery: Change Over from IN2 to IN1



IN1 Brownout Condition: Change Over from IN1 to IN2



Power Supply Recommendations

The SGM2535B/SGM2535BL is designed for a supply voltage from 2.7V to 18V. If the distance between the power supply and the device is more than a few inches away, it is recommended to place a bypass ceramic capacitor greater than 0.1μF at the VIN terminal. The rated current of the power supply must be greater than the over-current threshold set by the device, otherwise the supply voltage will drop in the event of an over-current or short-circuit.

Transient Protection

If the short-circuit or over-current limit case occurs, the device may cut off the current, and due to the parasitic inductance in series at the input and output of the device, a positive voltage spike will occur at the input with a negative voltage spike occur at the output. The amplitude of the voltage spike is determined by the parasitic inductance. These transients can cause the voltage on the device pins to exceed their maximum absolute rating if the following measures are not taken:

- The length of the wires at the input and output of the device is as small as possible.
- A TVS diode is paralleled at the input port of the device to absorb a positive voltage spike, and a Schottky diode is connected in parallel to the output port to absorb a negative voltage spike.
- Choose a large PCB GND plane.
- Connect a low ESR ceramic capacitor larger than 10μF near the VOUT pin.
- A ceramic capacitor greater than 10μF is connected near the input pin to absorb and suppress transient voltage spikes and ringing.

The value of the input capacitance can be calculated from the Equation 27:

$$V_{SPIKE\_ABSOLUTE} = V_{IN} + I_L \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (27)$$

Where V_{IN} is the rating of the input voltage, I_L is the load current, L_{IN} is the effective inductance seen looking into the source, and C_{IN} is the capacitance of the input.

For applications such as USB-C interfaces, the power cord may be plugged into the output of the device. In this case, the voltage stress from OUT to IN may exceed the absolute maximum rating, so it is recommended to add a TVS diode from OUT to IN to clamp the voltage for safety.

Output Short-Circuit Measurements

The output short-circuit waveform may be affected by factors such as input leads, power supply bypass, layout, device selection, circuit location, and output short-circuit method. It is difficult to obtain repeatable and similar output short-circuit test results. Therefore, the short-circuit results in this datasheet are for informational purposes only. Different short-circuit test results may be achieved because of different test conditions.

LAYOUT GUIDELINES

In any application, it is recommended to connect a decoupling capacitor of 0.1μF or greater between VIN and GND. This decoupling capacitor should be as close as possible to VIN and GND pins.

The power path should be as wide and short as possible, with a current carrying capacity of more than twice the device's current limit.

The GND pin of the device must be connected to PCB ground which is a copper plane or island as short as possible.

The VIN and VOUT pins of the device are used to dissipate heat. Therefore, these two pins should be dissipated as much as possible through the copper plane on the top layer or bottom layer on the PCB. Placing thermal vias on the copper plane improves on-resistance as well as current sensing accuracy.

External components of the device as follows should be placed as close to the corresponding pins as possible:

- R_{ILIM}
- C_{SS}
- Resistor dividers of EN/UVLO, OVLO and PGTH

The other end of these components is connected to ground via the shortest possible path. The ILIM pin should have a parasitic capacitance of less than 50pF, and the connection path of this pin should be away from the switching signal.

Protection components such as TVS or Schottky diodes should be connected to the device via a short path to avoid large line inductance. It is important to note that the loop area formed by the protection components should be as small as possible.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

APRIL 2025 – REV.A.2 to REV.A.3	Page
Updated figure 1, figure 13, figure 19 and figure 20	1, 23, 29, 30
Updated recommended operating conditions	2
Updated support component selections - R_6, R_7 and C_{IN} section	26

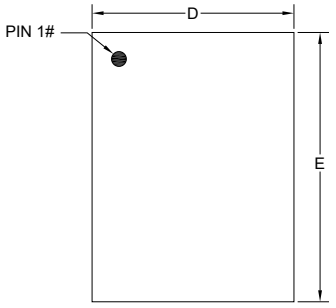
DECEMBER 2024 – REV.A.1 to REV.A.2	Page
Added SGM2535B and SGM2535BL versions	All

SEPTEMBER 2024 – REV.A to REV.A.1	Page
Adjusted the position of application curves	13, 22, 23, 24, 25
Added a typical block diagram and an application schematic	24, 25

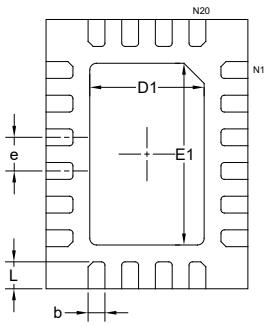
Changes from Original (JUNE 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

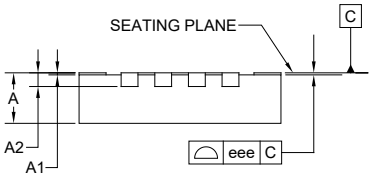
TQFN-3×4-20L



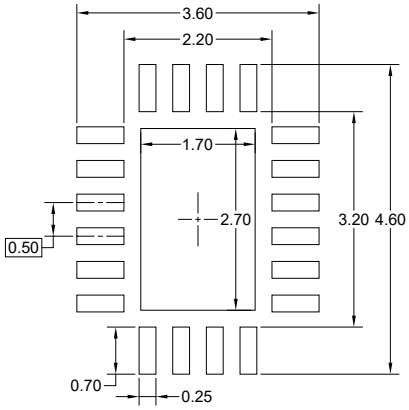
TOP VIEW



BOTTOM VIEW



SIDE VIEW



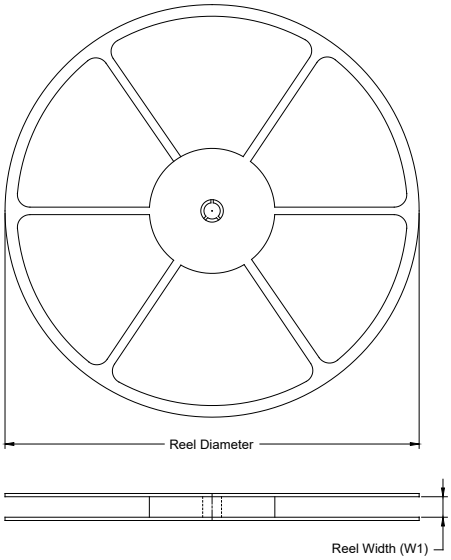
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	0.250	0.300
D	2.900	3.000	3.100
E	3.900	4.000	4.100
D1	1.600	1.700	1.800
E1	2.600	2.700	2.800
L	0.300	0.400	0.500
e	0.500 BSC		
eee	0.080		

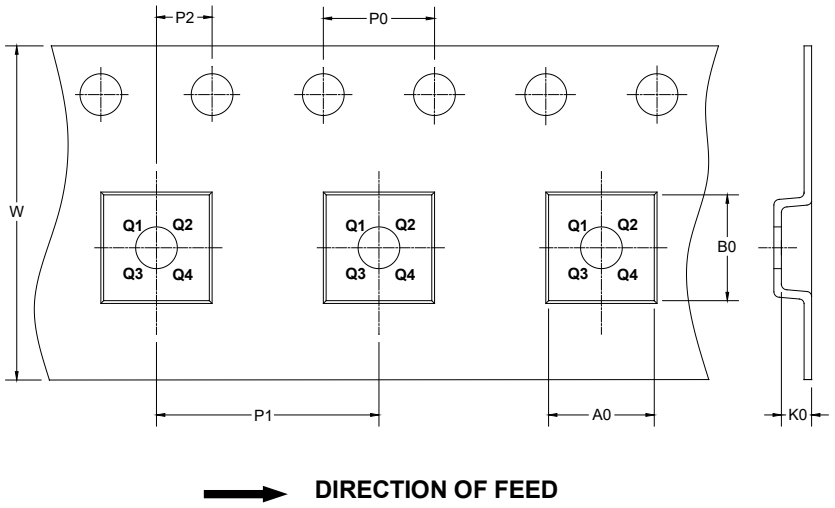
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



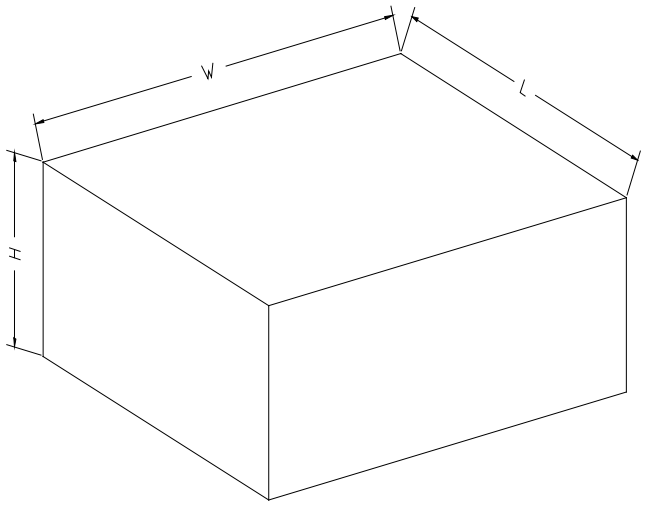
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×4-20L	13"	12.4	3.40	4.40	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002