SGM3888
Logic PMIC for OLED Panel

GENERAL DESCRIPTION

The SGM3888 is designed for OLED panels which require AVDD, VCORE, VIO, VDDI, VGH1/2, VGL1/2, VINT1/2, VINT3, VREFH/L.

The device integrates one synchronous Boost converter AVDD with a pass transistor, three synchronous Buck converters VCORE, VIO and VDDI, one 1:2 charge pump PVGH, one inverting asynchronous Buck-Boost converter PVGL, five positive OP amplifiers VGH1/2, VREFH/L, VINT3 and four negative OP amplifiers VGL1/2, VINT1/2. Output voltage of all channels can be programmed in digital steps through I^2C interface.

The SGM3888 is available in a Green TQFN-5×6-44L package.

FEATURES

- **2.7V to 4.8V Input Supply Voltage Range**
- **Synchronous Boost Converter AVDD**
  - **5.5V to 10.55V Output Voltage with 50mV Steps**
  - **7.6V Default Output Voltage**
  - **700mA Output Current Capability**
  - **With a Pass Transistor**
- **Synchronous Buck Converter VCORE**
  - **0.6V to 1.5V Output Voltage with 25mV Steps**
  - **0.9V Default Output Voltage**
  - **2.5A Output Current Capability**
- **Synchronous Buck Converter VIO**
  - **1V to 1.95V Output Voltage with 50mV Steps**
  - **1.8V Default Output Voltage**
  - **1.5A Output Current Capability**
- **Synchronous Buck Converter VDDI**
  - **1V to 1.95V Output Voltage with 50mV Steps**
  - **1.2V Default Output Voltage**
  - **1.5A Output Current Capability**
- **Inverting Buck-Boost Converter PVGL**
  - **-22V to -6V Output Voltage with 100mV Steps**
  - **-11V Default Output Voltage**
  - **250mA Output Current Capability**
- **Positive OP Amplifier VGH1/2**
  - **4V to 19.9V Output Voltage with 100mV Steps**
  - **10V Default Output Voltage**
  - **70mA Output Current Capability**
- **Negative OP Amplifier VGL1/2**
  - **-21V to -2V Output Voltage with 100mV Steps**
  - **-10V Default Output Voltage**
  - **70mA Output Current Capability**
- **Negative OP Amplifier VINT1/2**
  - **-19V to -0.5V Negative Output Voltage Range with 10mV Steps**
  - **-6V Default Output Voltage**
  - **50mA Output Current Capability**
- **Positive OP Amplifier VINT3**
  - **1V to 10V Output Voltage with 10mV Steps**
  - **7.2V Default Output Voltage**
  - **50mA Output Current Capability**
- **Positive OP Amplifier VREFH**
  - **4.4V to 9.5V Output Voltage with 10mV Steps**
  - **6.8V Default Output Voltage**
  - **50mA Output Current Capability**
- **Positive OP Amplifier VREFL**
  - **0.5V to 5.5V Output Voltage with 10mV Steps**
  - **1.5V Default Output Voltage**
  - **50mA Output Current Capability**
- **Outputs Power Off Discharge Function**
- **UVLO, UVP, OVP, SCP and OTP Protections**
- **I^2C Interface**
- **Available in a Green TQFN-5×6-44L Package**

APPLICATIONS

Infotainment OLED Panel

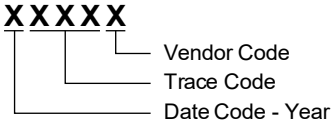
E-Mirror OLED Panel

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3888	TQFN-5×6-44L	-40℃ to +125℃	SGM3888XTYG44G/TR	2QJ TYG44 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to Ground Pin)
VIN1/2, VINB1/2 ..... -0.3V to 6V
PGND, PGNDB1/2/3 ..... -0.3V to 0.3V
PGNDC, PGNDN, AGND ..... -0.3V to 0.3V
SDA, SCL, EN1, EN2, nFAULT ..... -0.3V to 6V
SDA, SCL (Transient: 1ns) ..... -1V to 6V
SWB1/2/3 ..... -0.3V to 6V
SWB1/2/3 (Transient: 2ns) ..... -4.3V to 6V
VCORE, VIO, VDDI ..... -0.3V to 6V
ELVDDFB ..... -0.3V to 12V
VINN, CPCLK ..... -0.3V to 14V
SWP, PAVDD, AVDD ..... -0.3V to 14V
SWP (Transient: 2ns) ..... -5.3V to 19V
VREFH/L, VINT3 ..... -0.3V to 12V
OPP ..... -0.3V to 22V
PVGH, VGH1/2 ..... -0.3V to 24V
SWN ..... -24V to 14V
VINN to SWN ..... -0.3V to 32V
PVGL, VGL1/2 ..... -24V to 0.3V
VINT1/2, ELVSSFB ..... -20V to 0.3V
Package Thermal Resistance
TQFN-5×6-44L, θ_{JA} ..... 24.1℃/W
TQFN-5×6-44L, θ_{JB} ..... 1.9℃/W
TQFN-5×6-44L, $\theta_{JC\ (TOP)}$ ..... 9.1℃/W
TQFN-5×6-44L, $\theta_{JC\ (BOT)}$ ..... 2.2℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Input Voltage, V_{IN} ..... 2.7V to 4.8V
Operating Junction Temperature Range ..... -40℃ to +125℃
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

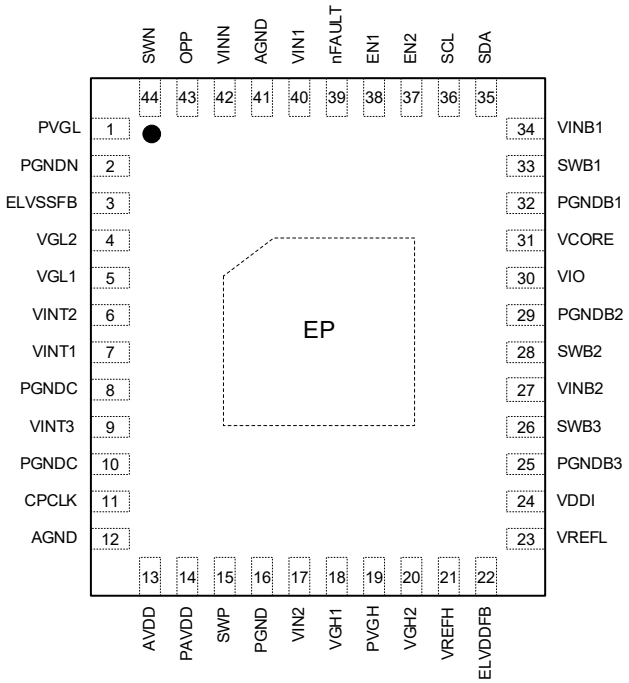
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-5×6-44L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	PVGL	P	PVGL Inverting Buck-Boost Converter Output Pin.
2	PGNDN	G	PVGL Inverting Buck-Boost Converter Power Ground.
3	ELVSSFB	I	ELVSS Voltage Sense Pin.
4	VGL2	P	VGL2 Negative OP Amplifier Output Pin.
5	VGL1	P	VGL1 Negative OP Amplifier Output Pin.
6	VINT2	P	VINT2 Negative OP Amplifier Output Pin.
7	VINT1	P	VINT1 Negative OP Amplifier Output Pin.
8, 10	PGNDC	G	PVGH Charge Pump Power Ground.
9	VINT3	P	VINT3 Positive OP Amplifier Output Pin.
11	CPCLK	P	PVGH Charge Pump Switching Node.
12, 41	AGND	G	Analog Ground.
13	AVDD	P	AVDD Boost Converter with Pass Transistor Output Pin.
14	PAVDD	P	PAVDD Boost Converter Output Pin.
15	SWP	P	PAVDD Boost Converter Switching Node.
16	PGND	G	PAVDD Boost Converter Power Ground.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
17	VIN2	P	Device Supply Input Pin.
18	VGH1	P	VGH1 Positive OP Amplifier Output Pin.
19	PVGH	P	VGH1/2 and VINT3 Positive OP Amplifiers Supply Pin.
20	VGH2	P	VGH2 Positive OP Amplifier Output Pin.
21	VREFH	P	VREFH Positive OP Amplifier Output Pin.
22	ELVDDFB	I	ELVDD Voltage Sense Pin.
23	VREFL	P	VREFL Positive OP Amplifier Output Pin.
24	VDDI	P	VDDI Buck Converter Output Sense Pin.
25	PGNDB3	G	VDDI Buck Converter Power Ground.
26	SWB3	P	VDDI Buck Converter Switching Node.
27	VINB2	P	VIO/VDDI Buck Converters Supply Input Pin.
28	SWB2	P	VIO Buck Converter Switching Node.
29	PGNDB2	G	VIO Buck Converter Power Ground.
30	VIO	P	VIO Buck Converter Output Sense Pin.
31	VCORE	P	VCORE Buck Converter Output Sense Pin.
32	PGNDB1	G	VCORE Buck Converter Power Ground.
33	SWB1	P	VCORE Buck Converter Switching Node.
34	VINB1	P	VCORE Buck Converter Supply Input Pin.
35	SDA	I/O	I^2C Interface Date Line.
36	SCL	I	I^2C Interface Clock Line.
37	EN2	I	PAVDD, AVDD, PVGH, PVGL, VGH1/2, VGL1/2, VINT1/2, VINT3, VREFH/L Enable Pin.
38	EN1	I	VCORE/VIO/VDDI Buck Converters Enable Pin.
39	nFAULT	O	FAULT Status Output Pin.
40	VIN1	P	Device Supply Input Pin.
42	VINN	P	PVGL Inverting Buck-Boost Converter Supply Pin.
43	OPP	P	Input Power for VREFH/L Positive OP Amplifiers.
44	SWN	P	PVGL Inverting Buck-Boost Converter Switching Node.
Exposed Pad	—	P	Thermal Pad. It is the ground reference for the device and also the thermal pad to conduct heat from the device (not suitable for high current return). Tie externally to the PCB ground plane (GND). Thermal vias under the pad are needed to conduct the heat to the PCB ground planes.

NOTE: I = input, O = output, I/O = input or output, P = Power, G = ground.

TYPICAL APPLICATION

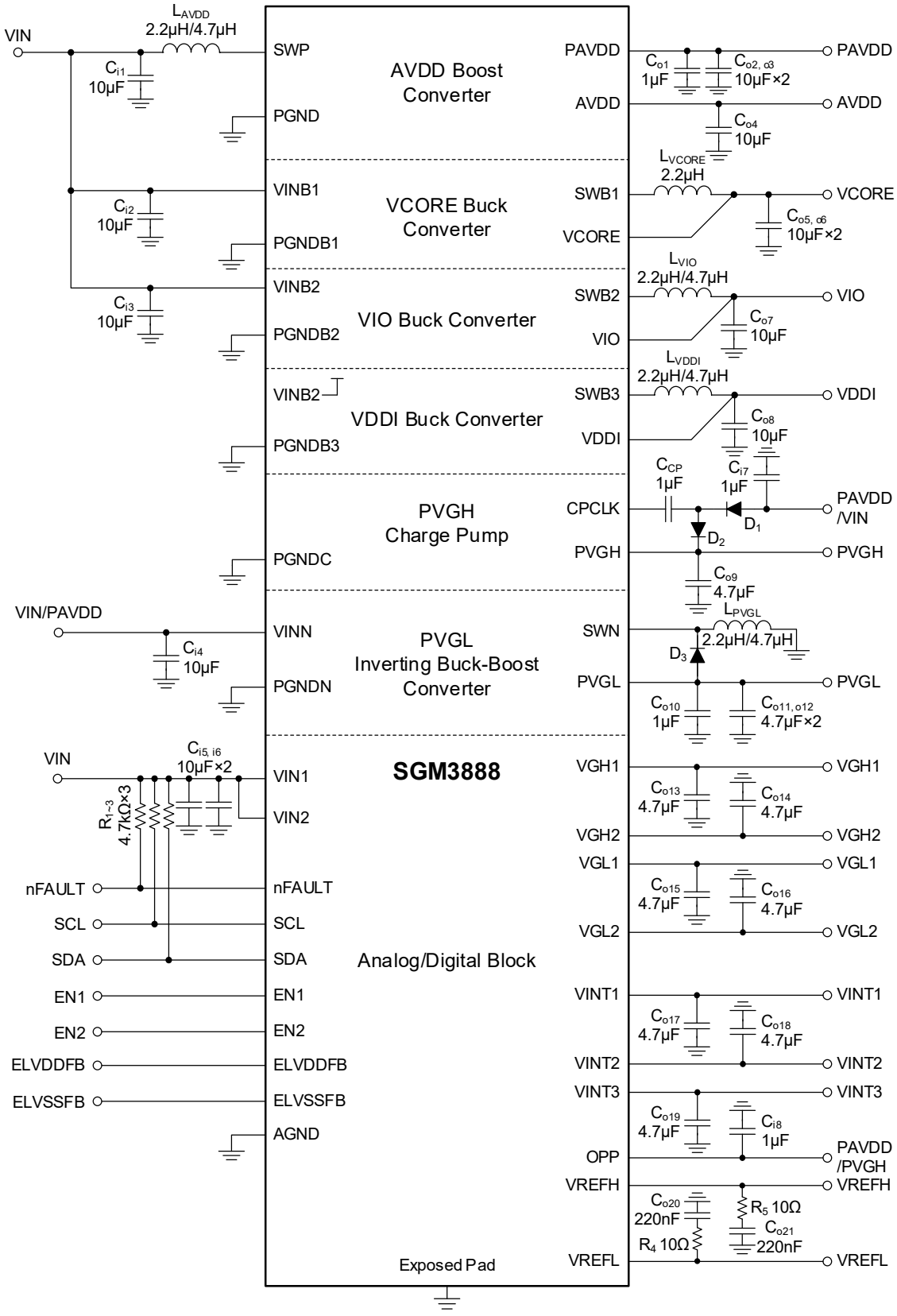


Figure 1. Typical Application Circuit

RECOMMENDED COMPONENT SELECTION

Table 1. Recommended Component Selection for SGM3888

Component	Value	Number	Electrical Spec	Part Number	Manufacturer
C_{i1} ~ C_{i6}	10μF	6	X5R, 6.3V, 0402	GRM155R60J106ME15	Murata
C_{o19}	4.7μF	1	X5R, 16V, 0402	GRM155R61C475ME01	Murata
C_{i7}, C_{o1}, C_{CP}	1μF	3	X5R, 16V, 0402	GRM155B31C105MA12	Murata
C_{o2} ~ C_{o4}	10μF	3	X5R, 25V, 0603	GRM188R61E106MA73	Murata
C_{o5} ~ C_{o8}	10μF	4	X5R, 6.3V, 0402	GRM155R60J106ME15	Murata
C_{o9}, C_{o11} ~ C_{o18}	4.7μF	9	X5R, 35V, 0603	GRM188R6YA475ME15	Murata
C_{i8}, C_{o10}	1μF	2	X5R, 35V, 0402	GRM155R6YA105ME11	Murata
C_{o20} ~ C_{o21}	220nF	2	X5R, 35V, 0402	GRM155R6YA224KE01	Murata
L_{AVDD}, L_{PVGL}	2.2μH	2	3.7A, 67mΩ, 252012	HTEG25201B-2R2MIR	Cyntec
	4.7μH		3.4A, 75mΩ, 322520	VCTA32252T-4R7MS6	Cyntec
L_{VCORE}	2.2μH	1	3.7A, 67mΩ, 252012	HTEG25201B-2R2MIR	Cyntec
L_{VIO}, L_{VDDI}	2.2μH	2	2.7A, 84mΩ, 201608	HTEK20160H-2R2MSR	Cyntec
	4.7μH		3.4A, 75mΩ, 322520	VCTA32252T-4R7MS6	Cyntec
R_1 ~ R_3	4.7kΩ	3	4.7kΩ, 0402	/	/
R_4 ~ R_5	10Ω	2	10Ω, 0402	/	/
D_1 ~ D_3		3	40V, 2A, SOD123HP	PMEG4020EXE	Nexperia

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, V_{VCORE} = 0.9V, V_{VIO} = 1.8V, V_{VDDI} = 1.2V, V_{AVDD} = 7.6V, V_{PVGL} = -11V, $V_{VGH1/2}$ = 10V, $V_{VGL1/2}$ = -10V, $V_{VINT1/2}$ = -6V, V_{VINT3} = 7.2V, V_{VREFH} = 6.8V, V_{VREFL} = 1.5V, f_{SW} = 1MHz, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
General						
VINx Supply Voltage Range	V_{IN}		2.7	3.3	4.8	V
Under-Voltage Lockout into VIN	V_{UVLO_H}	V_{IN} rising	2.2	2.35	2.5	V
	V_{UVLO_F}	V_{IN} falling	2	2.15	2.3	V
Quiescent Current into VIN	I_{Q_NOSW}	No switching		3	5	mA
	I_{Q_SW}	No load, all outputs on		8		mA
Switching Frequency	f_{OSC}	Frequency = 000b		0.6		MHz
		Frequency = 001b		0.9		
		Frequency = 010b		1.0		
		Frequency = 011b		1.2		
		Frequency = 100b		1.5		
		Frequency = 101b		1.8		
		Frequency = 110b		2.0		
		Frequency = 111b		2.2		
Switching Frequency Accuracy	f_{OSCACC}		-17		17	%
Switching Frequency Spread Spectrum		SS_CLK[1:0] = 01b	-3		3	%
		SS_CLK[1:0] = 10b	-6		6	
Under-Voltage Protection Percentage	UVP	Percentage of target output voltage	55	70	85	%
UVP Detection Time	t_{UVP}			2		ms
Short-Circuit Protection Percentage	SCP	Percentage of target output voltage		30		%
SCP Detection Time	t_{SCP}			15		μs
Thermal Shutdown	T_{SD}	Temperature rising		150		℃
	Δ_{TSD}	Hysteresis		15		℃
Logic Inputs (SDA, SCL, EN1, EN2)						
Input Logic High	V_{IH}		0.9			V
Input Logic Low	V_{IL}				0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, V_{VCORE} = 0.9V, V_{VIO} = 1.8V, V_{VDDI} = 1.2V, V_{AVDD} = 7.6V, V_{PVGL} = -11V, $V_{VGH1/2}$ = 10V, $V_{VGL1/2}$ = -10V, $V_{VINT1/2}$ = -6V, V_{VINT3} = 7.2V, V_{VREFH} = 6.8V, V_{VREFL} = 1.5V, f_{SW} = 1MHz, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Boost Converter (PAVDD)							
Output Voltage Range	V_{PAVDD}	5.5V to 10.55V with 50mV/step		5.5	7.6	10.55	V
Output Voltage Accuracy (1)	P_{PAVDD_ACC}	V_{IN} = 3.3V, all output voltage	T_J = +25℃	-1		1	%
			T_J = -40℃ to +85℃	-2		2	
Maximum Duty	$D_{MAXPAVDD}$				90		%
Over-Voltage Protection	OVP_{PAVDD}	PAVDD rising		112	120	128	%
	OVP_{PAVDD_HYS}				0.5		V
SW_{PAVDD} Current Limit	I_{PAVDD_LIM}	Inductor peak current, PAVDD_CL[1:0] = 10b			4.4		A
Low-side R_{ON}	$R_{DS(ON)\_PAVDD\_1}$	I_{PAVDD} = 100mA			50		mΩ
High-side R_{ON}	$R_{DS(ON)\_PAVDD\_2}$	I_{PAVDD} = 100mA			140		mΩ
Maximum Output Current	I_{PAVDD_MAX}	V_{IN} = 3.5V to 4.8V, all output voltage, PAVDD_CL[1:0] = 11b, T_A = -40℃ to +85℃		700			mA
		V_{IN} = 2.7V to 4.8V, V_{PAVDD} = 7.6V, PAVDD_CL[1:0] = 11b, T_A = -40℃ to +85℃		800			
Efficiency	EFF_{PAVDD}	V_{IN} = 3.3V, V_{PAVDD} = 7.6V, L = 2.2μH, I_{PAVDD} = 100mA			91.5		%
Soft-Start Time	t_{PAVDD_SS}				5		ms
Power On Delay Time	$t_{PAVDD\_ON\_DLY}$	Follow EN2 rising, programmable range		1		15	ms
Power Off Delay Time	$t_{PAVDD\_OFF\_DLY}$	Follow EN2 falling, programmable range		11		32	ms
Output Ripple	V_{PAVDD_RIPPLE}	Full range			70		mV_{PP}
Load Regulation	$V_{PAVDD\_LOADREG}$	I_{PAVDD} = 0mA to 700mA	T_A = +25℃	-1		1	%/A
			T_A = -40℃ to +85℃	-2		2	
Line Regulation	$V_{PAVDD\_LINEREG}$	V_{IN} = 2.7V to 4.8V		-0.3		0.3	%/V
Pass Transistor (AVDD)							
Output Voltage Range	V_{AVDD}	5.5V to 10.55V with 50mV/step		5.5	7.6	10.55	V
Output Voltage Accuracy (1)	V_{AVDD_ACC}	V_{IN} = 3.3V, all output voltage	T_J = +25℃	-1		1	%
			T_J = -40℃ to +85℃	-2		2	
Pass Transistor R_{ON}	$R_{DS(TR)\_AVDD}$	I_{AVDD} = 100mA			150		mΩ
Maximum Output Current	I_{AVDD_MAX}	V_{IN} = 3.5V to 4.8V, all output voltage, PAVDD_CL[1:0] = 11b, T_A = -40℃ to +85℃		700			mA
		V_{IN} = 2.7V to 4.8V, V_{PAVDD} = 7.6V, PAVDD_CL[1:0] = 11b, T_A = -40℃ to +85℃		800			
Soft-Start Time	t_{AVDD_SS}	Max soft-start setting time, programmable range, 1ms/step		4		7	ms
Power On Delay Time	$t_{AVDD\_ON\_DLY}$	Follow EN2 rising, programmable range		11		32	ms
Power Off Delay Time	$t_{AVDD\_OFF\_DLY}$	Follow EN2 falling, programmable range		3		9	ms
Output Ripple	V_{AVDD_RIPPLE}	Full range			35		mV_{PP}
AVDD Discharge Resistance	$R_{AVDD(DCG)}$				25		Ω
AVDD Output Capacitance	C_{AVDD_MAX}	Effective capacitance under 3V DC voltage				90	μF

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, V_{VCORE} = 0.9V, V_{VIO} = 1.8V, V_{VDDI} = 1.2V, V_{AVDD} = 7.6V, V_{PVGL} = -11V, $V_{VGH1/2}$ = 10V, $V_{VGL1/2}$ = -10V, $V_{VINT1/2}$ = -6V, V_{VINT3} = 7.2V, V_{VREFH} = 6.8V, V_{VREFL} = 1.5V, f_{SW} = 1MHz, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Buck Converter 1 (VCORE)							
Output Voltage Range	V_{VCORE}	0.6V to 1.5V with 25mV/step		0.6	0.9	1.5	V
Output Voltage Accuracy (1)	V_{VCORE_ACC}	V_{IN} = 3.3V, all output voltage	T_J = +25℃	-1		1	%
			T_J = -40℃ to +85℃	-2		2	
SWB1 Current Limit	I_{SWB1_LIM}	Inductor peak current, VCORE_CL[1:0] = 10b			3		A
Low-side R_{ON}	$R_{DS(ON)\_VCORE\_1}$	I_{VCORE} = 100mA			80		mΩ
High-side R_{ON}	$R_{DS(ON)\_VCORE\_2}$	I_{VCORE} = 100mA			130		mΩ
Maximum Output Current	I_{VCORE_MAX}	V_{IN} = 2.7V to 4.8V, all output voltage, VCORE_CL[1:0] = 11b, T_A = -40℃ to +85℃		2500			mA
Output Ripple	V_{VCORE_RIPPLE}	Full range			5		mV_{PP}
Load Regulation	$V_{VCORE\_LOADREG}$	I_{VCORE} = 0mA to 2000mA	T_A = +25℃	-1		1	%/A
			T_A = -40℃ to +85℃	-2		2	
Line Regulation	$V_{VCORE\_LINEREG}$	V_{IN} = 2.7V to 4.8V		-0.3		0.3	%/V
Efficiency	EFF_{VCORE}	V_{IN} = 3.3V, V_{VCORE} = 0.9V, L = 2.2μH, I_{VCORE} = 600mA			87.9		%
Soft-Start Time	t_{VCORE_SS}				1		ms
Power On Delay Time	$t_{VCORE\_ON\_DLY}$	Follow EN1 rising, programmable range		0.5		3.5	ms
Power Off Delay Time	$t_{VCORE\_OFF\_DLY}$	Follow EN1 falling, programmable range		3		17	ms
VCORE Discharge Resistance	$R_{VCORE(DCG)}$				50		Ω
Buck Converter 2 (VIO)							
Output Voltage Range	V_{VIO}	1V to 1.95V with 50mV/step		1	1.8	1.95	V
Output Voltage Accuracy (1)	V_{VIO_ACC}	V_{IN} = 3.3V, all output voltage	T_J = +25℃	-1		1	%
			T_J = -40℃ to +85℃	-2		2	
SWB2 Current Limit	I_{SWB2_LIM}	Inductor peak current, VIO_CL[1:0] = 10b			1.9		A
Low-side R_{ON}	$R_{DS(ON)\_VIO\_1}$	I_{VIO} = 100mA			140		mΩ
High-side R_{ON}	$R_{DS(ON)\_VIO\_2}$	I_{VIO} = 100mA			200		mΩ
Maximum Output Current	I_{VIO_MAX}	V_{IN} = 2.7V to 4.8V, all output voltage, VIO_CL[1:0] = 11b, T_A = -40℃ to +85℃		1500			mA
Output Ripple	V_{VIO_RIPPLE}	Full range			8		mV_{PP}
Load Regulation	$V_{VIO\_LOADREG}$	I_{VIO} = 0mA to 500mA	T_A = +25℃	-1		1	%/A
			T_A = -40℃ to +85℃	-2		2	
Line Regulation	$V_{VIO\_LINEREG}$	V_{IN} = 2.7V to 4.8V		-0.3		0.3	%/V
Efficiency	EFF_{VIO}	V_{IN} = 3.3V, V_{VIO} = 1.8V, L = 2.2μH, I_{VIO} = 100mA			93		%
Soft-Start Time	t_{VIO_SS}				2		ms
Power On Delay Time	$t_{VIO\_ON\_DLY}$	Follow EN1 rising, programmable range		0.5		3.5	ms
Power Off Delay Time	$t_{VIO\_OFF\_DLY}$	Follow EN1 falling, programmable range		3		17	ms
VIO Discharge Resistance	$R_{VIO(DCG)}$				50		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, V_{VCORE} = 0.9V, V_{VIO} = 1.8V, V_{VDDI} = 1.2V, V_{AVDD} = 7.6V, V_{PVGL} = -11V, $V_{VGH1/2}$ = 10V, $V_{VGL1/2}$ = -10V, $V_{VINT1/2}$ = -6V, V_{VINT3} = 7.2V, V_{VREFH} = 6.8V, V_{VREFL} = 1.5V, f_{SW} = 1MHz, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Buck Converter 3 (VDDI)							
Output Voltage Range	V_{VDDI}	1V to 1.95V with 50mV/step		1	1.2	1.95	V
Output Voltage Accuracy (1)	V_{VDDI_ACC}	V_{IN} = 3.3V, all output voltage	T_J = +25℃	-1		1	%
			T_J = -40℃ to +85℃	-2		2	
SWB3 Current Limit	I_{SWB3_LIM}	Inductor peak current, VDDI_CL[1:0] = 10b			1.9		A
Low-side R_{ON}	$R_{DS(ON)\_VDDI\_1}$	I_{VDDI} = 100mA			140		mΩ
High-side R_{ON}	$R_{DS(ON)\_VDDI\_2}$	I_{VDDI} = 100mA			200		mΩ
Maximum Output Current	I_{VDDI_MAX}	V_{IN} = 2.7V to 4.8V, all output voltage, VDDI_CL[1:0] = 11b, T_A = -40℃ to +85℃		1500			mA
Output Ripple	V_{VDDI_RIPPLE}	Full range			8		mV_{PP}
Load Regulation	$V_{VDDI\_LOADREG}$	I_{VDDI} = 0mA to 500mA	T_A = +25℃	-1		1	%/A
			T_A = -40℃ to +85℃	-2		2	
Line Regulation	$V_{VDDI\_LINEREG}$	V_{IN} = 2.7V to 4.8V		-0.3		0.3	%/V
Efficiency	EFF_{VDDI}	V_{IN} = 3.3V, V_{VDDI} = 1.2V, L = 2.2μH, I_{VDDI} = 100mA			90.6		%
Soft-Start Time	t_{VDDI_SS}				1		ms
Power On Delay Time	$t_{VDDI\_ON\_DLY}$	Follow EN1 rising, programmable range		0.5		3.5	ms
Power Off Delay Time	$t_{VDDI\_OFF\_DLY}$	Follow EN1 falling, programmable range		3		17	ms
VDDI Discharge Resistance	$R_{VDDIO(DCG)}$				50		Ω
Positive OP Amplifier (VGH1/2)							
Output Voltage Range	$V_{VGH1/2}$	4V to 19.9V with 0.1V/step		4	10	19.9	V
Output Voltage Accuracy (1)	$V_{VGH1/2\_ACC}$	V_{IN} = 3.3V, $V_{VGH1/2}$ = 4V to 18V, T_J = +25℃		-1		1	%
		V_{IN} = 3.3V, $V_{VGH1/2}$ = 18V to 19.9V, T_J = +25℃		-1.3		1.3	
		V_{IN} = 3.3V, all output voltage, T_J = -40℃ to +85℃		-2		2	
Maximum Output Current	$I_{VGH1/2\_MAX}$			70			mA
Soft-Start Time	$t_{VGH1/2\_SS}$	V_{VGH} = 10V (can be option as 5.6ms)			1.4		ms
Power On Delay Time	$t_{VGH1/2\_ON\_DLY}$	Follow EN2 rising		3		17	ms
Power Off Delay Time	$t_{VGH1/2\_OFF\_DLY}$	Follow EN2 falling		11		32	ms
VGH Discharge Resistance	$R_{VGH(DCG)}$				270		Ω
Positive OP Amplifier (VINT3)							
Output Voltage Range	V_{VINT3}	1V to 10V with 10mV/step		1	7.2	10	V
Output Voltage Accuracy (1)	V_{VINT3_ACC}	V_{IN} = 3.3V, all output voltage	T_J = +25℃	-100		100	mV
			T_J = -40℃ to +85℃	-200		200	
Maximum Output Current	I_{VINT3_MAX}			50			mA
Soft-Start Time	t_{VINT3_SS}	V_{IN} = 2.7V to 4.8V, V_{VINT3} = 7.2V (can be option as 4.4ms)			1		ms
Power On Delay Time	$t_{VINT3\_ON\_DLY}$	Follow EN2 rising, programmable range		11		32	ms
Power Off Delay Time	$t_{VINT3\_OFF\_DLY}$	Follow EN2 falling, programmable range		3		17	ms
Discharge Resistance	$R_{VINT3\ (DCG)}$				230		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, V_{VCORE} = 0.9V, V_{VIO} = 1.8V, V_{VDDI} = 1.2V, V_{AVDD} = 7.6V, V_{PVGL} = -11V, $V_{VGH1/2}$ = 10V, $V_{VGL1/2}$ = -10V, $V_{VINT1/2}$ = -6V, V_{VINT3} = 7.2V, V_{VREFH} = 6.8V, V_{VREFL} = 1.5V, f_{SW} = 1MHz, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Positive OP Amplifier (VREFH/L)							
Output Voltage Range	V_{VREFH}	4.4V to 9.5V with 10mV/step		4.4	6.8	9.5	V
	V_{VREFL}	0.5V to 5.5V with 10mV/step		0.5	1.5	5.5	V
Output Voltage Accuracy (1)	V_{VREFH/L_ACC}	V_{IN} = 3.3V, all output voltage	T_J = +25℃	-100		100	mV
			T_J = -40℃ to +85℃	-200		200	
Soft-Start Time	t_{VREFH_SS}	2.7V < V_{IN} < 4.8V, V_{VREFH} = 6.8V (can be option as 3.9ms)			0.5		ms
	t_{VREFL_SS}	2.7V < V_{IN} < 4.8V, V_{VREFL} = 1.5V (can be option as 3.9ms)			0.5		
Maximum Output Current	I_{VREFH/L_MAX}			50			mA
Power On Delay Time	t_{VREFH/L_ON_DLY}	Follow EN2 rising, programmable range		12		33	ms
Power Off Delay Time	t_{VREFH/L_OFF_DLY}	Follow EN2 falling, programmable range		3		17	ms
VREFH Discharge Resistance	$R_{VREFH(DCG)}$				450		Ω
VREFL Discharge Resistance	$R_{VREFL(DCG)}$				250		Ω
Inverting Buck-Boost Converter (PVGL)							
Output Voltage Range	V_{PVGL}	-22V to -6V with 0.1V/step		-22	-11	-6	V
Output Voltage Accuracy (1)	V_{PVGL_ACC}	V_{IN} = 3.3V, all output voltage	T_J = +25℃	-1		1	%
			T_J = -40℃ to +85℃	-2		2	
Maximum Duty	D_{MAXVGL}				90		%
SW_{PVGL} Current Limit	I_{PVGL_LIM}	Inductor peak current, PVGL_CL[1:0] = 10b			3		A
High-side R_{ON}	$R_{DS(ON)\_PVGL}$	I_{PVGL} = 100mA			130		mΩ
Maximum Output Current	I_{PVGL_MAX}	V_{IN} = 3.5V to 4.8V, all output voltage, PVGL_CL[1:0] = 11b, T_A = -40℃ to +85℃		250			mA
		V_{IN} = 2.7V to 4.8V, V_{PVGL} = -11V, PVGL_CL[1:0] = 11b, T_A = -40℃ to +85℃		280			
Load Regulation	$V_{PVGL\_LOADREG}$	I_{PVGL} = 0mA to 250mA	T_A = +25℃	-1		1	%/A
			T_A = -40℃ to +85℃	-2		2	
Line Regulation	$V_{PVGL\_LINEREG}$	V_{IN} = 2.7V to 4.8V		-0.3		0.3	%/V
Efficiency	EFF_{PVGL}	V_{IN} = 3.3V, V_{PVGL} = -11V, L = 2.2μH, I_{PVGL} = 150mA			84.7		%
Soft-Start Time	t_{PVGL_SS}				4		ms
Power On Delay Time	$t_{PVGL\_ON\_DLY}$	Follow EN2 rising, programmable range		1		15	ms
Power Off Delay Time	$t_{PVGL\_OFF\_DLY}$	Follow EN2 falling, programmable range		11		32	ms
PVGL Discharge Resistance	$R_{PVGL(DCG)}$				100		Ω
Negative OP Amplifier (VGL1/2)							
Output Voltage Range	$V_{VGL1/2}$	-21V to -2V with 0.1V/step		-21	-10	-2	V
Output Voltage Accuracy (1)	$V_{VGL1/2\_ACC}$	V_{IN} = 3.3V, $V_{VGL1/2}$ = -10V to -2V	T_J = +25℃	-100		100	mV
			T_J = -40℃ to +85℃	-200		200	
		V_{IN} = 3.3V, $V_{VGL1/2}$ = -21V to -10V	T_J = +25℃	-1		1	%
			T_J = -40℃ to +85℃	-2		2	
Maximum Output Current	$I_{VGL1/2\_MAX}$			70			mA
Soft-Start Time	$t_{VGL1/2\_SS}$	$V_{VGL1/2}$ = -10V (can be option as 5.07ms)			2.53		ms
Power On Delay Time	$t_{VGL1/2\_ON\_DLY}$	Follow EN2 rising, programmable range		3		17	ms
Power Off Delay Time	$t_{VGL1/2\_OFF\_DLY}$	Follow EN2 falling, programmable range		11		32	ms
VGL Discharge Resistance	$R_{PVGL(DCG)}$				50		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, V_{VCORE} = 0.9V, V_{VIO} = 1.8V, V_{VDDI} = 1.2V, V_{AVDD} = 7.6V, V_{PVGL} = -11V, $V_{VGH1/2}$ = 10V, $V_{VGL1/2}$ = -10V, $V_{VINT1/2}$ = -6V, V_{VINT3} = 7.2V, V_{VREFH} = 6.8V, V_{VREFL} = 1.5V, f_{SW} = 1MHz, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Negative OP Amplifier (Negative VINT1/2)							
Output Voltage Range	$V_{VINT1/2}$	-19V to -0.5V with 10mV/step		-19	-6	-0.5	V
Output Voltage Total Accuracy (1)	$V_{VINT1/2\_ACC}$	V_{IN} = 3.3V, all output voltage	T_J = +25℃	-100		100	mV
			T_J = -40℃ to +85℃	-200		200	
Maximum Output Current	$I_{VINT1/2\_MAX}$			50			mA
Soft-Start Time	$t_{VINT1/2\_SS}$	$V_{VINT1/2}$ = -6V			3.7		ms
Power On Delay Time	$t_{VINT1/2\_ON\_DLY}$	Follow EN2 rising, programmable range		11		32	ms
Power Off Delay Time	$t_{VINT1/2\_OFF\_DLY}$	Follow EN2 falling, programmable range		3		17	
Discharge Resistance	$R_{VINT1/2(DCG)}$				50		Ω

NOTE:

1. The output voltage accuracy parameters are initial accuracy values.

I²C INTERFACE TIMING CHARACTERISTICS (1)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		FAST MODE PLUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}		100	100	400		1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$	4		0.6		0.26		μs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		0.5		μs
High Period of SCL Clock	t_{HIGH}	4		0.6		0.26		μs
Setup Time for a Repeated START Condition	$t_{SU;STA}$	4.7		0.6		0.26		μs
Data Setup Time	$t_{SU;DATA}$	250		100		50		ns
Data Hold Time	$t_{HD;DATA}$	0		0		0		μs
Rising Time of SCL Clock	t_{RCL}		1000	20	300		120	ns
Falling Time of SCL Clock	t_{FCL}		300		300		120	ns
Rising Time of SDA Clock	t_{RDA}		1000	20	300		120	ns
Falling Time of SDA Clock	t_{FDA}		300		300		120	ns
Setup Time for STOP Condition	$t_{SU;STO}$	4		0.6		0.26		μs
Bus Free Time between a STOP and a START Condition	t_{BUF}	4.7		1.3		0.5		μs
Noise Margin at LOW	V_{nL}	0.1 × V_{VIO}		0.1 × V_{VIO}		0.1 × V_{VIO}		V
Noise Margin at HIGH	V_{nH}	0.2 × V_{VIO}		0.2 × V_{VIO}		0.2 × V_{VIO}		V
Pulse Width of Spikes must be Suppressed by the Input Filter	t_{SP}	0	50	0	50	0	50	ns
Data Valid Time	t_{VD_DAT}		3.45		0.9		0.45	μs
Data Valid Acknowledge Time	t_{VD_ACK}		3.45		0.9		0.45	μs

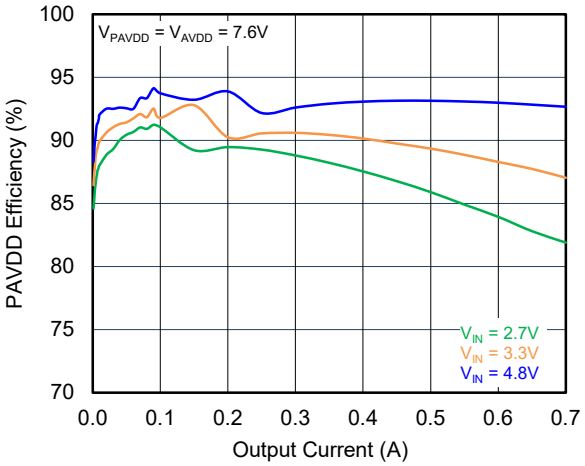
NOTE:

1. Industry standard I²C timing characteristics are according to I²C-Bus Specification. Not tested in production.

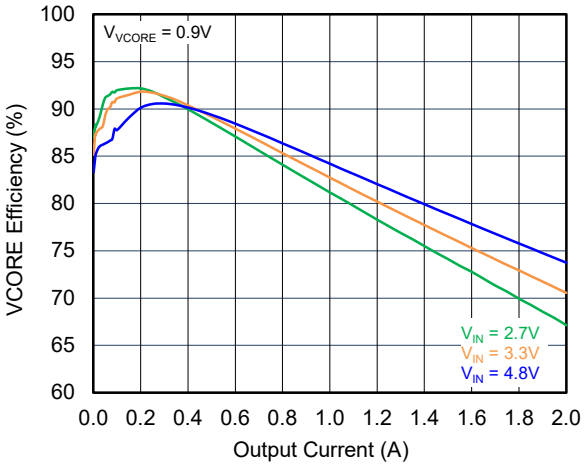
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, L_{AVDD} = L_{PVGL} = L_{VCORE} = 2.2μH (HTEG25201B-2R2MIR), L_{VIO} = L_{VDDI} = 2.2μH (HTEK20160H-2R2MSR), unless otherwise noted.

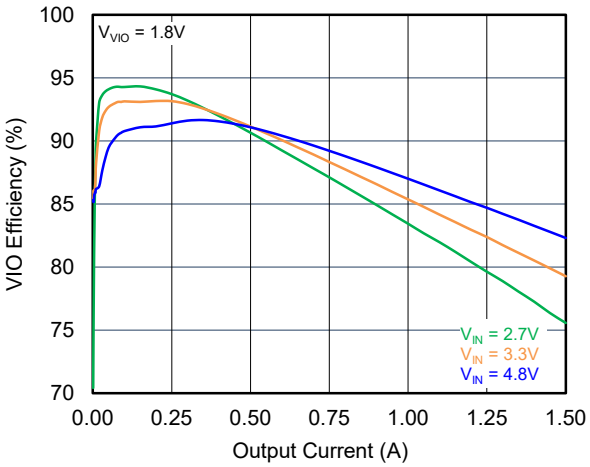
PAVDD Efficiency vs. Output Current



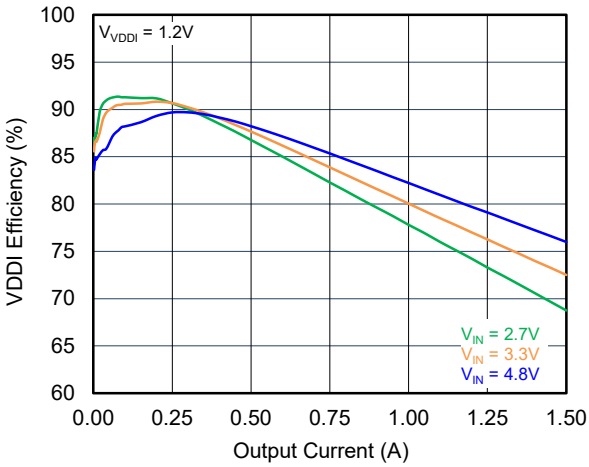
VCORE Efficiency vs. Output Current



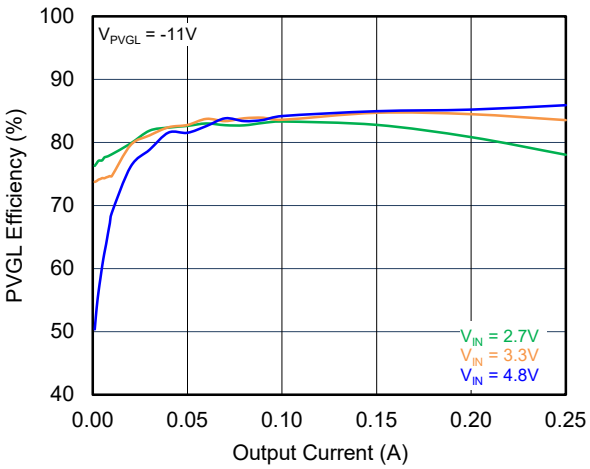
VIO Efficiency vs. Output Current



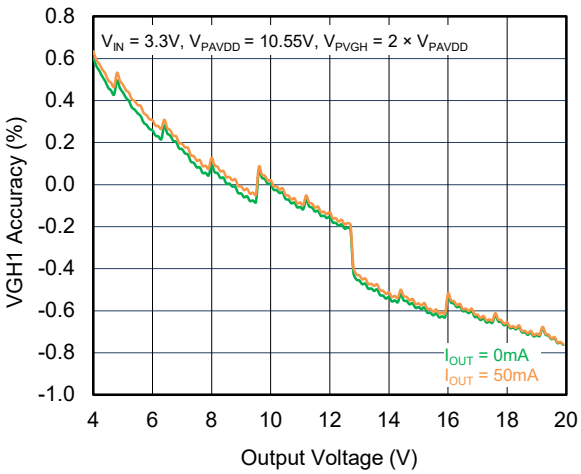
VDDI Efficiency vs. Output Current



PVGL Efficiency vs. Output Current



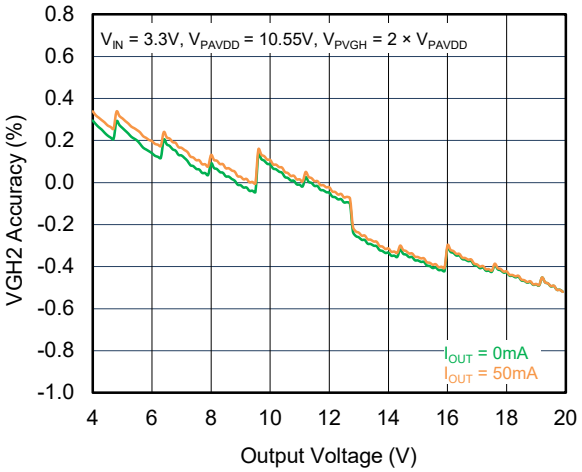
VGH1 Accuracy vs. Output Voltage



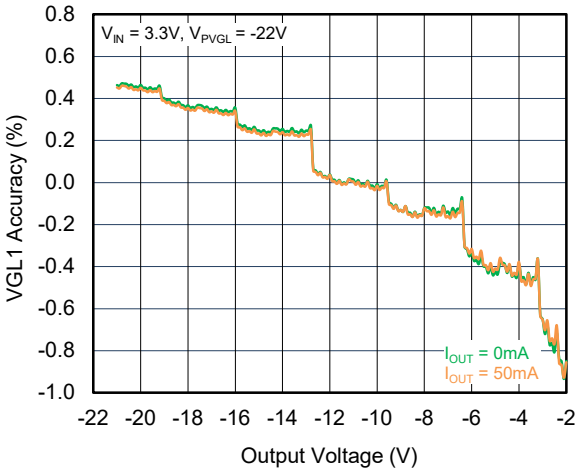
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, L_{AVDD} = L_{PVGL} = L_{VCORE} = 2.2μH (HTEG25201B-2R2MIR), L_{VIO} = L_{VDDI} = 2.2μH (HTEK20160H-2R2MSR), unless otherwise noted.

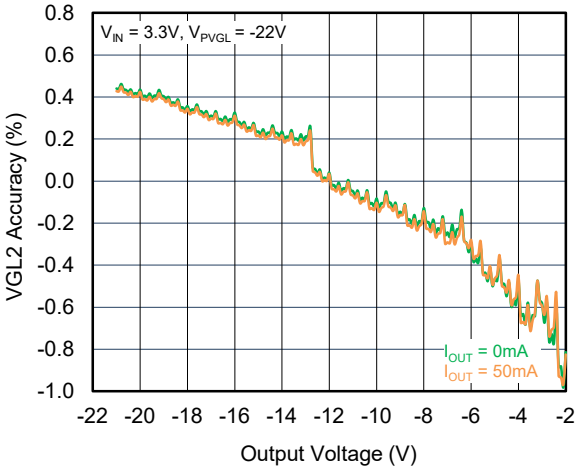
VGH2 Accuracy vs. Output Voltage



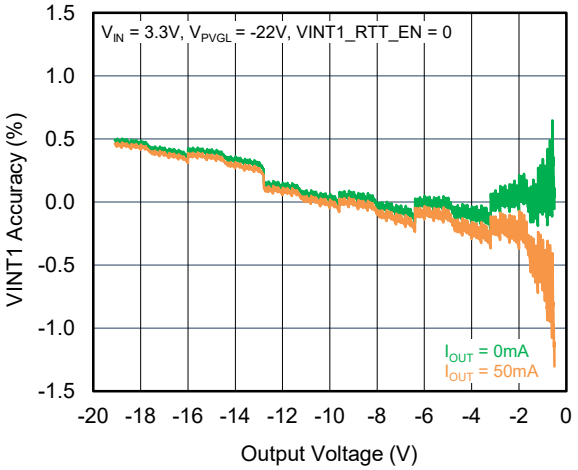
VGL1 Accuracy vs. Output Voltage



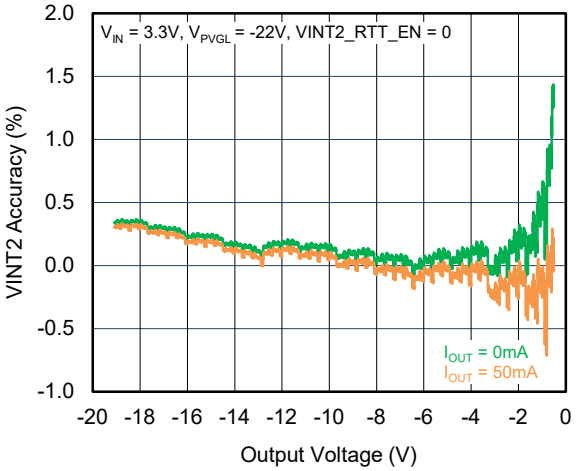
VGL2 Accuracy vs. Output Voltage



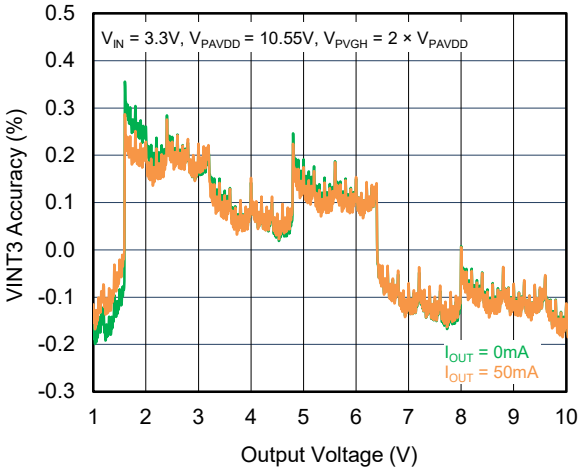
VINT1 Accuracy vs. Output Voltage



VINT2 Accuracy vs. Output Voltage



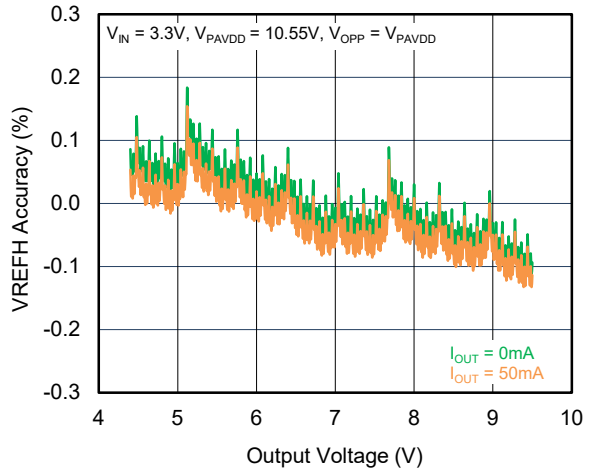
VINT3 Accuracy vs. Output Voltage



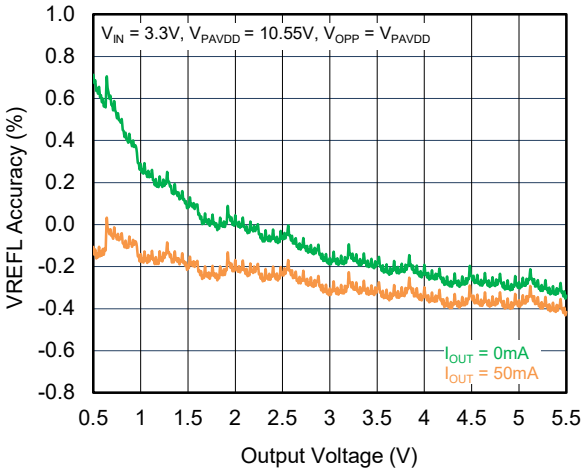
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, L_{AVDD} = L_{PVGL} = L_{VCORE} = 2.2μH (HTEG25201B-2R2MIR), L_{VIO} = L_{VDDI} = 2.2μH (HTEK20160H-2R2MSR), unless otherwise noted.

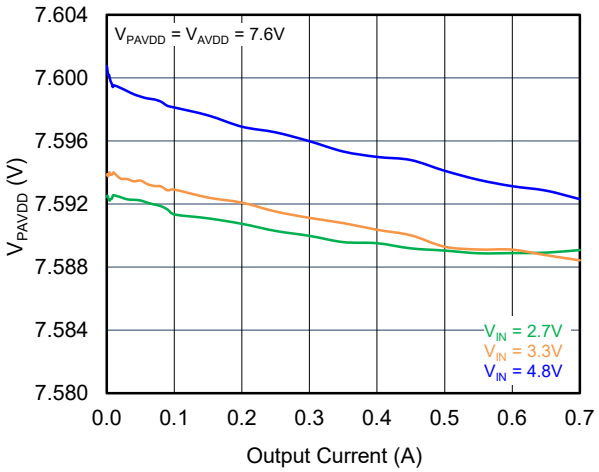
VREFH Accuracy vs. Output Voltage



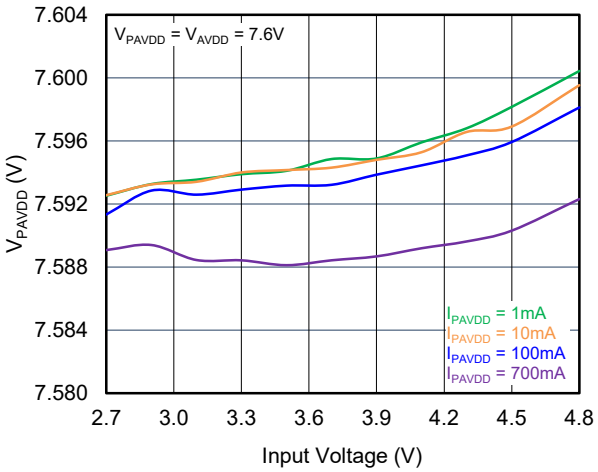
VREFL Accuracy vs. Output Voltage



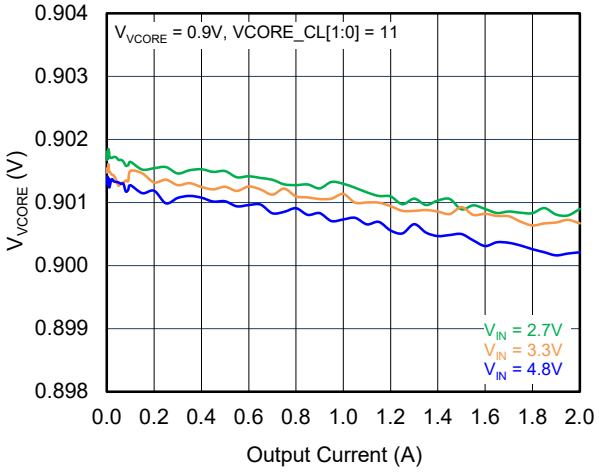
PAVDD Load Regulation



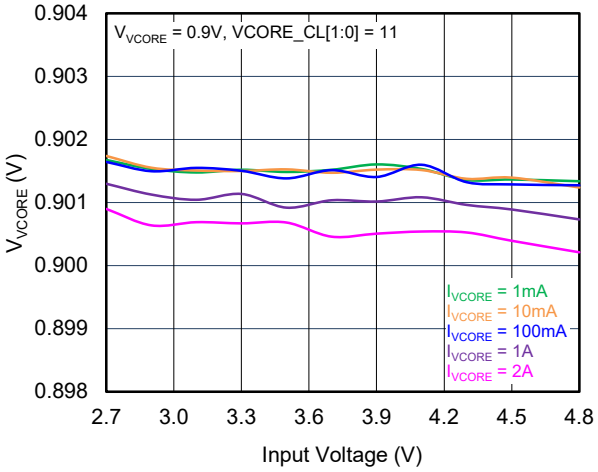
PAVDD Line Regulation



VCORE Load Regulation



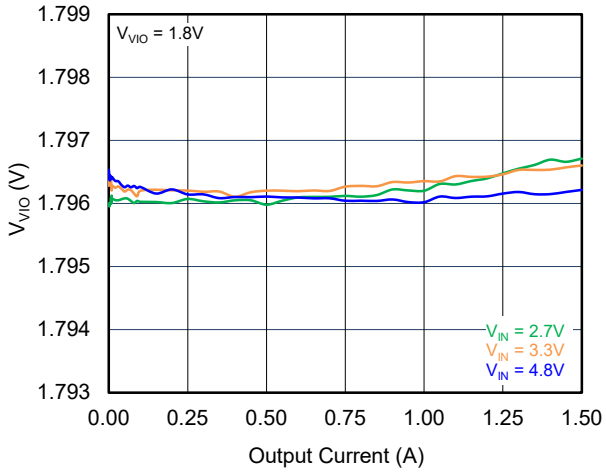
VCORE Line Regulation



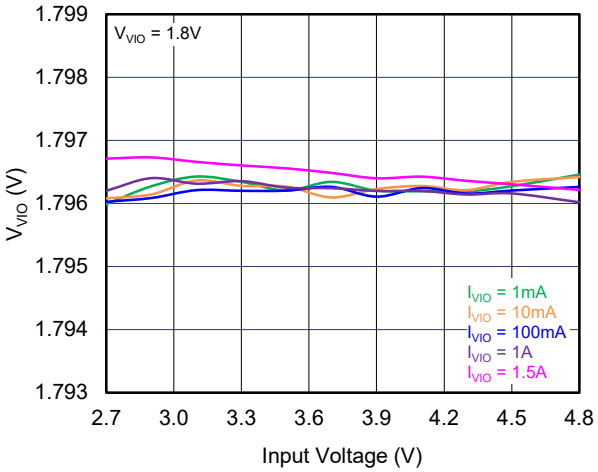
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, L_{AVDD} = L_{PVGL} = L_{VCORE} = 2.2μH (HTEG25201B-2R2MIR), L_{VIO} = L_{VDDI} = 2.2μH (HTEK20160H-2R2MSR), unless otherwise noted.

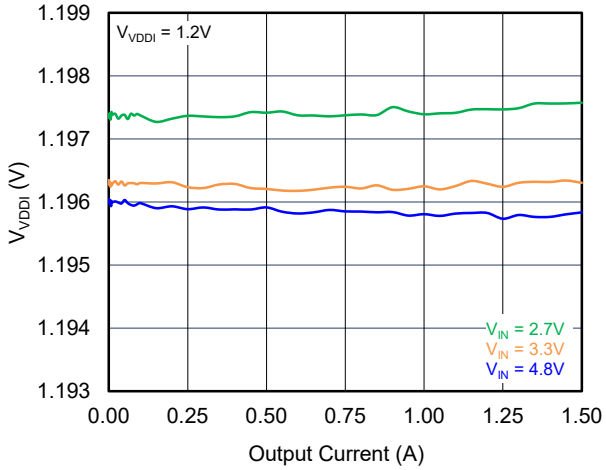
VIO Load Regulation



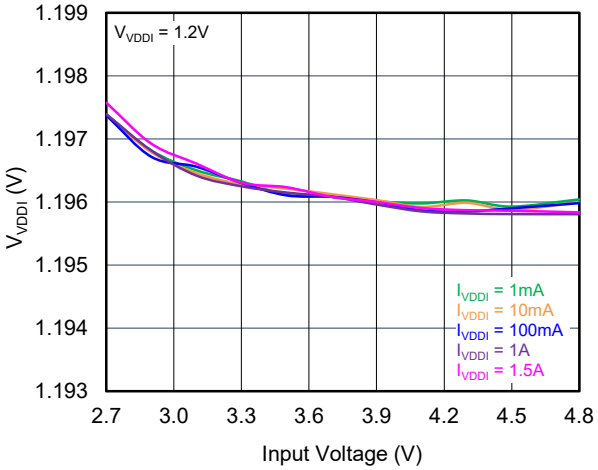
VIO Line Regulation



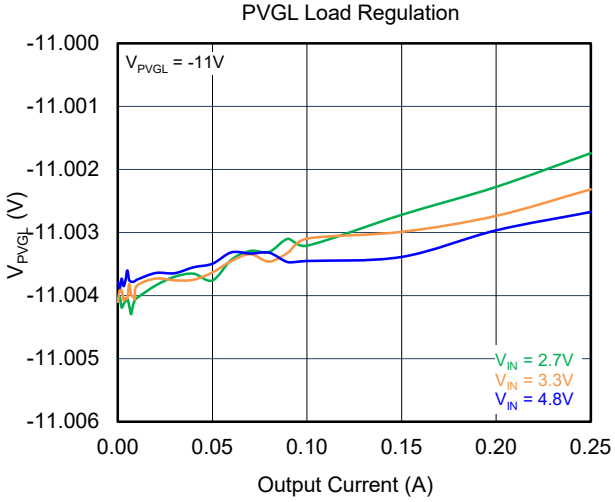
VDDI Load Regulation



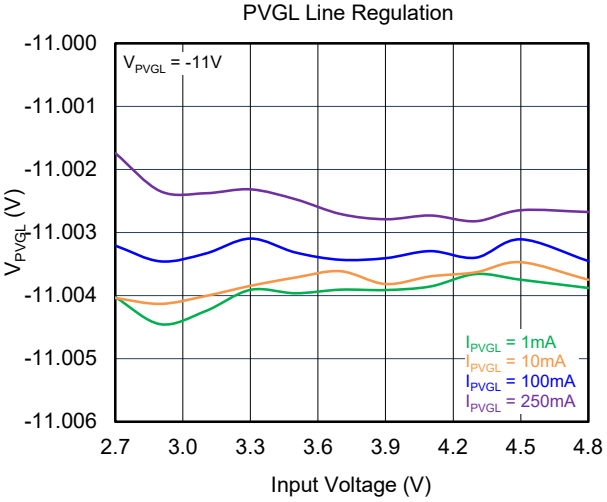
VDDI Line Regulation



PVGL Load Regulation



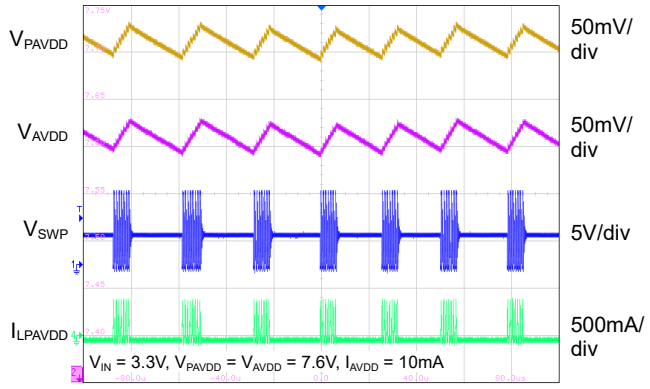
PVGL Line Regulation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

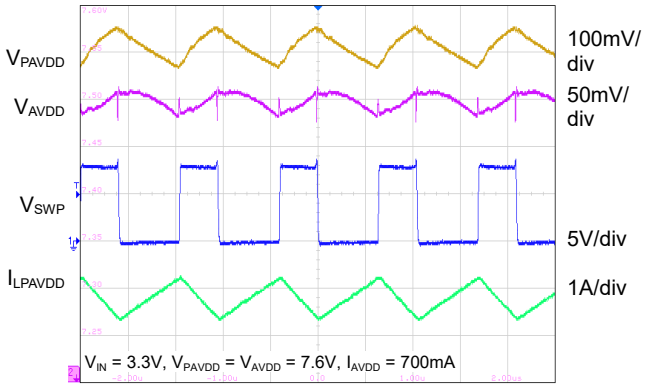
T_A = +25℃, L_{AVDD} = L_{PVGL} = L_{VCORE} = 2.2μH (HTEG25201B-2R2MIR), L_{VIO} = L_{VDDI} = 2.2μH (HTEK20160H-2R2MSR), unless otherwise noted.

PAVDD and AVDD Output Voltage Ripple at 10mA Load



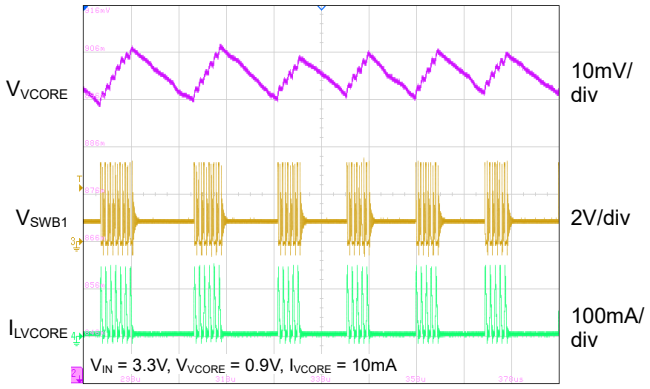
Time (20μs/div)

PAVDD and AVDD Output Voltage Ripple at 700mA Load



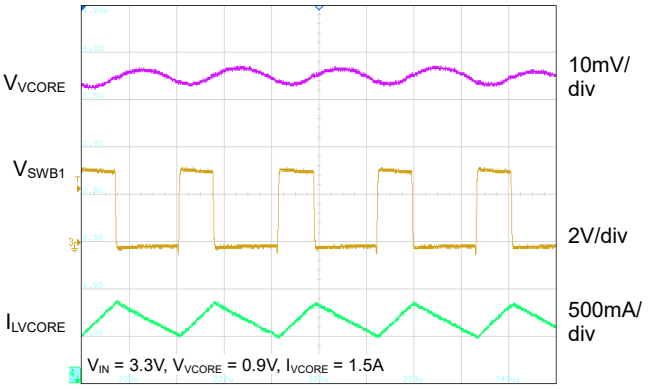
Time (500ns/div)

VCORE Output Voltage Ripple at 10mA Load



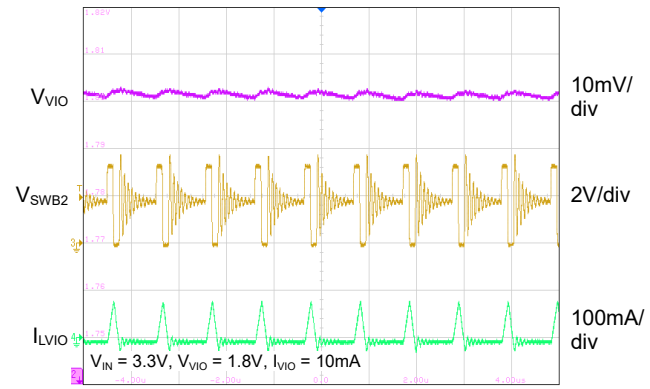
Time (10μs/div)

VCORE Output Voltage Ripple at 1.5A Load



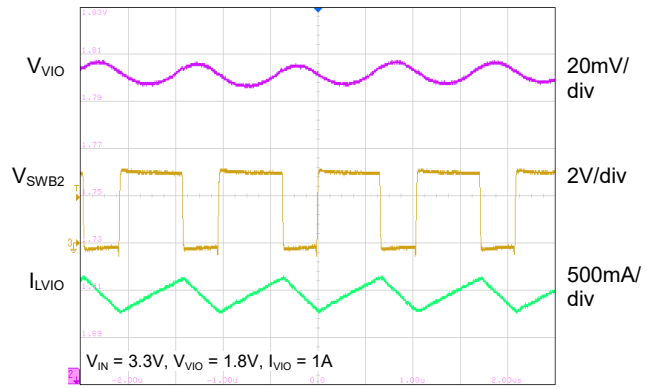
Time (500ns/div)

VIO Output Voltage Ripple at 10mA Load



Time (1μs/div)

VIO Output Voltage Ripple at 1A Load

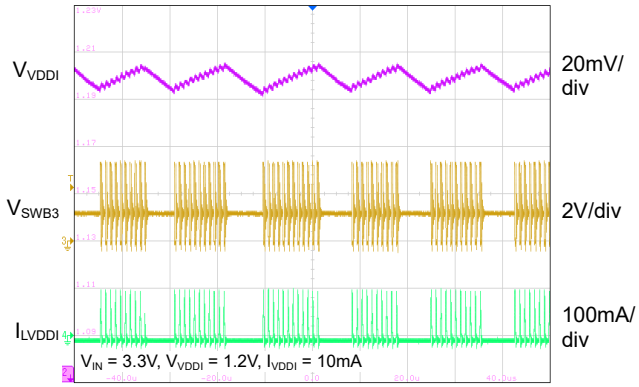


Time (500ns/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

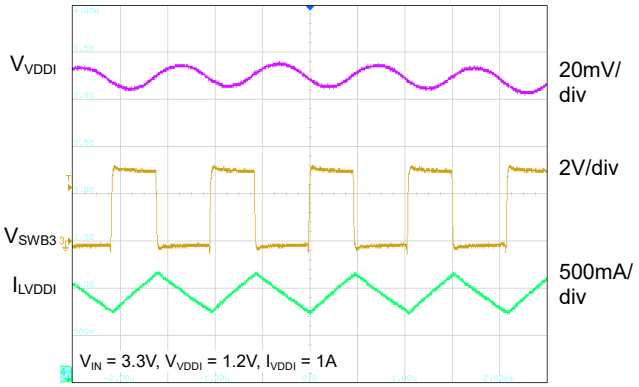
T_A = +25℃, L_{AVDD} = L_{PVGL} = L_{VCORE} = 2.2μH (HTEG25201B-2R2MIR), L_{VIO} = L_{VDDI} = 2.2μH (HTEK20160H-2R2MSR), unless otherwise noted.

VDDI Output Voltage Ripple at 10mA Load



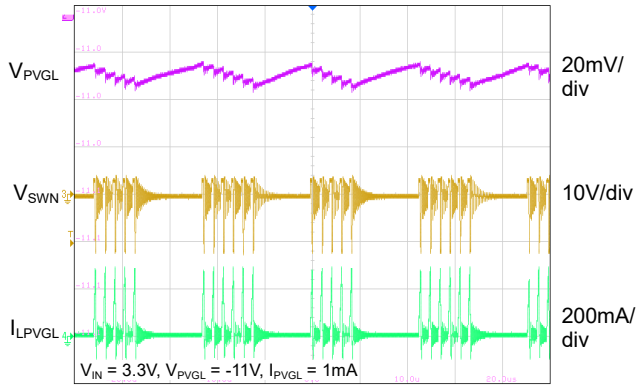
Time (10μs/div)

VDDI Output Voltage Ripple at 1A Load



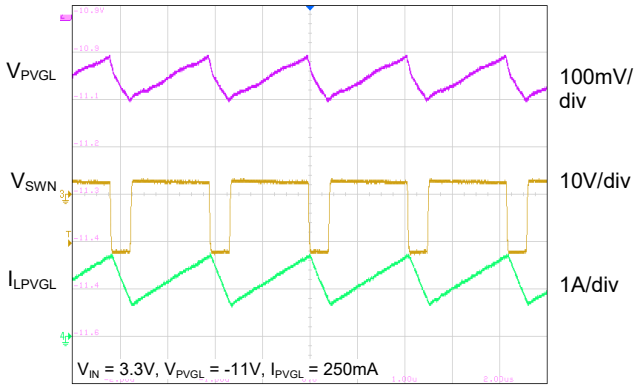
Time (500ns/div)

PVGL Output Voltage Ripple at 1mA Load



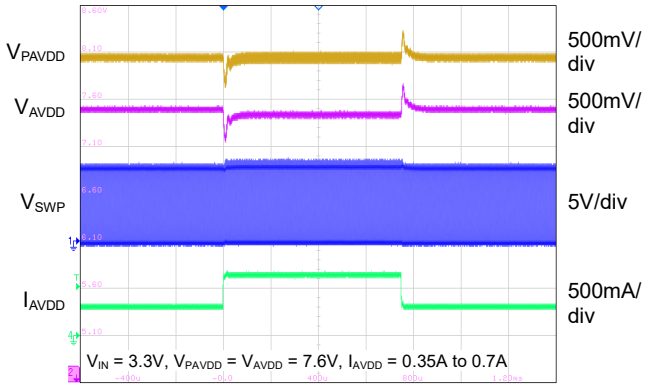
Time (5μs/div)

PVGL Output Voltage Ripple at 250mA Load



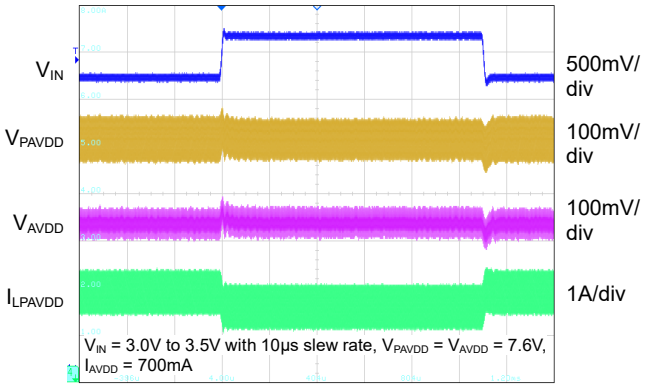
Time (500ns/div)

PAVDD and AVDD Load Transient



Time (200μs/div)

PAVDD and AVDD Line Transient

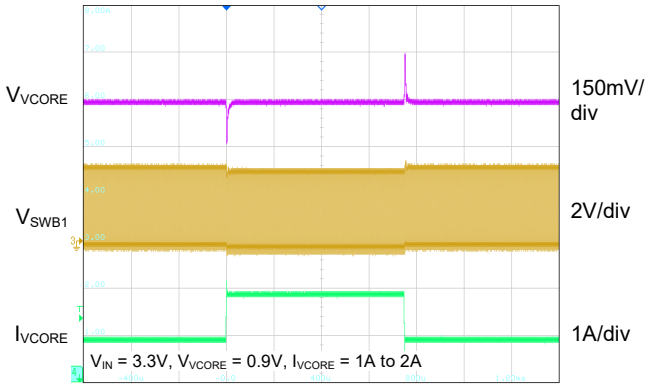


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

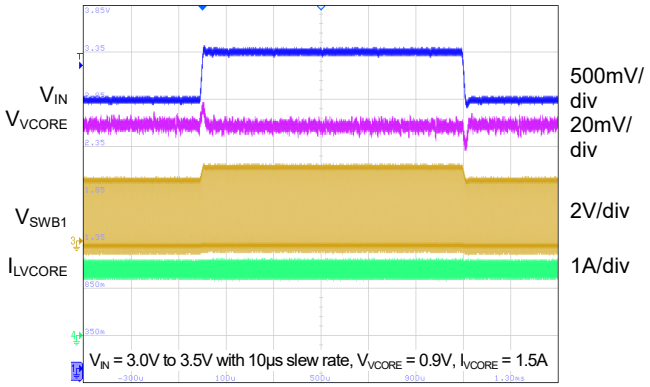
T_A = +25℃, L_{AVDD} = L_{PVGL} = L_{VCORE} = 2.2μH (HTEG25201B-2R2MIR), L_{VIO} = L_{VDDI} = 2.2μH (HTEK20160H-2R2MSR), unless otherwise noted.

VCORE Load Transient



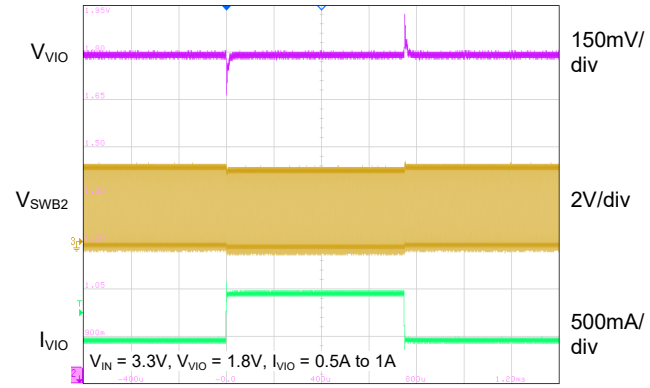
Time (200μs/div)

VCORE Line Transient



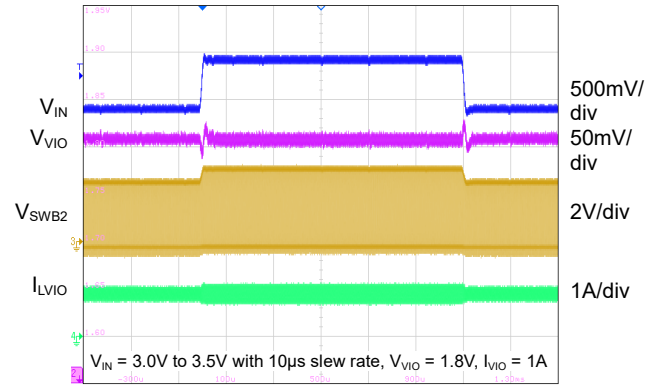
Time (200μs/div)

VIO Load Transient



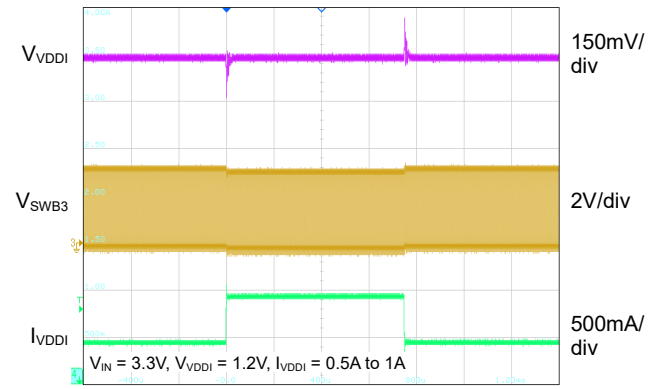
Time (200μs/div)

VIO Line Transient



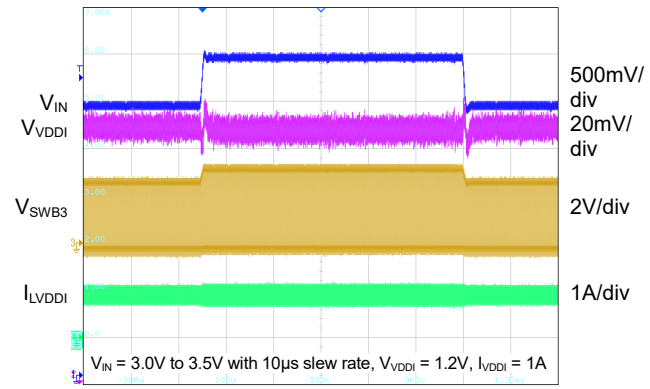
Time (200μs/div)

VDDI Load Transient



Time (200μs/div)

VDDI Line Transient

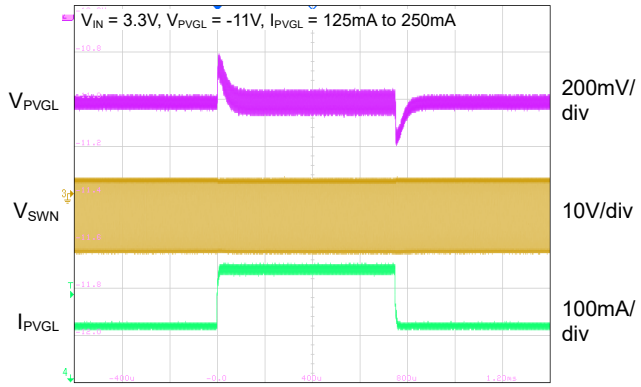


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

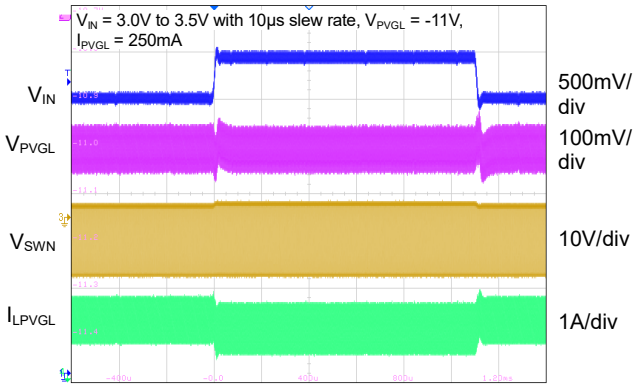
T_A = +25℃, L_{AVDD} = L_{PVGL} = L_{VCORE} = 2.2μH (HTEG25201B-2R2MIR), L_{VIO} = L_{VDDI} = 2.2μH (HTEK20160H-2R2MSR), unless otherwise noted.

PVGL Load Transient



Time (200μs/div)

PVGL Line Transient



Time (200μs/div)

FUNCTIONAL BLOCK DIAGRAM

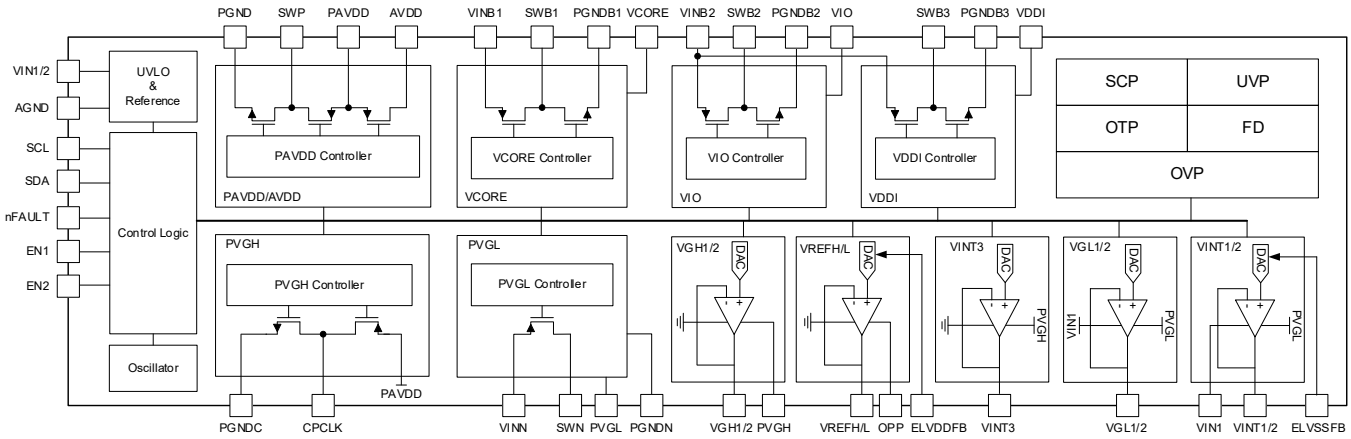


Figure 2. SGM3888 Functional Block Diagram

TIMING DIAGRAM

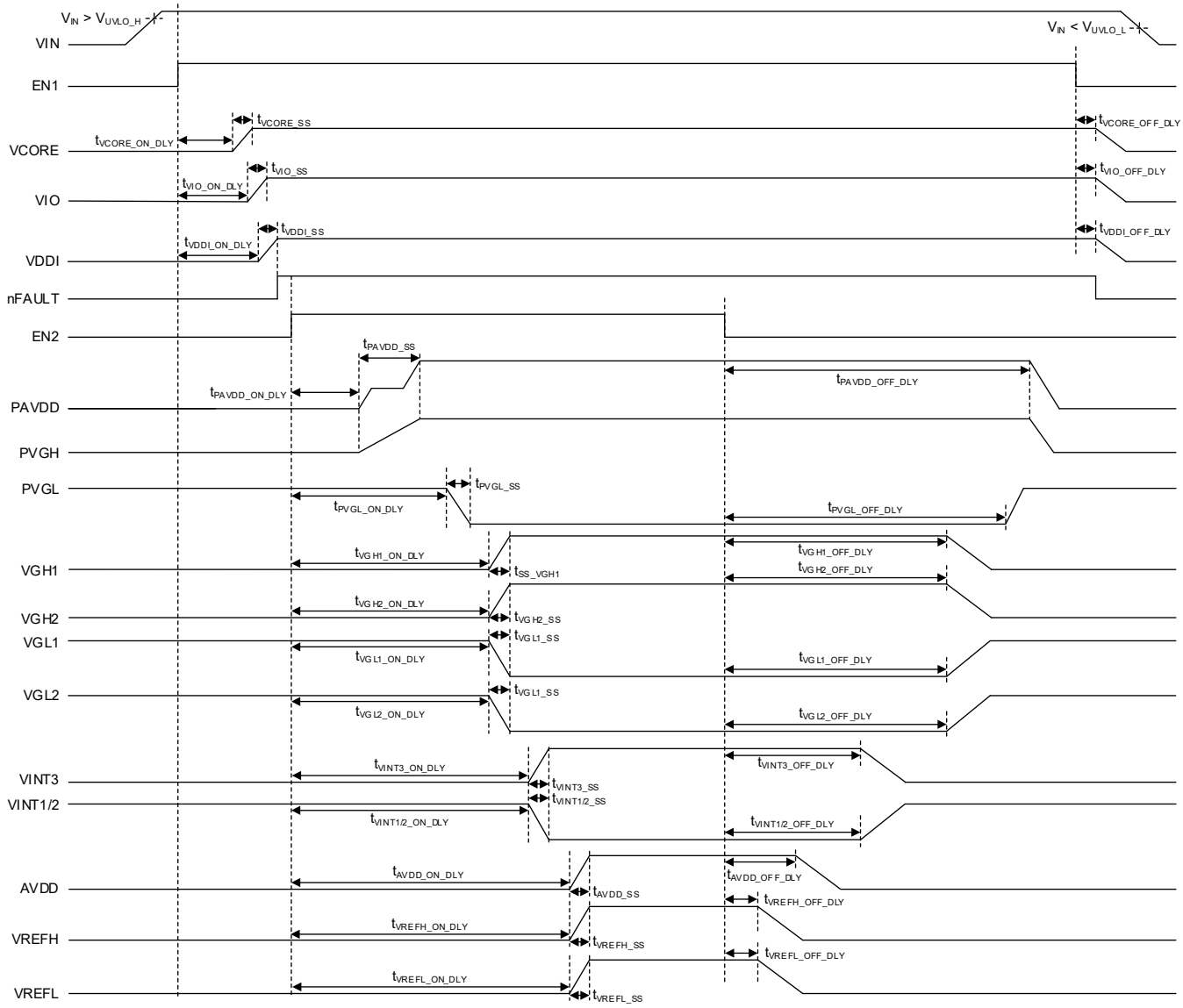


Figure 3. Power Sequence

NOTE: To guarantee normal operation, the power sequence should follow the conditions below:

- $t_{VGH1\_ON\_DLY}$, $t_{VGH2\_ON\_DLY}$, $t_{VINT3\_ON\_DLY}$, $t_{AVDD\_ON\_DLY}$, $t_{VREFH\_ON\_DLY}$, and $t_{VREFL\_ON\_DLY}$ > ($t_{PAVDD\_ON\_DLY}$ + t_{PAVDD_SS}).
- $t_{VGL1\_ON\_DLY}$, $t_{VGL2\_ON\_DLY}$ and $t_{VINT1/2\_ON\_DLY}$ > ($t_{PVGL\_ON\_DLY}$ + t_{PVGL_SS}).
- PVGH output voltage > VGH1, VGH2 and VINT3 output voltages.
- OPP input voltage > VREFH and VREFL output voltages.
- PVGL output voltage < VGL1, VGL2 and VINT1/2 output voltages.
- When the PVGL power source comes from PAVDD, $t_{PVGL\_ON\_DLY}$ > ($t_{PAVDD\_ON\_DLY}$ + t_{PAVDD_SS}).
- $t_{PAVDD\_OFF\_DLY}$ ≥ $t_{VGH1\_OFF\_DLY}$, $t_{VGH2\_OFF\_DLY}$, $t_{VINT3\_OFF\_DLY}$, $t_{AVDD\_OFF\_DLY}$, $t_{VREFH\_OFF\_DLY}$, and $t_{VREFL\_OFF\_DLY}$.
- $t_{PVGL\_OFF\_DLY}$ ≥ $t_{VGL1\_OFF\_DLY}$, $t_{VGL2\_OFF\_DLY}$, and $t_{VINT1/2\_OFF\_DLY}$.
- If EN1 is pulled high later than EN2, the real $t_{VCORE\_ON\_DLY}$ will be less than VCORE_ON_DLY[2:0] setting due to the load time of MTP.
- Before the soft-start of the channels complete, no load should be added to the outputs to prevent the power-up unsuccessfully.

DETAILED DESCRIPTION

UVLO-Voltage Lockout (UVLO)

The built-in under-voltage lockout function (UVLO) monitors the input voltage and disables the device when the input voltage is too low to operate.

Thermal Shutdown (TSD)

The device has thermal shutdown function, which prevents the device from damage due to overheating and excessive power dissipation. The device stops switching and shuts down all the outputs when the junction temperature exceeds +150℃ (TYP), and restarts with the same programmed voltages and sequences by toggling EN1 or EN2 when the temperature decreases to +135℃ (TYP).

Boost Converter (PAVDD)

The Boost converter PAVDD operates with a peak-current mode topology. It provides the voltage of AVDD through Pass Transistor and LDO OPP. The PAVDD/AVDD output can be programmed between 5.5V and 10.55V (default 7.6V) with 50mV steps (see PAVDD/AVDD Register).

Buck Converter 1 (VCORE)

The Buck converter 1 VCORE operates with a peak-current mode topology. The VCORE output voltage can be programmed between 0.6V and 1.5V (default 0.9V) with 25mV steps (see VCORE Register).

Buck Converter 2 (VIO)

The Buck converter 2 VIO operates with a peak-current mode topology. The VIO output voltage can be programmed between 1V and 1.95V (default 1.8V) with 50mV steps (see VIO Register).

Buck Converter 3 (VDDI)

The Buck converter 3 VDDI operates with a peak-current mode topology. The VDDI output voltage can be programmed between 1V and 1.95V (default 1.2V) with 50mV steps (see VDDI Register).

1:2 Charge Pump (PVGH)

The 1:2 charge pump PVGH is supplied by PAVDD. It works in external mode with two Schottky diodes. The PVGH output follows PAVDD and its output voltage is twice of PAVDD or PAVDD+VIN.

Inverting Buck-Boost Converter (PVGL)

The inverting Buck-Boost converter PVGL operates with a peak-current mode topology. The PVGL output voltage can be programmed between -22V and -6V (default -11V) with 100mV steps (see PVGL Register).

Positive Operational Amplifier (VGH1/2)

The positive operational amplifier VGH1/2 operates in positive mode. The VGH1/2 output voltage can be programmed between 4V and 19.9V (default 10V) with 100mV steps (see VGH1/2 Register).

Positive Operational Amplifier (VINT3)

The positive operational amplifier VINT3 operates in positive mode. The VINT3 output voltage can be programmed between 1V and 10V (default 7.2V) with 10mV steps (see VINT3 and VINT3_FT Registers).

Positive Operational Amplifier (VREFH)

The positive operational amplifier VREFH operates in positive mode. The VREFH output voltage can be programmed between 4.4V and 9.5V (default 6.8V) with 10mV steps (see VREFH Register).

Positive Operational Amplifier (VREFL)

The positive operational amplifier VREFL operates in positive mode. The VREFL output voltage can be programmed between 0.5V and 5.5V (default 1.5V) with 10mV steps (see VREFL Register)

Negative Operational Amplifier (VGL1/2)

The negative operational amplifier VGL1/2 operates in negative mode. The VGL1/2 output voltage can be programmed between -21V and -2V (default -10V) with 100mV steps (see VGL1/2 Register)

Negative Operational Amplifier (VINT1/2)

The VINT1/2 output voltage can be programmed between -19V and -0.5V (default -6V) with 10mV steps (see VINT1/2 and VINT1/2_FT Registers).

DETAILED DESCRIPTION (continued)

Soft-Start, Start-Up, Discharge and Shutdown

The built-in soft-start function is adopted to limit the inrush current.

Writing PAVDD_EN bit enables the PAVDD Boost converter and it starts with a precharge phase. The device sources a 350mA precharge current to charge the output voltage for 2ms firstly. Once the output voltage reaches the 1V (PAVDD_PRE_UVP trigger level) when the precharge phase ends, the device enters soft-start phase to turn on Boost switching and ramp the output voltage towards the programmed output voltage for 3ms with 1.5A current limit. Then the full current limit is active (4.4A, TYP).

Writing VCORE_EN bit starts the VCORE Buck converter. Before VCORE rises to the default value (0.9V), it rises linearly for 1ms with a 1A current limit. Then the full current limit is active (3A, TYP).

Toggling VIO_EN bit starts the VIO Buck converter. Before VIO rises to the default value (1.8V), it rises linearly for 2ms with a 0.5A current limit. Then the full current limit is active (1.9A, TYP).

Toggling VDDI_EN bit starts the VDDI Buck converter. Before VDDI rises to the default value (1.2V), it rises linearly for 1ms with a 0.5A current limit. Then the full current limit is active (1.9A, TYP).

Writing PVGL_EN bit starts the PVGL inverting Buck-Boost converter. Before PVGL rises to the default value (-11V), it rises linearly for 4ms with a 1.5A current limit. Then the full current limit is active (3A, TYP).

The output discharge function can be controlled by the fast discharge control bits (*_FD) except for VDDI. Disabling VDDI via I^2C not only turns off VDDI but also starts the fast discharge of VDDI.

Under-Voltage, Short-Circuit and Over-Voltage Protection

The device is protected from damage due to all the outputs shorting to ground.

The device detects an overload when anyone of outputs falls below 70% of programmed output voltage for longer than 2ms and then the corresponding UVP_F is set to 1. At the same time, the corresponding protection starts, and the IC shuts down. The UVP FAULT_FLAG registers can be cleared by POR, toggling ENx, or disabling the protection function.

NOTE: *ENx indicates which EN signal (EN1/EN2) controls the power rail that triggered the UVP.

The device detects a short when anyone of VCORE, VDDI, VIO, PAVDD, AVDD and PVGL falls below 30% of programmed output voltage for longer than 15μs and then the protection operation follows the UVP_ OPERATION.

An OVP fault occurs when PAVDD is higher than PAVDD × 120% and lasts for more 5ms.

An OVP fault occurs when PVGL is below PVGL × 120% and lasts for more 5ms.

Once any of the OVP faults occurs, the corresponding OVP_F flag bit is updated in the fault flag register. Compared with the UVP FAULT_FLAG clearing methods, the OVP FAULT_FLAG bits also can be cleared by reading.

Please refer to the Protection Table on the next page for details.

Output Current Capacity

The device operates with an input voltage range of 2.7V to 4.8V. However, due to different input voltage and different output voltage, the output current capacity is quite different. A lower input voltage (above UVLO) or a higher output voltage leads to a lower output current capacity.

Input Power Supply

The input power supply voltage is recommended between 2.7V and 4.8V. To achieve full performance, a stable and noise-free input source is needed. Once the distance between input source and SGM3888 is a bit long, additional capacitors are suggested to place as close to the device as possible. Please refer to the typical application circuit for the suggested input capacitance.

DETAILED DESCRIPTION (continued)

Protection Table

Block	Protection	Conditions	Behavior	Recovery	nFAULT
IC	VIN UVLO	V_{IN} < 2.15V (TYP)	IC Shutdown	VIN Exceeds UVLO_R	Y
	OTP	T_J > +150℃ (TYP)	IC Shutdown	EN1 or/and EN2 Toggle	Y
	EL_SD	ELVDDFB < 1V (Trigger Level)	All EN2 channels shut down	EN1 or/and EN2 Toggle	Y
PAVDD	CL	I_{SWP} Peak > PAVDD CL Setting	Normal operating with current limit	Peak I_{SWP} < CL	N
	UVP	PAVDD < 70% × PAVDD Setting	Stop switching and then all channels shut down	EN2 Toggle	Y
	Pre-Charge UVP	PAVDD < 1V (Trigger Level)	PAVDD shuts down only	EN2 Toggle	Y
	OVP	PAVDD > 120% × PAVDD Setting	Stop switching	/	N
PVGL	CL	I_{SWN} Peak > PVGL CL Setting	Normal operating with current limit	Peak I_{SWN} < CL	N
	UVP	|PVGL| < 70% × |PVGL| Setting	Stop switching and then all channels shut down	EN2 Toggle	Y
	OVP	|PVGL| >120% × |PVGL| Setting	Stop switching	/	N
VCORE	CL	I_{SWB1} Peak > VCORE CL Setting	Normal operating with current limit	Peak I_{SWB1} < CL	N
	UVP	VCORE < 70% × VCORE Setting	Stop switching and then all channels shut down	EN1 Toggle	Y
VIO	CL	I_{SWB2} Peak > VIO CL Setting	Normal operating with current limit	Peak I_{SWB2} < CL	N
	UVP	VIO < 70% × VIO Setting	Stop switching and then all channels shut down	EN1 Toggle	Y
VDDI	CL	I_{SWB3} Peak > VDDI CL Setting	Normal operating with current limit	Peak I_{SWB3} < CL	N
	UVP	VDDI < 70% × VDDI Setting	Stop switching and then all channels shut down	EN1 Toggle	Y
AVDD	Pre-Charge UVP	AVDD < 1V (Trigger Level)	AVDD shuts down only	EN2 Toggle	Y
	UVP	AVDD < 70% × AVDD Setting	Stop switching and then all channels shut down	EN2 Toggle	Y
	OCP	I_{AVDD} > OCP Setting	Stop switching and then AVDD shuts down only	EN2 Toggle	Y
VGH1/2	UVP	VGH1/2 < 70% × VGH1/2 Setting	All channels shut down	EN2 Toggle	Y
VGL1/2	UVP	|VGL1/2| < 70% × |VGL1/2| Setting	All channels shut down	EN2 Toggle	Y
VREFH/L	UVP	VREFH/L < 70% × VREFH/L Setting	All channels shut down	EN2 Toggle	Y
VINT1/2	UVP	|VINT1/2| < 70% × |VINT1/2| Setting	All channels shut down	EN2 Toggle	Y
	CL	$I_{INT1/2}$ > VINT1/2 CL Setting	Normal operating with current limit	Peak Current < CL	N
VINT3	UVP	VINT3 < 70% × VINT3 Setting	All channels shut down	EN2 Toggle	Y
	CL	I_{INT3} > VINT3 CL Setting	Normal operating with current limit	Peak Current < CL	N

NOTE: UVP_OPERATION[1:0] bits are set to 00b.

DETAILED DESCRIPTION (continued)

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM3888 parameters and get status reports. I²C is well-known 2 wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master and generates the SCL clock as long as it is master. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM3888 operates as a slave device with address 0x66 (66H).

Physical Layer

Bus lines are pulled high by pull-up resistors and in logic high state with no clocking when the bus is free. The pull-up resistors that are tied to SDA and SCL lines should meet I²C specification. The SGM3888 does not support the general call. The SDA pin is open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 4. All transactions begin by the master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.

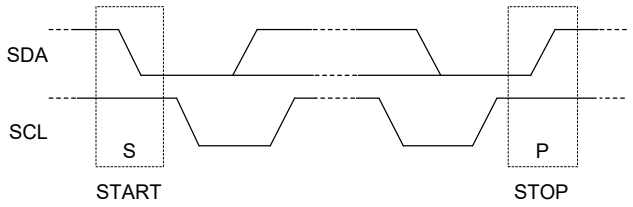


Figure 4. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the high period of the clock. The state of the SDA can only change when the clock (SCL) is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 5.

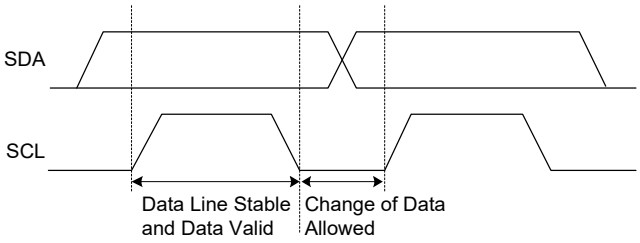


Figure 5. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 6 shows the byte transfer process with I²C interface.

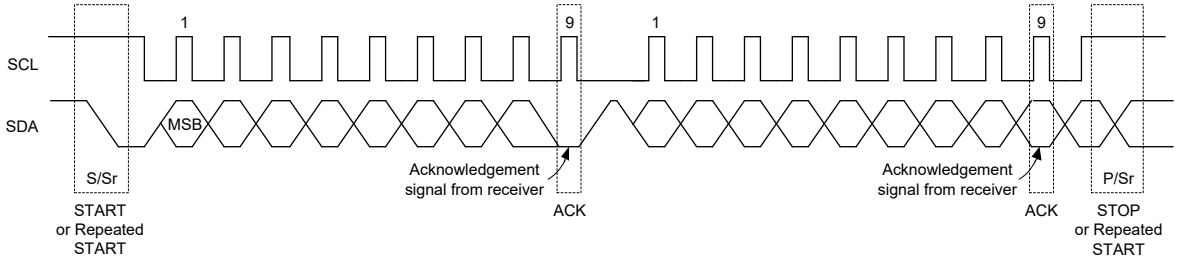


Figure 6. Byte Transfer Process

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by the master, including for the acknowledge clock pulse. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then without a STOP condition another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accesses in the next byte(s). The data transfer transaction is shown in Figure 7.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 8 and Figure 9 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 10 and Figure 11), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

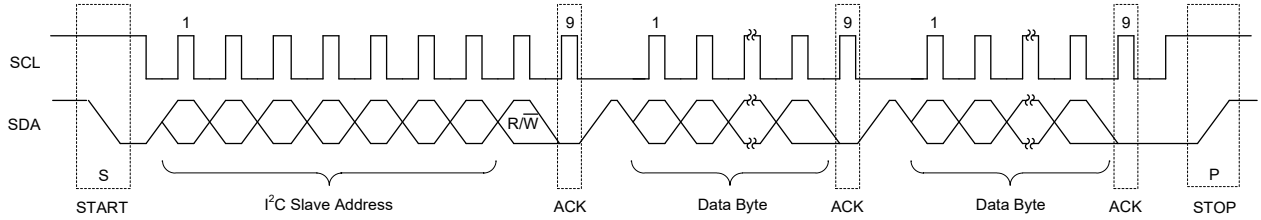


Figure 7. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

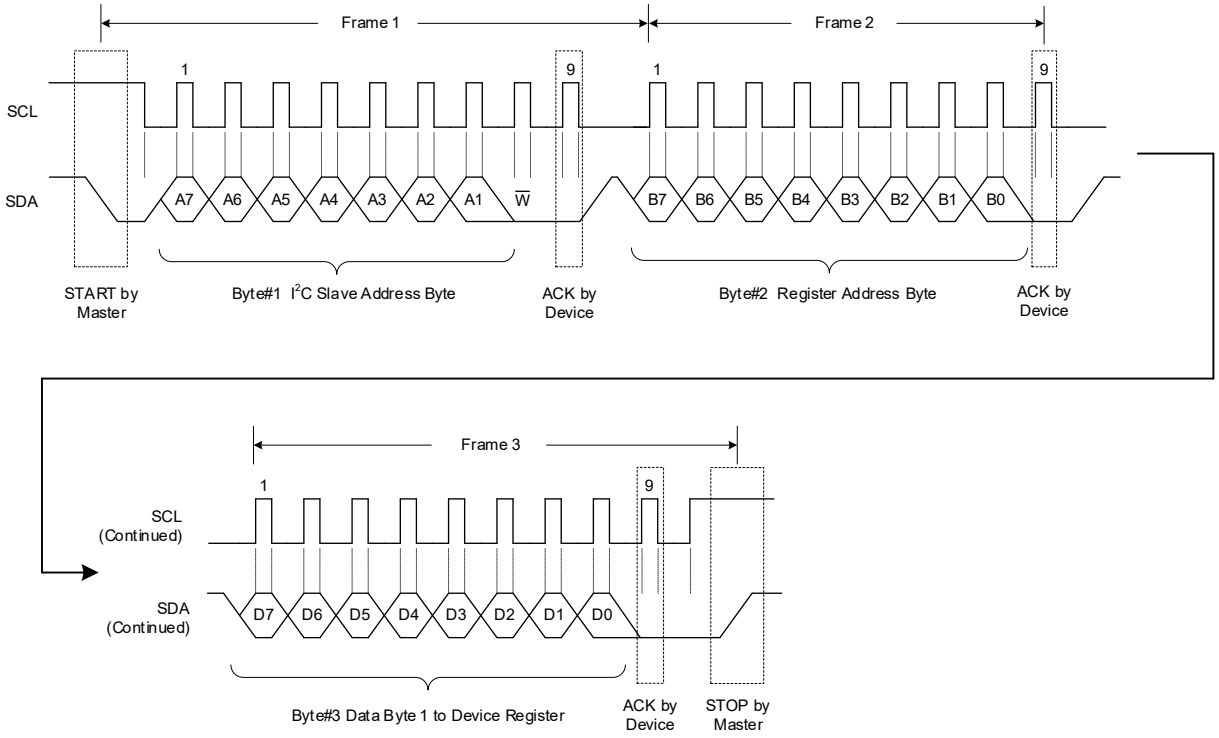


Figure 8. A Single Write Transaction (To DAC Register)

DETAILED DESCRIPTION (continued)

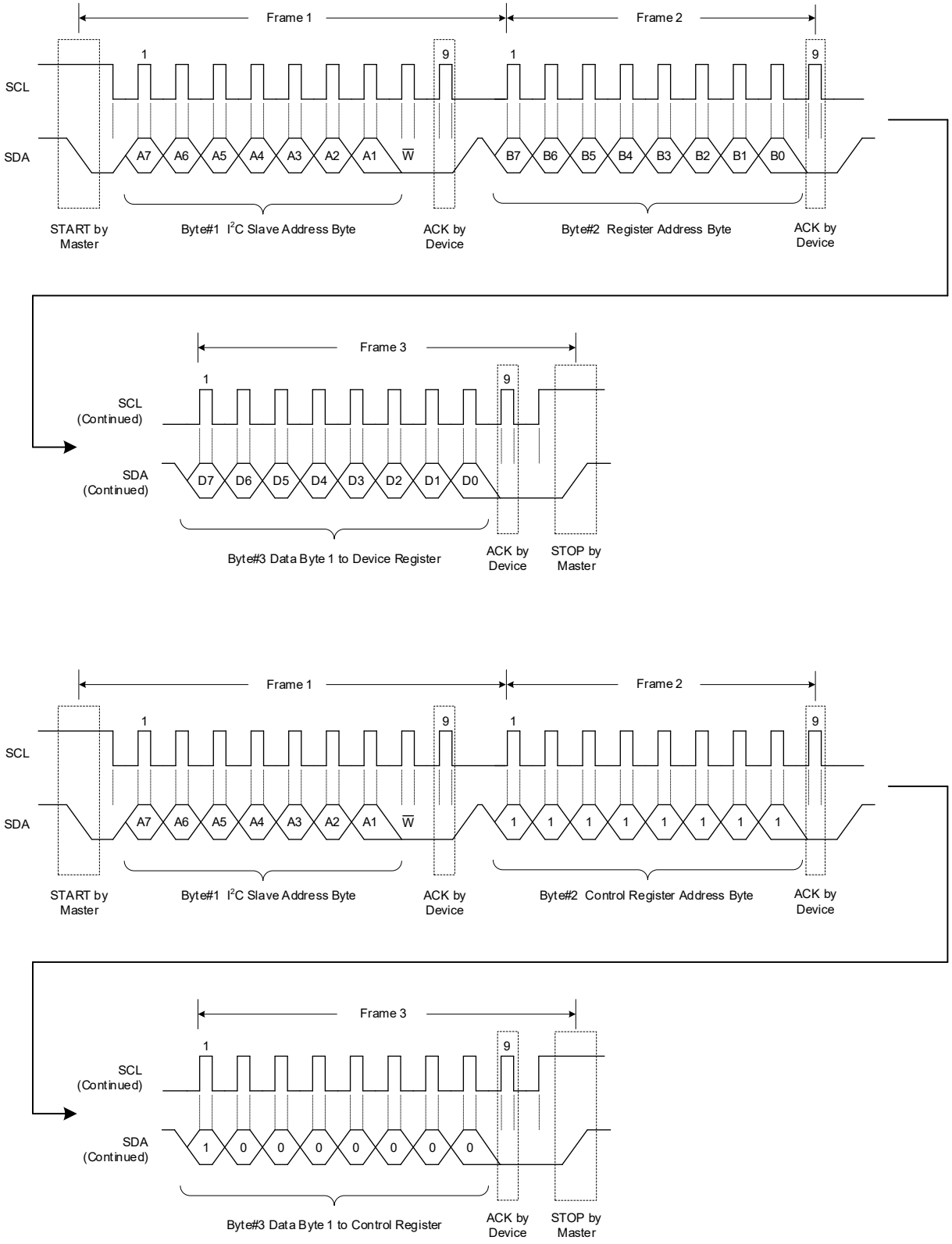


Figure 9. A Single Write Transaction (To MTP)

DETAILED DESCRIPTION (continued)

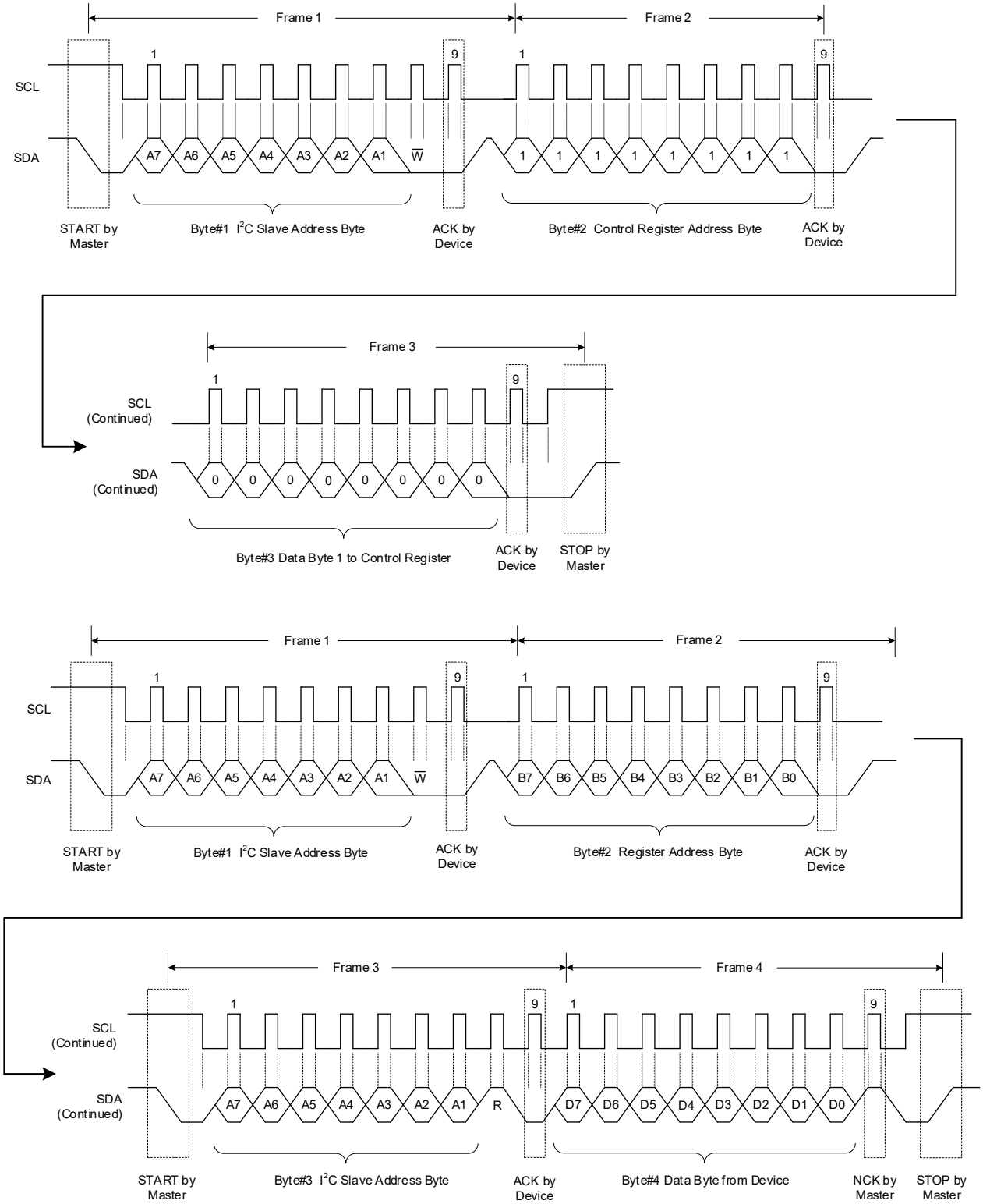


Figure 10. A Single Read Transaction (From DAC Register)

DETAILED DESCRIPTION (continued)

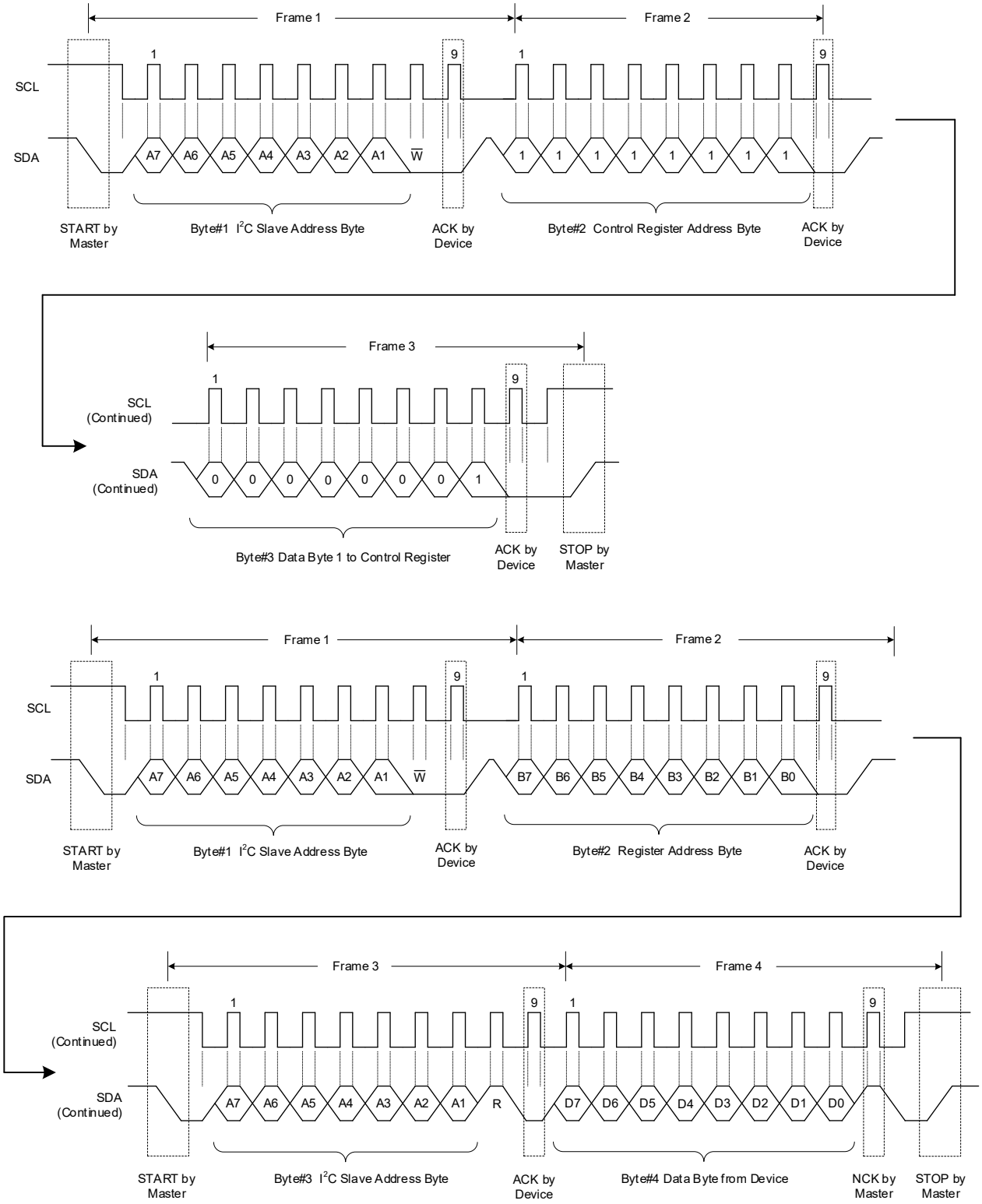


Figure 11. A Single Read Transaction (From MTP)

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM3888 as explained in Figure 12 to Figure 15. In a multi-write transaction, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (whose address is already written to the slave), the master replies with an ACK to ask the slave for sending the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues an STOP condition.

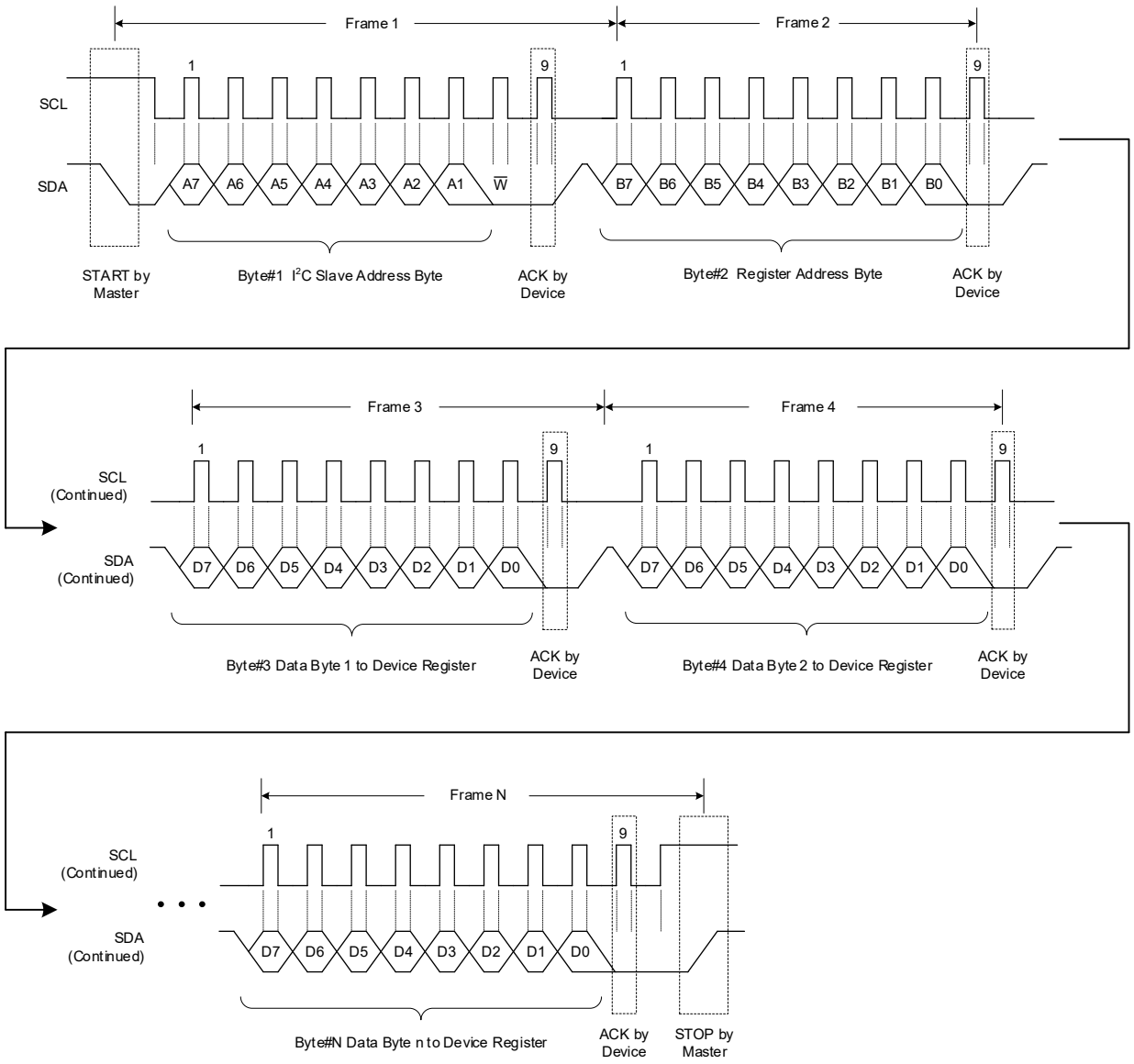


Figure 12. A Multi-Write Transaction (To DAC Register)

DETAILED DESCRIPTION (continued)

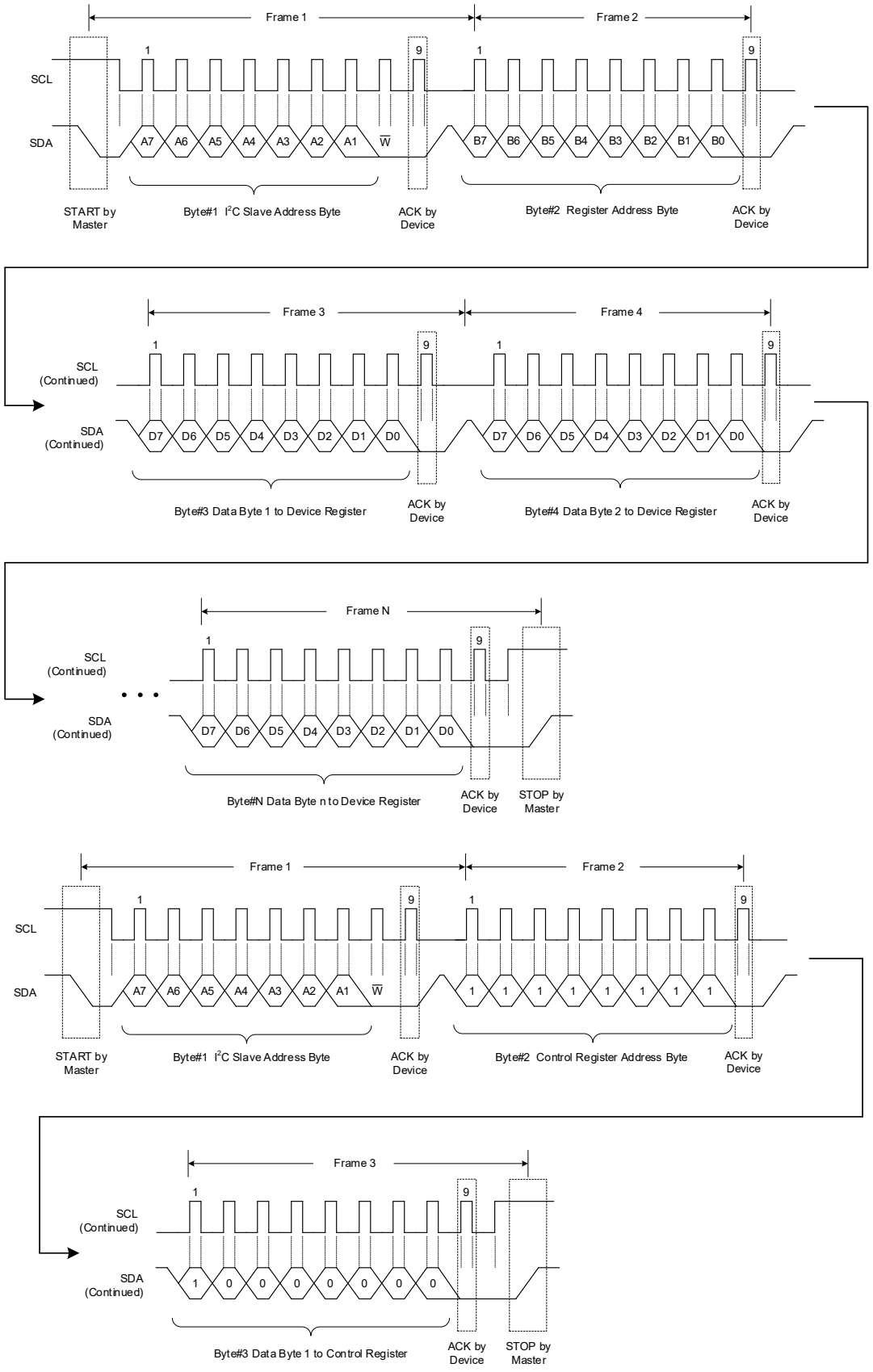


Figure 13. A Multi-Write Transaction (To MTP)

DETAILED DESCRIPTION (continued)

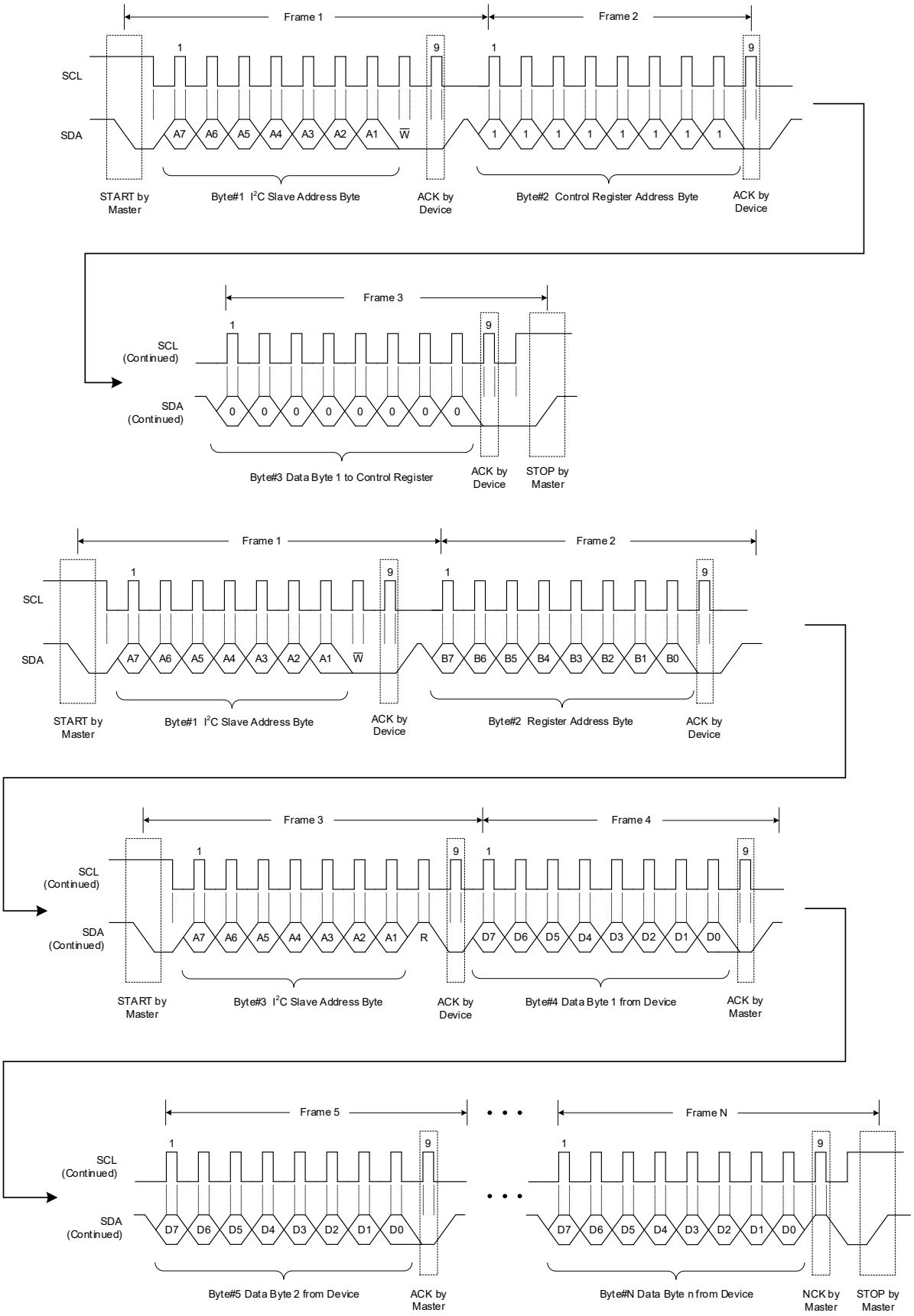


Figure 14. A Multi-Read Transaction (From DAC Register)

DETAILED DESCRIPTION (continued)

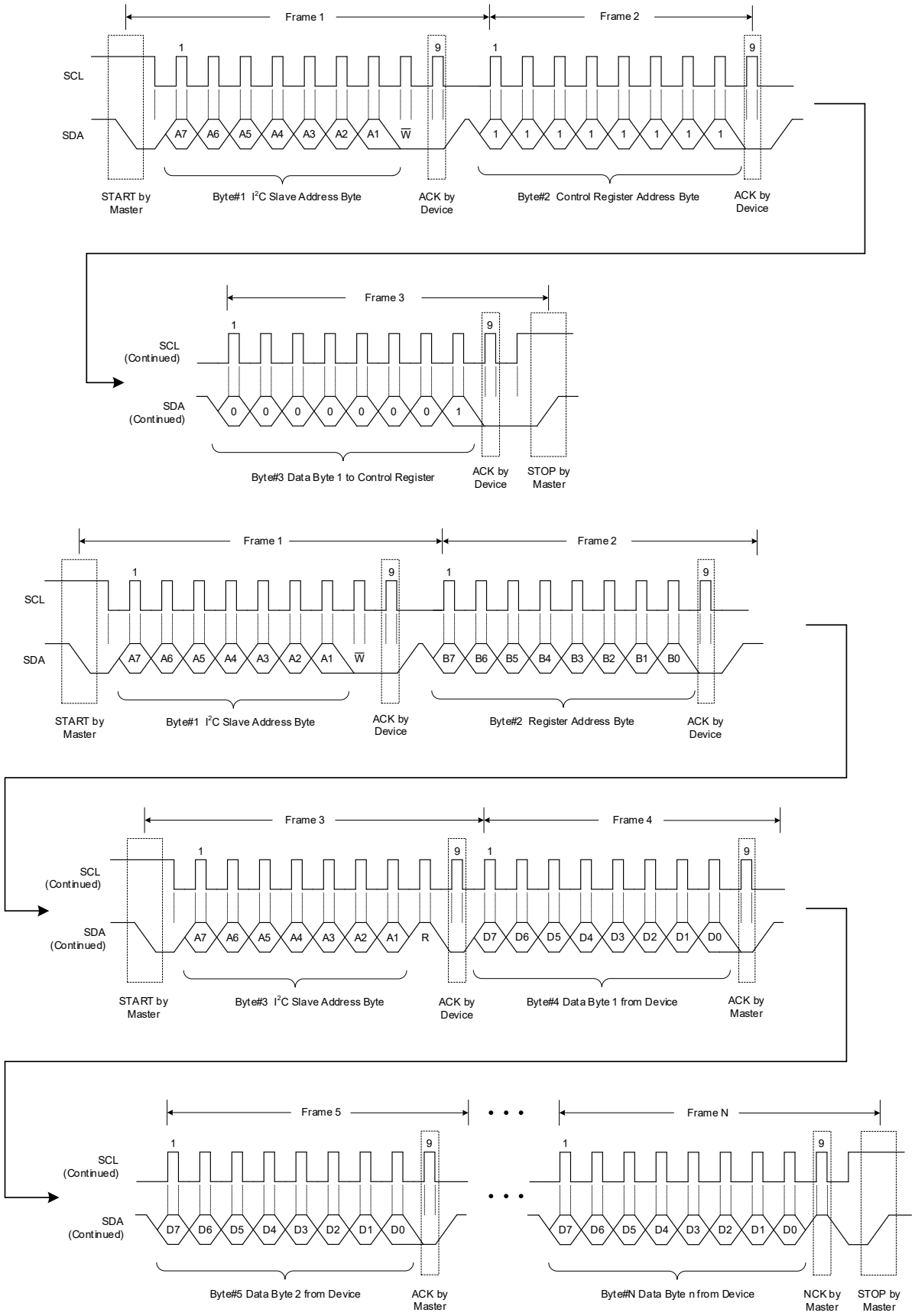


Figure 15. A Multi-Read Transaction (From MTP)

DETAILED DESCRIPTION (continued)

MTP Program Sequence for Single Chip

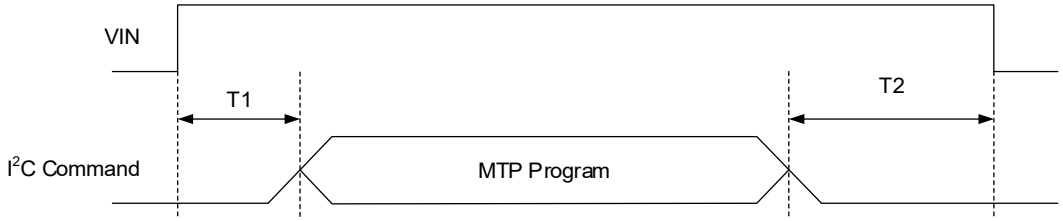


Figure 16. MTP Program Timing Sequence

Write Timing:
T1 = 50ms, T2 = 500ms
Read Timing:
T1 = 50ms, T2 = 10ms
f_{SCL} = 400kHz

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Slave Address of SGM3888: 0x66 (1100110 + W/R)

Bit Types:
R: Read only
R/W: Read/Write

Table 2. Register Map

REGISTER NAME	ADDRESS	BIT NAME AND DEFAULT VALUE								TYPE
		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	
V_SET	0x00	PAVDD_IND	PAVDD[6:0]							R/W
		0	0	1	0	1	0	1	0	
	0x01	Reserved		VCORE[5:0]						R/W
		0	0	0	0	1	1	0	0	
	0x02	VIO/VDDI_IND	PVGL_IND	Reserved	VIO[4:0]					R/W
		0	0	0	1	0	0	0	0	
	0x03	EN1_FD	PAVDD_FD	EN2_FD	VDDI[4:0]					R/W
		1	1	1	0	0	1	0	0	
	0x04	PVGL[7:0]								R/W
		0	0	1	1	0	0	1	0	
	0x05	VGH1[7:0]								R/W
		0	0	1	1	1	1	0	0	
	0x06	VGH2[7:0]								R/W
		0	0	1	1	1	1	0	0	
	0x07	VGL1[7:0]								R/W
		0	1	0	1	0	0	0	0	
	0x08	VGL2[7:0]								R/W
		0	1	0	1	0	0	0	0	
	0x09	VINT1[7:0]								R/W
		0	0	1	1	1	1	0	0	
	0x0A	VINT2[7:0]								R/W
		0	0	1	1	1	1	0	0	
	0x0B	VINT3[7:0]								R/W
		0	1	1	1	1	1	0	0	
	0x0C	Reserved						VREFH[9:8]		R/W
		0	0	0	0	0	0	1	0	
	0x0D	VREFH[7:0]								R/W
		1	0	1	0	1	0	0	0	
	0x0E	Reserved						VREFL[9:8]		R/W
		0	0	0	0	0	0	0	0	
	0x0F	VREFL[7:0]								R/W
		1	0	0	1	0	1	1	0	

REGISTER MAPS (continued)

Table 2. Register Map (continued)

REGISTER NAME	ADDRESS	BIT NAME AND DEFAULT VALUE								TYPE
		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	
V_SET	0x10	VINT2_FT[3:0]				VINT1_FT[3:0]				R/W
		0	0	0	0	0	0	0	0	
	0x11	Reserved				VREFH/L_SR	VINT3_FT[2:0]			
		0	0	0	0	0	0	0	0	
VCORE_CON	0x12	VCORE_ON_DLY[2:0]			VCORE_OFF_DLY[2:0]			VCORE_EN	Reserved	R/W
		0	0	1	0	1	1	1	0	
VIO_CON	0x13	VIO_ON_DLY[2:0]			VIO_OFF_DLY[2:0]			VIO_EN	Reserved	R/W
		0	0	1	0	1	1	1	0	
VDDI_CON	0x14	VDDI_ON_DLY[2:0]			VDDI__OFF_DLY[2:0]			VDDI_EN	Reserved	R/W
		0	0	1	0	1	1	1	0	
PAVDD_CON	0x15	PAVDD_ON_DLY[2:0]			PAVDD_OFF_DLY[2:0]			PAVDD_EN	Reserved	R/W
		0	0	0	1	0	0	1	0	
AVDD_CON	0x16	AVDD_ON_DLY[2:0]			AVDD_OFF_DLY[1:0]		AVDD_EN	AVDD_SST[1:0]		R/W
		1	0	0	1	0	1	0	0	
PVGH_CON	0x17	Reserved						PVGH_EN	Reserved	R/W
		0	1	0	0	0	0	1	0	
VGH1_CON	0x18	VGH1_ON_DLY[2:0]			VGH1_OFF_DLY[2:0]			VGH1_EN	Reserved	R/W
		0	1	1	0	1	0	0	0	
VGH2_CON	0x19	VGH2_ON_DLY[2:0]			VGH2_OFF_DLY[2:0]			VGH2_EN	Reserved	R/W
		1	0	0	0	1	0	0	0	
PVGL_CON	0x1A	PVGL_ON_DLY[2:0]			PVGL_OFF_DLY[2:0]			PVGL_EN	Reserved	R/W
		0	1	0	0	1	1	1	0	
VGL1_CON	0x1B	VGL1_ON_DLY[2:0]			VGL1_OFF_DLY[2:0]			VGL1_EN	Reserved	R/W
		1	0	1	0	1	0	0	0	
VGL2_CON	0x1C	VGL2_ON_DLY[2:0]			VGL2_OFF_DLY[2:0]			VGL2_EN	Reserved	R/W
		1	1	0	0	1	0	0	0	
VINT1_CON	0x1D	VINT1_ON_DLY[2:0]			VINT1_OFF_DLY[2:0]			VINT1_EN	Reserved	R/W
		0	1	0	1	0	0	0	0	
VINT2_CON	0x1E	VINT2_ON_DLY[2:0]			VINT2_OFF_DLY[2:0]			VINT2_EN	Reserved	R/W
		0	1	0	1	0	0	0	0	
VINT3_CON	0x1F	VINT3_ON_DLY[2:0]			VINT3_OFF_DLY[2:0]			VINT3_EN	Reserved	R/W
		0	1	1	1	0	0	0	0	

REGISTER MAPS (continued)

Table 2. Register Map (continued)

REGISTER NAME	ADDRESS	BIT NAME AND DEFAULT VALUE								TYPE
		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	
VREFH&L_CON	0x20	VREFH&L_ON_DLY[2:0]			VREFH&L_OFF_DLY[2:0]			VREFH&L_EN	Reserved	R/W
		1	0	1	0	0	0	0	0	
FSW&SR_1	0x21	VCORE_FSW[2:0]			VIO_FSW[2:0]			VCORE_SR[1:0]		R/W
		0	1	0	0	1	0	0	0	
FSW&SR_2	0x22	VDDI_FSW[2:0]			PAVDD_FSW[2:0]			VIO_SR[1:0]		R/W
		0	1	0	0	1	0	0	0	
FSW&SR_3	0x23	PVGL_FSW[2:0]			Reserved	PAVDD_SR[1:0]		VDDI_SR[1:0]		R/W
		0	1	0	0	0	0	0	0	
FSW&SR_4	0x24	Reserved						PVGL_SR[1:0]		R/W
		0	0	0	0	0	0	0	0	
VINT1/2_RTT	0x25	Reserved				VINT2_GPP	VINT1_GPP	VINT2_RTT_EN	VINT1_RTT_EN	R/W
		1	1	1	1	1	1	0	0	
VINT1_PGP	0x26	VINT1_PGP[7:0]								R/W
		1	0	0	1	0	1	1	0	
VINT2_PGP	0x27	VINT2_PGP[7:0]								R/W
		1	0	0	1	0	1	1	0	
VINT1_NGP	0x28	VINT1_NGP[7:0]								R/W
		0	0	0	0	0	0	0	0	
VINT2_NGP	0x29	VINT2_NGP[7:0]								R/W
		0	0	0	0	0	0	0	0	
Current Limit Register 1	0x2A	VCORE_CL[1:0]		VIO_CL[1:0]		VDDI_CL[1:0]		PVGL_CL[1:0]		R/W
		1	0	1	0	1	0	1	0	
Current Limit Register 2	0x2B	Reserved						PAVDD_CL[1:0]		R/W
		0	0	0	0	0	0	1	0	
Spread Spectrum Control	0x2C	VCORE_SSC	VIO_SSC	VDDI_SSC	PAVDD_SSC	PVGL_SSC	Reserved	SS_CLK[1:0]		R/W
		0	0	0	0	0	0	0	0	
UVP_EN 1	0x2D	VCORE_UVP_EN	VIO_UVP_EN	VDDI_UVP_EN	PAVDD_UVP_EN	AVDD_UVP_EN	PVGL_UVP_EN	VGH1_UVP_EN	VGH2_UVP_EN	R/W
		1	1	1	1	1	1	1	1	
UVP_EN 2	0x2E	VREFH_UVP_EN	VREFL_UVP_EN	VGL1_UVP_EN	VGL2_UVP_EN	VINT3_UVP_EN	Reserved	VINT1_UVP_EN	VINT2_UVP_EN	R/W
		1	1	1	1	1	1	1	1	
OVP_EN	0x2F	AVDD_CD_EN	PAVDD_OVP_EN	EL_SD_EN	Reserved					R/W
		1	1	0	1	0	1	0	1	

REGISTER MAPS (continued)

Table 2. Register Map (continued)

REGISTER NAME	ADDRESS	BIT NAME AND DEFAULT VALUE								TYPE
		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	
Current Limit	0x30	VINT1_CL_EN	VINT2_CL_EN	VINT3_CL_EN	UVP_OPERATION[1:0]		Reserved			R/W
		1	1	1	0	0	1	0	1	
FAULT_FLAG 1	0x31	VCORE_UVP_F	VIO_UVP_F	VDDI_UVP_F	PAVDD_UVP_F	AVDD_UVP_F	PVGL_UVP_F	VGH1_UVP_F	VGH2_UVP_F	R
		0	0	0	0	0	0	0	0	
FAULT_FLAG 2	0x32	VREFH_UVP_F	VREFL_UVP_F	VGL1_UVP_F	VGL2_UVP_F	VINT3_UVP_F	Reserved	VINT1_UVP_F	VINT2_UVP_F	R
		0	0	0	0	0	0	0	0	
FAULT_FLAG 4	0x33	OTP_F	UVLO_F	AVDD_CLD_F	PAVDD_OVP_F	EL_SD_F	Reserved	PAVDD_PRE_UVP_F	PVGL_CL_F	R
		0	0	0	0	0	0	0	0	
FAULT_FLAG 5	0x34	VIO_CL_F	VDDI_CL_F	VCORE_CL_F	PAVDD_CL_F	VINT1_CL_F	VINT2_CL_F	VINT3_CL_F	Reserved	R
		0	0	0	0	0	0	0	0	
TIME_CONF	0x35	Reserved		ELVDD_HOLD_LVL	ELVDD_HOLD_EN	Reserved		SST_RANGE	AVDD_DLY_HALF	R/W
		0	0	1	1	1	1	0	0	
ELVDD_REF	0x36	Reserved		ELVDD_REF[5:0]						R/W
		0	0	1	0	1	0	0	0	
DEVICE ID	0x37	DEVICE_ID[7:0]								R
		0	0	1	1	1	0	0	0	
Reserved	0x38	Reserved								R/W
		0	0	0	1	0	0	0	1	
Reserved	0x39 ~ 0x3C	Reserved								R/W
		0	0	0	0	0	0	0	0	

REGISTER MAPS (continued)

REG0x00: PAVDD Register [Reset = 0x2A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	PAVDD_IND	0	R/W	PAVDD Boost Converter Inductor Select 0 = 2.2μH (default) 1 = 4.7μH
D[6:0]	PAVDD[6:0]	0101010	R/W	PAVDD Output Control V_{PAVDD} = PAVDD[6:0] × 50mV + 5.5V Offset: 5.5V Range: 5.5V (0000000) ~ 10.55V (1100101) Default: 7.6V (0101010)

Table 3. PAVDD[6:0] Description

Data (Hex)	PAVDD	Data (Hex)	PAVDD	Data (Hex)	PAVDD	Data (Hex)	PAVDD	Data (Hex)	PAVDD	Data (Hex)	PAVDD	Data (Hex)	PAVDD
0x00	5.50V	0x10	6.30V	0x20	7.10V	0x30	7.90V	0x40	8.70V	0x50	9.50V	0x60	10.30V
0x01	5.55V	0x11	6.35V	0x21	7.15V	0x31	7.95V	0x41	8.75V	0x51	9.55V	0x61	10.35V
0x02	5.60V	0x12	6.40V	0x22	7.20V	0x32	8.00V	0x42	8.80V	0x52	9.60V	0x62	10.40V
0x03	5.65V	0x13	6.45V	0x23	7.25V	0x33	8.05V	0x43	8.85V	0x53	9.65V	0x63	10.45V
0x04	5.70V	0x14	6.50V	0x24	7.30V	0x34	8.10V	0x44	8.90V	0x54	9.70V	0x64	10.50V
0x05	5.75V	0x15	6.55V	0x25	7.35V	0x35	8.15V	0x45	8.95V	0x55	9.75V	0x65	10.55V
0x06	5.80V	0x16	6.60V	0x26	7.40V	0x36	8.20V	0x46	9.00V	0x56	9.80V		
0x07	5.85V	0x17	6.65V	0x27	7.45V	0x37	8.25V	0x47	9.05V	0x57	9.85V		
0x08	5.90V	0x18	6.70V	0x28	7.50V	0x38	8.30V	0x48	9.10V	0x58	9.90V		
0x09	5.95V	0x19	6.75V	0x29	7.55V	0x39	8.35V	0x49	9.15V	0x59	9.95V		
0x0A	6.00V	0x1A	6.80V	0x2A	7.60V	0x3A	8.40V	0x4A	9.20V	0x5A	10.00V		
0x0B	6.05V	0x1B	6.85V	0x2B	7.65V	0x3B	8.45V	0x4B	9.25V	0x5B	10.05V		
0x0C	6.10V	0x1C	6.90V	0x2C	7.70V	0x3C	8.50V	0x4C	9.30V	0x5C	10.10V		
0x0D	6.15V	0x1D	6.95V	0x2D	7.75V	0x3D	8.55V	0x4D	9.35V	0x5D	10.15V		
0x0E	6.20V	0x1E	7.00V	0x2E	7.80V	0x3E	8.60V	0x4E	9.40V	0x5E	10.20V		
0x0F	6.25V	0x1F	7.05V	0x2F	7.85V	0x2F	8.65V	0x4F	9.45V	0x5F	10.25V		

REGISTER MAPS (continued)

REG0x01: VCORE Register [Reset = 0x0C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5:0]	VCORE[5:0]	001100	R/W	VCORE Output Control V_{VCORE} = VCORE[5:0] × 25mV + 0.6V Offset: 0.6V Range: 0.6V (000000) ~ 1.5V (100100) Default: 0.9V (001100)

Table 4. VCORE[5:0] Description

Data (Hex)	VCORE	Data (Hex)	VCORE	Data (Hex)	VCORE	Data (Hex)	VCORE	Data (Hex)	VCORE
0x00	0.600V	0x08	0.800V	0x10	1.000V	0x18	1.200V	0x20	1.400V
0x01	0.625V	0x09	0.825V	0x11	1.025V	0x19	1.225V	0x21	1.425V
0x02	0.650V	0x0A	0.850V	0x12	1.050V	0x1A	1.250V	0x22	1.450V
0x03	0.675V	0x0B	0.875V	0x13	1.075V	0x1B	1.275V	0x23	1.475V
0x04	0.700V	0x0C	0.900V	0x14	1.100V	0x1C	1.300V	0x24	1.500V
0x05	0.725V	0x0D	0.925V	0x15	1.125V	0x1D	1.325V		
0x06	0.750V	0x0E	0.950V	0x16	1.150V	0x1E	1.350V		
0x07	0.775V	0x0F	0.975V	0x17	1.175V	0x1F	1.375V		

REG0x02: VIO Register [Reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VIO/VDDI_IND	0	R/W	VIO and VDDI Buck Converter Inductors Select 0 = 2.2μH (default) 1 = 4.7μH
D[6]	PVGL_IND	0	R/W	PVGL Inverting Converter Inductor Select 0 = 2.2μH (default) 1 = 4.7μH
D[5]	Reserved	0	R/W	Reserved
D[4:0]	VIO[4:0]	10000	R/W	VIO Output Control V_{VIO} = VIO[4:0] × 50mV + 1V Offset: 1V Range: 1V (00000) ~ 1.95V (10011) Default: 1.8V (10000)

Table 5. VIO[4:0] Description

Data (Hex)	VIO	Data (Hex)	VIO	Data (Hex)	VIO	Data (Hex)	VIO	Data (Hex)	VIO
0x00	1.00V	0x04	1.20V	0x08	1.40V	0x0C	1.60V	0x10	1.80V
0x01	1.05V	0x05	1.25V	0x09	1.45V	0x0D	1.65V	0x11	1.85V
0x02	1.10V	0x06	1.30V	0x0A	1.50V	0x0E	1.70V	0x12	1.90V
0x03	1.15V	0x07	1.35V	0x0B	1.55V	0x0F	1.75V	0x13	1.95V

REGISTER MAPS (continued)

REG0x03: VDDI Register [Reset = 0xE4]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	EN1_FD	1	R/W	EN1 Outputs (except VDDI) Fast Discharge Control 0 = Disable 1 = Enable (default)
D[6]	PAVDD_FD	1	R/W	PAVDD Fast Discharge Control 0 = Disable 1 = Enable (default)
D[5]	EN2_FD	1	R/W	EN2 Outputs (except PAVDD) Fast Discharge Control 0 = Disable 1 = Enable (default)
D[4:0]	VDDI[4:0]	00100	R/W	VDDI Output Control V_{VDDI} = VDDI[4:0] × 50mV + 1V Offset: 1V Range: 1V (00000) ~ 1.95V (10011) Default: 1.2V (00100)

Table 6. VDDI[4:0] Description

Data (Hex)	VIO	Data (Hex)	VIO	Data (Hex)	VIO	Data (Hex)	VIO	Data (Hex)	VIO
0x00	1.00V	0x04	1.20V	0x08	1.40V	0x0C	1.60V	0x10	1.80V
0x01	1.05V	0x05	1.25V	0x09	1.45V	0x0D	1.65V	0x11	1.85V
0x02	1.10V	0x06	1.30V	0x0A	1.50V	0x0E	1.70V	0x12	1.90V
0x03	1.15V	0x07	1.35V	0x0B	1.55V	0x0F	1.75V	0x13	1.95V

REG0x04: PVGL Register [Reset = 0x32]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	PVGL[7:0]	00110010	R/W	PVGL Output Control V_{PVGL} = -PVGL[7:0] × 100mV - 6V Offset: -6V Range: -6V (00000000) ~ -22V (10100000) Default: -11V (00110010)

REGISTER MAPS (continued)

Table 7. PVGL[7:0] Description

Data (Hex)	PVGL	Data (Hex)	PVGL	Data (Hex)	PVGL	Data (Hex)	PVGL	Data (Hex)	PVGL	Data (Hex)	PVGL
0x00	-6.0V	0x20	-9.2V	0x40	-12.4V	0x60	-15.6V	0x80	-18.8V	0xA0	-22.0V
0x01	-6.1V	0x21	-9.3V	0x41	-12.5V	0x61	-15.7V	0x81	-18.9V	0xA1	Null
0x02	-6.2V	0x22	-9.4V	0x42	-12.6V	0x62	-15.8V	0x82	-19.0V		
0x03	-6.3V	0x23	-9.5V	0x43	-12.7V	0x63	-15.9V	0x83	-19.1V		
0x04	-6.4V	0x24	-9.6V	0x44	-12.8V	0x64	-16.0V	0x84	-19.2V		
0x05	-6.5V	0x25	-9.7V	0x45	-12.9V	0x65	-16.1V	0x85	-19.3V		
0x06	-6.6V	0x26	-9.8V	0x46	-13.0V	0x66	-16.2V	0x86	-19.4V		
0x07	-6.7V	0x27	-9.9V	0x47	-13.1V	0x67	-16.3V	0x87	-19.5V		
0x08	-6.8V	0x28	-10.0V	0x48	-13.2V	0x68	-16.4V	0x88	-19.6V		
0x09	-6.9V	0x29	-10.1V	0x49	-13.3V	0x69	-16.5V	0x89	-19.7V		
0x0A	-7.0V	0x2A	-10.2V	0x4A	-13.4V	0x6A	-16.6V	0x8A	-19.8V		
0x0B	-7.1V	0x2B	-10.3V	0x4B	-13.5V	0x6B	-16.7V	0x8B	-19.9V		
0x0C	-7.2V	0x2C	-10.4V	0x4C	-13.6V	0x6C	-16.8V	0x8C	-20.0V		
0x0D	-7.3V	0x2D	-10.5V	0x4D	-13.7V	0x6D	-16.9V	0x8D	-20.1V		
0x0E	-7.4V	0x2E	-10.6V	0x4E	-13.8V	0x6E	-17.0V	0x8E	-20.2V		
0x0F	-7.5V	0x2F	-10.7V	0x4F	-13.9V	0x6F	-17.1V	0x8F	-20.3V		
0x10	-7.6V	0x30	-10.8V	0x50	-14.0V	0x70	-17.2V	0x90	-20.4V		
0x11	-7.7V	0x31	-10.9V	0x51	-14.1V	0x71	-17.3V	0x91	-20.5V		
0x12	-7.8V	0x32	-11.0V	0x52	-14.2V	0x72	-17.4V	0x92	-20.6V		
0x13	-7.9V	0x33	-11.1V	0x53	-14.3V	0x73	-17.5V	0x93	-20.7V		
0x14	-8.0V	0x34	-11.2V	0x54	-14.4V	0x74	-17.6V	0x94	-20.8V		
0x15	-8.1V	0x35	-11.3V	0x55	-14.5V	0x75	-17.7V	0x95	-20.9V		
0x16	-8.2V	0x36	-11.4V	0x56	-14.6V	0x76	-17.8V	0x96	-21.0V		
0x17	-8.3V	0x37	-11.5V	0x57	-14.7V	0x77	-17.9V	0x97	-21.1V		
0x18	-8.4V	0x38	-11.6V	0x58	-14.8V	0x78	-18.0V	0x98	-21.2V		
0x19	-8.5V	0x39	-11.7V	0x59	-14.9V	0x79	-18.1V	0x99	-21.3V		
0x1A	-8.6V	0x3A	-11.8V	0x5A	-15.0V	0x7A	-18.2V	0x9A	-21.4V		
0x1B	-8.7V	0x3B	-11.9V	0x5B	-15.1V	0x7B	-18.3V	0x9B	-21.5V		
0x1C	-8.8V	0x3C	-12.0V	0x5C	-15.2V	0x7C	-18.4V	0x9C	-21.6V		
0x1D	-8.9V	0x3D	-12.1V	0x5D	-15.3V	0x7D	-18.5V	0x9D	-21.7V		
0x1E	-9.0V	0x3E	-12.2V	0x5E	-15.4V	0x7E	-18.6V	0x9E	-21.8V		
0x1F	-9.1V	0x3F	-12.3V	0x5F	-15.5V	0x7F	-18.7V	0x9F	-21.9V		

REGISTER MAPS (continued)

REG0x05: VGH1 Register [Reset = 0x3C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VGH1[7:0]	00111100	R/W	VGH1 Output Control V_{VGH1} = VGH1[7:0] × 100mV + 4V Range: 4V (00000000) ~ 19.9V (10011111) Default: 10V (00111100)

REG0x06: VGH2 Register [Reset = 0x3C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VGH2[7:0]	00111100	R/W	VGH2 Output Control V_{VGH2} = VGH2[7:0] × 100mV + 4V Range: 4V (00000000) ~ 19.9V (10011111) Default: 10V (00111100)

Table 8. VGH1/2[7:0] Description

Data (Hex)	VGH1/2	Data (Hex)	VGH1/2	Data (Hex)	VGH1/2	Data (Hex)	VGH1/2	Data (Hex)	VGH1/2
0x00	4.0V	0x20	7.2V	0x40	10.4V	0x60	13.6V	0x80	16.8V
0x01	4.1V	0x21	7.3V	0x41	10.5V	0x61	13.7V	0x81	16.9V
0x02	4.2V	0x22	7.4V	0x42	10.6V	0x62	13.8V	0x82	17.0V
0x03	4.3V	0x23	7.5V	0x43	10.7V	0x63	13.9V	0x83	17.1V
0x04	4.4V	0x24	7.6V	0x44	10.8V	0x64	14.0V	0x84	17.2V
0x05	4.5V	0x25	7.7V	0x45	10.9V	0x65	14.1V	0x85	17.3V
0x06	4.6V	0x26	7.8V	0x46	11.0V	0x66	14.2V	0x86	17.4V
0x07	4.7V	0x27	7.9V	0x47	11.1V	0x67	14.3V	0x87	17.5V
0x08	4.8V	0x28	8.0V	0x48	11.2V	0x68	14.4V	0x88	17.6V
0x09	4.9V	0x29	8.1V	0x49	11.3V	0x69	14.5V	0x89	17.7V
0x0A	5.0V	0x2A	8.2V	0x4A	11.4V	0x6A	14.6V	0x8A	17.8V
0x0B	5.1V	0x2B	8.3V	0x4B	11.5V	0x6B	14.7V	0x8B	17.9V
0x0C	5.2V	0x2C	8.4V	0x4C	11.6V	0x6C	14.8V	0x8C	18.0V
0x0D	5.3V	0x2D	8.5V	0x4D	11.7V	0x6D	14.9V	0x8D	18.1V
0x0E	5.4V	0x2E	8.6V	0x4E	11.8V	0x6E	15.0V	0x8E	18.2V
0x0F	5.5V	0x2F	8.7V	0x4F	11.9V	0x6F	15.1V	0x8F	18.3V
0x10	5.6V	0x30	8.8V	0x50	12.0V	0x70	15.2V	0x90	18.4V
0x11	5.7V	0x31	8.9V	0x51	12.1V	0x71	15.3V	0x91	18.5V
0x12	5.8V	0x32	9.0V	0x52	12.2V	0x72	15.4V	0x92	18.6V
0x13	5.9V	0x33	9.1V	0x53	12.3V	0x73	15.5V	0x93	18.7V
0x14	6.0V	0x34	9.2V	0x54	12.4V	0x74	15.6V	0x94	18.8V
0x15	6.1V	0x35	9.3V	0x55	12.5V	0x75	15.7V	0x95	18.9V
0x16	6.2V	0x36	9.4V	0x56	12.6V	0x76	15.8V	0x96	19.0V
0x17	6.3V	0x37	9.5V	0x57	12.7V	0x77	15.9V	0x97	19.1V
0x18	6.4V	0x38	9.6V	0x58	12.8V	0x78	16.0V	0x98	19.2V
0x19	6.5V	0x39	9.7V	0x59	12.9V	0x79	16.1V	0x99	19.3V
0x1A	6.6V	0x3A	9.8V	0x5A	13.0V	0x7A	16.2V	0x9A	19.4V
0x1B	6.7V	0x3B	9.9V	0x5B	13.1V	0x7B	16.3V	0x9B	19.5V
0x1C	6.8V	0x3C	10.0V	0x5C	13.2V	0x7C	16.4V	0x9C	19.6V
0x1D	6.9V	0x3D	10.1V	0x5D	13.3V	0x7D	16.5V	0x9D	19.7V
0x1E	7.0V	0x3E	10.2V	0x5E	13.4V	0x7E	16.6V	0x9E	19.8V
0x1F	7.1V	0x3F	10.3V	0x5F	13.5V	0x7F	16.7V	0x9F	19.9V

REGISTER MAPS (continued)

REG0x07: VGL1 Register [Reset = 0x50]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VGL1[7:0]	01010000	R/W	VGL1 Output Control V_{VGL1} = -VGL1[7:0] × 100mV - 2V Offset: -2V Range: -2V (00000000) ~ -21V (10111110) Default: -10V (01010000)

REG0x08: VGL2 Register [Reset = 0x50]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VGL2[7:0]	01010000	R/W	VGL2 Output Control V_{VGL2} = -VGL2[7:0] × 100mV - 2V Offset: -2V Range: -2V (00000000) ~ -21V (10111110) Default: -10V (01010000)

Table 9. VGL1/2[7:0] Description

Data (Hex)	VGL1/2	Data (Hex)	VGL1/2	Data (Hex)	VGL1/2	Data (Hex)	VGL1/2	Data (Hex)	VGL1/2	Data (Hex)	VGL1/2
0x00	-2.0V	0x20	-5.2V	0x40	-8.4V	0x60	-11.6V	0x80	-14.8V	0xA0	-18.0V
0x01	-2.1V	0x21	-5.3V	0x41	-8.5V	0x61	-11.7V	0x81	-14.9V	0xA1	-18.1V
0x02	-2.2V	0x22	-5.4V	0x42	-8.6V	0x62	-11.8V	0x82	-15.0V	0xA2	-18.2V
0x03	-2.3V	0x23	-5.5V	0x43	-8.7V	0x63	-11.9V	0x83	-15.1V	0xA3	-18.3V
0x04	-2.4V	0x24	-5.6V	0x44	-8.8V	0x64	-12.0V	0x84	-15.2V	0xA4	-18.4V
0x05	-2.5V	0x25	-5.7V	0x45	-8.9V	0x65	-12.1V	0x85	-15.3V	0xA5	-18.5V
0x06	-2.6V	0x26	-5.8V	0x46	-9.0V	0x66	-12.2V	0x86	-15.4V	0xA6	-18.6V
0x07	-2.7V	0x27	-5.9V	0x47	-9.1V	0x67	-12.3V	0x87	-15.5V	0xA7	-18.7V
0x08	-2.8V	0x28	-6.0V	0x48	-9.2V	0x68	-12.4V	0x88	-15.6V	0xA8	-18.8V
0x09	-2.9V	0x29	-6.1V	0x49	-9.3V	0x69	-12.5V	0x89	-15.7V	0xA9	-18.9V
0x0A	-3.0V	0x2A	-6.2V	0x4A	-9.4V	0x6A	-12.6V	0x8A	-15.8V	0xAA	-19.0V
0x0B	-3.1V	0x2B	-6.3V	0x4B	-9.5V	0x6B	-12.7V	0x8B	-15.9V	0xAB	-19.1V
0x0C	-3.2V	0x2C	-6.4V	0x4C	-9.6V	0x6C	-12.8V	0x8C	-16.0V	0xAC	-19.2V
0x0D	-3.3V	0x2D	-6.5V	0x4D	-9.7V	0x6D	-12.9V	0x8D	-16.1V	0xAD	-19.3V
0x0E	-3.4V	0x2E	-6.6V	0x4E	-9.8V	0x6E	-13.0V	0x8E	-16.2V	0xAE	-19.4V
0x0F	-3.5V	0x2F	-6.7V	0x4F	-9.9V	0x6F	-13.1V	0x8F	-16.3V	0xAF	-19.5V
0x10	-3.6V	0x30	-6.8V	0x50	-10.0V	0x70	-13.2V	0x90	-16.4V	0xB0	-19.6V
0x11	-3.7V	0x31	-6.9V	0x51	-10.1V	0x71	-13.3V	0x91	-16.5V	0xB1	-19.7V
0x12	-3.8V	0x32	-7.0V	0x52	-10.2V	0x72	-13.4V	0x92	-16.6V	0xB2	-19.8V
0x13	-3.9V	0x33	-7.1V	0x53	-10.3V	0x73	-13.5V	0x93	-16.7V	0xB3	-19.9V
0x14	-4.0V	0x34	-7.2V	0x54	-10.4V	0x74	-13.6V	0x94	-16.8V	0xB4	-20.0V
0x15	-4.1V	0x35	-7.3V	0x55	-10.5V	0x75	-13.7V	0x95	-16.9V	0xB5	-20.1V
0x16	-4.2V	0x36	-7.4V	0x56	-10.6V	0x76	-13.8V	0x96	-17.0V	0xB6	-20.2V
0x17	-4.3V	0x37	-7.5V	0x57	-10.7V	0x77	-13.9V	0x97	-17.1V	0xB7	-20.3V
0x18	-4.4V	0x38	-7.6V	0x58	-10.8V	0x78	-14.0V	0x98	-17.2V	0xB8	-20.4V
0x19	-4.5V	0x39	-7.7V	0x59	-10.9V	0x79	-14.1V	0x99	-17.3V	0xB9	-20.5V
0x1A	-4.6V	0x3A	-7.8V	0x5A	-11.0V	0x7A	-14.2V	0x9A	-17.4V	0xBA	-20.6V
0x1B	-4.7V	0x3B	-7.9V	0x5B	-11.1V	0x7B	-14.3V	0x9B	-17.5V	0xBB	-20.7V
0x1C	-4.8V	0x3C	-8.0V	0x5C	-11.2V	0x7C	-14.4V	0x9C	-17.6V	0xBC	-20.8V
0x1D	-4.9V	0x3D	-8.1V	0x5D	-11.3V	0x7D	-14.5V	0x9D	-17.7V	0xBD	-20.9V
0x1E	-5.0V	0x3E	-8.2V	0x5E	-11.4V	0x7E	-14.6V	0x9E	-17.8V	0xBE	-21.0V
0x1F	-5.1V	0x3F	-8.3V	0x5F	-11.5V	0x7F	-14.7V	0x9F	-17.9V	0xBF	Null

REGISTER MAPS (continued)

REG0x09: Negative VINT1 Register [Reset = 0x3C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VINT1[7:0]	00111100	R/W	VINT1 Output Control V_{INT1} = -VINT1[7:0] × 100mV Range: -0.5V (00000101) ~ -19V (10111110) Default: -6V (00111100)

REG0x0A: Negative VINT2 Register [Reset = 0x3C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VINT2[7:0]	00111100	R/W	VINT2 Output Control V_{INT2} = -VINT2[7:0] × 100mV Range: -0.5V (00000101) ~ -19V (10111110) Default: -6V (00111100)

Table 10. VINT1/2[7:0] Description

Data (Hex)	VINT1/2	Data (Hex)	VINT1/2	Data (Hex)	VINT1/2	Data (Hex)	VINT1/2	Data (Hex)	VINT1/2	Data (Hex)	VINT1/2
0x05	-0.5V	0x25	-3.7V	0x45	-6.9V	0x65	-10.1V	0x85	-13.3V	0xA5	-16.5V
0x06	-0.6V	0x26	-3.8V	0x46	-7.0V	0x66	-10.2V	0x86	-13.4V	0xA6	-16.6V
0x07	-0.7V	0x27	-3.9V	0x47	-7.1V	0x67	-10.3V	0x87	-13.5V	0xA7	-16.7V
0x08	-0.8V	0x28	-4.0V	0x48	-7.2V	0x68	-10.4V	0x88	-13.6V	0xA8	-16.8V
0x09	-0.9V	0x29	-4.1V	0x49	-7.3V	0x69	-10.5V	0x89	-13.7V	0xA9	-16.9V
0x0A	-1.0V	0x2A	-4.2V	0x4A	-7.4V	0x6A	-10.6V	0x8A	-13.8V	0xAA	-17.0V
0x0B	-1.1V	0x2B	-4.3V	0x4B	-7.5V	0x6B	-10.7V	0x8B	-13.9V	0xAB	-17.1V
0x0C	-1.2V	0x2C	-4.4V	0x4C	-7.6V	0x6C	-10.8V	0x8C	-14.0V	0xAC	-17.2V
0x0D	-1.3V	0x2D	-4.5V	0x4D	-7.7V	0x6D	-10.9V	0x8D	-14.1V	0xAD	-17.3V
0x0E	-1.4V	0x2E	-4.6V	0x4E	-7.8V	0x6E	-11.0V	0x8E	-14.2V	0xAE	-17.4V
0x0F	-1.5V	0x2F	-4.7V	0x4F	-7.9V	0x6F	-11.1V	0x8F	-14.3V	0xAF	-17.5V
0x10	-1.6V	0x30	-4.8V	0x50	-8.0V	0x70	-11.2V	0x90	-14.4V	0xB0	-17.6V
0x11	-1.7V	0x31	-4.9V	0x51	-8.1V	0x71	-11.3V	0x91	-14.5V	0xB1	-17.7V
0x12	-1.8V	0x32	-5.0V	0x52	-8.2V	0x72	-11.4V	0x92	-14.6V	0xB2	-17.8V
0x13	-1.9V	0x33	-5.1V	0x53	-8.3V	0x73	-11.5V	0x93	-14.7V	0xB3	-17.9V
0x14	-2.0V	0x34	-5.2V	0x54	-8.4V	0x74	-11.6V	0x94	-14.8V	0xB4	-18.0V
0x15	-2.1V	0x35	-5.3V	0x55	-8.5V	0x75	-11.7V	0x95	-14.9V	0xB5	-18.1V
0x16	-2.2V	0x36	-5.4V	0x56	-8.6V	0x76	-11.8V	0x96	-15.0V	0xB6	-18.2V
0x17	-2.3V	0x37	-5.5V	0x57	-8.7V	0x77	-11.9V	0x97	-15.1V	0xB7	-18.3V
0x18	-2.4V	0x38	-5.6V	0x58	-8.8V	0x78	-12.0V	0x98	-15.2V	0xB8	-18.4V
0x19	-2.5V	0x39	-5.7V	0x59	-8.9V	0x79	-12.1V	0x99	-15.3V	0xB9	-18.5V
0x1A	-2.6V	0x3A	-5.8V	0x5A	-9.0V	0x7A	-12.2V	0x9A	-15.4V	0xBA	-18.6V
0x1B	-2.7V	0x3B	-5.9V	0x5B	-9.1V	0x7B	-12.3V	0x9B	-15.5V	0xBB	-18.7V
0x1C	-2.8V	0x3C	-6.0V	0x5C	-9.2V	0x7C	-12.4V	0x9C	-15.6V	0xBC	-18.8V
0x1D	-2.9V	0x3D	-6.1V	0x5D	-9.3V	0x7D	-12.5V	0x9D	-15.7V	0xBD	-18.9V
0x1E	-3.0V	0x3E	-6.2V	0x5E	-9.4V	0x7E	-12.6V	0x9E	-15.8V	0xBE	-19.0V
0x1F	-3.1V	0x3F	-6.3V	0x5F	-9.5V	0x7F	-12.7V	0x9F	-15.9V	0xBF	Null
0x20	-3.2V	0x40	-6.4V	0x60	-9.6V	0x80	-12.8V	0xA0	-16.0V		
0x21	-3.3V	0x41	-6.5V	0x61	-9.7V	0x81	-12.9V	0xA1	-16.1V		
0x22	-3.4V	0x42	-6.6V	0x62	-9.8V	0x82	-13.0V	0xA2	-16.2V		
0x23	-3.5V	0x43	-6.7V	0x63	-9.9V	0x83	-13.1V	0xA3	-16.3V		
0x24	-3.6V	0x44	-6.8V	0x64	-10.0V	0x84	-13.2V	0xA4	-16.4V		

REGISTER MAPS (continued)

REG0x0B: Positive VINT3 Register [Reset = 0x7C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VINT3[7:0]	01111100	R/W	VINT3 Output Control V_{VINT3} = VINT3[7:0] × 50mV + 1V Range: 1V (00000000) ~ 10V (10110100) Default: 7.2V (01111100)

Table 11. VINT3[7:0] Description

Data (Hex)	VINT3	Data (Hex)	VINT3	Data (Hex)	VINT3	Data (Hex)	VINT3	Data (Hex)	VINT3	Data (Hex)	VINT3
0x00	1.00V	0x20	2.60V	0x40	4.20V	0x60	5.80V	0x80	7.40V	0xA0	9.00V
0x01	1.05V	0x21	2.65V	0x41	4.25V	0x61	5.85V	0x81	7.45V	0xA1	9.05V
0x02	1.10V	0x22	2.70V	0x42	4.30V	0x62	5.90V	0x82	7.50V	0xA2	9.10V
0x03	1.15V	0x23	2.75V	0x43	4.35V	0x63	5.95V	0x83	7.55V	0xA3	9.15V
0x04	1.20V	0x24	2.80V	0x44	4.40V	0x64	6.00V	0x84	7.60V	0xA4	9.20V
0x05	1.25V	0x25	2.85V	0x45	4.45V	0x65	6.05V	0x85	7.65V	0xA5	9.25V
0x06	1.30V	0x26	2.90V	0x46	4.50V	0x66	6.10V	0x86	7.70V	0xA6	9.30V
0x07	1.35V	0x27	2.95V	0x47	4.55V	0x67	6.15V	0x87	7.75V	0xA7	9.35V
0x08	1.40V	0x28	3.00V	0x48	4.60V	0x68	6.20V	0x88	7.80V	0xA8	9.40V
0x09	1.45V	0x29	3.05V	0x49	4.65V	0x69	6.25V	0x89	7.85V	0xA9	9.45V
0x0A	1.50V	0x2A	3.10V	0x4A	4.70V	0x6A	6.30V	0x8A	7.90V	0xAA	9.50V
0x0B	1.55V	0x2B	3.15V	0x4B	4.75V	0x6B	6.35V	0x8B	7.95V	0xAB	9.55V
0x0C	1.60V	0x2C	3.20V	0x4C	4.80V	0x6C	6.40V	0x8C	8.00V	0xAC	9.60V
0x0D	1.65V	0x2D	3.25V	0x4D	4.85V	0x6D	6.45V	0x8D	8.05V	0xAD	9.65V
0x0E	1.70V	0x2E	3.30V	0x4E	4.90V	0x6E	6.50V	0x8E	8.10V	0xAE	9.70V
0x0F	1.75V	0x2F	3.35V	0x4F	4.95V	0x6F	6.55V	0x8F	8.15V	0xAF	9.75V
0x10	1.80V	0x30	3.40V	0x50	5.00V	0x70	6.60V	0x90	8.20V	0xB0	9.80V
0x11	1.85V	0x31	3.45V	0x51	5.05V	0x71	6.65V	0x91	8.25V	0xB1	9.85V
0x12	1.90V	0x32	3.50V	0x52	5.10V	0x72	6.70V	0x92	8.30V	0xB2	9.90V
0x13	1.95V	0x33	3.55V	0x53	5.15V	0x73	6.75V	0x93	8.35V	0xB3	9.95V
0x14	2.00V	0x34	3.60V	0x54	5.20V	0x74	6.80V	0x94	8.40V	0xB4	10.00V
0x15	2.05V	0x35	3.65V	0x55	5.25V	0x75	6.85V	0x95	8.45V	0xB5	Null
0x16	2.10V	0x36	3.70V	0x56	5.30V	0x76	6.90V	0x96	8.50V	0xB6	Null
0x17	2.15V	0x37	3.75V	0x57	5.35V	0x77	6.95V	0x97	8.55V	0xB7	Null
0x18	2.20V	0x38	3.80V	0x58	5.40V	0x78	7.00V	0x98	8.60V	0xB8	Null
0x19	2.25V	0x39	3.85V	0x59	5.45V	0x79	7.05V	0x99	8.65V	0xB9	Null
0x1A	2.30V	0x3A	3.90V	0x5A	5.50V	0x7A	7.10V	0x9A	8.70V	0xBA	Null
0x1B	2.35V	0x3B	3.95V	0x5B	5.55V	0x7B	7.15V	0x9B	8.75V	0xBB	Null
0x1C	2.40V	0x3C	4.00V	0x5C	5.60V	0x7C	7.20V	0x9C	8.80V	0xBC	Null
0x1D	2.45V	0x3D	4.05V	0x5D	5.65V	0x7D	7.25V	0x9D	8.85V	0xBD	Null
0x1E	2.50V	0x3E	4.10V	0x5E	5.70V	0x7E	7.30V	0x9E	8.90V	0xBE	Null
0x1F	2.55V	0x3F	4.15V	0x5F	5.75V	0x7F	7.35V	0x9F	8.95V	0xBF	Null

REGISTER MAPS (continued)

REG0x0C: VREFH 1 Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000000	R/W	Reserved
D[1:0]	VREFH[9:8]	10	R/W	High 2 Bits of VREFH Output Control V_{VREFH} = VREFH[9:0] × 10mV Range: 4.4V (01 1011 1000) ~ 9.5V (11 1011 0110) Default: 6.8V (10 1010 1000)

REG0x0D: VREFH 2 Register [Reset = 0xA8]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VREFH[7:0]	1010 1000	R/W	Low Byte of VREFH Output Control V_{VREFH} = VREFH[9:0] × 10mV Range: 4.4V (01 1011 1000) ~ 9.5V (11 1011 0110) Default: 6.8V (10 1010 1000)

Table 12. VREFH[9:0] Description

Data (Hex)	VREFH	Data (Hex)	VREFH	Data (Hex)	VREFH
…	…	…	…	…	…
0x01B8	4.40V	0x02A1	6.73V	0x03A1	9.29V
0x01B9	4.41V	0x02A2	6.74V	0x03A2	9.30V
0x01BA	4.42V	0x02A3	6.75V	0x03A3	9.31V
0x01BB	4.43V	0x02A4	6.76V	0x03A4	9.32V
0x01BC	4.44V	0x02A5	6.77V	0x03A5	9.33V
0x01BD	4.45V	0x02A6	6.78V	0x03A6	9.34V
0x01BE	4.46V	0x02A7	6.79V	0x03A7	9.35V
0x01BF	4.47V	0x02A8	6.80V	0x03A8	9.36V
0x01C0	4.48V	0x02A9	6.81V	0x03A9	9.37V
0x01C1	4.49V	0x02AA	6.82V	0x03AA	9.38V
0x01C2	4.50V	0x02AB	6.83V	0x03AB	9.39V
0x01C3	4.51V	0x02AC	6.84V	0x03AC	9.40V
0x01C4	4.52V	0x02AD	6.85V	0x03AD	9.41V
0x01C5	4.53V	0x02AE	6.86V	0x03AE	9.42V
0x01C6	4.54V	0x02AF	6.87V	0x03AF	9.43V
0x01C7	4.55V	0x02B0	6.88V	0x03B0	9.44V
0x01C8	4.56V	0x02B1	6.89V	0x03B1	9.45V
0x01C9	4.57V	0x02B2	6.90V	0x03B2	9.46V
0x01CA	4.58V	0x02B3	6.91V	0x03B3	9.47V
0x01CB	4.59V	0x02B4	6.92V	0x03B4	9.48V
0x01CC	4.60V	0x02B5	6.93V	0x03B5	9.49V
0x01CD	4.61V	0x02B6	6.94V	0x03B6	9.50V
0x01CE	4.62V	0x02B7	6.95V		
0x01CF	4.63V	0x02B8	6.96V		
…	…	…	…		

REGISTER MAPS (continued)

REG0x0E: VREFL 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000000	R/W	Reserved
D[1:0]	VREFL[9:8]	00	R/W	High 2 Bits of VREFL Output Control V_{VREFL} = VREFL[9:0] × 10mV Range: 0.5V (00 0011 0010) ~ 5.5V (10 0010 0110) Default: 1.5V (00 1001 0110)

REG0x0F: VREFL 2 Register [Reset = 0x96]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VREFL[7:0]	1001 0110	R/W	Low Byte of VREFL Output Control V_{VREFL} = VREFL[9:0] × 10mV Range: 0.5V (00 0011 0010) ~ 5.5V (10 0010 0110) Default: 1.5V (00 1001 0110)

Table 13. VREFL[9:0] Description

Data (Hex)	VREFL	Data (Hex)	VREFL	Data (Hex)	VREFL
…	…	…	…	…	…
0x0032	0.50V	0x0092	1.46V	0x0212	5.30V
0x0033	0.51V	0x0093	1.47V	0x0213	5.31V
0x0034	0.52V	0x0094	1.48V	0x0214	5.32V
0x0035	0.53V	0x0095	1.49V	0x0215	5.33V
0x0036	0.54V	0x0096	1.50V	0x0216	5.34V
0x0037	0.55V	0x0097	1.51V	0x0217	5.35V
0x0038	0.56V	0x0098	1.52V	0x0218	5.36V
0x0039	0.57V	0x0099	1.53V	0x0219	5.37V
0x003A	0.58V	0x009A	1.54V	0x021A	5.38V
0x003B	0.59V	0x009B	1.55V	0x021B	5.39V
0x003C	0.60V	0x009C	1.56V	0x021C	5.40V
0x003D	0.61V	0x009D	1.57V	0x021D	5.41V
0x003E	0.62V	0x009E	1.58V	0x021E	5.42V
0x003F	0.63V	0x009F	1.59V	0x021F	5.43V
0x0040	0.64V	0x00A0	1.60V	0x0220	5.44V
0x0041	0.65V	0x00A1	1.61V	0x0221	5.45V
0x0042	0.66V	0x00A2	1.62V	0x0222	5.46V
0x0043	0.67V	0x00A3	1.63V	0x0223	5.47V
0x0044	0.68V	0x00A4	1.64V	0x0224	5.48V
0x0045	0.69V	0x00A5	1.65V	0x0225	5.49V
0x0046	0.70V	0x00A6	1.66V	0x0226	5.50V
0x0047	0.71V	0x00A7	1.67V		
0x0048	0.72V	0x00A8	1.68V		
0x0049	0.73V	0x00A9	1.69V		
…	…	…	…		

REGISTER MAPS (continued)

REG0x10: VINT1/2[7:0] Voltage Fine Tuner Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	VINT2_FT[3:0]	0000	R/W	VINT2[7:0] Absolute Voltage Fine Tuner: 0000 = |VINT2[7:0]| (default) 0001 = |VINT2[7:0]| + 10mV 0010 = |VINT2[7:0]| + 20mV 0011 = |VINT2[7:0]| + 30mV 0100 = |VINT2[7:0]| + 40mV 0101 = |VINT2[7:0]| + 50mV 0110 = |VINT2[7:0]| + 60mV 0111 = |VINT2[7:0]| + 70mV 1000 = |VINT2[7:0]| + 80mV 1001 = |VINT2[7:0]| + 90mV Others = Null
D[3:0]	VINT1_FT[3:0]	0000	R/W	VINT1[7:0] Absolute Voltage Fine Tuner 0000 = |VINT1[7:0]| (default) 0001 = |VINT1[7:0]| + 10mV 0010 = |VINT1[7:0]| + 20mV 0011 = |VINT1[7:0]| + 30mV 0100 = |VINT1[7:0]| + 40mV 0101 = |VINT1[7:0]| + 50mV 0110 = |VINT1[7:0]| + 60mV 0111 = |VINT1[7:0]| + 70mV 1000 = |VINT1[7:0]| + 80mV 1001 = |VINT1[7:0]| + 90mV Others = Null

REG0x11: VINT3[7:0] Voltage Fine Tuner Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	Reserved
D[3]	VREFH/L_SR	0	R/W	VREFH & VREFL Slew Rate Control 0 = Fast (default) 1 = Slow
D[2:0]	VINT3_FT[2:0]	000	R/W	VINT3[7:0] Voltage Fine Tuner 000 = VINT3[7:0] (default) 001 = VINT3[7:0] + 10mV 010 = VINT3[7:0] + 20mV 011 = VINT3[7:0] + 30mV 100 = VINT3[7:0] + 40mV Others = Null

REGISTER MAPS (continued)

REG0x12: VCORE_ON/OFF Control Register [Reset = 0x2E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VCORE_ON_DLY[2:0]	001	R/W	VCORE Power On Delay Timer Setting: 000 = 0.5ms 001 = 0.5ms (default) 010 = 1.0ms 011 = 1.5ms 100 = 2.0ms 101 = 2.5ms 110 = 3.0ms 111 = 3.5ms
D[4:2]	VCORE_OFF_DLY[2:0]	011	R/W	VCORE Power Off Delay Timer Setting: 000 = 3ms 001 = 5ms 010 = 7ms 011 = 9ms (default) 100 = 11ms 101 = 13ms 110 = 15ms 111 = 17ms
D[1]	VCORE_EN	1	R/W	VCORE Enable Control: 0 = Disable 1 = Enable (default)
D[0]	Reserved	0	R/W	Reserved

REG0x13: VIO_ON/OFF Control Register [Reset = 0x2E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VIO_ON_DLY[2:0]	001	R/W	VIO Power On Delay Timer Setting: 000 = 0.5ms 001 = 0.5ms (default) 010 = 1.0ms 011 = 1.5ms 100 = 2.0ms 101 = 2.5ms 110 = 3.0ms 111 = 3.5ms
D[4:2]	VIO_OFF_DLY[2:0]	011	R/W	VIO Power Off Delay Timer Setting: 000 = 3ms 001 = 5ms 010 = 7ms 011 = 9ms (default) 100 = 11ms 101 = 13ms 110 = 15ms 111 = 17ms
D[1]	VIO_EN	1	R/W	VIO Enable Control: 0 = Disable 1 = Enable (default)
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x14: VDDI_ON/OFF Control Register [Reset = 0x2E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VDDI_ON_DLY[2:0]	001	R/W	VDDI Power On Delay Timer Setting: 000 = 0.5ms 001 = 0.5ms (default) 010 = 1.0ms 011 = 1.5ms 100 = 2.0ms 101 = 2.5ms 110 = 3.0ms 111 = 3.5ms
D[4:2]	VDDI_OFF_DLY[2:0]	011	R/W	VDDI Power Off Delay Timer Setting: 000 = 3ms 001 = 5ms 010 = 7ms 011 = 9ms (default) 100 = 11ms 101 = 13ms 110 = 15ms 111 = 17ms
D[1]	VDDI_EN	1	R/W	VDDI Enable Control: 0 = Disable 1 = Enable (default)
D[0]	Reserved	0	R/W	Reserved

REG0x15: PAVDD_ON/OFF Control Register [Reset = 0x12]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	PAVDD_ON_DLY[2:0]	000	R/W	PAVDD Power On Delay Timer Setting: 000 = 1ms (default) 001 = 3ms 010 = 5ms 011 = 7ms 100 = 9ms 101 = 11ms 110 = 13ms 111 = 15ms
D[4:2]	PAVDD_OFF_DLY[2:0]	100	R/W	PAVDD Power Off Delay Timer Setting: 000 = 11ms 001 = 14ms 010 = 17ms 011 = 20ms 100 = 23ms (default) 101 = 26ms 110 = 29ms 111 = 32ms
D[1]	PAVDD_EN	1	R/W	PAVDD Enable Control: 0 = Disable 1 = Enable (default)
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x16: AVDD_ON/OFF Control Register [Reset = 0x94]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	AVDD_ON_DLY[2:0]	100	R/W	AVDD Power On Delay Timer Setting: 000 = 11ms 001 = 14ms 010 = 17ms 011 = 20ms 100 = 23ms (default) 101 = 26ms 110 = 29ms 111 = 32ms
D[4:3]	AVDD_OFF_DLY[1:0]	10	R/W	AVDD Power Off Delay Timer Setting: 00 = 3ms 01 = 5ms 10 = 7ms (default) 11 = 9ms
D[2]	AVDD_EN	1	R/W	AVDD Enable Control: 0 = Disable 1 = Enable (default)
D[1:0]	AVDD_SST[1:0]	00	R/W	AVDD Soft-Start Timer Setting: 00 = 4ms (default) 01 = 5ms 10 = 6ms 11 = 7ms

REG0x17: PVGH_ON/OFF Control Register [Reset = 0x42]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	010000	R/W	Reserved
D[1]	PVGH_EN	1	R/W	PVGH Enable Control: 0 = Disable 1 = Enable (default)
D[0]	Reserved	0	R/W	Reserved

REG0x18: VGH1_ON/OFF Control Register [Reset = 0x68]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VGH1_ON_DLY[2:0]	011	R/W	VGH1 Power On Delay Timer Setting: 000 = 3ms 001 = 5ms 010 = 7ms 011 = 9ms (default) 100 = 11ms 101 = 13ms 110 = 15ms 111 = 17ms
D[4:2]	VGH1_OFF_DLY[2:0]	010	R/W	VGH1 Power Off Delay Timer Setting: 000 = 11ms 001 = 14ms 010 = 17ms (default) 011 = 20ms 100 = 23ms 101 = 26ms 110 = 29ms 111 = 32ms
D[1]	VGH1_EN	0	R/W	VGH1 Enable Control: 0 = Disable (default) 1 = Enable
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x19: VGH2_ON/OFF Control Register [Reset = 0x88]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VGH2_ON_DLY[2:0]	100	R/W	VGH2 Power On Delay Timer Setting: 000 = 3ms 001 = 5ms 010 = 7ms 011 = 9ms 100 = 11ms (default) 101 = 13ms 110 = 15ms 111 = 17ms
D[4:2]	VGH2_OFF_DLY[2:0]	010	R/W	VGH2 Power Off Delay Timer Setting: 000 = 11ms 001 = 14ms 010 = 17ms (default) 011 = 20ms 100 = 23ms 101 = 26ms 110 = 29ms 111 = 32ms
D[1]	VGH2_EN	0	R/W	VGH2 Enable Control: 0 = Disable (default) 1 = Enable
D[0]	Reserved	0	R/W	Reserved

REG0x1A: PVGL_ON/OFF Control Register [Reset = 0x4E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	PVGL_ON_DLY[2:0]	010	R/W	PVGL Power On Delay Timer Setting: 000 = 1ms 001 = 3ms 010 = 5ms (default) 011 = 7ms 100 = 9ms 101 = 11ms 110 = 13ms 111 = 15ms
D[4:2]	PVGL_OFF_DLY[2:0]	011	R/W	PVGL Power Off Delay Timer Setting: 000 = 11ms 001 = 14ms 010 = 17ms 011 = 20ms (default) 100 = 23ms 101 = 26ms 110 = 29ms 111 = 32ms
D[1]	PVGL_EN	1	R/W	PVGL Enable Control: 0 = Disable 1 = Enable (default)
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x1B: VGL1_ON/OFF Control Register [Reset = 0xA8]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VGL1_ON_DLY[2:0]	101	R/W	VGL1 Power On Delay Timer Setting: 000 = 3ms 001 = 5ms 010 = 7ms 011 = 9ms 100 = 11ms 101 = 13ms (default) 110 = 15ms 111 = 17ms
D[4:2]	VGL1_OFF_DLY[2:0]	010	R/W	VGL1 Power Off Delay Timer Setting: 000 = 11ms 001 = 14ms 010 = 17ms (default) 011 = 20ms 100 = 23ms 101 = 26ms 110 = 29ms 111 = 32ms
D[1]	VGL1_EN	0	R/W	VGL1 Enable Control: 0 = Disable (default) 1 = Enable
D[0]	Reserved	0	R/W	Reserved

REG0x1C: VGL2_ON/OFF Control Register [Reset = 0xC8]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VGL2_ON_DLY[2:0]	110	R/W	VGL2 Power On Delay Timer Setting: 000 = 3ms 001 = 5ms 010 = 7ms 011 = 9ms 100 = 11ms 101 = 13ms 110 = 15ms (default) 111 = 17ms
D[4:2]	VGL2_OFF_DLY[2:0]	010	R/W	VGL2 Power Off Delay Timer Setting: 000 = 11ms 001 = 14ms 010 = 17ms (default) 011 = 20ms 100 = 23ms 101 = 26ms 110 = 29ms 111 = 32ms
D[1]	VGL2_EN	0	R/W	VGL2 Enable Control: 0 = Disable (default) 1 = Enable
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x1D: VINT1_ON/OFF Control Register [Reset = 0x50]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VINT1_ON_DLY[2:0]	010	R/W	VINT1 Power On Delay Timer Setting: 000 = 11ms 001 = 14ms 010 = 17ms (default) 011 = 20ms 100 = 23ms 101 = 26ms 110 = 29ms 111 = 32ms
D[4:2]	VINT1_OFF_DLY[2:0]	100	R/W	VINT1 Power Off Delay Timer Setting: 000 = 3ms 001 = 5ms 010 = 7ms 011 = 9ms 100 = 11ms (default) 101 = 13ms 110 = 15ms 111 = 17ms
D[1]	VINT1_EN	0	R/W	VINT1 Enable Control: 0 = Disable (default) 1 = Enable
D[0]	Reserved	0	R/W	Reserved

REG0x1E: VINT2_ON/OFF Control Register [Reset = 0x50]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VINT2_ON_DLY[2:0]	010	R/W	VINT2 Power On Delay Timer Setting: 000 = 11ms 001 = 14ms 010 = 17ms (default) 011 = 20ms 100 = 23ms 101 = 26ms 110 = 29ms 111 = 32ms
D[4:2]	VINT2_OFF_DLY[2:0]	100	R/W	VINT2 Power Off Delay Timer Setting: 000 = 3ms 001 = 5ms 010 = 7ms 011 = 9ms 100 = 11ms (default) 101 = 13ms 110 = 15ms 111 = 17ms
D[1]	VINT2_EN	0	R/W	VINT2 Enable Control: 0 = Disable (default) 1 = Enable
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x1F: VINT3_ON/OFF Control Register [Reset = 0x70]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VINT3_ON_DLY[2:0]	011	R/W	VINT3 Power On Delay Timer Setting: 000 = 11ms 001 = 14ms 010 = 17ms 011 = 20ms (default) 100 = 23ms 101 = 26ms 110 = 29ms 111 = 32ms
D[4:2]	VINT3_OFF_DLY[2:0]	100	R/W	VINT3 Power Off Delay Timer Setting: 000 = 3ms 001 = 5ms 010 = 7ms 011 = 9ms 100 = 11ms (default) 101 = 13ms 110 = 15ms 111 = 17ms
D[1]	VINT3_EN	0	R/W	VINT3 Enable Control: 0 = Disable (default) 1 = Enable
D[0]	Reserved	0	R/W	Reserved

REG0x20: VREFH&L_ON/OFF Control Register [Reset = 0xA0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VREFH&L_ON_DLY[2:0]	101	R/W	VREFH & VREFL Power On Delay Timer Setting: 000 = 12ms 001 = 15ms 010 = 18ms 011 = 21ms 100 = 24ms 101 = 27ms (default) 110 = 30ms 111 = 33ms
D[4:2]	VREFH&L_OFF_DLY[2:0]	000	R/W	VREFH & VREFL Power Off Delay Timer Setting: 000 = 3ms (default) 001 = 5ms 010 = 7ms 011 = 9ms 100 = 11ms 101 = 13ms 110 = 15ms 111 = 17ms
D[1]	VREFH&L_EN	0	R/W	VREFH & VREFL Enable Control: 0 = Disable (default) 1 = Enable)
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x21: FSW & SR_CTRL1 Register [Reset = 0x48]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VCORE_FSW[2:0]	010	R/W	VCORE SWB1 Switching Frequency Setting: 000 = 0.6MHz 001 = 0.9MHz 010 = 1.0MHz (default) 011 = 1.2MHz 100 = 1.5MHz 101 = 1.8MHz 110 = 2.0MHz 111 = 2.2MHz
D[4:2]	VIO_FSW[2:0]	010	R/W	VIO SWB2 Switching Frequency Setting: 000 = 0.6MHz 001 = 0.9MHz 010 = 1.0MHz (default) 011 = 1.2MHz 100 = 1.5MHz 101 = 1.8MHz 110 = 2.0MHz 111 = 2.2MHz
D[1:0]	VCORE_SR[1:0]	00	R/W	VCORE SWB1 Slew Rate Setting: 00 = Fast (default) 01 = Normal 10 = Slow 11 = Slowest

REG0x22: FSW & SR_CTRL2 Register [Reset = 0x48]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	VDDI_FSW[2:0]	010	R/W	VDDI SWB3 Switching Frequency Setting: 000 = 0.6MHz 001 = 0.9MHz 010 = 1.0MHz (default) 011 = 1.2MHz 100 = 1.5MHz 101 = 1.8MHz 110 = 2.0MHz 111 = 2.2MHz
D[4:2]	PAVDD_FSW[2:0]	010	R/W	PAVDD SWP Switching Frequency Setting: 000 = 0.6MHz 001 = 0.9MHz 010 = 1.0MHz (default) 011 = 1.2MHz 100 = 1.5MHz 101 = 1.8MHz 110 = 2.0MHz 111 = 2.2MHz
D[1:0]	VIO_SR[1:0]	00	R/W	VIO SWB2 Slew Rate Setting: 00 = Fast (default) 01 = Normal 10 = Slow 11 = Slowest

REGISTER MAPS (continued)

REG0x23: FSW & SR_CTRL3 Register [Reset = 0x40]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	PVGL_FSW[2:0]	010	R/W	PVGL SWN Switching Frequency Setting: 000 = 0.6MHz 001 = 0.9MHz 010 = 1.0MHz (default) 011 = 1.2MHz 100 = 1.5MHz 101 = 1.8MHz 110 = 2.0MHz 111 = 2.2MHz
D[4]	Reserved	0	R/W	Reserved
D[3:2]	PAVDD_SR[1:0]	00	R/W	PAVDD SWP Slew Rate Setting: 00 = Fast (default) 01 = Normal 10 = Slow 11 = Slowest
D[1:0]	VDDI_SR[1:0]	00	R/W	VDDI SWB3 Slew Rate Setting: 00 = Fast (default) 01 = Normal 10 = Slow 11 = Slowest

REG0x24: FSW & SR_CTRL4 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000000	R/W	Reserved
D[1:0]	PVGL_SR[1:0]	00	R/W	PVGL SWN Slew Rate Setting: 00 = Fast (default) 01 = Normal 10 = Slow 11 = Slowest

REG0x25: VINT1/2_RTT Register [Reset = 0xFC]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	1111	R/W	Reserved
D[3]	VINT2_GPP	1	R/W	VINT2 Gap Polarity Setting: 0 = Negative 1 = Positive (default)
D[2]	VINT1_GPP	1	R/W	VINT1 Gap Polarity Setting: 0 = Negative 1 = Positive (default)
D[1]	VINT2_RTT_EN	0	R/W	VINT2 Real-time Tracking Enable Setting (Tracking ELVSS): 0 = Disable (default) 1 = Enable
D[0]	VINT1_RTT_EN	0	R/W	VINT1 Real-time Tracking Enable Setting (Tracking ELVSS): 0 = Disable (default) 1 = Enable

REGISTER MAPS (continued)

REG0x26: VINT1_PGP Register [Reset = 0x96]

REG0x27: VINT2_PGP Register [Reset = 0x96]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VINT1/2_PGP[7:0]	10010110	R/W	VINT1/2 Positive Gap Level for Voltage Setting: VINT1/2_PGP = VINT1/2_PGP[7:0] × 10mV Range: 0V (00000000) ~ 2.5V (11111010), 2.6V (11111011), 2.7V (11111100), 2.8V (11111101) 2.9V (11111110), 3.0V (11111111) Default: 1.5V (10010110)

Table 14. VINT1/2 PGP Description

Data (Hex)	VINT1/2_PGP	Data (Hex)	VINT1/2_PGP	Data (Hex)	VINT1/2_PGP	Data (Hex)	VINT1/2_PGP	Data (Hex)	VINT1/2_PGP	Data (Hex)	VINT1/2_PGP	Data (Hex)	VINT1/2_PGP	Data (Hex)	VINT1/2_PGP
0x00	0.00V	0x20	0.32V	0x40	0.64V	0x60	0.96V	0x80	1.28V	0xA0	1.60V	0xC0	1.92V	0xE0	2.24V
0x01	0.01V	0x21	0.33V	0x41	0.65V	0x61	0.97V	0x81	1.29V	0xA1	1.61V	0xC1	1.93V	0xE1	2.25V
0x02	0.02V	0x22	0.34V	0x42	0.66V	0x62	0.98V	0x82	1.30V	0xA2	1.62V	0xC2	1.94V	0xE2	2.26V
0x03	0.03V	0x23	0.35V	0x43	0.67V	0x63	0.99V	0x83	1.31V	0xA3	1.63V	0xC3	1.95V	0xE3	2.27V
0x04	0.04V	0x24	0.36V	0x44	0.68V	0x64	1.00V	0x84	1.32V	0xA4	1.64V	0xC4	1.96V	0xE4	2.28V
0x05	0.05V	0x25	0.37V	0x45	0.69V	0x65	1.01V	0x85	1.33V	0xA5	1.65V	0xC5	1.97V	0xE5	2.29V
0x06	0.06V	0x26	0.38V	0x46	0.70V	0x66	1.02V	0x86	1.34V	0xA6	1.66V	0xC6	1.98V	0xE6	2.30V
0x07	0.07V	0x27	0.39V	0x47	0.71V	0x67	1.03V	0x87	1.35V	0xA7	1.67V	0xC7	1.99V	0xE7	2.31V
0x08	0.08V	0x28	0.40V	0x48	0.72V	0x68	1.04V	0x88	1.36V	0xA8	1.68V	0xC8	2.00V	0xE8	2.32V
0x09	0.09V	0x29	0.41V	0x49	0.73V	0x69	1.05V	0x89	1.37V	0xA9	1.69V	0xC9	2.01V	0xE9	2.33V
0x0A	0.10V	0x2A	0.42V	0x4A	0.74V	0x6A	1.06V	0x8A	1.38V	0xAA	1.70V	0xCA	2.02V	0xEA	2.34V
0x0B	0.11V	0x2B	0.43V	0x4B	0.75V	0x6B	1.07V	0x8B	1.39V	0xAB	1.71V	0xCB	2.03V	0xEB	2.35V
0x0C	0.12V	0x2C	0.44V	0x4C	0.76V	0x6C	1.08V	0x8C	1.40V	0xAC	1.72V	0xCC	2.04V	0xEC	2.36V
0x0D	0.13V	0x2D	0.45V	0x4D	0.77V	0x6D	1.09V	0x8D	1.41V	0xAD	1.73V	0xCD	2.05V	0xED	2.37V
0x0E	0.14V	0x2E	0.46V	0x4E	0.78V	0x6E	1.10V	0x8E	1.42V	0xAE	1.74V	0xCE	2.06V	0xEE	2.38V
0x0F	0.15V	0x2F	0.47V	0x4F	0.79V	0x6F	1.11V	0x8F	1.43V	0xAF	1.75V	0xCF	2.07V	0xEF	2.39V
0x10	0.16V	0x30	0.48V	0x50	0.80V	0x70	1.12V	0x90	1.44V	0xB0	1.76V	0xD0	2.08V	0xF0	2.40V
0x11	0.17V	0x31	0.49V	0x51	0.81V	0x71	1.13V	0x91	1.45V	0xB1	1.77V	0xD1	2.09V	0xF1	2.41V
0x12	0.18V	0x32	0.50V	0x52	0.82V	0x72	1.14V	0x92	1.46V	0xB2	1.78V	0xD2	2.10V	0xF2	2.42V
0x13	0.19V	0x33	0.51V	0x53	0.83V	0x73	1.15V	0x93	1.47V	0xB3	1.79V	0xD3	2.11V	0xF3	2.43V
0x14	0.20V	0x34	0.52V	0x54	0.84V	0x74	1.16V	0x94	1.48V	0xB4	1.80V	0xD4	2.12V	0xF4	2.44V
0x15	0.21V	0x35	0.53V	0x55	0.85V	0x75	1.17V	0x95	1.49V	0xB5	1.81V	0xD5	2.13V	0xF5	2.45V
0x16	0.22V	0x36	0.54V	0x56	0.86V	0x76	1.18V	0x96	1.50V	0xB6	1.82V	0xD6	2.14V	0xF6	2.46V
0x17	0.23V	0x37	0.55V	0x57	0.87V	0x77	1.19V	0x97	1.51V	0xB7	1.83V	0xD7	2.15V	0xF7	2.47V
0x18	0.24V	0x38	0.56V	0x58	0.88V	0x78	1.20V	0x98	1.52V	0xB8	1.84V	0xD8	2.16V	0xF8	2.48V
0x19	0.25V	0x39	0.57V	0x59	0.89V	0x79	1.21V	0x99	1.53V	0xB9	1.85V	0xD9	2.17V	0xF9	2.49V
0x1A	0.26V	0x3A	0.58V	0x5A	0.90V	0x7A	1.22V	0x9A	1.54V	0xBA	1.86V	0xDA	2.18V	0xFA	2.50V
0x1B	0.27V	0x3B	0.59V	0x5B	0.91V	0x7B	1.23V	0x9B	1.55V	0xBB	1.87V	0xDB	2.19V	0xFB	2.60V
0x1C	0.28V	0x3C	0.60V	0x5C	0.92V	0x7C	1.24V	0x9C	1.56V	0xBC	1.88V	0xDC	2.20V	0xFC	2.70V
0x1D	0.29V	0x3D	0.61V	0x5D	0.93V	0x7D	1.25V	0x9D	1.57V	0xBD	1.89V	0xDD	2.21V	0xFD	2.80V
0x1E	0.30V	0x3E	0.62V	0x5E	0.94V	0x7E	1.26V	0x9E	1.58V	0xBE	1.90V	0xDE	2.22V	0xFE	2.90V
0x1F	0.31V	0x3F	0.63V	0x5F	0.95V	0x7F	1.27V	0x9F	1.59V	0xBF	1.91V	0xDF	2.23V	0xFF	3.00V

REGISTER MAPS (continued)

REG0x28: VINT1_NGP Register [Reset = 0x00]

REG0x29: VINT2_NGP Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VINT1/2_NGP[7:0]	00000000	R/W	VINT1/2 Negative Gap Level for Voltage Setting: VINT1/2_NGP = -VINT1/2_NGP[7:0] × 10mV Range: 0V (00000000) ~ -2.5V (11111010) -2.6V (11111011), -2.7V (11111100), -2.8V (11111101) -2.9V (11111110), -3.0V (11111111) Default: 0V (00000000)

Table 15. VINT1/2_NGP Description

Data (Hex)	VINT1/2_NGP	Data (Hex)	VINT1/2_NGP	Data (Hex)	VINT1/2_NGP	Data (Hex)	VINT1/2_NGP	Data (Hex)	VINT1/2_NGP	Data (Hex)	VINT1/2_NGP	Data (Hex)	VINT1/2_NGP	Data (Hex)	VINT1/2_NGP
0x00	0.00V	0x20	-0.32V	0x40	-0.64V	0x60	-0.96V	0x80	-1.28V	0xA0	-1.60V	0xC0	-1.92V	0xE0	-2.24V
0x01	-0.01V	0x21	-0.33V	0x41	-0.65V	0x61	-0.97V	0x81	-1.29V	0xA1	-1.61V	0xC1	-1.93V	0xE1	-2.25V
0x02	-0.02V	0x22	-0.34V	0x42	-0.66V	0x62	-0.98V	0x82	-1.30V	0xA2	-1.62V	0xC2	-1.94V	0xE2	-2.26V
0x03	-0.03V	0x23	-0.35V	0x43	-0.67V	0x63	-0.99V	0x83	-1.31V	0xA3	-1.63V	0xC3	-1.95V	0xE3	-2.27V
0x04	-0.04V	0x24	-0.36V	0x44	-0.68V	0x64	-1.00V	0x84	-1.32V	0xA4	-1.64V	0xC4	-1.96V	0xE4	-2.28V
0x05	-0.05V	0x25	-0.37V	0x45	-0.69V	0x65	-1.01V	0x85	-1.33V	0xA5	-1.65V	0xC5	-1.97V	0xE5	-2.29V
0x06	-0.06V	0x26	-0.38V	0x46	-0.70V	0x66	-1.02V	0x86	-1.34V	0xA6	-1.66V	0xC6	-1.98V	0xE6	-2.30V
0x07	-0.07V	0x27	-0.39V	0x47	-0.71V	0x67	-1.03V	0x87	-1.35V	0xA7	-1.67V	0xC7	-1.99V	0xE7	-2.31V
0x08	-0.08V	0x28	-0.40V	0x48	-0.72V	0x68	-1.04V	0x88	-1.36V	0xA8	-1.68V	0xC8	-2.00V	0xE8	-2.32V
0x09	-0.09V	0x29	-0.41V	0x49	-0.73V	0x69	-1.05V	0x89	-1.37V	0xA9	-1.69V	0xC9	-2.01V	0xE9	-2.33V
0x0A	-0.10V	0x2A	-0.42V	0x4A	-0.74V	0x6A	-1.06V	0x8A	-1.38V	0xAA	-1.70V	0xCA	-2.02V	0xEA	-2.34V
0x0B	-0.11V	0x2B	-0.43V	0x4B	-0.75V	0x6B	-1.07V	0x8B	-1.39V	0xAB	-1.71V	0xCB	-2.03V	0xEB	-2.35V
0x0C	-0.12V	0x2C	-0.44V	0x4C	-0.76V	0x6C	-1.08V	0x8C	-1.40V	0xAC	-1.72V	0xCC	-2.04V	0xEC	-2.36V
0x0D	-0.13V	0x2D	-0.45V	0x4D	-0.77V	0x6D	-1.09V	0x8D	-1.41V	0xAD	-1.73V	0xCD	-2.05V	0xED	-2.37V
0x0E	-0.14V	0x2E	-0.46V	0x4E	-0.78V	0x6E	-1.10V	0x8E	-1.42V	0xAE	-1.74V	0xCE	-2.06V	0xEE	-2.38V
0x0F	-0.15V	0x2F	-0.47V	0x4F	-0.79V	0x6F	-1.11V	0x8F	-1.43V	0xAF	-1.75V	0xCF	-2.07V	0xEF	-2.39V
0x10	-0.16V	0x30	-0.48V	0x50	-0.80V	0x70	-1.12V	0x90	-1.44V	0xB0	-1.76V	0xD0	-2.08V	0xF0	-2.40V
0x11	-0.17V	0x31	-0.49V	0x51	-0.81V	0x71	-1.13V	0x91	-1.45V	0xB1	-1.77V	0xD1	-2.09V	0xF1	-2.41V
0x12	-0.18V	0x32	-0.50V	0x52	-0.82V	0x72	-1.14V	0x92	-1.46V	0xB2	-1.78V	0xD2	-2.10V	0xF2	-2.42V
0x13	-0.19V	0x33	-0.51V	0x53	-0.83V	0x73	-1.15V	0x93	-1.47V	0xB3	-1.79V	0xD3	-2.11V	0xF3	-2.43V
0x14	-0.20V	0x34	-0.52V	0x54	-0.84V	0x74	-1.16V	0x94	-1.48V	0xB4	-1.80V	0xD4	-2.12V	0xF4	-2.44V
0x15	-0.21V	0x35	-0.53V	0x55	-0.85V	0x75	-1.17V	0x95	-1.49V	0xB5	-1.81V	0xD5	-2.13V	0xF5	-2.45V
0x16	-0.22V	0x36	-0.54V	0x56	-0.86V	0x76	-1.18V	0x96	-1.50V	0xB6	-1.82V	0xD6	-2.14V	0xF6	-2.46V
0x17	-0.23V	0x37	-0.55V	0x57	-0.87V	0x77	-1.19V	0x97	-1.51V	0xB7	-1.83V	0xD7	-2.15V	0xF7	-2.47V
0x18	-0.24V	0x38	-0.56V	0x58	-0.88V	0x78	-1.20V	0x98	-1.52V	0xB8	-1.84V	0xD8	-2.16V	0xF8	-2.48V
0x19	-0.25V	0x39	-0.57V	0x59	-0.89V	0x79	-1.21V	0x99	-1.53V	0xB9	-1.85V	0xD9	-2.17V	0xF9	-2.49V
0x1A	-0.26V	0x3A	-0.58V	0x5A	-0.90V	0x7A	-1.22V	0x9A	-1.54V	0xBA	-1.86V	0xDA	-2.18V	0xFA	-2.50V
0x1B	-0.27V	0x3B	-0.59V	0x5B	-0.91V	0x7B	-1.23V	0x9B	-1.55V	0xBB	-1.87V	0xDB	-2.19V	0xFB	-2.60V
0x1C	-0.28V	0x3C	-0.60V	0x5C	-0.92V	0x7C	-1.24V	0x9C	-1.56V	0xBC	-1.88V	0xDC	-2.20V	0xFC	-2.70V
0x1D	-0.29V	0x3D	-0.61V	0x5D	-0.93V	0x7D	-1.25V	0x9D	-1.57V	0xBD	-1.89V	0xDD	-2.21V	0xFD	-2.80V
0x1E	-0.30V	0x3E	-0.62V	0x5E	-0.94V	0x7E	-1.26V	0x9E	-1.58V	0xBE	-1.90V	0xDE	-2.22V	0xFE	-2.90V
0x1F	-0.31V	0x3F	-0.63V	0x5F	-0.95V	0x7F	-1.27V	0x9F	-1.59V	0xBF	-1.91V	0xDF	-2.23V	0xFF	-3.00V

REGISTER MAPS (continued)

REG0x2A: Current Limit Register 1 [Reset = 0xAA]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	VCORE_CL[1:0]	10	R/W	VCORE Current Limit Setting 00 = 2100mA 01 = 2400mA 10 = 2700mA (default) 11 = 3000mA
D[5:4]	VIO_CL[1:0]	10	R/W	VIO Current Limit Setting 00 = 1100mA 01 = 1400mA 10 = 1700mA (default) 11 = 2000mA
D[3:2]	VDDI_CL[1:0]	10	R/W	VDDI Current Limit Setting 00 = 1100mA 01 = 1400mA 10 = 1700mA (default) 11 = 2000mA
D[1:0]	PVGL_CL[1:0]	10	R/W	PVGL Current Limit Setting 00 = 2100mA 01 = 2400mA 10 = 2700mA (default) 11 = 3000mA

REG0x2B: Current Limit Register 2 [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000000	R/W	Reserved
D[1:0]	PAVDD_CL[1:0]	10	R/W	PAVDD Current Limit Setting 00 = 3000mA 01 = 3500mA 10 = 4000mA (default) 11 = 4500mA

REG0x2C: Spread Spectrum Control Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VCORE_SSC	0	R/W	VCORE Spread Spectrum Enable: 0 = Disable (default) 1 = Enable
D[6]	VIO_SSC	0	R/W	VIO Spread Spectrum Enable: 0 = Disable (default) 1 = Enable
D[5]	VDDI_SSC	0	R/W	VDDI Spread Spectrum Enable: 0 = Disable (default) 1 = Enable
D[4]	PAVDD_SSC	0	R/W	PAVDD Spread Spectrum Enable: 0 = Disable (default) 1 = Enable
D[3]	PVGL_SSC	0	R/W	PVGL Spread Spectrum Enable: 0 = Disable (default) 1 = Enable
D[2]	Reserved	0	R/W	Reserved
D[1:0]	SS_CLK[1:0]	00	R/W	Spread Spectrum Level Setting: 00 = 0 (default) 01 = 3% 10 = 6% 11 = 10%

REGISTER MAPS (continued)

REG0x2D: UVP_EN Register 1 [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VCORE_UVP_EN	1	R/W	VCORE Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[6]	VIO_UVP_EN	1	R/W	VIO Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[5]	VDDI_UVP_EN	1	R/W	VDDI Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[4]	PAVDD_UVP_EN	1	R/W	PAVDD Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[3]	AVDD_UVP_EN	1	R/W	AVDD Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[2]	PVGL_UVP_EN	1	R/W	PVGL Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[1]	VGH1_UVP_EN	1	R/W	VGH1 Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[0]	VGH2_UVP_EN	1	R/W	VGH2 Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)

REG0x2E: UVP_EN Register 2 [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VREFH_UVP_EN	1	R/W	VREFH Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[6]	VREFL_UVP_EN	1	R/W	VREFL Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[5]	VGL1_UVP_EN	1	R/W	VGL1 Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[4]	VGL2_UVP_EN	1	R/W	VGL2 Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[3]	VINT3_UVP_EN	1	R/W	VINT3 Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[2]	Reserved	1	R/W	Reserved
D[1]	VINT1_UVP_EN	1	R/W	VINT1 Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)
D[0]	VINT2_UVP_EN	1	R/W	VINT2 Under-Voltage Protection Enable: 0 = Disable 1 = Enable (default)

REGISTER MAPS (continued)

REG0x2F: UVP_EN Register 3 [Reset = 0xD5]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	AVDD_CD_EN	1	R/W	AVDD Current Detection Enable: 0 = Disable 1 = Enable (default)
D[6]	PAVDD_OVP_EN	1	R/W	PAVDD Over Voltage Detection Enable: 0 = Disable 1 = Enable (default)
D[5]	EL_SD_EN	0	R/W	EL Shutdown Detection Enable: 0 = Disable (default) 1 = Enable
D[4:0]	Reserved	10101	R/W	Reserved

REG0x30: Current Limit Register [Reset = 0xE5]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VINT1_CL_EN	1	R/W	VINT1 Current Limit Detection Enable: 0 = Disable 1 = Enable (default)
D[6]	VINT2_CL_EN	1	R/W	VINT2 Current Limit Detection Enable: 0 = Disable 1 = Enable (default)
D[5]	VINT3_CL_EN	1	R/W	VINT3 Current Limit Enable: 0 = Disable 1 = Enable (default)
D[4:3]	UVP_ OPERATION[1:0]	00	R/W	UVP Operation Mode Setting: 00 = All channels shutdown (default) 01 = The channels controlled by ENx shutdown 10 & 11 = The UV channel shutdown only
D[2:0]	Reserved	101	R/W	Reserved

REGISTER MAPS (continued)

REG0x31: FAULT_FLAG Register 1 [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VCORE_UVP_F	0	R	VCORE Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[6]	VIO_UVP_F	0	R	VIO Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[5]	VDDI_UVP_F	0	R	VDDI Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[4]	PAVDD_UVP_F	0	R	PAVDD Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[3]	AVDD_UVP_F	0	R	AVDD Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[2]	PVGL_UVP_F	0	R	PVGL Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[1]	VGH1_UVP_F	0	R	VGH1 Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[0]	VGH2_UVP_F	0	R	VGH2 Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag

REG0x32: FAULT_FLAG Register 2 [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VREFH_UVP_F	0	R	VREFH Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[6]	VREFL_UVP_F	0	R	VREFL Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[5]	VGL1_UVP_F	0	R	VGL1 Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[4]	VGL2_UVP_F	0	R	VGL2 Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[3]	VINT3_UVP_F	0	R	VINT3 Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[2]	Reserved	0	R	Reserved
D[1]	VINT1_UVP_F	0	R	VINT1 Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[0]	VINT2_UVP_F	0	R	VINT2 Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag

REGISTER MAPS (continued)

REG0x33: FAULT_FLAG Register 4 [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	OTP_F	0	R	Over-Temperature Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[6]	UVLO_F	0	R	UVLO Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[5]	AVDD_CLD_F	0	R	AVDD Current Limit Detection Flag: 0 = Normal (default) 1 = Fault Flag
D[4]	PAVDD_OVP_F	0	R	PAVDD Over-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[3]	EL_SD_F	0	R	EL Shutdown Detection Flag: 0 = Normal (default) 1 = Fault Flag
D[2]	Reserved	0	R	Reserved
D[1]	PAVDD_PRE_UVP_F	0	R	PAVDD Pre-charge Under-Voltage Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[0]	PVGL_CL_F	0	R	PVGL Current Limit Protection Flag: 0 = Normal (default) 1 = Fault Flag

REG0x34: FAULT_FLAG Register 5 [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VIO_CL_F	0	R	VIO Current Limit Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[6]	VDDI_CL_F	0	R	VDDI Current Limit Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[5]	VCORE_CL_F	0	R	VCORE Current Limit Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[4]	PAVDD_CL_F	0	R	PAVDD Current Limit Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[3]	VINT1_CL_F	0	R	VINT1 Current Limit Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[2]	VINT2_CL_F	0	R	VINT2 Current Limit Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[1]	VINT3_CL_F	0	R	VINT3 Current Limit Protection Flag: 0 = Normal (default) 1 = Fault Flag
D[0]	Reserved	0	R	Reserved

REGISTER MAPS (continued)

REG0x35: TIME_CONF Register [Reset = 0x3C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5]	ELVDD_HOLD _LVL	1	R/W	ELVDDFB - ELVDD_REF Voltage Clamp Level: 0 = ±0.5V 1 = ±1V (default)
D[4]	ELVDD_HOLD_EN	1	R/W	VREFH/L Real-Time Tracking Enable Setting (Tracking ELVDDFB): 0 = Disable 1 = Enable (default) When this bit is enabled, the real VREFH output voltage VREFH = ELVDDFB - ELVDD_REF[5:0] + VREFH[7:0], and the real VREFL output voltage VREFL = ELVDDFB - ELVDD_REF[5:0] + VREFL[7:0] Note: ELVDDFB - ELVDD_REF[5:0] is clamped to ±1V/±0.5V (refer to ELVDD_HOLD_LVL).
D[3:2]	Reserved	11	R/W	Reserved
D[1]	SST_RANGE	0	R/W	Extend Soft-Start Time of all OP Amp 0 = Fast (default) VGH1/2 1.4ms; VINT3 1ms; VREFH/L 0.5ms; VGL1/2 2.5ms. 1 = Slow VGH1/2 5.6ms; VINT3 4.4ms; VREFH/L 3.9ms; VGL1/2 5ms.
D[0]	AVDD_DLY_HALF	0	R/W	Delay Time of AVDD is Divided by 2. 0 = Disable (default) 1 = Enable

REG0x36: ELVDD_REF Register [Reset = 0x28]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5:0]	ELVDD_REF[5:0]	101000	R/W	ELVDD_REF Voltage Setting: ELVDD_REF = ELVDD_REF[5:0] × 50mV + 2.6V Range: 2.6V (000000) ~ 5.5V (111010) Default: 4.6V (101000)

Table 16. ELVDD_REF Description

Data (Hex)	ELVDD_REF	Data (Hex)	ELVDD_REF	Data (Hex)	ELVDD_REF	Data (Hex)	ELVDD_REF
0x00	2.60V	0x10	3.40V	0x20	4.20V	0x30	5.00V
0x01	2.65V	0x11	3.45V	0x21	4.25V	0x31	5.05V
0x02	2.70V	0x12	3.50V	0x22	4.30V	0x32	5.10V
0x03	2.75V	0x13	3.55V	0x23	4.35V	0x33	5.15V
0x04	2.80V	0x14	3.60V	0x24	4.40V	0x34	5.20V
0x05	2.85V	0x15	3.65V	0x25	4.45V	0x35	5.25V
0x06	2.90V	0x16	3.70V	0x26	4.50V	0x36	5.30V
0x07	2.95V	0x17	3.75V	0x27	4.55V	0x37	5.35V
0x08	3.00V	0x18	3.80V	0x28	4.60V	0x38	5.40V
0x09	3.05V	0x19	3.85V	0x29	4.65V	0x39	5.45V
0x0A	3.10V	0x1A	3.90V	0x2A	4.70V	0x3A	5.50V
0x0B	3.15V	0x1B	3.95V	0x2B	4.75V	0x3B	Null
0x0C	3.20V	0x1C	4.00V	0x2C	4.80V	0x3C	Null
0x0D	3.25V	0x1D	4.05V	0x2D	4.85V	0x3D	Null
0x0E	3.30V	0x1E	4.10V	0x2E	4.90V	0x3E	Null
0x0F	3.35V	0x1F	4.15V	0x2F	4.95V	0x3F	Null

REGISTER MAPS (continued)

REG0x37: DEVICE ID Register [Reset = 0x38]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	DEVICE_ID[7:0]	00111000	R	Device ID

REG0x38: Reserved Register [Reset = 0x11]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	00010001	R/W	Reserved

REG0x39 ~ REG0x3C: Reserved Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	00000000	R/W	Reserved

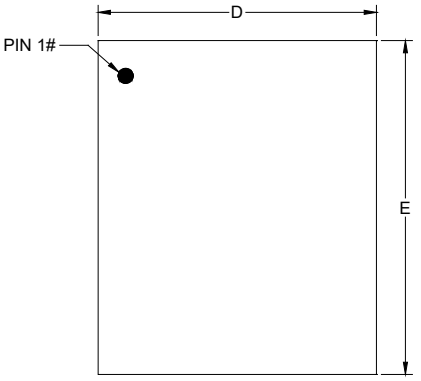
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

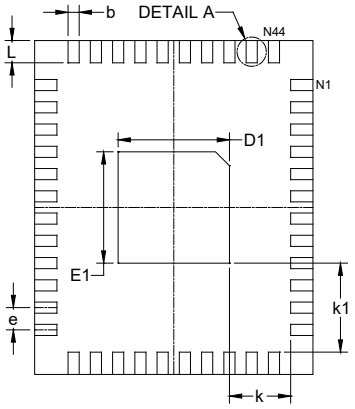
Changes from Original to REV.A (APRIL 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

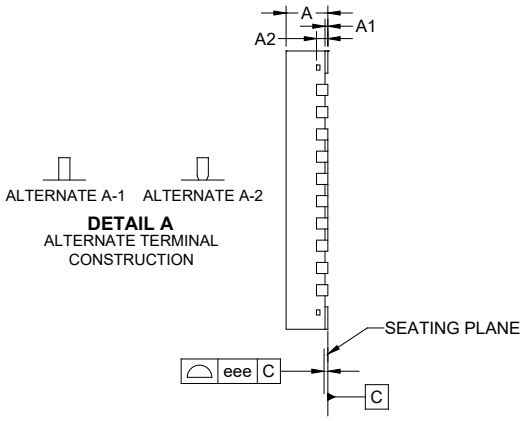
TQFN-5×6-44L



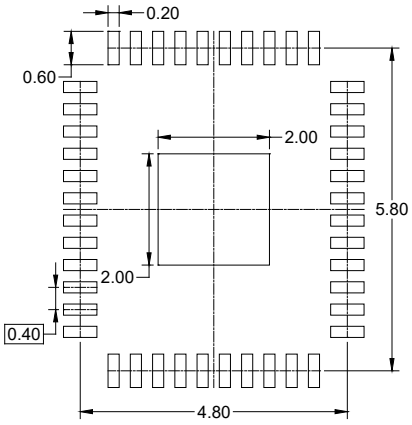
TOP VIEW



BOTTOM VIEW



SIDE VIEW



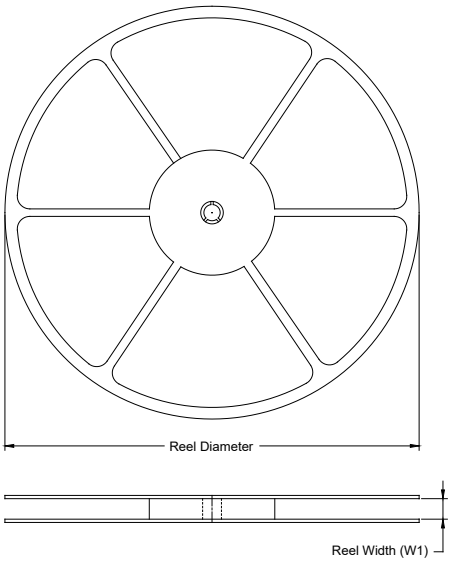
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.150	-	0.250
D	4.900	-	5.100
D1	1.900	-	2.100
E	5.900	-	6.100
E1	1.900	-	2.100
e	0.400 BSC		
k	1.100 REF		
k1	1.600 REF		
L	0.300	-	0.500
eee	0.080		

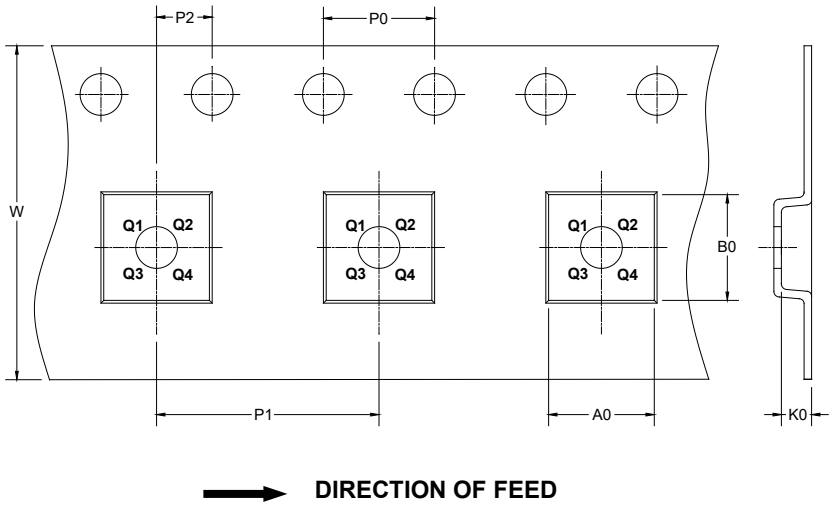
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



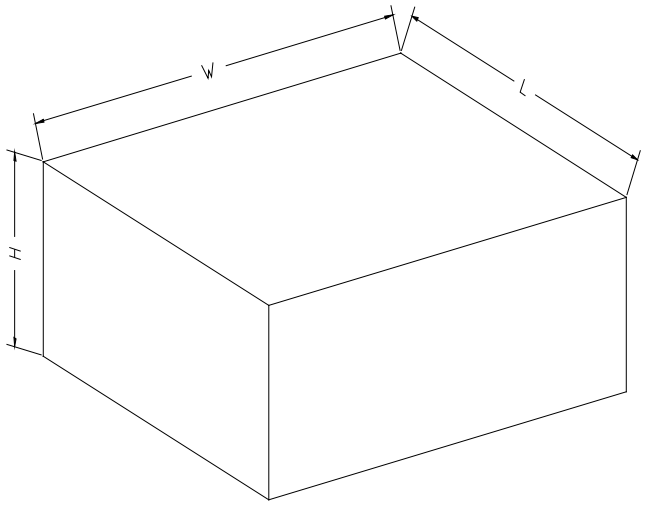
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-5×6-44L	13"	16.4	5.30	6.30	1.10	4.0	12.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002