SGM38120
Dedicated Camera PMIC

GENERAL DESCRIPTION

The SGM38120 is a 7-channel LDO PMIC, which has two low-dropout NMOS LDO channels, five high-PSRR and low-noise PMOS LDO channels.

The SGM38120 has a high priority RESET_B pin for hardware reset, an INT pin for interrupt indication and I^2C communication peripheral.

The SGM38120 operates over an operating temperature range of -40℃ to +85℃. It is available in a Green WLCSP-1.83×1.51-20B package.

APPLICATIONS

Portable Equipment
Smart Wearable Device
Health Monitoring Equipment

TYPICAL APPLICATION

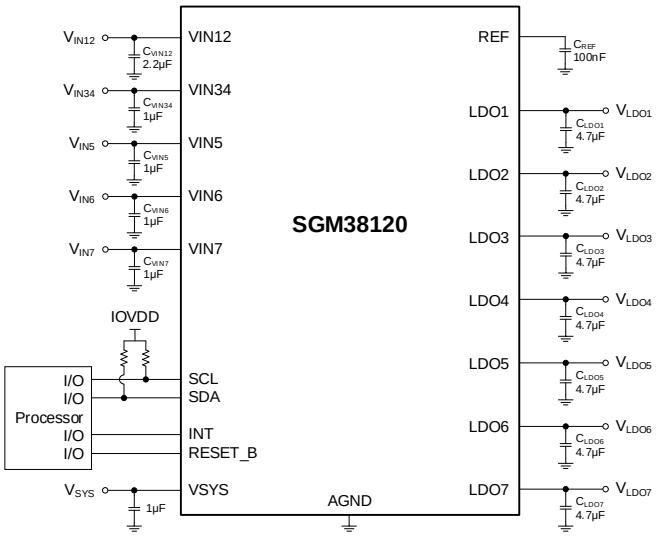


Figure 1. Typical Application Circuit

FEATURES

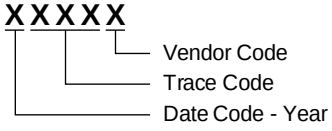
- **LDO1 and LDO2:**
  - **1.4A Output Current Capability**
  - **Programmable Output Voltage: 0.528V to 1.504V in 8mV Steps**
  - **0.7V to 2.0V Input Voltage Range**
  - **1.3% Accuracy**
- **LDO3, LDO4 and LDO6:**
  - **500mA Output Current Capability**
  - **Programmable Output Voltage: 1.504V to 3.544V in 8mV Steps**
  - **1.8V to 5.5V Input Voltage Range**
  - **PSRR to VSYS: 105dB at 1kHz**
  - **PSRR to VSYS: 70dB at 1MHz**
  - **15μV_{RMS} (TYP) Noise for LDO3 and LDO4**
  - **17μV_{RMS} (TYP) Noise for LDO6**
- **LDO5 and LDO7:**
  - **750mA Output Current Capability**
  - **Programmable Output Voltage: 1.2V and 1.504V to 3.544V in 8mV Steps**
  - **1.8V to 5.5V Input Voltage Range**
  - **PSRR to VSYS: 105dB at 1kHz**
  - **PSRR to VSYS: 70dB at 1MHz**
  - **17μV_{RMS} (TYP) Noise**
- **Over-Temperature Protection (OTP)**
- **Output Over-Current Protection (OCP)**
- **Under-Voltage Protection (UVP)**
- **Under-Voltage Lockout Protection (UVLO)**
- **I^2C Communication Peripheral (Default Slave Address: 0x35 Configured via I^2C)**
- **Fault Interrupt**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in a Green WLCSP-1.83×1.51-20B Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM38120	WLCSP-1.83×1.51-20B	-40℃ to +85℃	SGM38120YG/TR	XXXXX 38120	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{SYS} Range ..... -0.3V to 6.5V
V_{IN12} Range ..... -0.3V to 6.5V
$V_{IN34, 5-7}$ Range ..... -0.3V to 6.5V
Interrupt and RESET_B Pin ..... -0.3V to 6.5V
Package Thermal Resistance
WLCSP-1.83×1.51-20B, θ_{JA} ..... 65.2℃/W
WLCSP-1.83×1.51-20B, θ_{JB} ..... 22℃/W
WLCSP-1.83×1.51-20B, θ_{JC} ..... 26.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

V_{SYS} Range ..... 2.5V to 5.5V
V_{IN12} Input Voltage Range ..... 0.7V to 2.0V
V_{IN34} Input Voltage Range ..... 1.8V to 5.5V
$V_{IN5/6/7}$ Input Voltage Range ..... 1.8V to 5.5V
Operating Junction Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

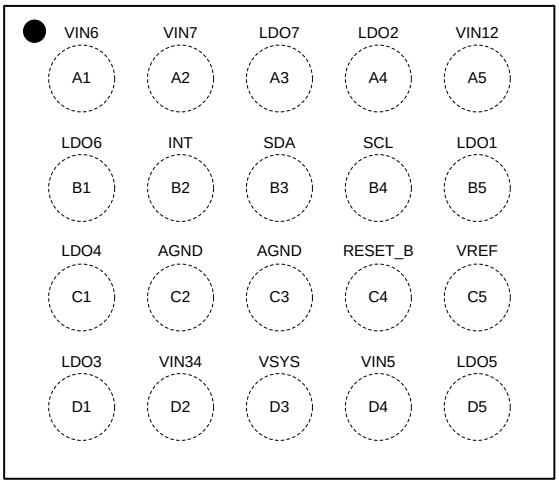
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM38120 (TOP VIEW)



WLCSP-1.83×1.51-20B

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
A5	VIN12	PI	VIN for LDO1 and LDO2.
D2	VIN34	PI	VIN for LDO3 and LDO4.
D4	VIN5	PI	VIN for LDO5.
A1	VIN6	PI	VIN for LDO6.
A2	VIN7	PI	VIN for LDO7.
B5	LDO1	PO	LDO1 Regulated Output.
A4	LDO2	PO	LDO2 Regulated Output.
D1	LDO3	PO	LDO3 Regulated Output.
C1	LDO4	PO	LDO4 Regulated Output.
D5	LDO5	PO	LDO5 Regulated Output.
B1	LDO6	PO	LDO6 Regulated Output.
A3	LDO7	PO	LDO7 Regulated Output.
C5	VREF	AI, AO	Bypass Capacitor for Dedicated Master Bandgap Regulator. C_{REF} = 100nF. Do not load the VREF pin.
B4	SCL	DI	I^2C Communication Bus Clock Signal.
B3	SDA	DI, DO	I^2C Communication Bus Data Signal.
B2	INT	DO	Interface Pin for Interrupt.
C4	RESET_B	DI	Brings Part out of Reset; Enables I^2C communication.
D3	VSYS	PI	Power Supply with Range from 2.5V to 5.5V.
C2, C3	AGND	GNDC	Ground for All Nonspecialized Circuits.

NOTE:
1. AI = analog input, AO = analog output, DI = digital input (CMOS), DO = digital output (CMOS), PI = power input, PO = power output, GNDC = common ground.

FUNCTIONAL BLOCK DIAGRAM

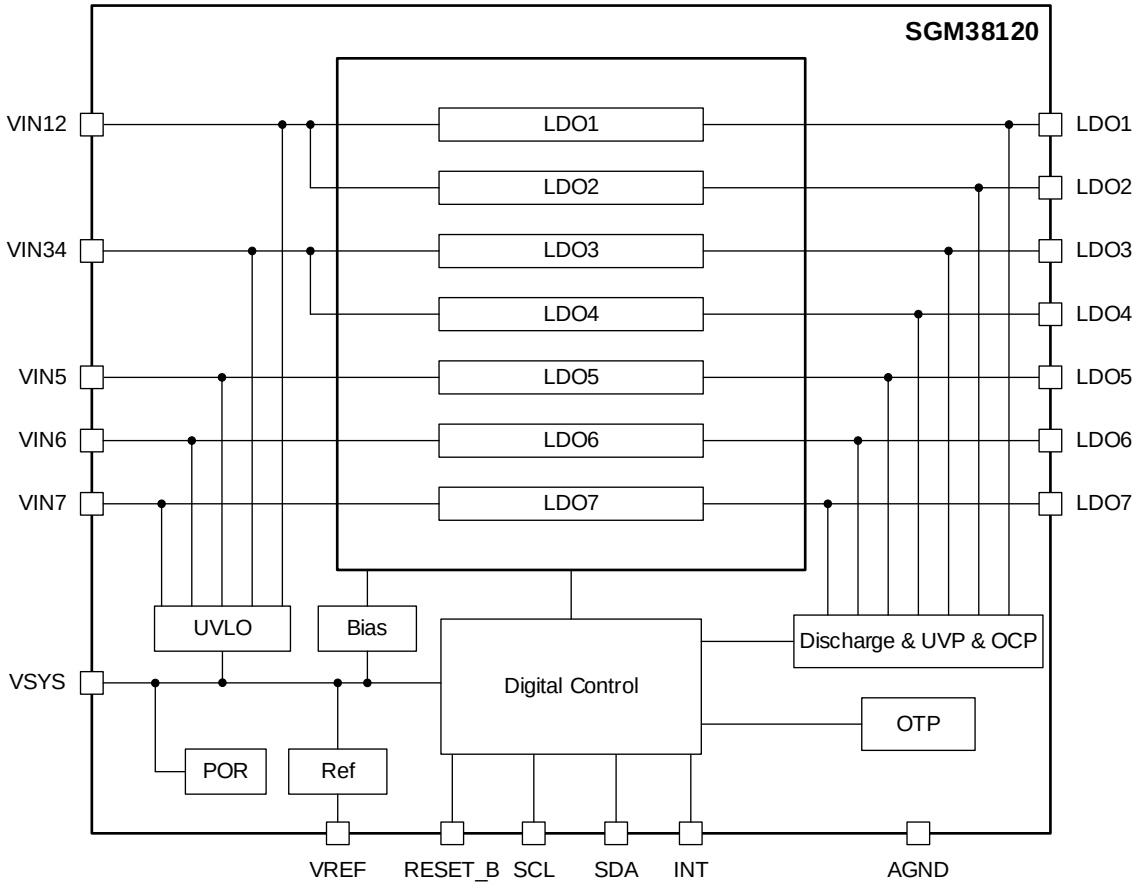


Figure 2. Functional Block Diagram

ELECTRICAL CHARACTERISTICS

(Minimum and Maximum values are measured at T_J = -40℃ to +85℃, V_{SYS} = 2.5V to 5.5V or ($V_{LDO1/2}$ + 1.6V) or (V_{LDO3-7} + 0.5V) (whichever is greater); at V_{IN12} = (0.7V to 2.0V) or ($V_{LDO1/2}$ + 0.2V) (whichever is greater); at $V_{IN34, 5-7}$ ≥ 1.8V or (V_{LDO3-7} + 0.2V) (whichever is greater), and $V_{IN34, 5-7}$ ≤ 5.5V or V_{SYS} (whichever is lower). Typical values are at T_J = +25℃, V_{SYS} = 3.8V, V_{IN12} = 1.5V, $V_{IN34, 5-7}$ = 3.8V, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, C_{IN12} = 2.2μF, $C_{IN34, 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF and C_{LDO1-7} = 4.7μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Input Voltage Range	V_{RNG_SYS}		2.5	3.8	5.5	V
VIN12 Input Voltage Range	V_{RNG_IN12}		0.7	1.5	2.0	V
$V_{IN34, 5-7}$ Input Voltage Range	$V_{RNG\_IN34, 5-7}$		1.8	3.8	5.5	V
Under-Voltage Lockout Threshold	$V_{UVLO\_RS\_SYS}$	Rising V_{SYS}	2.3	2.36	2.42	V
	$V_{UVLO\_FL\_SYS}$	Falling V_{SYS}	2.2	2.25	2.31	
	$V_{UVLO\_RS\_IN12}$	Rising V_{IN12}	0.47	0.54	0.61	
	$V_{UVLO\_FL\_IN12}$	Falling V_{IN12}	0.39	0.45	0.52	
	$V_{UVLO\_RS\_IN34, 5-7}$	Rising $V_{IN34, 5-7}$	1.57	1.65	1.74	
	$V_{UVLO\_FL\_IN34, 5-7}$	Falling $V_{IN34, 5-7}$	1.5	1.55	1.6	
Shutdown Supply Current	I_{SD_VSYS}	RESET_B = low, current on VSYS		0.25	2	μA
	I_{SD_VIN12}	RESET_B = low, current on VIN12		0.01	1	
	$I_{SD\_VIN34, 5-7}$	RESET_B = low, current either on VIN34, VIN5, VIN6 or VIN7		0.01	1	
Sleep Mode Supply Current (1)	I_{SLP}	RESET_B = high, register 0x03h = 00h		1.5	4.2	μA
Standby Mode Supply Current (1)	I_{STB}	RESET_B = high, register 0x03h = 80h		43	63	μA
Quiescent Current (1)	$I_{Q\_LDO1/2}$	No load, LDO1 or LDO2 on, others off		77	115	μA
	$I_{Q\_LDO3/4/6}$	No load, LDO3, LDO4 or LDO6 on, others off		77	115	μA
	$I_{Q\_LDO5/7}$	No load, LDO5 or LDO7 on, others off		77	115	μA
	I_{Q_TOT}	No load, RESET_B = high, all LDOs (2) on		270	370	μA
Thermal Shutdown Threshold	T_{SHDN}	I_{OUT} = 1mA		143		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}	I_{OUT} = 1mA		15		℃
LDO1/2 Output Voltage						
LDO1/2 Output Voltage Range	$V_{RNG\_LDO1/2}$		0.528		1.504	V
LDO1/2 Default Output Voltage	$V_{Default\_LDO1/2}$			1.2		V
LDO1/2 Output Voltage Step Size	V_{STEP}			8		mV
LDO1/2 Output Voltage Accuracy	$V_{ACC\_LDO1/2}$	$I_{LDO1/2}$ = 10mA, $V_{LDO1/2}$ = 1.2V, T_J = +25℃	-0.8		0.8	%
		$I_{LDO1/2}$ = 10mA, $V_{LDO1/2}$ = 0.528V to 1.504V, T_J = -40℃ to +125℃	-1.3		1.3	%
LDO1/2 Dropout Voltage	$V_{DROPOUT\_LDO1/2}$	$I_{LDO1/2}$ = 1200mA, $V_{LDO1/2}$ = 1.2V		90	125	mV
LDO1/2 Current Limit						
Low Current Limit	$I_{LIML\_LDO1/2}$		1150			mA
High Current Limit	$I_{LIMH\_LDO1/2}$		1400			mA
LDO1/2 Output Protection						
LDO1/2 Falling UVP Threshold	$UVP_{FL\_LDO1/2}$	V_{SYS} = 3.8V, $V_{LDO1/2}$ = 1.2V		90		% of $V_{LDO1/2}$
LDO1/2 Rising UVP Threshold	$UVP_{RS\_LDO1/2}$	V_{SYS} = 3.8V, $V_{LDO1/2}$ = 1.2V		95		% of $V_{LDO1/2}$
Output Discharge Resistance	$R_{DCHG\_LDO1/2}$			270		Ω

NOTES:

1. Sleep mode supply current, standby mode supply current and quiescent current is the total current on VSYS, VIN12, VIN34, VIN5, VIN6 and VIN7.
2. All LDOs correspond to LDO1, LDO2, LDO3, LDO4, LDO5, LDO6 and LDO7.

ELECTRICAL CHARACTERISTICS (continued)

(Minimum and Maximum values are measured at T_J = -40℃ to +85℃, V_{SYS} = 2.5V to 5.5V or ($V_{LDO1/2}$ + 1.6V) or (V_{LDO3-7} + 0.5V) (whichever is greater); at V_{IN12} = (0.7V to 2.0V) or ($V_{LDO1/2}$ + 0.2V) (whichever is greater); at $V_{IN34, 5-7}$ ≥ 1.8V or (V_{LDO3-7} + 0.2V) (whichever is greater), and $V_{IN34, 5-7}$ ≤ 5.5V or V_{SYS} (whichever is lower). Typical values are at T_J = +25℃, V_{SYS} = 3.8V, V_{IN12} = 1.5V, $V_{IN34, 5-7}$ = 3.8V, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, C_{IN12} = 2.2μF, $C_{IN34, 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF and C_{LDO1-7} = 4.7μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO1/2 PSRR and Noise							
Power Supply Rejection Ratio on VIN12	$PSRR_{VIN12\_LDO1/2}$	V_{IN12} = 1.5V + 0.2V_{P-P}, V_{SYS} = 3.8V, $V_{LDO1/2}$ = 1.2V, $I_{LDO1/2}$ = 150mA, no C_{SYS} and C_{IN12}	f_{REQ} = 1kHz		80		dB
			f_{REQ} = 10kHz		65		
			f_{REQ} = 100kHz		45		
			f_{REQ} = 1MHz		38		
Power Supply Rejection Ratio on VSYS	$PSRR_{VSYS\_LDO1/2}$	V_{SYS} = 3.8V + 0.2V_{P-P}, V_{IN12} = 1.5V, $V_{LDO1/2}$ = 1.2V, $I_{LDO1/2}$ = 150mA, no C_{SYS} and C_{IN12}	f_{REQ} = 1kHz		75		dB
			f_{REQ} = 10kHz		70		
			f_{REQ} = 100kHz		50		
			f_{REQ} = 1MHz		38		
LDO1/2 Output Noise	$V_{NOISE\_LDO1/2}$	f_{REQ} = 10Hz to 100kHz, $I_{LDO1/2}$ = 150mA			30		μV_{RMS}
LDO1/2 Regulation and Transient Performance							
LDO Load Regulation	$\Delta V_{LDR\_LDO1/2}$	$I_{LDO1/2}$ = 1mA to 800mA, $V_{LDO1/2}$ = 1.2V			3		mV
LDO Line Regulation	$\Delta V_{LNR\_VIN\_LDO1/2}$	V_{IN12} = 1.5V to 2.0V, $I_{LDO1/2}$ = 10mA, $V_{LDO1/2}$ = 1.2V			0.1		mV
	$\Delta V_{LNR\_VSYS\_LDO1/2}$	V_{SYS} = 2.8V to 5.5V, $I_{LDO1/2}$ = 10mA, $V_{LDO1/2}$ = 1.2V			0.1		
LDO1/2 Soft-Start							
Turn-On Delay Time	$t_{DLY\_LDO1/2}$	From assertion of LDO output to soft-start ramp			200		μs
Soft-Start Time	$t_{SS\_LDO1/2}$	$V_{LDO1/2}$ from 5% to 95%, $V_{LDO1/2}$ = 1.2V, $I_{LDO1/2}$ = 10mA			300		μs
Startup Fault Disable Timer	$t_{SUFD\_LDO1/2}$	Disable fault detection timer			1.5		ms
LDO1/2 Short-Circuit							
Hiccup Timer	t_{HICCUP}	Protection shutdown to recovery startup timer			22		ms
LDO3/4 Output Voltage							
LDO3/4 Output Voltage Range	$V_{RNG\_LDO3/4}$			1.504		3.544	V
LDO3/4 Default Output Voltage	$V_{Default\_LDO3/4}$				2.8		V
LDO3/4 Output Voltage Step Size	V_{STEP}				8		mV
LDO3/4 Output Voltage Accuracy	$V_{ACC\_LDO3/4}$	$I_{LDO3/4}$ = 10mA, $V_{LDO3/4}$ = 2.2V and 2.8V, T_J = +25℃		-1.5		1.5	%
		$I_{LDO3/4}$ = 10mA, $V_{LDO3/4}$ = 2.000V to 3.544V, T_J = -40℃ to +125℃		-1.8		1.8	
LDO3/4 Dropout Voltage	$V_{DROPOUT\_LDO3/4}$	$I_{LDO3/4}$ = 300mA, $V_{LDO3/4}$ = 2.8V			110	150	mV
LDO3/4 Current Limit							
Low LDO3/4 Current Limit	$I_{LIML\_LDO3/4}$	V_{IN34} ≥ $V_{LDO3/4}$ + 0.5V, V_{SYS} = 3.8V		400			mA
High LDO3/4 Current Limit	$I_{LIMH\_LDO3/4}$	V_{IN34} ≥ $V_{LDO3/4}$ + 0.5V, V_{SYS} = 3.8V		500			mA
LDO3/4 Output Protection							
LDO3/4 Falling UVP Threshold	$UVP_{FL\_LDO3/4}$	V_{SYS} = 3.8V, $V_{LDO3/4}$ = 2.8V			80		% of $V_{LDO3/4}$
LDO3/4 Rising UVP Threshold	$UVP_{RS\_LDO3/4}$	V_{SYS} = 3.8V, $V_{LDO3/4}$ = 2.8V			90		% of $V_{LDO3/4}$
Output Discharge Resistance	$R_{DCHG\_LDO3/4}$				250		Ω

ELECTRICAL CHARACTERISTICS (continued)

(Minimum and Maximum values are measured at T_J = -40℃ to +85℃, V_{SYS} = 2.5V to 5.5V or ($V_{LDO1/2}$ + 1.6V) or (V_{LDO3-7} + 0.5V) (whichever is greater); at V_{IN12} = (0.7V to 2.0V) or ($V_{LDO1/2}$ + 0.2V) (whichever is greater); at $V_{IN34, 5-7}$ ≥ 1.8V or (V_{LDO3-7} + 0.2V) (whichever is greater), and $V_{IN34, 5-7}$ ≤ 5.5V or V_{SYS} (whichever is lower). Typical values are at T_J = +25℃, V_{SYS} = 3.8V, V_{IN12} = 1.5V, $V_{IN34, 5-7}$ = 3.8V, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, C_{IN12} = 2.2μF, $C_{IN34, 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF and C_{LDO1-7} = 4.7μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO3/4 PSRR and Noise							
Power Supply Rejection Ratio on VIN34	$PSRR_{VIN34\_LDO3/4}$	V_{IN34} = 3.8V + 0.2V_{P-P}, V_{SYS} = 4.0V, $V_{LDO3/4}$ = 2.8V, $I_{LDO3/4}$ = 100mA, no C_{SYS} and C_{IN34}	f_{REQ} = 1kHz		100		dB
			f_{REQ} = 10kHz		85		
			f_{REQ} = 100kHz		65		
			f_{REQ} = 1MHz		55		
Power Supply Rejection Ratio on VSYS	$PSRR_{VSYS\_LDO3/4}$	V_{SYS} = 4.0V + 0.2V_{P-P}, V_{IN34} = 3.8V, $V_{LDO3/4}$ = 2.8V, $I_{LDO3/4}$ = 100mA, no C_{SYS} and C_{IN34}	f_{REQ} = 1kHz		105		dB
			f_{REQ} = 10kHz		90		
			f_{REQ} = 100kHz		75		
			f_{REQ} = 1MHz		70		
LDO3/4 Output Noise	$V_{NOISE\_LDO3/4}$	f_{REQ} = 10Hz to 100kHz, $I_{LDO3/4}$ = 100mA			15		μV_{RMS}
LDO3/4 Regulation and Transient Performance							
LDO Load Regulation	$\Delta V_{LDR\_LDO3/4}$	$I_{LDO3/4}$ = 1mA to 200mA, $V_{LDO3/4}$ = 2.8V			3		mV
LDO Line Regulation	$\Delta V_{LNR\_VIN\_LDO3/4}$	V_{IN34} = 3.0V to 5.5V, V_{SYS} = 5.5V, $I_{LDO3/4}$ = 10mA, $V_{LDO3/4}$ = 2.8V			0.1		mV
	$\Delta V_{LNR\_VSYS\_LDO3/4}$	V_{SYS} = 3.3V to 5.5V, V_{IN34} = 3.0V, $I_{LDO3/4}$ = 10mA, $V_{LDO3/4}$ = 2.8V			0.1		
LDO3/4 Soft-Start							
Turn-On Delay Time	$t_{DLY\_LDO3/4}$	From assertion of LDO output to soft start ramp			350		μs
Soft-Start Time	$t_{SS\_LDO3/4}$	$V_{LDO3/4}$ from 5% to 95%, $V_{LDO3/4}$ = 2.8V, $I_{LDO3/4}$ = 10mA			400		μs
Startup Fault Disable Timer	$t_{SUFD\_LDO3/4}$	Disable fault detection timer			1.5		ms
LDO3/4 Short-Circuit							
Hiccup Timer	t_{HICCUP}	Protection shutdown to recovery startup timer			22		ms
LDO6 Output Voltage							
LDO6 Output Voltage Range	V_{RNG_LDO6}			1.504		3.544	V
LDO6 Default Output Voltage	$V_{Default\_LDO6}$				2.8		V
LDO6 Output Voltage Step Size	V_{STEP}				8		mV
LDO6 Output Voltage Accuracy	V_{ACC_LDO6}	I_{LDO6} = 10mA, V_{LDO6} = 2.2V and 2.8V, T_J = +25℃		-0.9		0.9	%
		I_{LDO6} = 10mA, V_{LDO6} = 1.504V to 3.544V, T_J = -40℃ to +125℃		-1.3		1.3	
LDO6 Dropout Voltage	$V_{DROPOUT\_LDO6}$	I_{LDO6} = 300mA, V_{LDO6} = 2.8V			110	150	mV
LDO6 Current Limit							
Low LDO6 Current Limit	I_{LIML_LDO6}	V_{IN6} ≥ V_{LDO6} + 0.5V, V_{SYS} = 3.8V		400			mA
High LDO6 Current Limit	I_{LIMH_LDO6}	V_{IN6} ≥ V_{LDO6} + 0.5V, V_{SYS} = 3.8V		500			mA
LDO6 Output Protection							
LDO6 Falling UVP Threshold	UVP_{FL_LDO6}	V_{SYS} = 3.8V, V_{LDO6} = 2.8V			80		% of V_{LDO6}
LDO6 Rising UVP Threshold	UVP_{RS_LDO6}	V_{SYS} = 3.8V, V_{LDO6} = 2.8V			90		% of V_{LDO6}
Output Discharge Resistance	R_{DCHG_LDO6}				260		Ω

ELECTRICAL CHARACTERISTICS (continued)

(Minimum and Maximum values are measured at T_J = -40℃ to +85℃, V_{SYS} = 2.5V to 5.5V or ($V_{LDO1/2}$ + 1.6V) or (V_{LDO3-7} + 0.5V) (whichever is greater); at V_{IN12} = (0.7V to 2.0V) or ($V_{LDO1/2}$ + 0.2V) (whichever is greater); at $V_{IN34, 5-7}$ ≥ 1.8V or (V_{LDO3-7} + 0.2V) (whichever is greater), and $V_{IN34, 5-7}$ ≤ 5.5V or V_{SYS} (whichever is lower). Typical values are at T_J = +25℃, V_{SYS} = 3.8V, V_{IN12} = 1.5V, $V_{IN34, 5-7}$ = 3.8V, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, C_{IN12} = 2.2μF, $C_{IN34, 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF and C_{LDO1-7} = 4.7μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO6 PSRR and Noise							
Power Supply Rejection Ratio on VIN6	$PSRR_{VIN34\_LDO6}$	V_{IN6} = 3.8V + 0.2V_{P-P}, V_{SYS} = 4.0V, V_{LDO6} = 2.8V, I_{LDO6} = 100mA, no C_{SYS} and C_{IN6}	f_{REQ} = 1kHz		95		dB
			f_{REQ} = 10kHz		85		
			f_{REQ} = 100kHz		65		
			f_{REQ} = 1MHz		55		
Power Supply Rejection Ratio on VSYS	$PSRR_{VSYS\_LDO6}$	V_{SYS} = 4.0V + 0.2V_{P-P}, V_{IN6} = 3.8V, V_{LDO6} = 2.8V, I_{LDO6} = 100mA, no C_{SYS} and C_{IN6}	f_{REQ} = 1kHz		105		dB
			f_{REQ} = 10kHz		90		
			f_{REQ} = 100kHz		70		
			f_{REQ} = 1MHz		70		
LDO6 Output Noise	V_{NOISE_LDO6}	f_{REQ} = 10Hz to 100kHz, I_{LDO6} = 100mA			17		μV_{RMS}
LDO6 Regulation and Transient Performance							
LDO Load Regulation	ΔV_{LDR_LDO6}	I_{LDO6} = 1mA to 200mA, V_{LDO6} = 2.8V			1.5		mV
LDO Line Regulation	$\Delta V_{LNR\_VIN\_LDO6}$	V_{IN6} = 3.0V to 5.5V, V_{SYS} = 5.5V, I_{LDO6} = 10mA, V_{LDO6} = 2.8V			0.1		mV
	$\Delta V_{LNR\_VSYS\_LDO6}$	V_{SYS} = 3.3V to 5.5V, V_{IN6} = 3.0V, I_{LDO6} = 10mA, V_{LDO6} = 2.8V			0.1		
LDO6 Soft-Start							
Turn-On Delay Time	t_{DLY_LDO6}	From assertion of LDO output to soft-start ramp			350		μs
Soft-Start Time	t_{SS_LDO6}	V_{LDO6} from 5% to 95%, V_{LDO6} = 2.8V, I_{LDO6} = 10mA			400		μs
Startup Fault Disable Timer	t_{SUFD_LDO6}	Disable fault detection timer			1.5		ms
LDO6 Short-Circuit							
Hiccup Timer	t_{HICCUP}	Protection shutdown to recovery startup timer			22		ms
LDO5/7 Output Voltage							
LDO5/7 Output Voltage Range	$V_{RNG\_LDO5/7}$			1.504		3.544	V
LDO5/7 Extra Output Voltage	$V_{EX\_LDO5/7}$	I^2C programmable in 0x1F register			1.2		V
LDO5/7 Default Output Voltage	$V_{DEFAULT\_LDO5/7}$				2.8		V
LDO5/7 Output Voltage Step Size	V_{STEP}				8		mV
LDO5/7 Output Voltage Accuracy	$V_{ACC\_LDO5/7}$	$I_{LDO5/7}$ = 10mA, $V_{LDO5/7}$ = 2.2V and 2.8V, T_J = +25℃		-0.9		0.9	%
		$I_{LDO5/7}$ = 10mA, $V_{LDO5/7}$ = 1.504V to 3.544V, T_J = -40℃ to +125℃		-1.3		1.3	
LDO5/7 Dropout Voltage	$V_{DROPOUT\_LDO5/7}$	$I_{LDO5/7}$ = 600mA, $V_{LDO5/7}$ = 2.8V			140	190	mV
LDO5/7 Current Limit							
LDO5/7 Low Current Limit	$I_{LIML\_LDO5/7}$	$V_{IN5/7}$ ≥ $V_{LDO5/7}$ + 0.5V, V_{SYS} = 3.8V		550			mA
LDO5/7 High Current Limit	$I_{LIMH\_LDO5/7}$	$V_{IN5/7}$ ≥ $V_{LDO5/7}$ + 0.5V, V_{SYS} = 3.8V		750			mA
LDO5/7 Output Protection							
LDO5/7 Falling UVP Threshold	$UVP_{FL\_LDO5/7}$	V_{SYS} = 3.8V, $V_{LDO5/7}$ = 2.8V			80		% of $V_{LDO5/7}$
LDO5/7 Rising UVP Threshold	$UVP_{RS\_LDO5/7}$	V_{SYS} = 3.8V, $V_{LDO5/7}$ = 2.8V			90		% of $V_{LDO5/7}$
Output Discharge Resistance	$R_{DCHG\_LDO5/7}$				260		Ω

ELECTRICAL CHARACTERISTICS (continued)

(Minimum and Maximum values are measured at T_J = -40℃ to +85℃, V_{SYS} = 2.5V to 5.5V or ($V_{LDO1/2}$ + 1.6V) or (V_{LDO3-7} + 0.5V) (whichever is greater); at V_{IN12} = (0.7V to 2.0V) or ($V_{LDO1/2}$ + 0.2V) (whichever is greater); at $V_{IN34, 5-7}$ ≥ 1.8V or (V_{LDO3-7} + 0.2V) (whichever is greater), and $V_{IN34, 5-7}$ ≤ 5.5V or V_{SYS} (whichever is lower). Typical values are at T_J = +25℃, V_{SYS} = 3.8V, V_{IN12} = 1.5V, $V_{IN34, 5-7}$ = 3.8V, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, C_{IN12} = 2.2μF, $C_{IN34, 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF and C_{LDO1-7} = 4.7μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO5/7 PSRR and Noise							
Power Supply Rejection Ratio on VIN5/7	$PSRR_{VIN5/7\_LDO5/7}$	$V_{IN5/7}$ = 3.8V + 0.2V_{P-P}, V_{SYS} = 4.0V, $V_{LDO5/7}$ = 2.8V, $I_{LDO5/7}$ = 100mA, no C_{SYS} and $C_{IN5/7}$	f_{REQ} = 1kHz		95		dB
			f_{REQ} = 10kHz		85		
			f_{REQ} = 100kHz		65		
			f_{REQ} = 1MHz		55		
Power Supply Rejection Ratio on VSYS	$PSRR_{VSYS\_LDO5/7}$	V_{SYS} = 4.0V + 0.2V_{P-P}, $V_{IN5/7}$ = 3.8V, $V_{LDO5/7}$ = 2.8V, $I_{LDO5/7}$ = 100mA, no C_{SYS} and $C_{IN5/7}$	f_{REQ} = 1kHz		105		dB
			f_{REQ} = 10kHz		90		
			f_{REQ} = 100kHz		70		
			f_{REQ} = 1MHz		70		
LDO5/7 Output Noise	$V_{NOISE\_LDO5/7}$	f_{REQ} = 10Hz to 100kHz, $I_{LDO5/7}$ = 100mA			17		μV_{RMS}
LDO5/7 Regulation and Transient Performance							
LDO Load Regulation	$\Delta V_{LDR\_LDO5/7}$	$I_{LDO5/7}$ = 1mA to 200mA, $V_{LDO5/7}$ = 2.8V			2		mV
LDO Line Regulation	$\Delta V_{LNR\_VIN\_LDO5/7}$	$V_{IN5/7}$ = 3.0V to 5.5V, V_{SYS} = 5.5V, $I_{LDO5/7}$ = 10mA, $V_{LDO5/7}$ = 2.8V			0.1		mV
	$\Delta V_{LNR\_VSYS\_LDO5/7}$	V_{SYS} = 3.3V to 5.5V, $V_{IN5/7}$ = 3.0V, $I_{LDO5/7}$ = 10mA, $V_{LDO5/7}$ = 2.8V			0.1		
LDO5/7 Soft-Start							
Turn-On Delay Time	$t_{DLY\_LDO5/7}$	From assertion of LDO output to soft start ramp			350		μs
Soft-Start Time	$t_{SS\_LDO5/7}$	$V_{LDO5/7}$ from 5% to 95%, $V_{LDO5/7}$ = 2.8V, $I_{LDO5/7}$ = 10mA			400		μs
Startup Fault Disable Timer	$t_{SUFD\_LDO5/7}$	Disable fault detection timer			1.5		ms
LDO5/7 Short-Circuit							
Hiccup Timer	t_{HICCUP}	Protection shutdown to recovery startup timer			22		ms
Reset_B Logic Input							
Reset_B Leakage Current	$I_{LEAKAGE\_RESET\_B}$				0.1		μA
Reset_B Logic High Threshold	V_{IH}			0.9		5.50	V
Reset_B Logic Low Threshold	V_{IL}			0		0.4	V
INT Logic Output							
INT Leakage Current	$I_{LEAKAGE\_INT}$				0.1		μA
INT Logic High Voltage	V_{OH_INT}				1.8		V
I^2C Logic Input/ Output							
SDA and SCL Logic Low Threshold	V_{IL}					0.4	V
SDA and SCL Logic High Threshold	V_{IH}			0.9			V
SDA Logic Low Output	V_{OL}	3mA Sink				0.4	V

COMMUNICATION CHARACTERISTICS

PARAMETER	SYMBOL	FAST MODE		FAST MODE PLUS		UNITS
		MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}		400		1000	kHz
Bus-Free Time between STOP and START Condition	t_{BUF}	1.3		0.5		μs
START or Repeated START Hold Time	$t_{HD;STA}$	0.6		0.26		μs
Repeated START Setup Time	$t_{SU;STA}$	0.6		0.26		μs
STOP Condition Setup Time	$t_{SU;STO}$	0.6		0.26		μs
Data Hold Time	$t_{HD,DAT}$	0		0		μs
Data Setup Time	$t_{SU;DAT}$	100		50		ns
SCL Low Period	t_{LOW}	1.3		0.5		μs
SCL High Period	t_{HIGH}	0.6		0.26		μs
SDA and SCL Rise Time	t_R		300		120	ns
SDA and SCL Fall Time	t_F		300		120	ns
Data Valid Time	$t_{VD;DAT}$		0.9		0.45	μs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9		0.45	μs

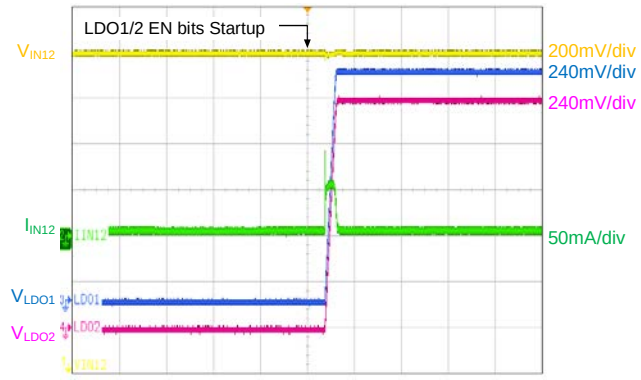
OUTPUT POWER MANAGEMENT

REGULATOR	CIRCUIT TYPE	I_{RATED} (mA)	DEFAULT HARDWARE VOLTAGE (V)	SPECIFIED/PROGRAMMABLE RANGE (V)	EXPECTED USE
LDO1	Linear NMOS LDO	1400	1.2	0.528 to 1.504	Sensor DVDD
LDO2	Linear NMOS LDO	1400	1.2	0.528 to 1.504	Sensor DVDD
LDO3	Linear PMOS LDO	500	2.8	1.504 to 3.544	All are fully programmable and can be used for AVDD, AF, IO, and OIS
LDO4	Linear PMOS LDO	500	2.8	1.504 to 3.544	All are fully programmable and can be used for AVDD, AF, IO, and OIS
LDO5	Linear PMOS LDO	750	2.8	1.2, 1.504 to 3.544	All are fully programmable and can be used for AVDD, AF, IO, and OIS
LDO6	Linear PMOS LDO	500	2.8	1.504 to 3.544	All are fully programmable and can be used for AVDD, AF, IO, and OIS
LDO7	Linear PMOS LDO	750	2.8	1.2, 1.504 to 3.544	All are fully programmable and can be used for AVDD, AF, IO, and OIS

TYPICAL PERFORMANCE CHARACTERISTICS

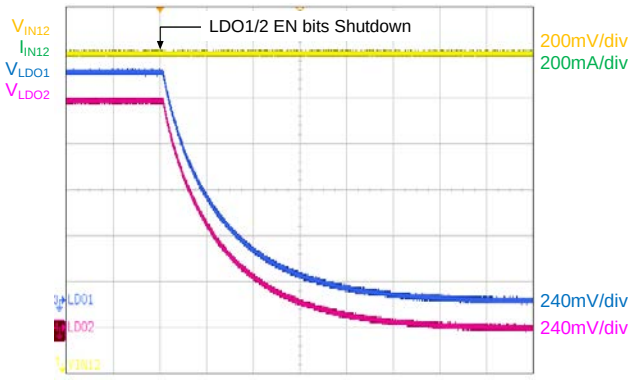
T_J = +25℃, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, V_{IN12} = 1.5V, $V_{IN34,\ 5-7}$ = 3.8V, V_{SYS} = 3.8V, C_{IN12} = 2.2μF, $C_{IN34,\ 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF, C_{LDO1-7} = 4.7μF, unless otherwise noted.

LDO1/2 EN bits Startup at $I_{LDO1/2}$ = 0mA



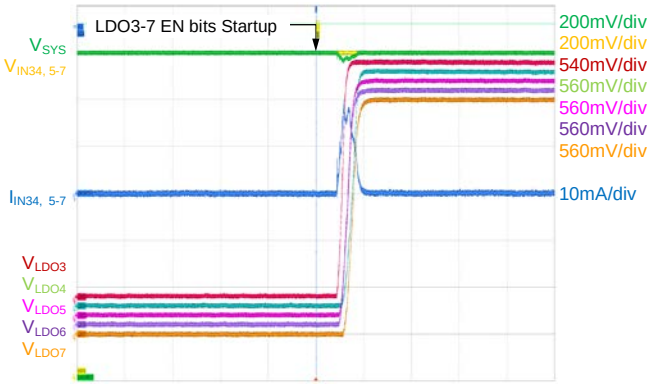
Time (1ms/div)

LDO1/2 EN bits Shutdown at $I_{LDO1/2}$ = 0mA



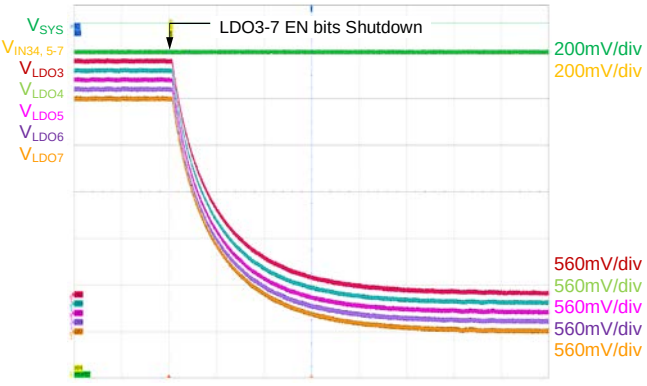
Time (1ms/div)

LDO3-7 EN bits Startup at I_{LDO3-7} = 0mA



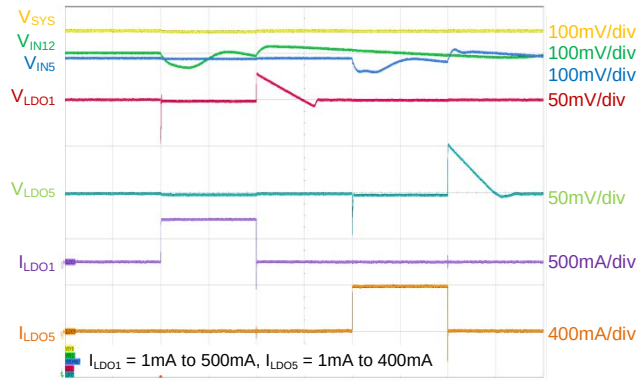
Time (1ms/div)

LDO3-7 EN bits Shutdown at I_{LDO3-7} = 0mA



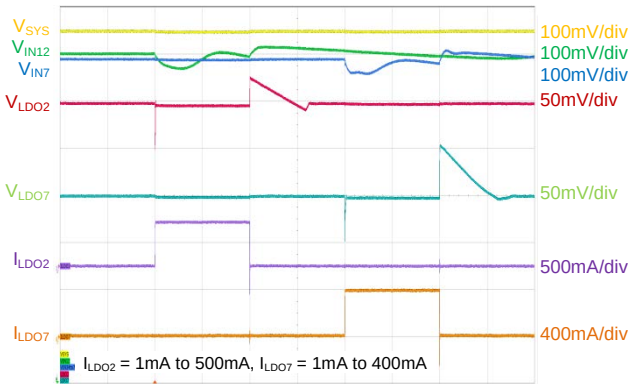
Time (1ms/div)

LDO1 and LDO5 Load Transient Response, t_R = t_F = 1μs



Time (100μs/div)

LDO2 and LDO7 Load Transient Response, t_R = t_F = 1μs

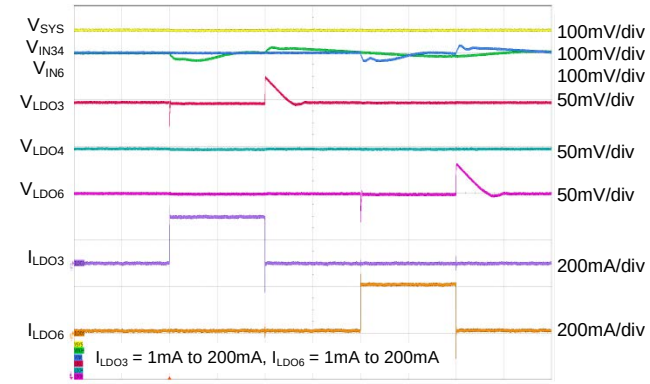


Time (100μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

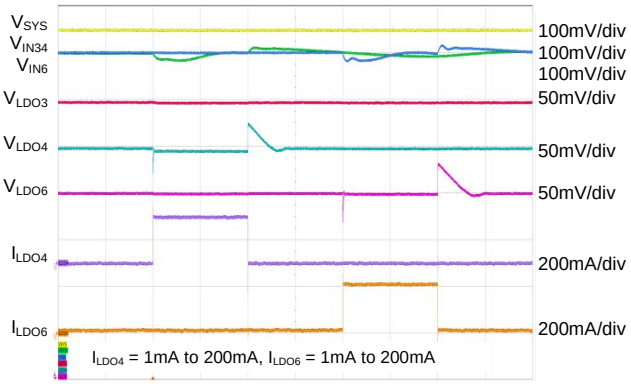
T_J = +25℃, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, V_{IN12} = 1.5V, $V_{IN34,\ 5-7}$ = 3.8V, V_{SYS} = 3.8V, C_{IN12} = 2.2μF, $C_{IN34,\ 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF, C_{LDO1-7} = 4.7μF, unless otherwise noted.

LDO3 and LDO6 Load Transient Response, $t_R = t_F$ = 1μs



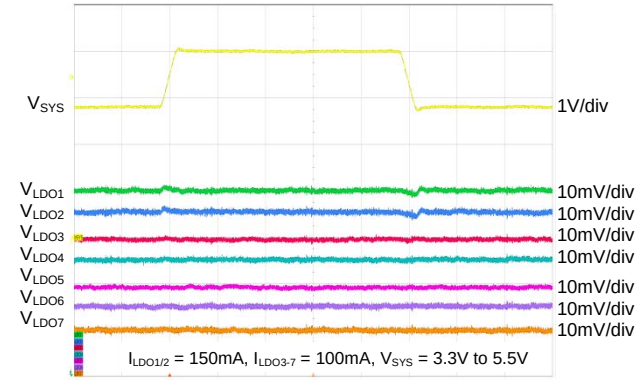
Time (100μs/div)

LDO4 and LDO6 Load Transient Response, $t_R = t_F$ = 1μs



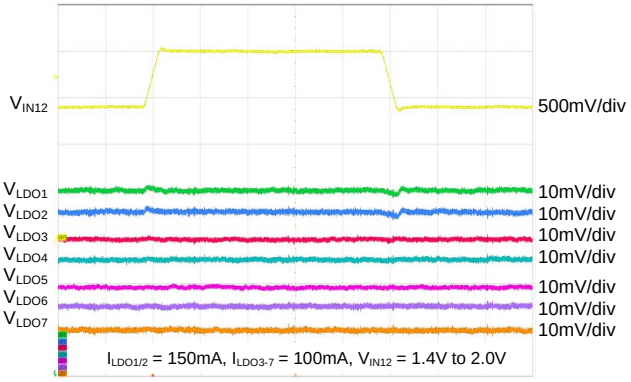
Time (100μs/div)

V_{SYS} Line Transient Response, $t_R = t_F$ = 5μs



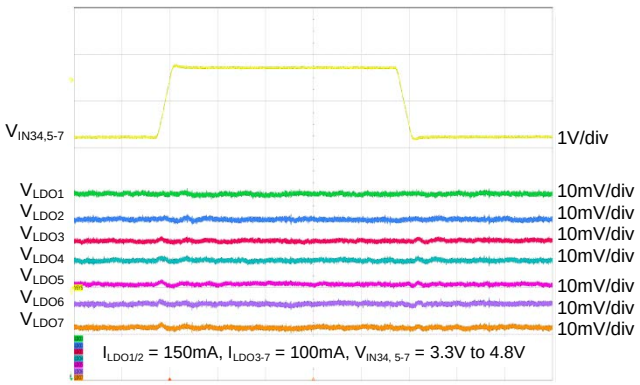
Time (20μs/div)

V_{IN12} Line Transient Response, $t_R = t_F$ = 5μs



Time (20μs/div)

$V_{IN34,\ 5-7}$ Line Transient Response, $t_R = t_F$ = 5μs

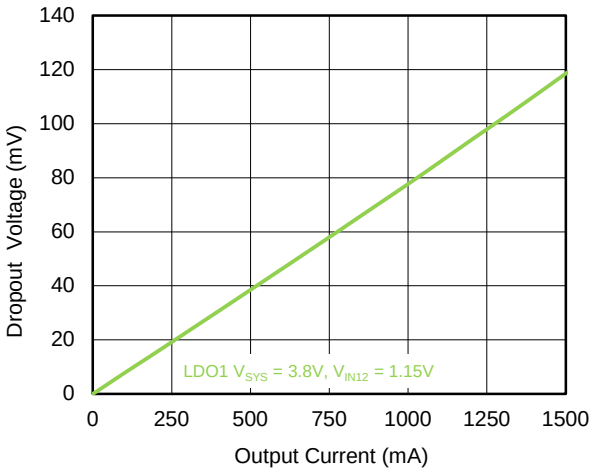


Time (20μs/div)

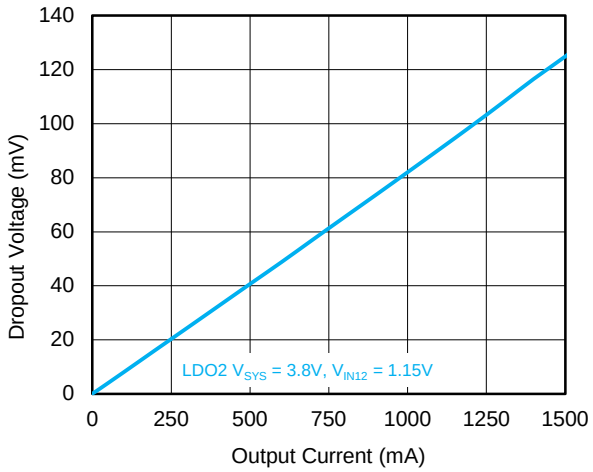
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, V_{IN12} = 1.5V, $V_{IN34,\ 5-7}$ = 3.8V, V_{SYS} = 3.8V, C_{IN12} = 2.2μF, $C_{IN34,\ 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF, C_{LDO1-7} = 4.7μF, unless otherwise noted.

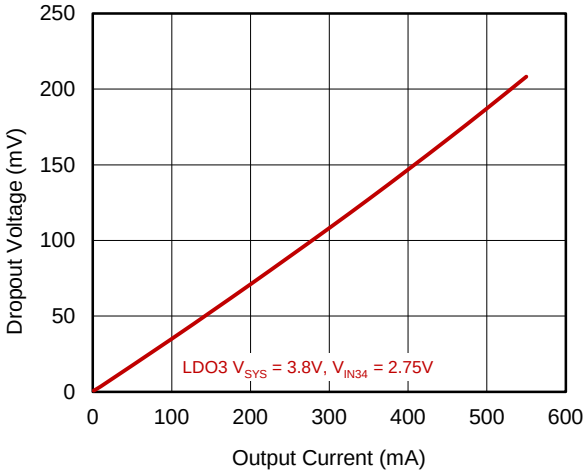
Dropout Voltage vs. Output Current



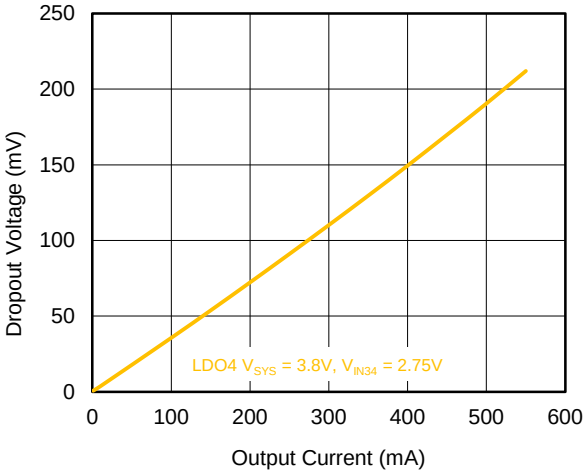
Dropout Voltage vs. Output Current



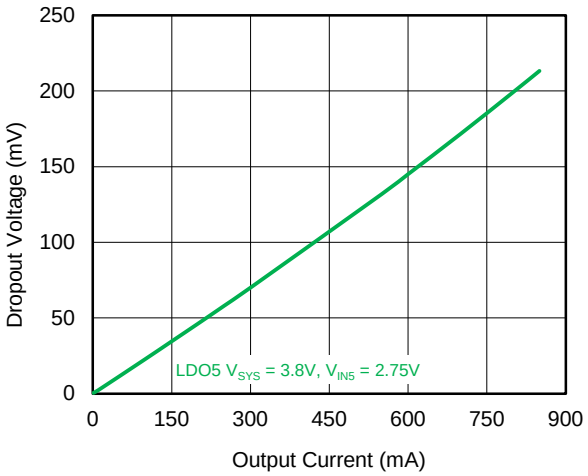
Dropout Voltage vs. Output Current



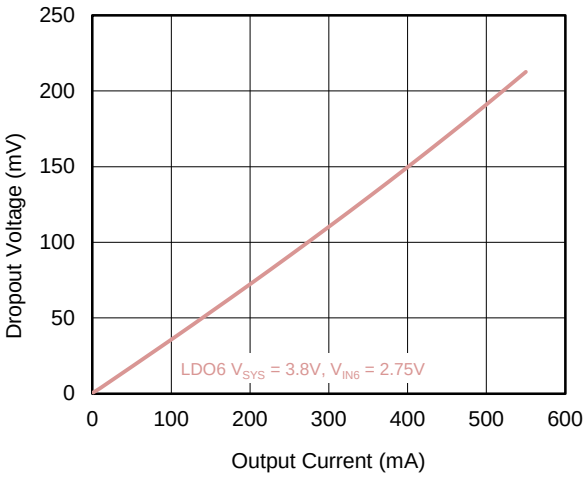
Dropout Voltage vs. Output Current



Dropout Voltage vs. Output Current



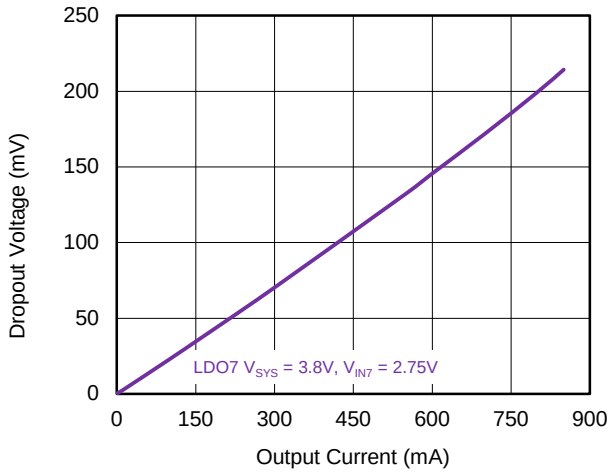
Dropout Voltage vs. Output Current



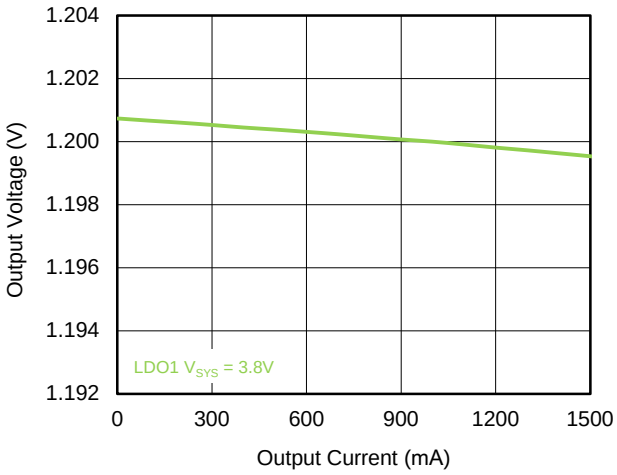
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, V_{IN12} = 1.5V, $V_{IN34,\ 5-7}$ = 3.8V, V_{SYS} = 3.8V, C_{IN12} = 2.2μF, $C_{IN34,\ 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF, C_{LDO1-7} = 4.7μF, unless otherwise noted.

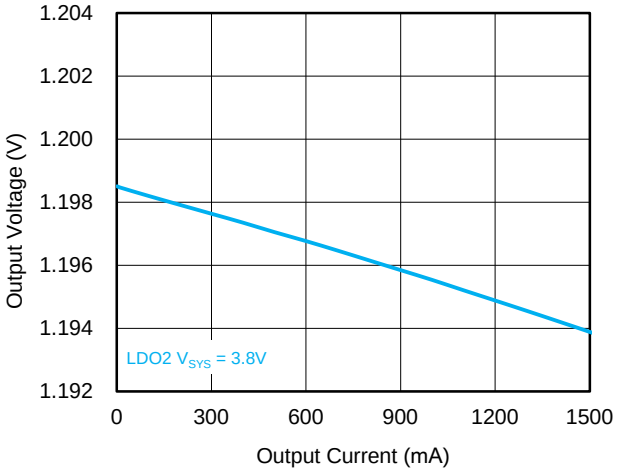
Dropout Voltage vs. Output Current



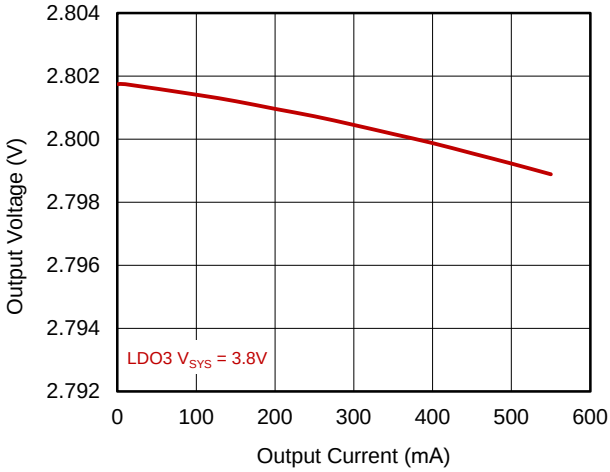
Output Voltage vs. Output Current



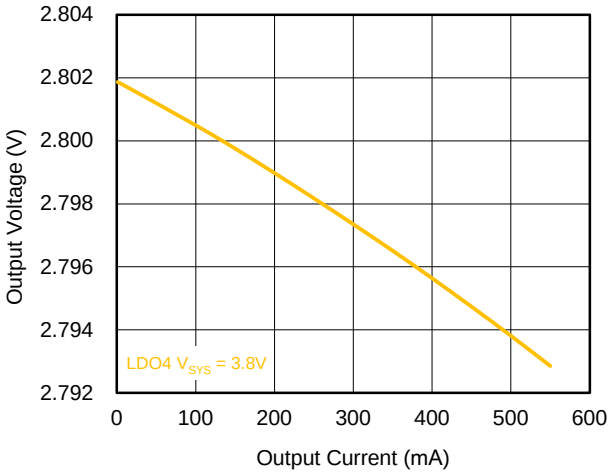
Output Voltage vs. Output Current



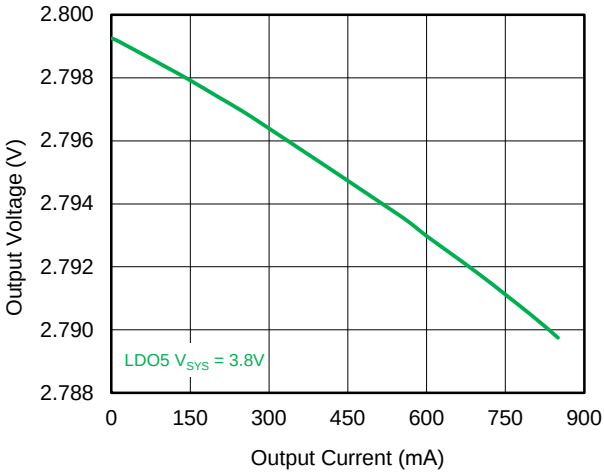
Output Voltage vs. Output Current



Output Voltage vs. Output Current



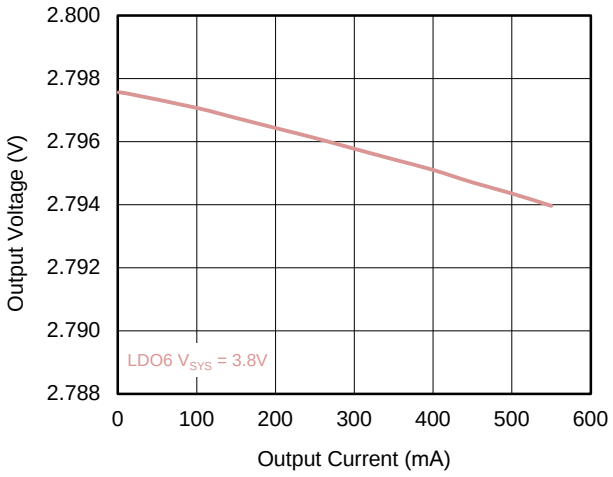
Output Voltage vs. Output Current



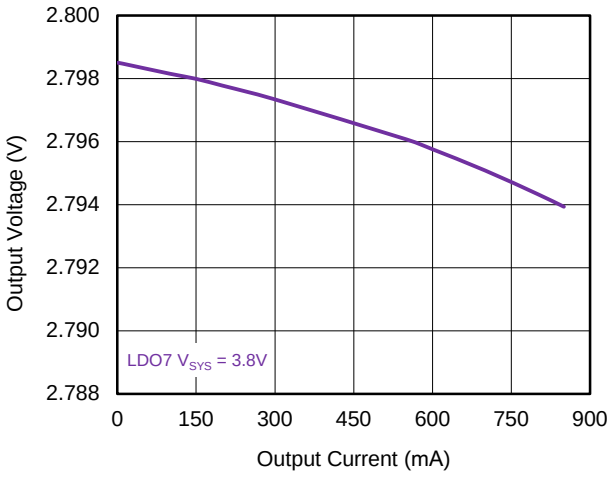
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, V_{IN12} = 1.5V, $V_{IN34, 5-7}$ = 3.8V, V_{SYS} = 3.8V, C_{IN12} = 2.2μF, $C_{IN34, 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF, C_{LDO1-7} = 4.7μF, unless otherwise noted.

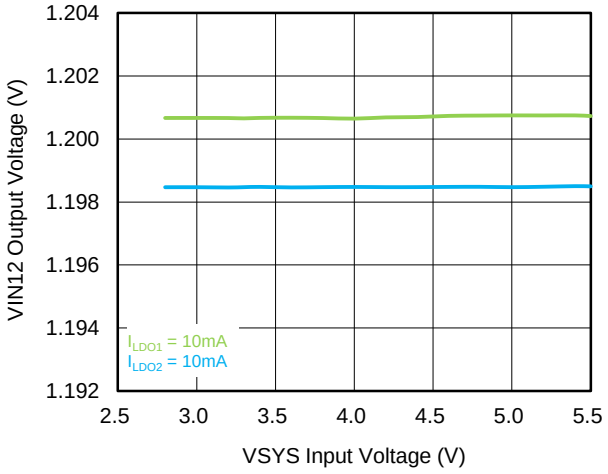
Output Voltage vs. Output Current



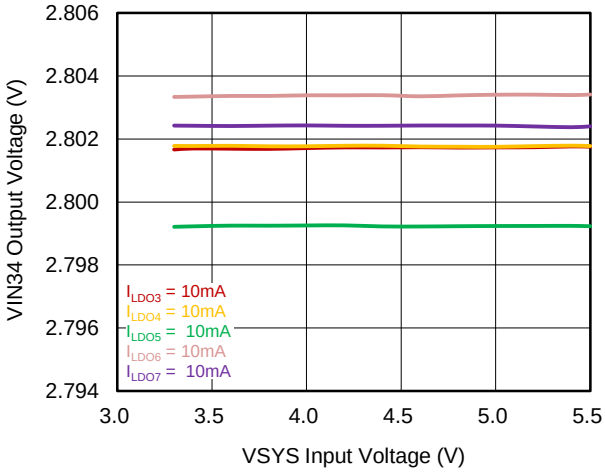
Output Voltage vs. Output Current



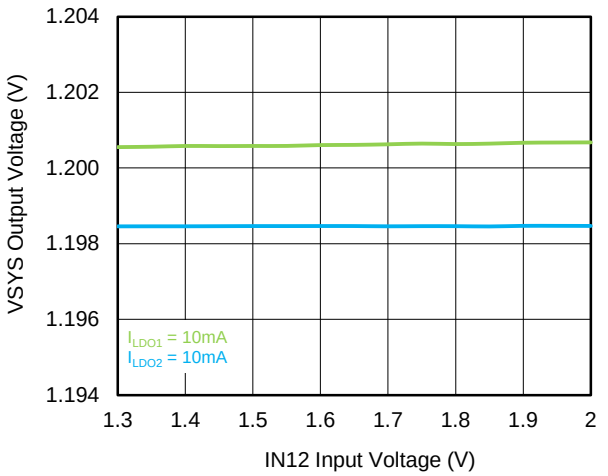
VIN12 Output Voltage vs. VSYS Input Voltage



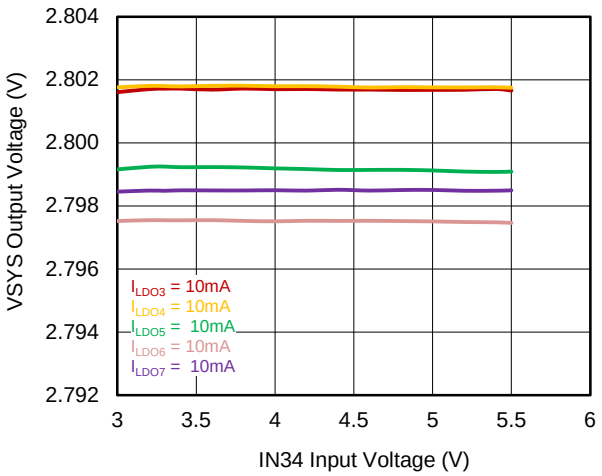
VIN34 Output Voltage vs. VSYS Input Voltage



V_{SYS} Output Voltage vs. IN12 Input Voltage



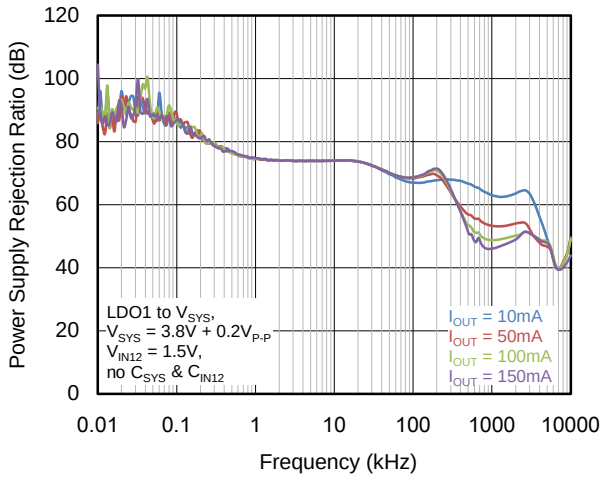
V_{SYS} Output Voltage vs. IN34 Input Voltage



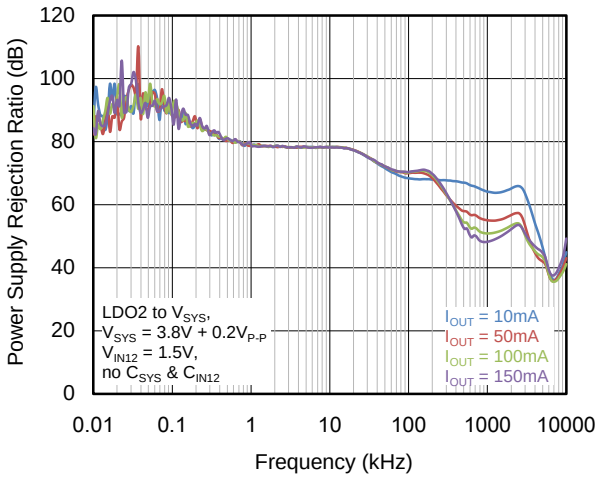
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, V_{IN12} = 1.5V, $V_{IN34, 5-7}$ = 3.8V, V_{SYS} = 3.8V, C_{IN12} = 2.2μF, $C_{IN34, 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF, C_{LDO1-7} = 4.7μF, unless otherwise noted.

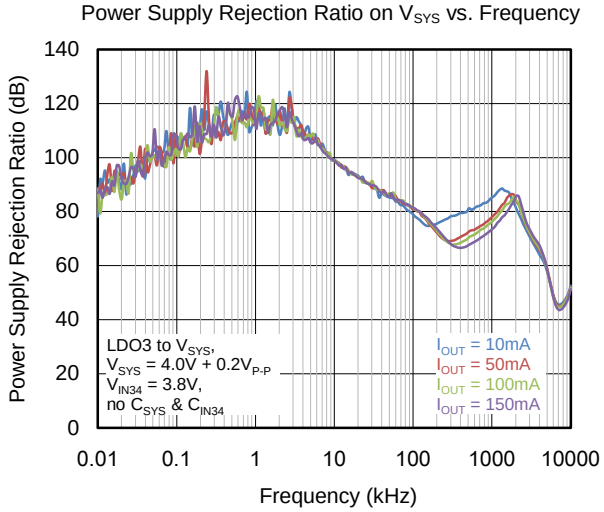
Power Supply Rejection Ratio on V_{SYS} vs. Frequency



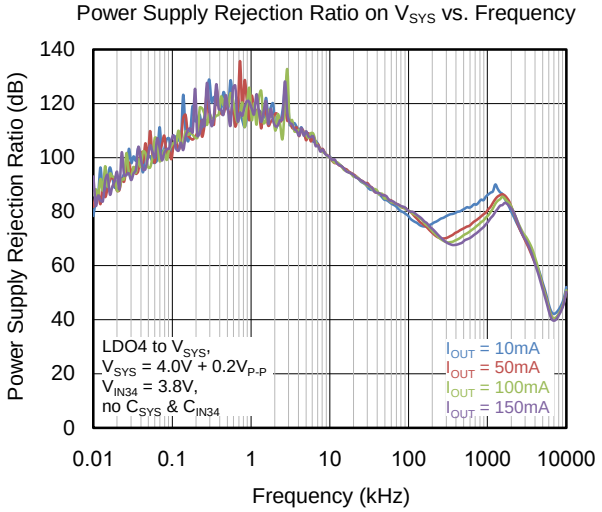
Power Supply Rejection Ratio on V_{SYS} vs. Frequency



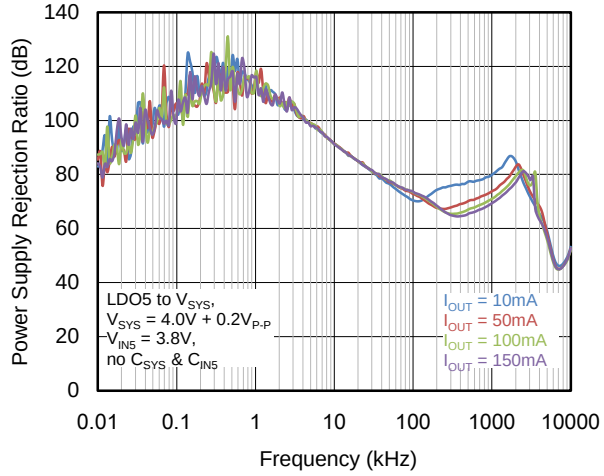
Power Supply Rejection Ratio on V_{SYS} vs. Frequency



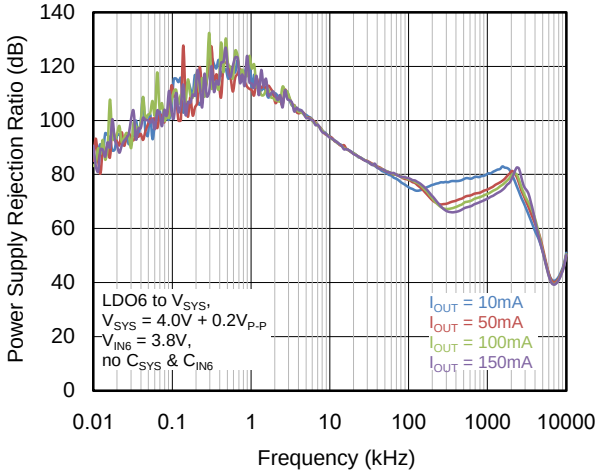
Power Supply Rejection Ratio on V_{SYS} vs. Frequency



Power Supply Rejection Ratio on V_{SYS} vs. Frequency



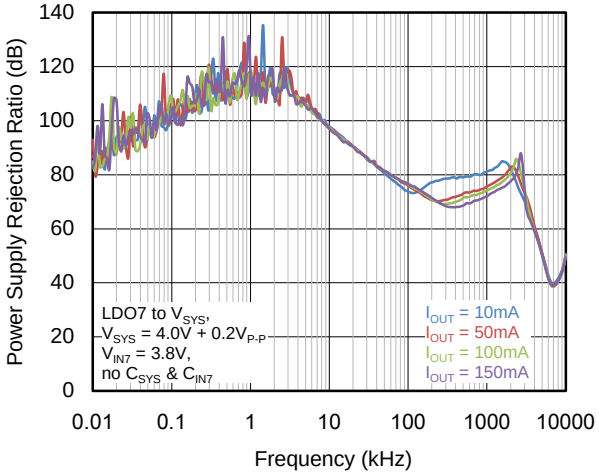
Power Supply Rejection Ratio on V_{SYS} vs. Frequency



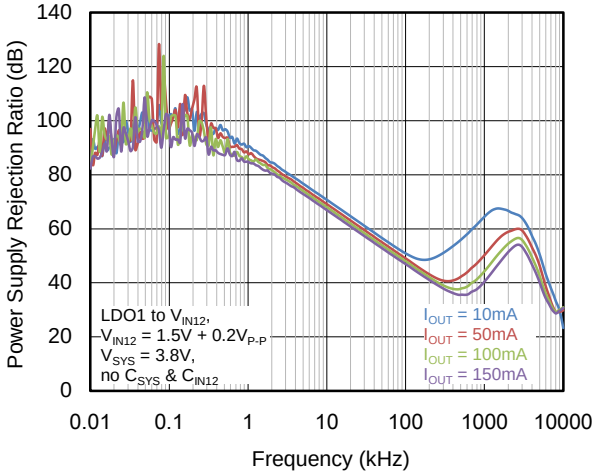
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, V_{IN12} = 1.5V, $V_{IN34,\ 5-7}$ = 3.8V, V_{SYS} = 3.8V, C_{IN12} = 2.2μF, $C_{IN34,\ 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF, C_{LDO1-7} = 4.7μF, unless otherwise noted.

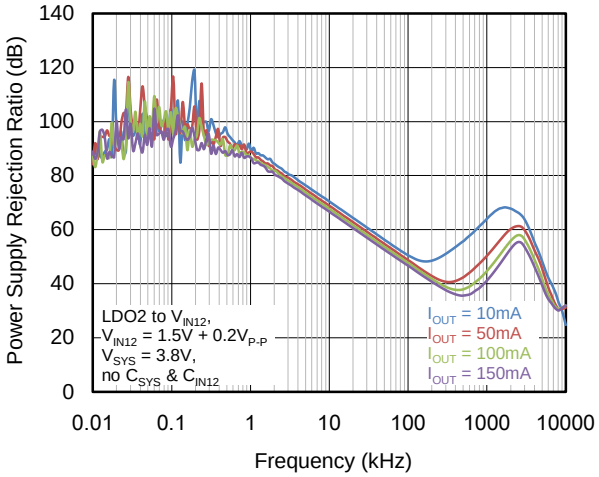
Power Supply Rejection Ratio on V_{SYS} vs. Frequency



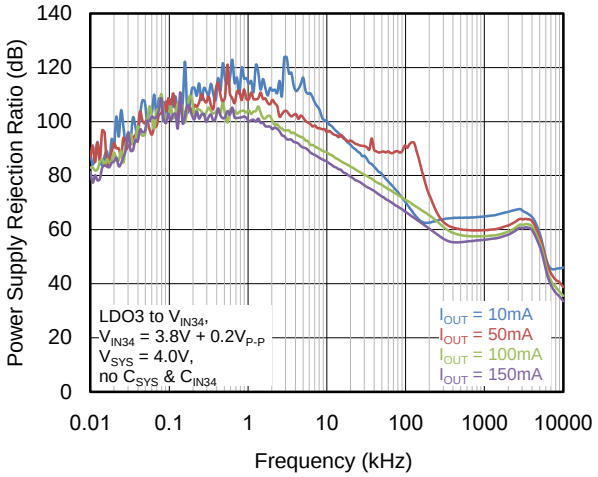
Power Supply Rejection Ratio on V_{IN12} vs. Frequency



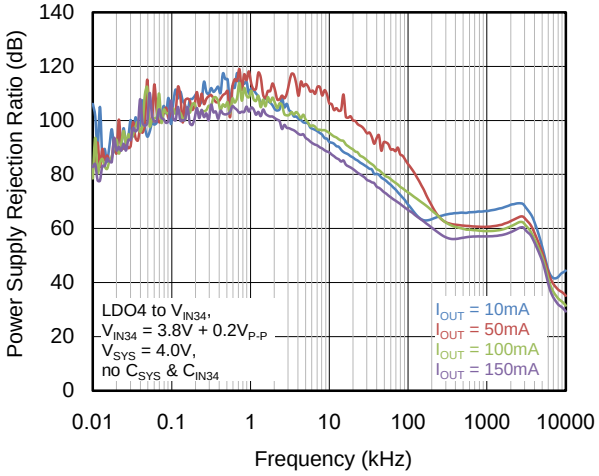
Power Supply Rejection Ratio on V_{IN12} vs. Frequency



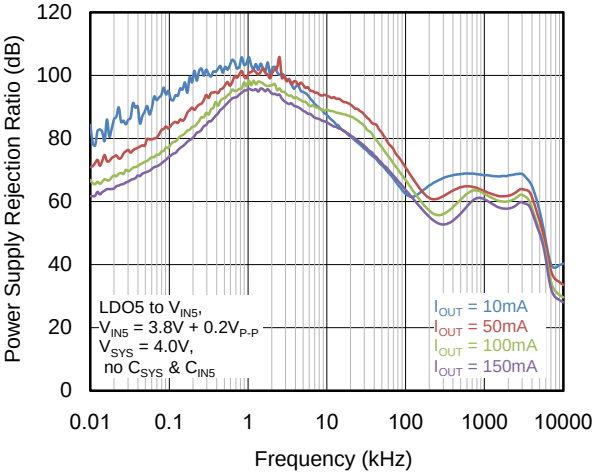
Power Supply Rejection Ratio on V_{IN34} vs. Frequency



Power Supply Rejection Ratio on V_{IN34} vs. Frequency



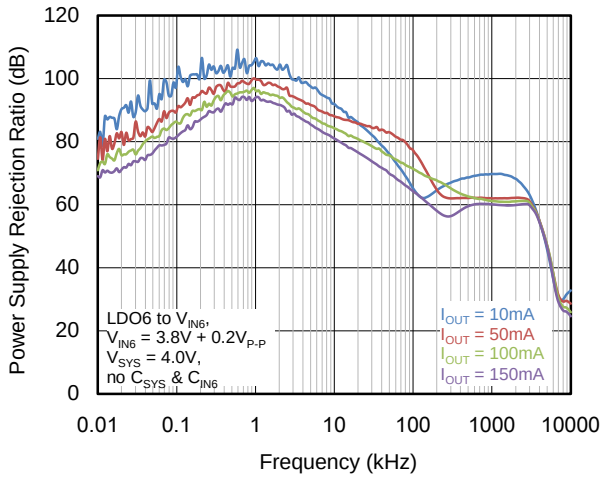
Power Supply Rejection Ratio on V_{IN5} vs. Frequency



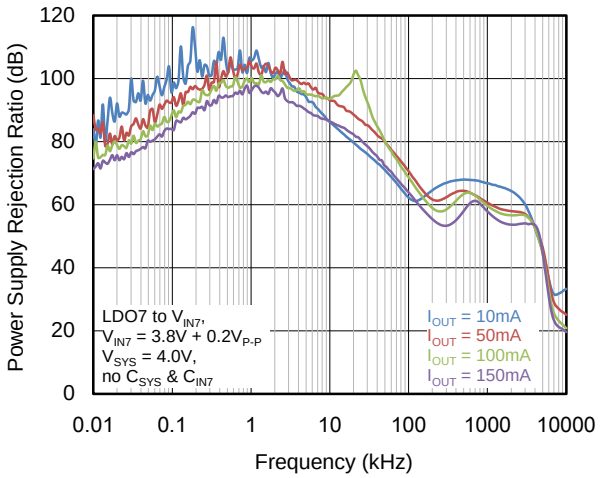
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, $V_{LDO1/2}$ = 1.2V, V_{LDO3-7} = 2.8V, V_{IN12} = 1.5V, $V_{IN34,\ 5-7}$ = 3.8V, V_{SYS} = 3.8V, C_{IN12} = 2.2μF, $C_{IN34,\ 5-7}$ = 1μF, C_{SYS} = 1μF, C_{REF} = 0.1μF, C_{LDO1-7} = 4.7μF, unless otherwise noted.

Power Supply Rejection Ratio on V_{IN6} vs. Frequency



Power Supply Rejection Ratio on V_{IN7} vs. Frequency



DETAILED DESCRIPTION

Startup and Shutdown Behavior

The SGM38120 has 7 LDO regulators. The hardware RESET_B pin has high priority to shut down the chip, so it is supposed to be set high before any LDO regulators are ready for powering up.

The 7 LDO regulators can start up by setting LDOx_EN bits to high when LDOx_SEQ[2:0] are respectively equal to '000'. (x means the number of the output LDOs, which is from 1 to 7.) Additionally, if configuring the LDOx_SEQ[2:0] to specific time slot number, the LDO regulators can be outputted in a sequential mode by setting SEQ_CTRL to '01'.

For shutdown behavior, there are three methods.
1. Pull the hardware RESET_B pin to low.
2. If enabled by LDOx_EN bits, set EN bits to low.
3. If enabled by SEQ CTRL bits, set SEQ CTRL to '10'.

Enable Register ON/OFF Control

The startup and shutdown of LDOx channels can be controlled by enable control register, LDOx_EN bits, only if LDOx_SEQ[2:0] bits are set to '000'. Before outputting, user can modify voltage level of each channel through output voltage level definition registers.

Sequence Enable Control

The sequence enable function of the SGM38120 allows the output to power up and off in a specific timing sequence. Each output needs to be pre-configured with a time slot to active sequence enable function. Configuring the time slot from 0 to the value between 1 and 7 means that the LDO can no longer be activated through the EN bit.

Once the sequence startup function is activated by SEQ_CTRL by writing to 2-bit code, '01', SEQ_COUNT begins to increment immediately. When the LDO encounters its time slot smaller than or equal to the SEQ_COUNT, the LDO will be activated. The duration of the time slot can be controlled by SEQ_SPEED. And the end of SEQ_COUNT is time slot 7.

The shutdown behavior of the sequence is initiated by writing SEQ_CTRL to 2-bit code, '10', causing SEQ_CNT to drop from 7 to 0 by the interval configured by SEQ_SPEED. When the time slot of LDO_SEQ is larger than the SEQ_COUNT value, the LDO will be turned off.

SEQ_ON is the activation signal of SEQ, which will flip to high, when SEQ_CTRL writing to 2-bit code, '01' and will return to low, once SEQ_CTRL writing to 2-bit code, '10'.

Thermal Protection

The SGM38120 has two thermal protection functions when the chip is enabled, and VSYS_EN = 1. One is the over-temperature warning (TSD_WRN), and the other is the over-temperature shutdown (TSD).

For TSD_WRN function, if the die temperature is over +128℃, the interrupt and state registers of TSD_WRN will flip to high. However, this thermal warning function will not influence the outputs to shutdown.

For TSD function, if the die temperature goes over +143℃, the interrupt and state registers of TSD will flip to high and the startup and shutdown chip-state register, CHIP_SUSD, will go high. This will cause all outputs shutdown.

VSYS and VINx (x = 12, 34, 5, 6, 7) UVLO Protection

The SGM38120 detects VSYS UVLO in terms of VSYS_EN = 1. The assertion of the state and interrupt register will present the VSYS UVLO fault. Besides, the startup and shutdown chip-state register, CHIP_SUSD, will go high, which means all outputs shutdown.

The VINx UVLO detection is on when both VSYS_EN and LDOs are enabled. If VINx drops below the low threshold, the interrupt and state registers of VINx UVLO will flip to high, and the startup and shutdown channel state register, LDOx_SUSD, will go high. This will cause the LDOx shutdown.

DETAILED DESCRIPTION (continued)

Output Over-Current and Under-Voltage Protection

The SGM38120 has the same protection logic to deal with the output over-current fault and under-voltage fault. Firstly, when OCP/UVP fault happens, the OCP/UVP state will go high. After the detection deglitch time (adjustable by register for OCP and fixed 50μs for UVP), the relevant LDO will shut down and its interrupt register will go high.

In the no fault shutdown mode (FLT_SDB = 1), the OCP/UVP faults are not required to shutdown any LDOs. The single channel fault counter will not react to the faults. But the UVP/OCP states and interrupt registers will go high.

Output Fault Recovery

The SGM38120 has three system faults (TSD_WRN, TSD, VSYS_UVLO) and three single-channel faults (VINx UVLO, LDOx OCP and UVP). The recovery from the fault shutdown to normal operation depends on the type of faults and the shutdown counts.

When the system faults TSD and VSYS UVLO occurred, the chip will not recover until all the system faults disappear at the minimum interval of 20ms. But if the system-fault counter is up to 4, the chip will permanently shut down. Then the LDOx_EN bits and LDO_SEQ registers will be cleared. To reactivate the outputs, the only programmable approach is to change the VSYS_EN bit from 1 to 0 and then to 1 again.

For example, if the chip triggers the TSD , there will be no recovery behavior until the die temperature under the TSD_WRN recovery threshold, because of the fault of TSD_WRN.

For the single-channel faults, the output will not recover until VINxUVLO faults are disappeared at the minimum interval of 20ms, and it will try to recover at the next 20ms in OCP and UVP fault recovery. When the single-channel fault count reaches 4, the channel will shut down permanently, then the LDO_EN bit and LDO_SEQ registers will be cleared. In addition, the single-channel fault counter will be cleared if LDO operates normally for 10ms.

Besides, system fault counter does not influence any single-channel fault counter, and every channel has its own independent fault counter.

Interrupt Function

The hardware interrupt pin on the SGM38120 indicates specific fault of the system faults and single channel faults. If the interrupt registers of the faults go high and the relevant fault mask register remains unset, the external interrupt pin will go high. The high-state interrupt pin and the interrupt bits in faults will not be reset until interrupt registers read.

Additionally, the interrupt pin features two output modes: open-drain and push-pull, which can be configured by the INT_MODE_SEL bit. In push-pull mode, the high level can be selected as 1.2V or 1.8V, with 1.8V by default.

Adjustable Output Current Limit

The adjustable output current limit is at 0x02[6:0] register. By default, all the channels are at their high level current limit. For LDO1/2, the current limit is 1400mA for high level and 1150mA for low level. For LDO3/4/6, the current limit is 500mA for high level and 400mA for low level. For LDO5/7, the current limit is 750mA for high level and 550mA for low level.

Output Discharge Function

By default, the output discharge resistors are all placed, for 250Ω. The discharge resistor can be configured in the Discharge Resistor Selection Register.

Soft Reset Function

The reset register is 0x11[7:4], which is supposed to write 4-bit code, ‘1011’ to execute software reset function. This function will reset the registers from 0x00 to 0x1F.

DETAILED DESCRIPTION (continued)

Programmable I²C Address Selection

The SGM38120 operates as a slave device that address is 0x35 by default. In the I2C_ADDR register, there are other three select-able device addresses for I²C communication. In the one or more SGM38120 application (see Figure 3), those applications that need to adjust the address of I2C should first pull up the RESET_B pin for address setting. The programmed device address will be reset by soft reset function, RESET_B pin low state and VSYS input voltage under 1.8V. To reuse the LDOs, users need to set RESET_B and I2C_ADDR register again.

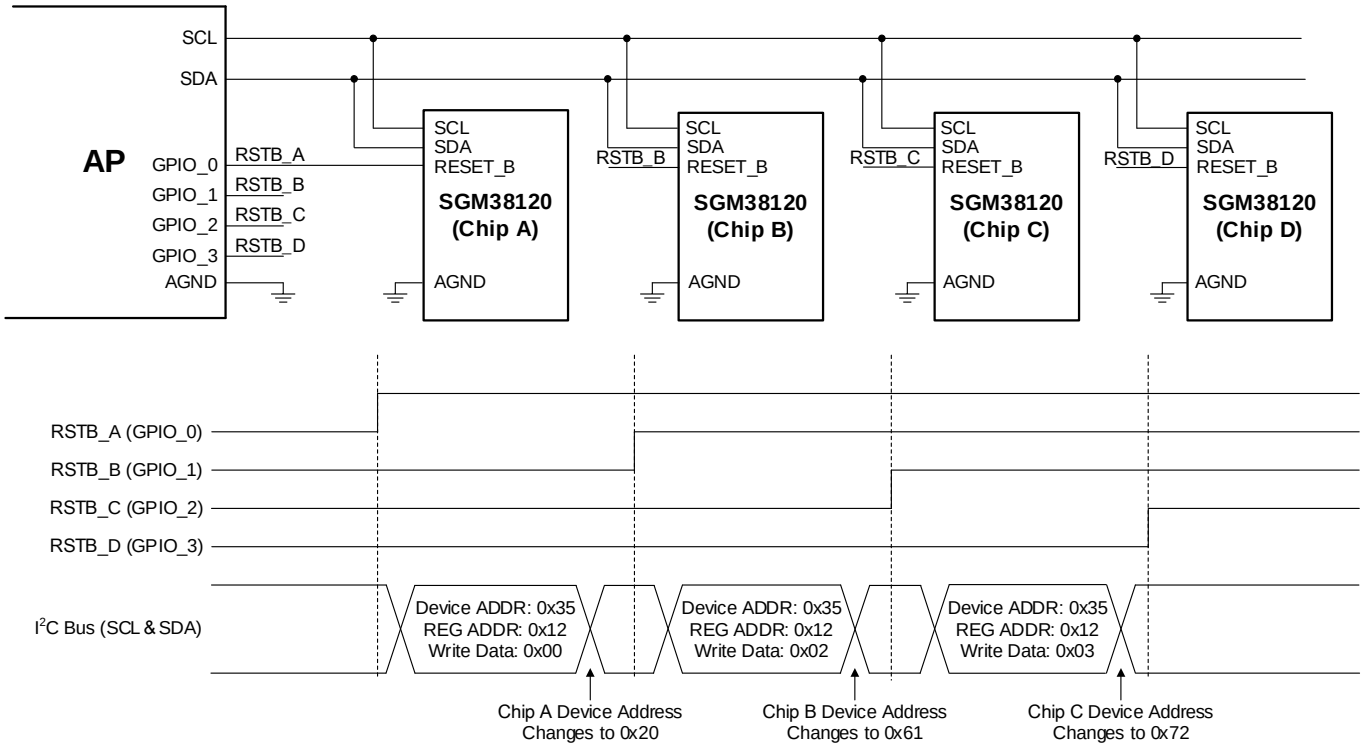


Figure 3. I²C Address Configuration in Four SGM38120 Application

REGISTER MAPS

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE
CHIP_ID	0x00[7:0]				
CHIP_REV	0x01[7:0]				
VSYS_EN					0x03[7]
LDO1_EN					0x03[0]
LDO1_SEQ	0x0B[2:0]				
LDO1_DISCH_EN					0x10[0]
LDO1_ILIM				0x02[0]	
LDO1_VOUT	0x04[7:0]				
LDO1_UVP	0x18[0]	0x15[0]	0x1C[0]		
LDO1_OCP	0x19[0]	0x16[0]	0x1D[0]		
LDO1_SUSD	0x1B[0]				
LDO2_EN					0x03[1]
LDO2_SEQ	0x0B[5:3]				
LDO2_DISCH_EN					0x10[1]
LDO2_ILIM				0x02[1]	
LDO2_VOUT	0x05[7:0]				
LDO2_UVP	0x18[1]	0x15[1]	0x1C[1]		
LDO2_OCP	0x19[1]	0x16[1]	0x1D[1]		
LDO2_SUSD	0x1B[1]				
LDO3_EN					0x03[2]
LDO3_SEQ	0x0C[2:0]				
LDO3_DISCH_EN					0x10[2]
LDO3_ILIM				0x02[2]	
LDO3_VOUT	0x06[7:0]				
LDO3_UVP	0x18[2]	0x15[2]	0x1C[2]		
LDO3_OCP	0x19[2]	0x16[2]	0x1D[2]		
LDO3_SUSD	0x1B[2]				
LDO4_EN					0x03[3]
LDO4_SEQ	0x0C[5:3]				
LDO4_DISCH_EN					0x10[3]
LDO4_ILIM				0x02[3]	
LDO4_VOUT	0x07[7:0]				
LDO4_UVP	0x18[3]	0x15[3]	0x1C[3]		
LDO4_OCP	0x19[3]	0x16[3]	0x1D[3]		
LDO4_SUSD	0x1B[3]				
LDO5_EN					0x03[4]
LDO5_SEQ	0x0D[2:0]				
LDO5_DISCH_EN					0x10[4]
LDO5_ILIM				0x02[4]	
LDO5_VOUT	0x08[7:0], 0x1F[0]				
LDO5_UVP	0x18[4]	0x15[4]	0x1C[4]		
LDO5_OCP	0x19[4]	0x16[4]	0x1D[4]		

REGISTER MAPS (continued)

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE
LDO5_SUSD	0x1B[4]				
LDO6_EN					0x03[5]
LDO6_SEQ	0x0D[5:3]				
LDO6_DISCH_EN					0x10[5]
LDO6_ILIM				0x02[5]	
LDO6_VOUT	0x09[7:0]				
LDO6_UVP	0x18[5]	0x15[5]	0x1C[5]		
LDO6_OCP	0x19[5]	0x16[5]	0x1D[5]		
LDO6_SUSD	0x1B[5]				
LDO7_EN					0x03[6]
LDO7_SEQ	0x0E[2:0]				
LDO7_DISCH_EN					0x10[6]
LDO7_ILIM				0x02[6]	
LDO7_VOUT	0x0A[7:0], 0x1F[1]				
LDO7_UVP	0x18[6]	0x15[6]	0x1C[6]		
LDO7_OCP	0x19[6]	0x16[6]	0x1D[6]		
LDO7_SUSD	0x1B[6]				
TSD	0x1A[7]	0x17[7]	0x1E[7]		
TSD_WRN	0x1A[6]	0x17[6]	0x1E[6]		
VSYS_UVLO	0x1A[5]	0x17[5]	0x1E[5]		
VIN7_UVLO	0x1A[4]	0x17[4]	0x1E[4]		
VIN6_UVLO	0x1A[3]	0x17[3]	0x1E[3]		
VIN5_UVLO	0x1A[2]	0x17[2]	0x1E[2]		
VIN34_UVLO	0x1A[1]	0x17[1]	0x1E[1]		
VIN12_UVLO	0x1A[0]	0x17[0]	0x1E[0]		
CHIP_SUSD	0x1B[7]				
SEQ_CONTROL	0x0F[3]				0x0F[5:4]
SEQ_SPEED	0x0F[7:6]				
SEQ_COUNT	0x0F[2:0]				
INT_LEVEL_SEL	0x12[7]				
INT_MODE_SEL	0x12[6]				
I2C_ADDR_SEL	0x12[1:0]				
SOFT_RESET					0x11[7:4]
OCP_TIMER	0x11[2:1]				
FLT_SD_B	0x11[0]				

REGISTER MAPS (continued)

I²C Slave Address of SGM38120: 0x35

Bit Types:
R: Read only
W: Write only
R/W: Read/Write
RCLR: Read Clear to 0
WCLR: Write Clear to 0

REG0x00: Product ID Register [Reset = 0xD9]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	CHIP_ID	11011001	R	Identifies vendor and device type 11011001 = SGM38120

REG0x01: SILICON REV ID Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	CHIP_REV	00000000	R	Identifies silicon revision

REG0x02: Current Limit Register [Reset = 0x7F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved
D[6]	LDO7_ILIM	1	R/W	Current Limit 0 = 550mA 1 = 750mA (default)
D[5]	LDO6_ILIM	1	R/W	Current Limit 0 = 400mA 1 = 500mA (default)
D[4]	LDO5_ILIM	1	R/W	Current Limit 0 = 550mA 1 = 750mA (default)
D[3]	LDO4_ILIM	1	R/W	Current Limit 0 = 400mA 1 = 500mA (default)
D[2]	LDO3_ILIM	1	R/W	Current Limit 0 = 400mA 1 = 500mA (default)
D[1]	LDO2_ILIM	1	R/W	Current Limit 0 = 1150mA 1 = 1400mA (default)
D[0]	LDO1_ILIM	1	R/W	Current Limit 0 = 1150mA 1 = 1400mA (default)

REGISTER MAPS (continued)

REG0x03: Enable Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VSYS_EN	0	R/W	Enable bit for system. The system bias will get ready for enabling individual. 0 = Disabled (default) 1 = Enabled
D[6]	LDO7_EN	0	R/W	Enable bit for LDO7. This bit only controls the state of LDO7 if LDO7_SEQ = 000. 0 = Disabled (default) 1 = Enabled
D[5]	LDO6_EN	0	R/W	Enable bit for LDO6. This bit only controls the state of LDO6 if LDO6_SEQ = 000. 0 = Disabled (default) 1 = Enabled
D[4]	LDO5_EN	0	R/W	Enable bit for LDO5. This bit only controls the state of LDO5 if LDO5_SEQ = 000. 0 = Disabled (default) 1 = Enabled
D[3]	LDO4_EN	0	R/W	Enable bit for LDO4. This bit only controls the state of LDO4 if LDO4_SEQ = 000. 0 = Disabled (default) 1 = Enabled
D[2]	LDO3_EN	0	R/W	Enable bit for LDO3. This bit only controls the state of LDO3 if LDO3_SEQ = 000. 0 = Disabled (default) 1 = Enabled
D[1]	LDO2_EN	0	R/W	Enable bit for LDO2. This bit only controls the state of LDO2 if LDO2_SEQ = 000. 0 = Disabled (default) 1 = Enabled
D[0]	LDO1_EN	0	R/W	Enable bit for LDO1. This bit only controls the state of LDO1 if LDO1_SEQ = 000. 0 = Disabled (default) 1 = Enabled

REGISTER MAPS (continued)

REG0x04: LDO1 Output Voltage Level Definition Register [Reset = 0x57]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	LDO1_VOUT	01010111	R/W	Sets LDO1 regulation target voltage. Equation: V_{LDO1} = (504 + 8 × *d*) × 1mV, where *d* is the decimal value of the register. See Table 1.

Table 1. LDO1 Output Voltage Level Definition

Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)
00	Reserved	2E	0.872	5C	1.240	8A	Reserved	B8	Reserved	E6	Reserved
01	Reserved	2F	0.880	5D	1.248	8B	Reserved	B9	Reserved	E7	Reserved
02	Reserved	30	0.888	5E	1.256	8C	Reserved	BA	Reserved	E8	Reserved
03	0.528	31	0.896	5F	1.264	8D	Reserved	BB	Reserved	E9	Reserved
04	0.536	32	0.904	60	1.272	8E	Reserved	BC	Reserved	EA	Reserved
05	0.544	33	0.912	61	1.280	8F	Reserved	BD	Reserved	EB	Reserved
06	0.552	34	0.920	62	1.288	90	Reserved	BE	Reserved	EC	Reserved
07	0.560	35	0.928	63	1.296	91	Reserved	BF	Reserved	ED	Reserved
08	0.568	36	0.936	64	1.304	92	Reserved	C0	Reserved	EE	Reserved
09	0.576	37	0.944	65	1.312	93	Reserved	C1	Reserved	EF	Reserved
0A	0.584	38	0.952	66	1.320	94	Reserved	C2	Reserved	F0	Reserved
0B	0.592	39	0.960	67	1.328	95	Reserved	C3	Reserved	F1	Reserved
0C	0.600	3A	0.968	68	1.336	96	Reserved	C4	Reserved	F2	Reserved
0D	0.608	3B	0.976	69	1.344	97	Reserved	C5	Reserved	F3	Reserved
0E	0.616	3C	0.984	6A	1.352	98	Reserved	C6	Reserved	F4	Reserved
0F	0.624	3D	0.992	6B	1.360	99	Reserved	C7	Reserved	F5	Reserved
10	0.632	3E	1.000	6C	1.368	9A	Reserved	C8	Reserved	F6	Reserved
11	0.640	3F	1.008	6D	1.376	9B	Reserved	C9	Reserved	F7	Reserved
12	0.648	40	1.016	6E	1.384	9C	Reserved	CA	Reserved	F8	Reserved
13	0.656	41	1.024	6F	1.392	9D	Reserved	CB	Reserved	F9	Reserved
14	0.664	42	1.032	70	1.400	9E	Reserved	CC	Reserved	FA	Reserved
15	0.672	43	1.040	71	1.408	9F	Reserved	CD	Reserved	FB	Reserved
16	0.680	44	1.048	72	1.416	A0	Reserved	CE	Reserved	FC	Reserved
17	0.688	45	1.056	73	1.424	A1	Reserved	CF	Reserved	FD	Reserved
18	0.696	46	1.064	74	1.432	A2	Reserved	D0	Reserved	FE	Reserved
19	0.704	47	1.072	75	1.440	A3	Reserved	D1	Reserved	FF	Reserved
1A	0.712	48	1.080	76	1.448	A4	Reserved	D2	Reserved		
1B	0.720	49	1.088	77	1.456	A5	Reserved	D3	Reserved		
1C	0.728	4A	1.096	78	1.464	A6	Reserved	D4	Reserved		
1D	0.736	4B	1.104	79	1.472	A7	Reserved	D5	Reserved		
1E	0.744	4C	1.112	7A	1.480	A8	Reserved	D6	Reserved		
1F	0.752	4D	1.120	7B	1.488	A9	Reserved	D7	Reserved		
20	0.760	4E	1.128	7C	1.496	AA	Reserved	D8	Reserved		
21	0.768	4F	1.136	7D	1.504	AB	Reserved	D9	Reserved		
22	0.776	50	1.144	7E	Reserved	AC	Reserved	DA	Reserved		
23	0.784	51	1.152	7F	Reserved	AD	Reserved	DB	Reserved		
24	0.792	52	1.160	80	Reserved	AE	Reserved	DC	Reserved		
25	0.800	53	1.168	81	Reserved	AF	Reserved	DD	Reserved		
26	0.808	54	1.176	82	Reserved	B0	Reserved	DE	Reserved		
27	0.816	55	1.184	83	Reserved	B1	Reserved	DF	Reserved		
28	0.824	56	1.192	84	Reserved	B2	Reserved	E0	Reserved		
29	0.832	57	1.200	85	Reserved	B3	Reserved	E1	Reserved		
2A	0.840	58	1.208	86	Reserved	B4	Reserved	E2	Reserved		
2B	0.848	59	1.216	87	Reserved	B5	Reserved	E3	Reserved		
2C	0.856	5A	1.224	88	Reserved	B6	Reserved	E4	Reserved		
2D	0.864	5B	1.232	89	Reserved	B7	Reserved	E5	Reserved		

REGISTER MAPS (continued)

REG0x05: LDO2 Output Voltage Level Definition Register [Reset = 0x57]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	LDO2_VOUT	01010111	R/W	Sets LDO2 regulation target voltage. Equation: V_{LDO2} = (504 + 8 × *d*) × 1mV, where *d* is the decimal value of the register. See Table 2.

Table 2. LDO2 Output Voltage Level Definition

Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)
00	Reserved	2E	0.872	5C	1.240	8A	Reserved	B8	Reserved	E6	Reserved
01	Reserved	2F	0.880	5D	1.248	8B	Reserved	B9	Reserved	E7	Reserved
02	Reserved	30	0.888	5E	1.256	8C	Reserved	BA	Reserved	E8	Reserved
03	0.528	31	0.896	5F	1.264	8D	Reserved	BB	Reserved	E9	Reserved
04	0.536	32	0.904	60	1.272	8E	Reserved	BC	Reserved	EA	Reserved
05	0.544	33	0.912	61	1.280	8F	Reserved	BD	Reserved	EB	Reserved
06	0.552	34	0.920	62	1.288	90	Reserved	BE	Reserved	EC	Reserved
07	0.560	35	0.928	63	1.296	91	Reserved	BF	Reserved	ED	Reserved
08	0.568	36	0.936	64	1.304	92	Reserved	C0	Reserved	EE	Reserved
09	0.576	37	0.944	65	1.312	93	Reserved	C1	Reserved	EF	Reserved
0A	0.584	38	0.952	66	1.320	94	Reserved	C2	Reserved	F0	Reserved
0B	0.592	39	0.960	67	1.328	95	Reserved	C3	Reserved	F1	Reserved
0C	0.600	3A	0.968	68	1.336	96	Reserved	C4	Reserved	F2	Reserved
0D	0.608	3B	0.976	69	1.344	97	Reserved	C5	Reserved	F3	Reserved
0E	0.616	3C	0.984	6A	1.352	98	Reserved	C6	Reserved	F4	Reserved
0F	0.624	3D	0.992	6B	1.360	99	Reserved	C7	Reserved	F5	Reserved
10	0.632	3E	1.000	6C	1.368	9A	Reserved	C8	Reserved	F6	Reserved
11	0.640	3F	1.008	6D	1.376	9B	Reserved	C9	Reserved	F7	Reserved
12	0.648	40	1.016	6E	1.384	9C	Reserved	CA	Reserved	F8	Reserved
13	0.656	41	1.024	6F	1.392	9D	Reserved	CB	Reserved	F9	Reserved
14	0.664	42	1.032	70	1.400	9E	Reserved	CC	Reserved	FA	Reserved
15	0.672	43	1.040	71	1.408	9F	Reserved	CD	Reserved	FB	Reserved
16	0.680	44	1.048	72	1.416	A0	Reserved	CE	Reserved	FC	Reserved
17	0.688	45	1.056	73	1.424	A1	Reserved	CF	Reserved	FD	Reserved
18	0.696	46	1.064	74	1.432	A2	Reserved	D0	Reserved	FE	Reserved
19	0.704	47	1.072	75	1.440	A3	Reserved	D1	Reserved	FF	Reserved
1A	0.712	48	1.080	76	1.448	A4	Reserved	D2	Reserved		
1B	0.720	49	1.088	77	1.456	A5	Reserved	D3	Reserved		
1C	0.728	4A	1.096	78	1.464	A6	Reserved	D4	Reserved		
1D	0.736	4B	1.104	79	1.472	A7	Reserved	D5	Reserved		
1E	0.744	4C	1.112	7A	1.480	A8	Reserved	D6	Reserved		
1F	0.752	4D	1.120	7B	1.488	A9	Reserved	D7	Reserved		
20	0.760	4E	1.128	7C	1.496	AA	Reserved	D8	Reserved		
21	0.768	4F	1.136	7D	1.504	AB	Reserved	D9	Reserved		
22	0.776	50	1.144	7E	Reserved	AC	Reserved	DA	Reserved		
23	0.784	51	1.152	7F	Reserved	AD	Reserved	DB	Reserved		
24	0.792	52	1.160	80	Reserved	AE	Reserved	DC	Reserved		
25	0.800	53	1.168	81	Reserved	AF	Reserved	DD	Reserved		
26	0.808	54	1.176	82	Reserved	B0	Reserved	DE	Reserved		
27	0.816	55	1.184	83	Reserved	B1	Reserved	DF	Reserved		
28	0.824	56	1.192	84	Reserved	B2	Reserved	E0	Reserved		
29	0.832	57	1.200	85	Reserved	B3	Reserved	E1	Reserved		
2A	0.840	58	1.208	86	Reserved	B4	Reserved	E2	Reserved		
2B	0.848	59	1.216	87	Reserved	B5	Reserved	E3	Reserved		
2C	0.856	5A	1.224	88	Reserved	B6	Reserved	E4	Reserved		
2D	0.864	5B	1.232	89	Reserved	B7	Reserved	E5	Reserved		

REGISTER MAPS (continued)

REG0x06: LDO3 Output Voltage Level Definition Register [Reset = 0xA2]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	LDO3_VOUT	10100010	R/W	Sets LDO3 regulation target voltage. Equation: V_{LDO3} = (1504 + 8 × d) × 1mV, where d is the decimal value of the register. See Table 3.

Table 3. LDO3 Output Voltage Level Definition

Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)
00	1.504	2E	1.872	5C	2.240	8A	2.608	B8	2.976	E6	3.344
01	1.512	2F	1.880	5D	2.248	8B	2.616	B9	2.984	E7	3.352
02	1.520	30	1.888	5E	2.256	8C	2.624	BA	2.992	E8	3.360
03	1.528	31	1.896	5F	2.264	8D	2.632	BB	3.000	E9	3.368
04	1.536	32	1.904	60	2.272	8E	2.640	BC	3.008	EA	3.376
05	1.544	33	1.912	61	2.280	8F	2.648	BD	3.016	EB	3.384
06	1.552	34	1.920	62	2.288	90	2.656	BE	3.024	EC	3.392
07	1.560	35	1.928	63	2.296	91	2.664	BF	3.032	ED	3.400
08	1.568	36	1.936	64	2.304	92	2.672	C0	3.040	EE	3.408
09	1.576	37	1.944	65	2.312	93	2.680	C1	3.048	EF	3.416
0A	1.584	38	1.952	66	2.320	94	2.688	C2	3.056	F0	3.424
0B	1.592	39	1.960	67	2.328	95	2.696	C3	3.064	F1	3.432
0C	1.600	3A	1.968	68	2.336	96	2.704	C4	3.072	F2	3.440
0D	1.608	3B	1.976	69	2.344	97	2.712	C5	3.080	F3	3.448
0E	1.616	3C	1.984	6A	2.352	98	2.720	C6	3.088	F4	3.456
0F	1.624	3D	1.992	6B	2.360	99	2.728	C7	3.096	F5	3.464
10	1.632	3E	2.000	6C	2.368	9A	2.736	C8	3.104	F6	3.472
11	1.640	3F	2.008	6D	2.376	9B	2.744	C9	3.112	F7	3.480
12	1.648	40	2.016	6E	2.384	9C	2.752	CA	3.120	F8	3.488
13	1.656	41	2.024	6F	2.392	9D	2.760	CB	3.128	F9	3.496
14	1.664	42	2.032	70	2.400	9E	2.768	CC	3.136	FA	3.504
15	1.672	43	2.040	71	2.408	9F	2.776	CD	3.144	FB	3.512
16	1.680	44	2.048	72	2.416	A0	2.784	CE	3.152	FC	3.520
17	1.688	45	2.056	73	2.424	A1	2.792	CF	3.160	FD	3.528
18	1.696	46	2.064	74	2.432	A2	2.800	D0	3.168	FE	3.536
19	1.704	47	2.072	75	2.440	A3	2.808	D1	3.176	FF	3.544
1A	1.712	48	2.080	76	2.448	A4	2.816	D2	3.184		
1B	1.720	49	2.088	77	2.456	A5	2.824	D3	3.192		
1C	1.728	4A	2.096	78	2.464	A6	2.832	D4	3.200		
1D	1.736	4B	2.104	79	2.472	A7	2.840	D5	3.208		
1E	1.744	4C	2.112	7A	2.480	A8	2.848	D6	3.216		
1F	1.752	4D	2.120	7B	2.488	A9	2.856	D7	3.224		
20	1.760	4E	2.128	7C	2.496	AA	2.864	D8	3.232		
21	1.768	4F	2.136	7D	2.504	AB	2.872	D9	3.240		
22	1.776	50	2.144	7E	2.512	AC	2.880	DA	3.248		
23	1.784	51	2.152	7F	2.520	AD	2.888	DB	3.256		
24	1.792	52	2.160	80	2.528	AE	2.896	DC	3.264		
25	1.800	53	2.168	81	2.536	AF	2.904	DD	3.272		
26	1.808	54	2.176	82	2.544	B0	2.912	DE	3.280		
27	1.816	55	2.184	83	2.552	B1	2.920	DF	3.288		
28	1.824	56	2.192	84	2.560	B2	2.928	E0	3.296		
29	1.832	57	2.200	85	2.568	B3	2.936	E1	3.304		
2A	1.840	58	2.208	86	2.576	B4	2.944	E2	3.312		
2B	1.848	59	2.216	87	2.584	B5	2.952	E3	3.320		
2C	1.856	5A	2.224	88	2.592	B6	2.960	E4	3.328		
2D	1.864	5B	2.232	89	2.600	B7	2.968	E5	3.336		

REGISTER MAPS (continued)

REG0x07: LDO4 Output Voltage Level Definition Register [Reset = 0xA2]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	LDO4_VOUT	10100010	R/W	Sets LDO4 regulation target voltage. Equation: V_{LDO4} = (1504 + 8 × *d*) × 1mV, where *d* is the decimal value of the register. See Table 4.

Table 4. LDO4 Output Voltage Level Definition

Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)
00	1.504	2E	1.872	5C	2.240	8A	2.608	B8	2.976	E6	3.344
01	1.512	2F	1.880	5D	2.248	8B	2.616	B9	2.984	E7	3.352
02	1.520	30	1.888	5E	2.256	8C	2.624	BA	2.992	E8	3.360
03	1.528	31	1.896	5F	2.264	8D	2.632	BB	3.000	E9	3.368
04	1.536	32	1.904	60	2.272	8E	2.640	BC	3.008	EA	3.376
05	1.544	33	1.912	61	2.280	8F	2.648	BD	3.016	EB	3.384
06	1.552	34	1.920	62	2.288	90	2.656	BE	3.024	EC	3.392
07	1.560	35	1.928	63	2.296	91	2.664	BF	3.032	ED	3.400
08	1.568	36	1.936	64	2.304	92	2.672	C0	3.040	EE	3.408
09	1.576	37	1.944	65	2.312	93	2.680	C1	3.048	EF	3.416
0A	1.584	38	1.952	66	2.320	94	2.688	C2	3.056	F0	3.424
0B	1.592	39	1.960	67	2.328	95	2.696	C3	3.064	F1	3.432
0C	1.600	3A	1.968	68	2.336	96	2.704	C4	3.072	F2	3.440
0D	1.608	3B	1.976	69	2.344	97	2.712	C5	3.080	F3	3.448
0E	1.616	3C	1.984	6A	2.352	98	2.720	C6	3.088	F4	3.456
0F	1.624	3D	1.992	6B	2.360	99	2.728	C7	3.096	F5	3.464
10	1.632	3E	2.000	6C	2.368	9A	2.736	C8	3.104	F6	3.472
11	1.640	3F	2.008	6D	2.376	9B	2.744	C9	3.112	F7	3.480
12	1.648	40	2.016	6E	2.384	9C	2.752	CA	3.120	F8	3.488
13	1.656	41	2.024	6F	2.392	9D	2.760	CB	3.128	F9	3.496
14	1.664	42	2.032	70	2.400	9E	2.768	CC	3.136	FA	3.504
15	1.672	43	2.040	71	2.408	9F	2.776	CD	3.144	FB	3.512
16	1.680	44	2.048	72	2.416	A0	2.784	CE	3.152	FC	3.520
17	1.688	45	2.056	73	2.424	A1	2.792	CF	3.160	FD	3.528
18	1.696	46	2.064	74	2.432	A2	2.800	D0	3.168	FE	3.536
19	1.704	47	2.072	75	2.440	A3	2.808	D1	3.176	FF	3.544
1A	1.712	48	2.080	76	2.448	A4	2.816	D2	3.184		
1B	1.720	49	2.088	77	2.456	A5	2.824	D3	3.192		
1C	1.728	4A	2.096	78	2.464	A6	2.832	D4	3.200		
1D	1.736	4B	2.104	79	2.472	A7	2.840	D5	3.208		
1E	1.744	4C	2.112	7A	2.480	A8	2.848	D6	3.216		
1F	1.752	4D	2.120	7B	2.488	A9	2.856	D7	3.224		
20	1.760	4E	2.128	7C	2.496	AA	2.864	D8	3.232		
21	1.768	4F	2.136	7D	2.504	AB	2.872	D9	3.240		
22	1.776	50	2.144	7E	2.512	AC	2.880	DA	3.248		
23	1.784	51	2.152	7F	2.520	AD	2.888	DB	3.256		
24	1.792	52	2.160	80	2.528	AE	2.896	DC	3.264		
25	1.800	53	2.168	81	2.536	AF	2.904	DD	3.272		
26	1.808	54	2.176	82	2.544	B0	2.912	DE	3.280		
27	1.816	55	2.184	83	2.552	B1	2.920	DF	3.288		
28	1.824	56	2.192	84	2.560	B2	2.928	E0	3.296		
29	1.832	57	2.200	85	2.568	B3	2.936	E1	3.304		
2A	1.840	58	2.208	86	2.576	B4	2.944	E2	3.312		
2B	1.848	59	2.216	87	2.584	B5	2.952	E3	3.320		
2C	1.856	5A	2.224	88	2.592	B6	2.960	E4	3.328		
2D	1.864	5B	2.232	89	2.600	B7	2.968	E5	3.336		

REGISTER MAPS (continued)

REG0x08: LDO5 Output Voltage Level Definition Register [Reset = 0xA2]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	LDO5_VOUT	10100010	R/W	Sets LDO5 regulation target voltage. Equation: V_{LDO5} = (1504 + 8 × *d*) × 1mV, where *d* is the decimal value of the register. See Table 5.

Table 5. LDO5 Output Voltage Level Definition

Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)
00	1.504	2E	1.872	5C	2.240	8A	2.608	B8	2.976	E6	3.344
01	1.512	2F	1.880	5D	2.248	8B	2.616	B9	2.984	E7	3.352
02	1.520	30	1.888	5E	2.256	8C	2.624	BA	2.992	E8	3.360
03	1.528	31	1.896	5F	2.264	8D	2.632	BB	3.000	E9	3.368
04	1.536	32	1.904	60	2.272	8E	2.640	BC	3.008	EA	3.376
05	1.544	33	1.912	61	2.280	8F	2.648	BD	3.016	EB	3.384
06	1.552	34	1.920	62	2.288	90	2.656	BE	3.024	EC	3.392
07	1.560	35	1.928	63	2.296	91	2.664	BF	3.032	ED	3.400
08	1.568	36	1.936	64	2.304	92	2.672	C0	3.040	EE	3.408
09	1.576	37	1.944	65	2.312	93	2.680	C1	3.048	EF	3.416
0A	1.584	38	1.952	66	2.320	94	2.688	C2	3.056	F0	3.424
0B	1.592	39	1.960	67	2.328	95	2.696	C3	3.064	F1	3.432
0C	1.600	3A	1.968	68	2.336	96	2.704	C4	3.072	F2	3.440
0D	1.608	3B	1.976	69	2.344	97	2.712	C5	3.080	F3	3.448
0E	1.616	3C	1.984	6A	2.352	98	2.720	C6	3.088	F4	3.456
0F	1.624	3D	1.992	6B	2.360	99	2.728	C7	3.096	F5	3.464
10	1.632	3E	2.000	6C	2.368	9A	2.736	C8	3.104	F6	3.472
11	1.640	3F	2.008	6D	2.376	9B	2.744	C9	3.112	F7	3.480
12	1.648	40	2.016	6E	2.384	9C	2.752	CA	3.120	F8	3.488
13	1.656	41	2.024	6F	2.392	9D	2.760	CB	3.128	F9	3.496
14	1.664	42	2.032	70	2.400	9E	2.768	CC	3.136	FA	3.504
15	1.672	43	2.040	71	2.408	9F	2.776	CD	3.144	FB	3.512
16	1.680	44	2.048	72	2.416	A0	2.784	CE	3.152	FC	3.520
17	1.688	45	2.056	73	2.424	A1	2.792	CF	3.160	FD	3.528
18	1.696	46	2.064	74	2.432	A2	2.800	D0	3.168	FE	3.536
19	1.704	47	2.072	75	2.440	A3	2.808	D1	3.176	FF	3.544
1A	1.712	48	2.080	76	2.448	A4	2.816	D2	3.184		
1B	1.720	49	2.088	77	2.456	A5	2.824	D3	3.192		
1C	1.728	4A	2.096	78	2.464	A6	2.832	D4	3.200		
1D	1.736	4B	2.104	79	2.472	A7	2.840	D5	3.208		
1E	1.744	4C	2.112	7A	2.480	A8	2.848	D6	3.216		
1F	1.752	4D	2.120	7B	2.488	A9	2.856	D7	3.224		
20	1.760	4E	2.128	7C	2.496	AA	2.864	D8	3.232		
21	1.768	4F	2.136	7D	2.504	AB	2.872	D9	3.240		
22	1.776	50	2.144	7E	2.512	AC	2.880	DA	3.248		
23	1.784	51	2.152	7F	2.520	AD	2.888	DB	3.256		
24	1.792	52	2.160	80	2.528	AE	2.896	DC	3.264		
25	1.800	53	2.168	81	2.536	AF	2.904	DD	3.272		
26	1.808	54	2.176	82	2.544	B0	2.912	DE	3.280		
27	1.816	55	2.184	83	2.552	B1	2.920	DF	3.288		
28	1.824	56	2.192	84	2.560	B2	2.928	E0	3.296		
29	1.832	57	2.200	85	2.568	B3	2.936	E1	3.304		
2A	1.840	58	2.208	86	2.576	B4	2.944	E2	3.312		
2B	1.848	59	2.216	87	2.584	B5	2.952	E3	3.320		
2C	1.856	5A	2.224	88	2.592	B6	2.960	E4	3.328		
2D	1.864	5B	2.232	89	2.600	B7	2.968	E5	3.336		

REGISTER MAPS (continued)

REG0x09: LDO6 Output Voltage Level Definition Register [Reset = 0xA2]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	LDO6_VOUT	10100010	R/W	Sets LDO6 regulation target voltage. Equation: V_{LDO6} = (1504 + 8 × *d*) × 1mV, where *d* is the decimal value of the register. See Table 6.

Table 6. LDO6 Output Voltage Level Definition

Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)
00	1.504	2E	1.872	5C	2.240	8A	2.608	B8	2.976	E6	3.344
01	1.512	2F	1.880	5D	2.248	8B	2.616	B9	2.984	E7	3.352
02	1.520	30	1.888	5E	2.256	8C	2.624	BA	2.992	E8	3.360
03	1.528	31	1.896	5F	2.264	8D	2.632	BB	3.000	E9	3.368
04	1.536	32	1.904	60	2.272	8E	2.640	BC	3.008	EA	3.376
05	1.544	33	1.912	61	2.280	8F	2.648	BD	3.016	EB	3.384
06	1.552	34	1.920	62	2.288	90	2.656	BE	3.024	EC	3.392
07	1.560	35	1.928	63	2.296	91	2.664	BF	3.032	ED	3.400
08	1.568	36	1.936	64	2.304	92	2.672	C0	3.040	EE	3.408
09	1.576	37	1.944	65	2.312	93	2.680	C1	3.048	EF	3.416
0A	1.584	38	1.952	66	2.320	94	2.688	C2	3.056	F0	3.424
0B	1.592	39	1.960	67	2.328	95	2.696	C3	3.064	F1	3.432
0C	1.600	3A	1.968	68	2.336	96	2.704	C4	3.072	F2	3.440
0D	1.608	3B	1.976	69	2.344	97	2.712	C5	3.080	F3	3.448
0E	1.616	3C	1.984	6A	2.352	98	2.720	C6	3.088	F4	3.456
0F	1.624	3D	1.992	6B	2.360	99	2.728	C7	3.096	F5	3.464
10	1.632	3E	2.000	6C	2.368	9A	2.736	C8	3.104	F6	3.472
11	1.640	3F	2.008	6D	2.376	9B	2.744	C9	3.112	F7	3.480
12	1.648	40	2.016	6E	2.384	9C	2.752	CA	3.120	F8	3.488
13	1.656	41	2.024	6F	2.392	9D	2.760	CB	3.128	F9	3.496
14	1.664	42	2.032	70	2.400	9E	2.768	CC	3.136	FA	3.504
15	1.672	43	2.040	71	2.408	9F	2.776	CD	3.144	FB	3.512
16	1.680	44	2.048	72	2.416	A0	2.784	CE	3.152	FC	3.520
17	1.688	45	2.056	73	2.424	A1	2.792	CF	3.160	FD	3.528
18	1.696	46	2.064	74	2.432	A2	2.800	D0	3.168	FE	3.536
19	1.704	47	2.072	75	2.440	A3	2.808	D1	3.176	FF	3.544
1A	1.712	48	2.080	76	2.448	A4	2.816	D2	3.184		
1B	1.720	49	2.088	77	2.456	A5	2.824	D3	3.192		
1C	1.728	4A	2.096	78	2.464	A6	2.832	D4	3.200		
1D	1.736	4B	2.104	79	2.472	A7	2.840	D5	3.208		
1E	1.744	4C	2.112	7A	2.480	A8	2.848	D6	3.216		
1F	1.752	4D	2.120	7B	2.488	A9	2.856	D7	3.224		
20	1.760	4E	2.128	7C	2.496	AA	2.864	D8	3.232		
21	1.768	4F	2.136	7D	2.504	AB	2.872	D9	3.240		
22	1.776	50	2.144	7E	2.512	AC	2.880	DA	3.248		
23	1.784	51	2.152	7F	2.520	AD	2.888	DB	3.256		
24	1.792	52	2.160	80	2.528	AE	2.896	DC	3.264		
25	1.800	53	2.168	81	2.536	AF	2.904	DD	3.272		
26	1.808	54	2.176	82	2.544	B0	2.912	DE	3.280		
27	1.816	55	2.184	83	2.552	B1	2.920	DF	3.288		
28	1.824	56	2.192	84	2.560	B2	2.928	E0	3.296		
29	1.832	57	2.200	85	2.568	B3	2.936	E1	3.304		
2A	1.840	58	2.208	86	2.576	B4	2.944	E2	3.312		
2B	1.848	59	2.216	87	2.584	B5	2.952	E3	3.320		
2C	1.856	5A	2.224	88	2.592	B6	2.960	E4	3.328		
2D	1.864	5B	2.232	89	2.600	B7	2.968	E5	3.336		

REGISTER MAPS (continued)

REG0x0A: LDO7 Output Voltage Level Definition Register [Reset = 0xA2]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	LDO7_VOUT	10100010	R/W	Sets LDO7 regulation target voltage. Equation: V_{LDO7} = (1504 + 8 × *d*) × 1mV, where *d* is the decimal value of the register. See Table 7.

Table 7. LDO7 Output Voltage Level Definition

Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)	Hex	V_{OUT} (V)
00	1.504	2E	1.872	5C	2.240	8A	2.608	B8	2.976	E6	3.344
01	1.512	2F	1.880	5D	2.248	8B	2.616	B9	2.984	E7	3.352
02	1.520	30	1.888	5E	2.256	8C	2.624	BA	2.992	E8	3.360
03	1.528	31	1.896	5F	2.264	8D	2.632	BB	3.000	E9	3.368
04	1.536	32	1.904	60	2.272	8E	2.640	BC	3.008	EA	3.376
05	1.544	33	1.912	61	2.280	8F	2.648	BD	3.016	EB	3.384
06	1.552	34	1.920	62	2.288	90	2.656	BE	3.024	EC	3.392
07	1.560	35	1.928	63	2.296	91	2.664	BF	3.032	ED	3.400
08	1.568	36	1.936	64	2.304	92	2.672	C0	3.040	EE	3.408
09	1.576	37	1.944	65	2.312	93	2.680	C1	3.048	EF	3.416
0A	1.584	38	1.952	66	2.320	94	2.688	C2	3.056	F0	3.424
0B	1.592	39	1.960	67	2.328	95	2.696	C3	3.064	F1	3.432
0C	1.600	3A	1.968	68	2.336	96	2.704	C4	3.072	F2	3.440
0D	1.608	3B	1.976	69	2.344	97	2.712	C5	3.080	F3	3.448
0E	1.616	3C	1.984	6A	2.352	98	2.720	C6	3.088	F4	3.456
0F	1.624	3D	1.992	6B	2.360	99	2.728	C7	3.096	F5	3.464
10	1.632	3E	2.000	6C	2.368	9A	2.736	C8	3.104	F6	3.472
11	1.640	3F	2.008	6D	2.376	9B	2.744	C9	3.112	F7	3.480
12	1.648	40	2.016	6E	2.384	9C	2.752	CA	3.120	F8	3.488
13	1.656	41	2.024	6F	2.392	9D	2.760	CB	3.128	F9	3.496
14	1.664	42	2.032	70	2.400	9E	2.768	CC	3.136	FA	3.504
15	1.672	43	2.040	71	2.408	9F	2.776	CD	3.144	FB	3.512
16	1.680	44	2.048	72	2.416	A0	2.784	CE	3.152	FC	3.520
17	1.688	45	2.056	73	2.424	A1	2.792	CF	3.160	FD	3.528
18	1.696	46	2.064	74	2.432	A2	2.800	D0	3.168	FE	3.536
19	1.704	47	2.072	75	2.440	A3	2.808	D1	3.176	FF	3.544
1A	1.712	48	2.080	76	2.448	A4	2.816	D2	3.184		
1B	1.720	49	2.088	77	2.456	A5	2.824	D3	3.192		
1C	1.728	4A	2.096	78	2.464	A6	2.832	D4	3.200		
1D	1.736	4B	2.104	79	2.472	A7	2.840	D5	3.208		
1E	1.744	4C	2.112	7A	2.480	A8	2.848	D6	3.216		
1F	1.752	4D	2.120	7B	2.488	A9	2.856	D7	3.224		
20	1.760	4E	2.128	7C	2.496	AA	2.864	D8	3.232		
21	1.768	4F	2.136	7D	2.504	AB	2.872	D9	3.240		
22	1.776	50	2.144	7E	2.512	AC	2.880	DA	3.248		
23	1.784	51	2.152	7F	2.520	AD	2.888	DB	3.256		
24	1.792	52	2.160	80	2.528	AE	2.896	DC	3.264		
25	1.800	53	2.168	81	2.536	AF	2.904	DD	3.272		
26	1.808	54	2.176	82	2.544	B0	2.912	DE	3.280		
27	1.816	55	2.184	83	2.552	B1	2.920	DF	3.288		
28	1.824	56	2.192	84	2.560	B2	2.928	E0	3.296		
29	1.832	57	2.200	85	2.568	B3	2.936	E1	3.304		
2A	1.840	58	2.208	86	2.576	B4	2.944	E2	3.312		
2B	1.848	59	2.216	87	2.584	B5	2.952	E3	3.320		
2C	1.856	5A	2.224	88	2.592	B6	2.960	E4	3.328		
2D	1.864	5B	2.232	89	2.600	B7	2.968	E5	3.336		

REGISTER MAPS (continued)

REG0x0B: Power Sequence Setting Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved
D[5:3]	LDO2_SEQ	000	R/W	There are 7 time slots defined as following table. The power-up sequence starts from slot1 to slot7, and shutdown starts from slot7 to slot1. Power-up and shutdown of LDO2 regulator can be set at any one of the slots. 000 = Controlled by I^2C register 0x03[1] (default) 001 = Slot1 010 = Slot2 011 = Slot3 100 = Slot4 101 = Slot5 110 = Slot6 111 = Slot7
D[2:0]	LDO1_SEQ	000	R/W	There are 7 time slots defined as following table. The power-up sequence starts from slot1 to slot7, and shutdown start from slot7 to slot1. Power-up and shutdown of LDO1 regulator can be set at any one of the slots. 000 =Controlled by I^2C register 0x03[0] (default) 001 = Slot1 010 = Slot2 011 = Slot3 100 = Slot4 101 = Slot5 110 = Slot6 111 = Slot7

REG0x0C: Power Sequence Setting Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved
D[5:3]	LDO4_SEQ	000	R/W	There are 7 time slots defined as following table. The power-up sequence starts from slot1 to slot7, and shutdown starts from slot7 to slot1. Power-up and shutdown of LDO4 regulator can be set at any one of the slots. 000 = Controlled by I^2C register 0x03[3] (default) 001 = Slot1 010 = Slot2 011 = Slot3 100 = Slot4 101 = Slot5 110 = Slot6 111 = Slot7
D[2:0]	LDO3_SEQ	000	R/W	There are 7 time slots defined as following table. The power-up sequence starts from slot1 to slot7, and shutdown starts from slot7 to slot1. Power-up and shutdown of LDO3 regulator can be set at any one of the slots. 000 = Controlled by I^2C register 0x03[2] (default) 001 = Slot1 010 = Slot2 011 = Slot3 100 = Slot4 101 = Slot5 110 = Slot6 111 = Slot7

REGISTER MAPS (continued)

REG0x0D: Power Sequence Setting Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved
D[5:3]	LDO6_SEQ	000	R/W	There are 7 time slots defined as following table. The power-up sequence starts from slot1 to slot7, and shutdown starts from slot7 to slot1. Power-up and shutdown of LDO6 regulator can be set at any one of the slots. 000 = Controlled by I^2C register 0x03[5] (default) 001 = Slot1 010 = Slot2 011 = Slot3 100 = Slot4 101 = Slot5 110 = Slot6 111 = Slot7
D[2:0]	LDO5_SEQ	000	R/W	There are 7 time slots defined as following table. The power-up sequence starts from slot1 to slot7, and shutdown starts from slot7 to slot1. Power-up and shutdown of LDO3 regulator can be set at any one of the slots. 000 = Controlled by I^2C register 0x03[4] (default) 001 = Slot1 010 = Slot2 011 = Slot3 100 = Slot4 101 = Slot5 110 = Slot6 111 = Slot7

REG0x0E: Power Sequence Setting Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:3]	Reserved	00000	R	Reserved
D[2:0]	LDO7_SEQ	000	R/W	There are 7 time slots defined as following table. The power-up sequence starts from slot1 to slot7, and shutdown starts from slot7 to slot1. Power-up and shutdown of LDO7 regulator can be set at any one of the slots. 000 = Controlled by I^2C register 0x03[6] (default) 001 = Slot1 010 = Slot2 011 = Slot3 100 = Slot4 101 = Slot5 110 = Slot6 111 = Slot7

REGISTER MAPS (continued)

REG0x0F: Sequence Control Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	SEQ_SPEED[1:0]	00	R/W	SEQ_SPEED Define the slot period as following: 00 = 2.00ms (default) 01 = 1.00ms 10 = 0.50ms 11 = 0.25ms
D[5:4]	SEQ_CONTROL[1:0]	00	WCLR	Enables power-up or shutdown of SEQ. Write and clear: 00 = Default 01 = Power-Up 10 = Shutdown 11 = Ignored
D[3]	SEQ_ON	0	R	Indicates the activation signal of SEQ. Read only: 0 = Shutdown (default). Indicates that the sequencing is not in process. 1 = Power-Up. Indicates that the sequencing is executing and somewhere between the start of slot 1 and the end of slot 7.
D[2:0]	SEQ_COUNT[2:0]	000	R	Indicates the slot number of SEQ at the moment. Read only: 000 = No LDO starts (default) 001 = Slot1 starts 010 = Slot2 starts 011 = Slot3 starts 100 = Slot4 starts 101 = Slot5 starts 110 = Slot6 starts 111 = Slot7 starts

REG0x10: Discharge Resistor Selection Register [Reset = 0x7F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved
D[6]	LDO7_DISCH_EN	1	R/W	LDO7 Discharge Resistor Enable/Disable Control 0 = Disable 1 = Enable (default)
D[5]	LDO6_DISCH_EN	1	R/W	LDO6 Discharge Resistor Enable/Disable Control 0 = Disable 1 = Enable (default)
D[4]	LDO5_DISCH_EN	1	R/W	LDO5 Discharge Resistor Enable/Disable Control 0 = Disable 1 = Enable (default)
D[3]	LDO4_DISCH_EN	1	R/W	LDO4 Discharge Resistor Enable/Disable Control 0 = Disable 1 = Enable (default)
D[2]	LDO3_DISCH_EN	1	R/W	LDO3 Discharge Resistor Enable/Disable Control 0 = Disable 1 = Enable (default)
D[1]	LDO2_DISCH_EN	1	R/W	LDO2 Discharge Resistor Enable/Disable Control 0 = Disable 1 = Enable (default)
D[0]	LDO1_DISCH_EN	1	R/W	LDO1 Discharge Resistor Enable/Disable Control 0 = Disable 1 = Enable (default)

REGISTER MAPS (continued)

REG0x11: Reset Register [Reset = 0x06]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	SOFT_RESET[3:0]	0000	WCLR	Writing a “1011” begins a soft reset of the device I²C registers to their default values. This bit is cleared upon the execution of the reset function. Any other value than “1011” will be ignored.
D[3]	Reserved	0	R	Reserved
D[2:1]	OCP_TIMER[1:0]	11	R/W	Option bits to control the length of the deglitch timer for current limit on all LDOs before a fault is triggered. 00 = 125µs 01 = 250µs 10 = 500µs 11 = 1ms (default)
D[0]	FLT_SD_B	0	R/W	LDO shuts down if a UVP or OCP event occurs or if the LDO’s input VIN12, VIN34, VIN5, VIN6 or VIN7 has a UVLO event. LDO does not shut down if a UVP or OCP event occurs. If the LDO’s input VIN12, VIN34, VIN5, VIN6 or VIN7 has a UVLO event, the associated LDO will shut down until the supply returns, but the fault will not be counted. 0 = Shutdown (default) 1 = Power-Up NOTE: If this bit function is desired, FLT_SD_B should be set to “1” prior to enabling any LDOs after a Power-on reset.

REG0x12: I2C_ADDR Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	INT_LEVEL_SEL	0	R/W	INT Push-Pull Output Voltage Level, only for D[6] = 0. 0 = 1.8V (default) 1 = 1.2V
D[6]	INT_MODE_SEL	0	R/W	INT Mode Selection 0 = Push-pull on INT pin (default) 1 = Open drain on INT pin
D[5:2]	Reserved	0000	R	Reserved
D[1:0]	I2C_ADDR_SEL[1:0]	01	R/W	I²C Address Settings 00 = 0x20 01 = 0x35 (default) 10 = 0x61 11 = 0x72

REGISTER MAPS (continued)

REG0x15: UVP Interrupt Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved
D[6]	LDO7_UVP_INT	0	RCLR	LDO7 UVP Interrupt 0 = Clear (default) 1 = Under-voltage event occurred on LDO7 output.
D[5]	LDO6_UVP_INT	0	RCLR	LDO6 UVP Interrupt 0 = Clear (default) 1 = Under-voltage event occurred on LDO6 output.
D[4]	LDO5_UVP_INT	0	RCLR	LDO5 UVP Interrupt 0 = Clear (default) 1 = Under-voltage event occurred on LDO5 output.
D[3]	LDO4_UVP_INT	0	RCLR	LDO4 UVP Interrupt 0 = Clear (default) 1 = Under-voltage event occurred on LDO4 output.
D[2]	LDO3_UVP_INT	0	RCLR	LDO3 UVP Interrupt 0 = Clear (default) 1 = Under-voltage event occurred on LDO3 output.
D[1]	LDO2_UVP_INT	0	RCLR	LDO2 UVP Interrupt 0 = Clear (default) 1 = Under-voltage event occurred on LDO2 output.
D[0]	LDO1_UVP_INT	0	RCLR	LDO1 UVP Interrupt 0 = Clear (default) 1 = Under-voltage event occurred on LDO1 output.

REG0x16: OCP Interrupt Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved
D[6]	LDO7_OCP_INT	0	RCLR	LDO7 OCP Interrupt 0 = Clear (default) 1 = Over-current event occurred on LDO7 output.
D[5]	LDO6_OCP_INT	0	RCLR	LDO6 OCP Interrupt 0 = Clear (default) 1 = Over-current event occurred on LDO6 output.
D[4]	LDO5_OCP_INT	0	RCLR	LDO5 OCP Interrupt 0 = Clear (default) 1 = Over-current event occurred on LDO5 output.
D[3]	LDO4_OCP_INT	0	RCLR	LDO4 OCP Interrupt 0 = Clear (default) 1 = Over-current event occurred on LDO4 output.
D[2]	LDO3_OCP_INT	0	RCLR	LDO3 OCP Interrupt 0 = Clear (default) 1 = Over-current event occurred on LDO3 output.
D[1]	LDO2_OCP_INT	0	RCLR	LDO2 OCP Interrupt 0 = Clear (default) 1 = Over-current event occurred on LDO2 output.
D[0]	LDO1_OCP_INT	0	RCLR	LDO1 OCP Interrupt 0 = Clear (default) 1 = Over-current event occurred on LDO1 output.

REGISTER MAPS (continued)

REG0x17: TSD and UVLO Interrupt Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	TSD_INT	0	RCLR	Thermal Shutdown Interrupt 0 = Clear (default) 1 = A thermal shutdown event occurred or that the temperature has fallen below the hysteresis level.
D[6]	TSD_WRN_INT	0	RCLR	Thermal Warning Interrupt 0 = Clear (default) 1 = Thermal shutdown warning threshold was surpassed or that the temperature has fallen below the hysteresis level.
D[5]	VSYS_UVLO_INT	0	RCLR	VSYS Under-Voltage-Lockout Interrupt 0 = Clear (default) 1 = VSYS fell below the UVLO falling threshold or that VSYS have risen above the UVLO rising threshold after a UVLO fault. Reading the associated status bit provides present state of the input voltage.
D[4]	VIN7_UVLO_INT	0	RCLR	VIN7 Under-Voltage-Lockout Interrupt 0 = Clear (default) 1 = VIN7 fell below the UVLO falling threshold while LDO7 was enabled or that VIN7 has risen above the UVLO rising threshold after a UVLO fault. Reading the associated status bit provides present state of the input voltage.
D[3]	VIN6_UVLO_INT	0	RCLR	VIN6 Under-Voltage-Lockout Interrupt 0 = Clear (default) 1 = VIN6 fell below the UVLO falling threshold while LDO6 was enabled or that VIN6 has risen above the UVLO rising threshold after a UVLO fault. Reading the associated status bit provides present state of the input voltage.
D[2]	VIN5_UVLO_INT	0	RCLR	VIN5 Under-Voltage-Lockout Interrupt 0 = Clear (default) 1 = VIN5 fell below the UVLO falling threshold while LDO5 was enabled or that VIN5 has risen above the UVLO rising threshold after a UVLO fault. Reading the associated status bit provides present state of the input voltage.
D[1]	VIN34_UVLO_INT	0	RCLR	VIN34 Under-Voltage-Lockout Interrupt 0 = Clear (default) 1 = VIN34 fell below the UVLO falling threshold while LDO3 or LDO4 were enabled or that VIN34 has risen above the rising UVLO thresholds after a UVLO fault. Reading the associated status bit provides present state of the input voltage.
D[0]	VIN12_UVLO_INT	0	RCLR	VIN12 Under-Voltage-Lockout Interrupt 0 = Clear (default) 1 = VIN12 fell below the UVLO falling threshold while LDO1 or LDO2 were enabled or that VIN12 has risen above the UVLO rising threshold after a UVLO fault. Reading the associated status bit provides present state of the input voltage.

REGISTER MAPS (continued)

REG0x18: UVP Status Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved
D[6]	LDO7_UVP_STAT	0	R	LDO7 UVP Status 0 = Normal operation (default) 1 = An under-voltage condition exists on LDO7 output.
D[5]	LDO6_UVP_STAT	0	R	LDO6 UVP Status 0 = Normal operation (default) 1 = An under-voltage condition exists on LDO6 output.
D[4]	LDO5_UVP_STAT	0	R	LDO5 UVP Status 0 = Normal operation (default) 1 = An under-voltage condition exists on LDO5 output.
D[3]	LDO4_UVP_STAT	0	R	LDO4 UVP Status 0 = Normal operation (default) 1 = An under-voltage condition exists on LDO4 output.
D[2]	LDO3_UVP_STAT	0	R	LDO3 UVP Status 0 = Normal operation (default) 1 = An under-voltage condition exists on LDO3 output.
D[1]	LDO2_UVP_STAT	0	R	LDO2 UVP Status 0 = Normal operation (default) 1 = An under-voltage condition exists on LDO2 output.
D[0]	LDO1_UVP_STAT	0	R	LDO1 UVP Status 0 = Normal operation (default) 1 = An under-voltage condition exists on LDO1 output.

REG0x19: OCP Status Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved
D[6]	LDO7_OCP_STAT	0	R	LDO7 OCP Status 0 = Normal operation (default) 1 = An over-current condition exists on LDO7 output.
D[5]	LDO6_OCP_STAT	0	R	LDO6 OCP Status 0 = Normal operation (default) 1 = An over-current condition exists on LDO6 output.
D[4]	LDO5_OCP_STAT	0	R	LDO5 OCP Status 0 = Normal operation (default) 1 = An over-current condition exists on LDO5 output.
D[3]	LDO4_OCP_STAT	0	R	LDO4 OCP Status 0 = Normal operation (default) 1 = An over-current condition exists on LDO4 output.
D[2]	LDO3_OCP_STAT	0	R	LDO3 OCP Status 0 = Normal operation (default) 1 = An over-current condition exists on LDO3 output.
D[1]	LDO2_OCP_STAT	0	R	LDO2 OCP Status 0 = Normal operation (default) 1 = An over-current condition exists on LDO2 output.
D[0]	LDO1_OCP_STAT	0	R	LDO1 OCP Status 0 = Normal operation (default) 1 = An over-current condition exists on LDO1 output.

REGISTER MAPS (continued)

REG0x1A: TSD and UVLO Status Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	TSD_STAT	0	R	Thermal Shutdown Status 0 = Normal operation (default) 1 = Device is in thermal shutdown.
D[6]	TSD_WRN_STAT	0	R	Thermal Warning Status 0 = Normal operation (default) 1 = The temperature is above the thermal warning level.
D[5]	VSYS_UVLO_STAT	0	R	VSYS Under-Voltage-Lockout Status 0 = Normal operation (default) 1 = VSYS is below the UVLO threshold.
D[4]	VIN7_UVLO_STAT	0	R	VIN7 Under-Voltage-Lockout Status 0 = Normal operation (default) 1 = VIN7 is below the UVLO threshold while LDO7 is enabled.
D[3]	VIN6_UVLO_STAT	0	R	VIN6 Under-Voltage-Lockout Status 0 = Normal operation (default) 1 = VIN6 is below the UVLO threshold while LDO6 is enabled.
D[2]	VIN5_UVLO_STAT	0	R	VIN5 Under-Voltage-Lockout Status 0 = Normal operation (default) 1 = VIN5 is below the UVLO threshold while LDO5 is enabled.
D[1]	VIN34_UVLO_STAT	0	R	VIN34 Under-Voltage-Lockout Status 0 = Normal operation (default) 1 = VIN34 is below the UVLO threshold while LDO3 or LDO4 are enabled.
D[0]	VIN12_UVLO_STAT	0	R	VIN12 Under-Voltage-Lockout Status 0 = Normal operation (default) 1 = VIN12 is below the UVLO threshold while LDO1 or LDO2 are enabled.

REG0x1B: Output Suspended Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	CHIP_SUSD	0	R	Chip Suspension 0 = Chip in normal state (default) 1 = The entire chip has been suspended due to the global fault condition.
D[6]	LDO7_SUSD	0	R	LDO7 Output Suspended 0 = LDO7 in normal state (default) 1 = LDO7 has been suspended due to the fault condition.
D[5]	LDO6_SUSD	0	R	LDO6 Output Suspended 0 = LDO6 in normal state (default) 1 = LDO6 has been suspended due to the fault condition.
D[4]	LDO5_SUSD	0	R	LDO5 Output Suspended 0 = LDO5 in normal state (default) 1 = LDO5 has been suspended due to the fault condition.
D[3]	LDO4_SUSD	0	R	LDO4 Output Suspended 0 = LDO4 in normal state (default) 1 = LDO4 has been suspended due to the fault condition.
D[2]	LDO3_SUSD	0	R	LDO3 Output Suspended 0 = LDO3 in normal state (default) 1 = LDO3 has been suspended due to the fault condition.
D[1]	LDO2_SUSD	0	R	LDO2 Output Suspended 0 = LDO2 in normal state (default) 1 = LDO2 has been suspended due to the fault condition.
D[0]	LDO1_SUSD	0	R	LDO1 Output Suspended 0 = LDO1 in normal state (default) 1 = LDO1 has been suspended due to the fault condition.

REGISTER MAPS (continued)

REG0x1C: UVP Mask Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved
D[6]	MASK_LDO7_UVP	0	R/W	LDO7 UVP MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO7 under-voltage interrupt occurs.
D[5]	MASK_LDO6_UVP	0	R/W	LDO6 UVP MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO6 under-voltage interrupt occurs.
D[4]	MASK_LDO5_UVP	0	R/W	LDO5 UVP MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO5 under-voltage interrupt occurs.
D[3]	MASK_LDO4_UVP	0	R/W	LDO4 UVP MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO4 under-voltage interrupt occurs.
D[2]	MASK_LDO3_UVP	0	R/W	LDO3 UVP MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO3 under-voltage interrupt occurs.
D[1]	MASK_LDO2_UVP	0	R/W	LDO2 UVP MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO2 under-voltage interrupt occurs.
D[0]	MASK_LDO1_UVP	0	R/W	LDO1 UVP MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO1 under-voltage interrupt occurs.

REG0x1D: OCP Mask Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved
D[6]	MASK_LDO7_OCP	0	R/W	LDO7 OCP Mask 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO7 over-current interrupt occurs.
D[5]	MASK_LDO6_OCP	0	R/W	LDO6 OCP Mask 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO6 over-current interrupt occurs.
D[4]	MASK_LDO5_OCP	0	R/W	LDO5 OCP Mask 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO5 over-current interrupt occurs.
D[3]	MASK_LDO4_OCP	0	R/W	LDO4 OCP Mask 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO4 over-current interrupt occurs.
D[2]	MASK_LDO3_OCP	0	R/W	LDO3 OCP Mask 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO3 over-current interrupt occurs.
D[1]	MASK_LDO2_OCP	0	R/W	LDO2 OCP Mask 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO2 over-current interrupt occurs.
D[0]	MASK_LDO1_OCP	0	R/W	LDO1 OCP Mask 0 = No masking of interrupt (default) 1 = INT pin will not change state when LDO1 over-current interrupt occurs.

REGISTER MAPS (continued)

REG0x1E: TSD and UVLO Mask Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	MASK_TSD	0	R/W	Thermal Shutdown MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when a thermal shutdown interrupt occurs.
D[6]	MASK_TSD_WRN	0	R/W	Thermal Warning MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when a thermal warning interrupt occurs.
D[5]	MASK_VSYS_UVLO	0	R/W	VSYS UVLO MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when VSYS input power under-voltage interrupt occurs.
D[4]	MASK_VIN7_UVLO	0	R/W	VIN7 UVLO MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when VIN7 input power under-voltage interrupt occurs.
D[3]	MASK_VIN6_UVLO	0	R/W	VIN6 UVLO MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when VIN6 input power under-voltage interrupt occurs.
D[2]	MASK_VIN5_UVLO	0	R/W	VIN5 UVLO MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when VIN5 input power under-voltage interrupt occurs.
D[1]	MASK_VIN34_UVLO	0	R/W	VIN34 UVLO MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when VIN34 input power under-voltage interrupt occurs.
D[0]	MASK_VIN12_UVLO	0	R/W	VIN12 UVLO MASK 0 = No masking of interrupt (default) 1 = INT pin will not change state when VIN12 input power under-voltage interrupt occurs.

REG0x1F: EXTRA Output Voltage Configuration Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000000	R	Reserved
D[1]	LDO7_1V2	0	R/W	LDO7 OUTPUT Voltage 0 = LDO7 output voltage is configured by LDO7 Output Level Definition Register. (REG0x0A) (default) 1 = Force LDO7 output voltage level to 1.2V regardless of LDO7 Output Level Definition Register setting.
D[0]	LDO5_1V2	0	R/W	LDO5 OUTPUT Voltage 0 = LDO5 output voltage is configured by LDO5 Output Level Definition Register. (REG0x08) (default) 1 = Force LDO5 output voltage level to 1.2V regardless of LDO5 Output Level Definition Register setting.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JANUARY 2025 – REV.A to REV.A.1 **Page**

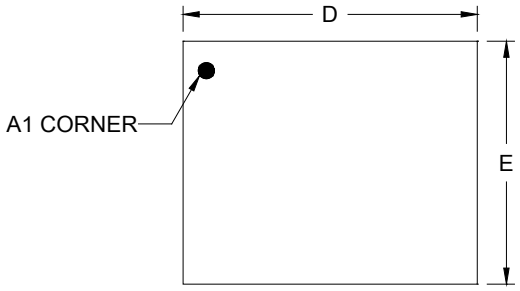
Updated Electrical Characteristics section and Communication Characteristics 9, 10

Changes from Original (DECEMBER 2024) to REV.A **Page**

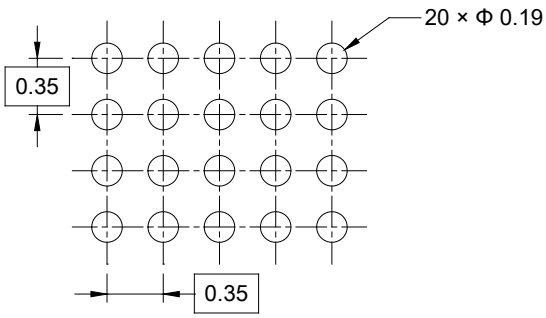
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

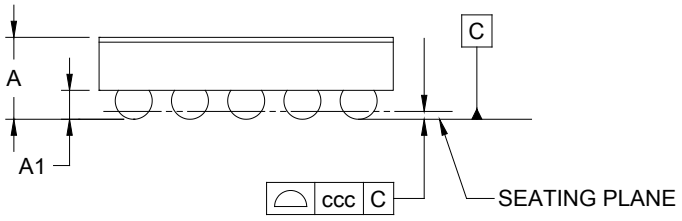
WLCSP-1.83×1.51-20B



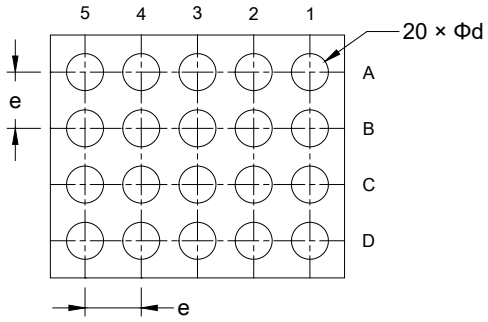
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



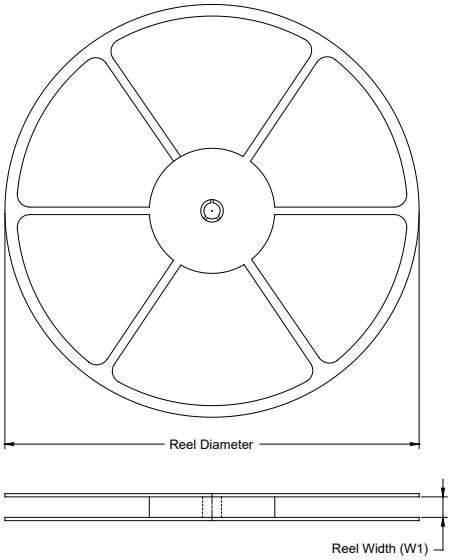
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.550
A1	0.160	-	0.200
D	1.801	-	1.861
E	1.482	-	1.542
d	0.200	-	0.260
e	0.350 BSC		
ccc	0.050		

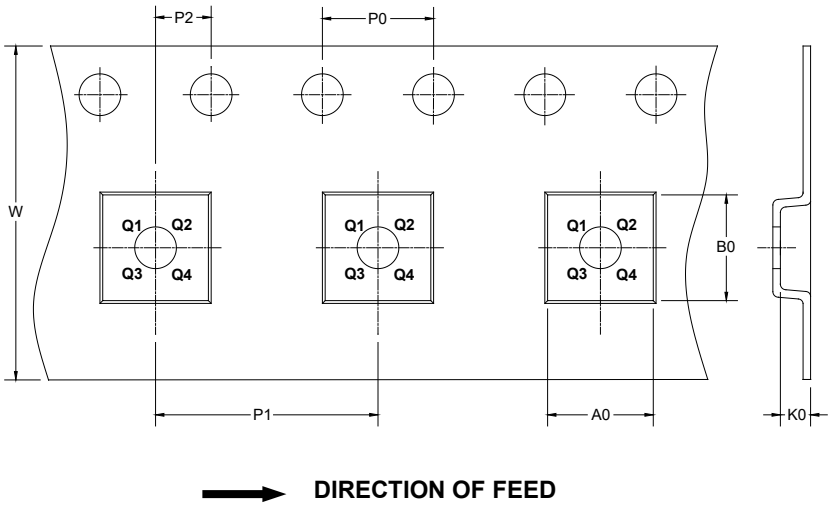
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



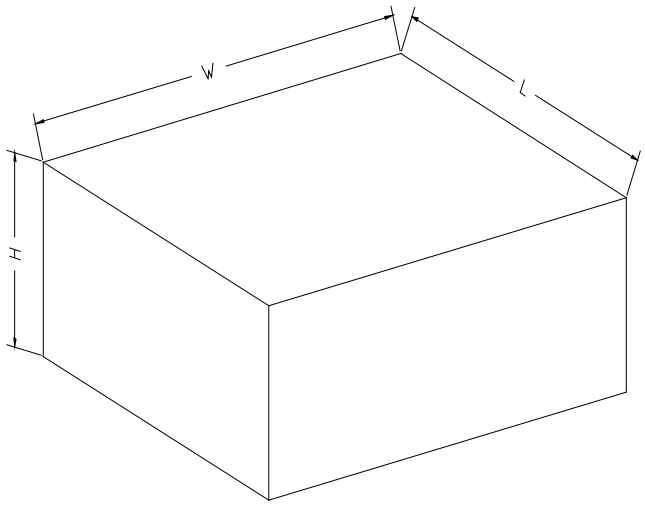
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.83×1.51-20B	7"	9.5	1.65	2.00	0.65	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002