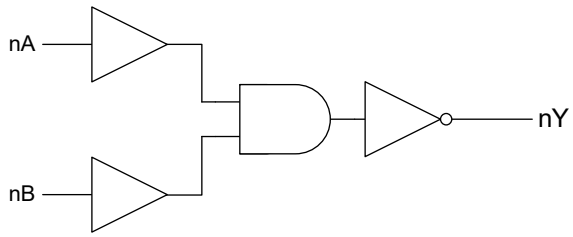
74AHC00
Quadruple 2-Input Positive-NAND Gate

GENERAL DESCRIPTION

The 74AHC00 is a quadruple 2-input positive-NAND gate. The supply voltage can range from 2.0V to 5.5V. The device implements the Boolean function $Y = \overline{A}+\overline{B}$ or $Y = \overline{A \times B}$ in positive logic.

The 74AHC00 is available in Green TSSOP-14 and SOIC-14 packages. It operates over an ambient temperature range of -40℃ to +125℃.

LOGIC DIAGRAM



APPLICATIONS

Industrial Equipment
Medical Devices
Telecom Equipment
Computing Devices

FEATURES

- **Wide Supply Voltage Range: 2.0V to 5.5V**
- **Inputs Accept Voltages Higher than the Supply Voltage and up to 5.5V**
- **+8mA/-8mA Output Current**
- **Low Power Consumption: I_{CC} = 0.1μA (TYP)**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TSSOP-14 and SOIC-14 Packages**

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
H	H	L
L	*X*	H
X	L	H

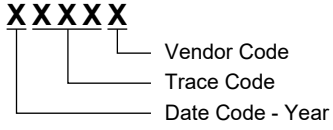
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74AHC00	TSSOP-14	-40℃ to +125℃	74AHC00XTS14G/TR	74AHC00 XTS14 XXXXX	Tape and Reel, 4000
	SOIC-14	-40℃ to +125℃	74AHC00XS14G/TR	74AHC00XS14 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -0.5V to 7.0V
Input Voltage, V_I (1) ..... -0.5V to 7.0V
Output Voltage, V_O (1) ..... -0.5V to MIN(7.0V, V_{CC} + 0.5V)
Input Clamp Current, I_{IK} (V_I < 0V) ..... -20mA
Output Clamp Current, I_{OK} (V_O < 0V or V_O > V_{CC}) ..... ±20mA
Continuous Output Current, I_O (V_O = 0V to V_{CC}) ..... ±25mA
Continuous Current through V_{CC} or GND ..... ±50mA
Junction Temperature (2) ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (3) (4)
HBM ..... ±6000V
CDM ..... ±1000V

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

3. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

4. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... 2.0V to 5.5V
Input Voltage, V_I ..... 0V to 5.5V
Output Voltage, V_O ..... 0V to V_{CC}
Output Current, I_O ..... ±8mA
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 3.3V ± 0.3V ..... 100ns/V (MAX)
V_{CC} = 5V ± 0.5V ..... 20ns/V (MAX)
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

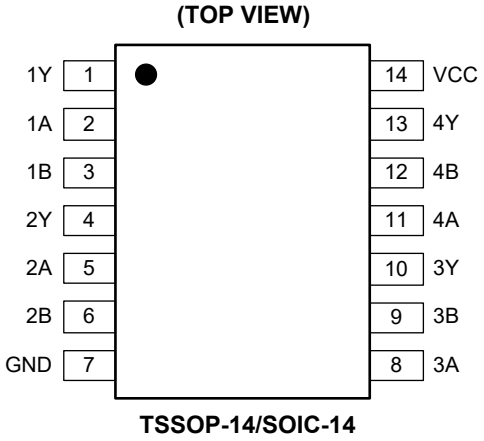
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 4, 10, 13	1Y, 2Y, 3Y, 4Y	Data Outputs.
2, 5, 8, 11	1A, 2A, 3A, 4A	Data Inputs.
3, 6, 9, 12	1B, 2B, 3B, 4B	Data Inputs.
7	GND	Ground.
14	VCC	Power Supply Pin.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 2.0V	Full	1.5			V
		V_{CC} = 3.0V	Full	2.1			
		V_{CC} = 5.5V	Full	3.85			
Low-Level Input Voltage	V_{IL}	V_{CC} = 2.0V	Full			0.5	V
		V_{CC} = 3.0V	Full			0.9	
		V_{CC} = 5.5V	Full			1.65	
High-Level Output Voltage	V_{OH}	V_{CC} = 2.0V, I_{OH} = -50μA	Full	1.9	1.99		V
		V_{CC} = 3.0V, I_{OH} = -50μA	Full	2.9	2.99		
		V_{CC} = 4.5V, I_{OH} = -50μA	Full	4.4	4.49		
		V_{CC} = 3.0V, I_{OH} = -4mA	Full	2.48	2.85		
		V_{CC} = 4.5V, I_{OH} = -8mA	Full	3.8	4.29		
Low-Level Output Voltage	V_{OL}	V_{CC} = 2.0V, I_{OL} = 50μA	Full		0.01	0.1	V
		V_{CC} = 3.0V, I_{OL} = 50μA	Full		0.01	0.1	
		V_{CC} = 4.5V, I_{OL} = 50μA	Full		0.01	0.1	
		V_{CC} = 3.0V, I_{OL} = 4mA	Full		0.12	0.5	
		V_{CC} = 4.5V, I_{OL} = 8mA	Full		0.2	0.5	
Input Leakage Current	I_I	V_{CC} = 0V to 5.5V, V_I = 5.5V or GND	Full		±0.1	±1	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, V_I = V_{CC} or GND, I_O = 0A	Full		0.1	10	μA
Input Capacitance	C_I	V_{CC} = 5.0V, V_I = V_{CC} or GND	+25℃		4		pF

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Low to High Propagation Delay	t_{PLH}	nA or nB to nY, see Figure 2	V_{CC} = 3.0V to 3.6V, C_L = 15pF	Full	0.5	5.0	8.8	ns
			V_{CC} = 3.0V to 3.6V, C_L = 50pF	Full	1.0	7.3	14.2	
			V_{CC} = 4.5V to 5.5V, C_L = 15pF	Full	0.5	3.7	6.0	ns
			V_{CC} = 4.5V to 5.5V, C_L = 50pF	Full	0.5	4.8	9.0	
High to Low Propagation Delay	t_{PHL}		V_{CC} = 3.0V to 3.6V, C_L = 15pF	Full	0.5	4.5	8.1	ns
			V_{CC} = 3.0V to 3.6V, C_L = 50pF	Full	1.0	5.6	10.5	
			V_{CC} = 4.5V to 5.5V, C_L = 15pF	Full	0.5	3.4	5.8	ns
			V_{CC} = 4.5V to 5.5V, C_L = 50pF	Full	0.5	4.2	7.6	
Power Dissipation Capacitance (2)	C_{PD}	no load, f = 1MHz	V_{CC} = 5.0V	+25℃		6		pF

NOTES:

1. Specified by design and characterization, not production tested.
2. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

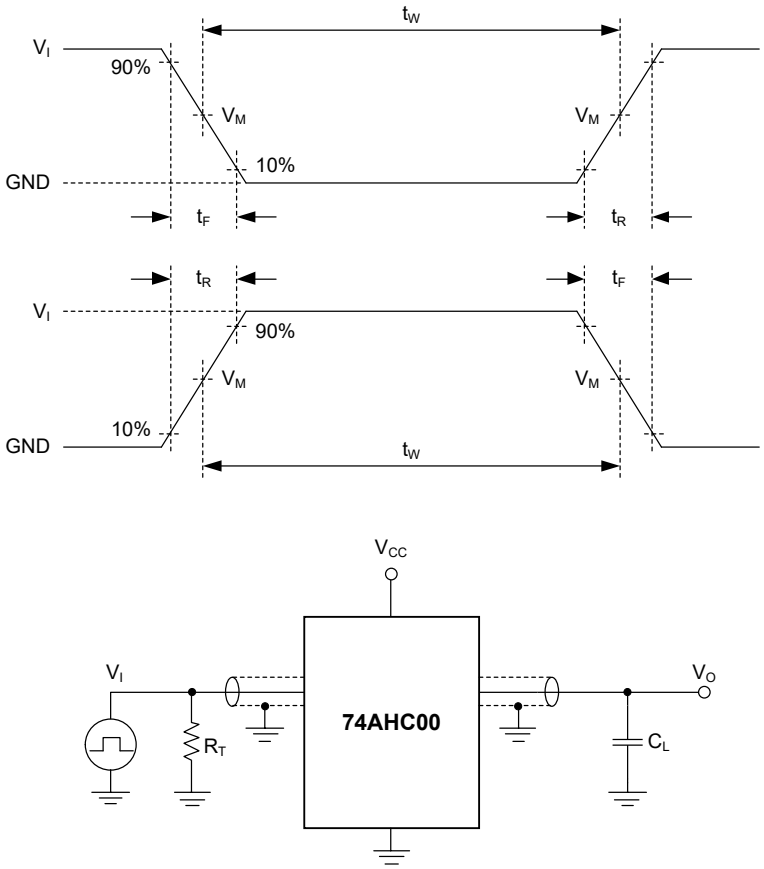
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of the outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

C_L: Load capacitance (includes jig and probe).

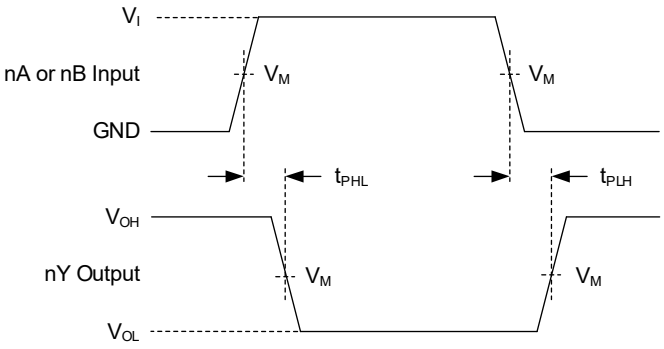
R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD	TEST
V_{CC}	V_I	t_R, t_F	C_L	
2.0V to 5.5V	V_{CC}	≤ 3.0ns	15pF, 50pF	t_{PHL}, t_{PLH}

WAVEFORMS



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (nA or nB) to Output (nY) Propagation Delays

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT
V_{CC}	V_I	V_M (1)	V_M
2.0V to 5.5V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}

NOTE:
1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 3.0ns.

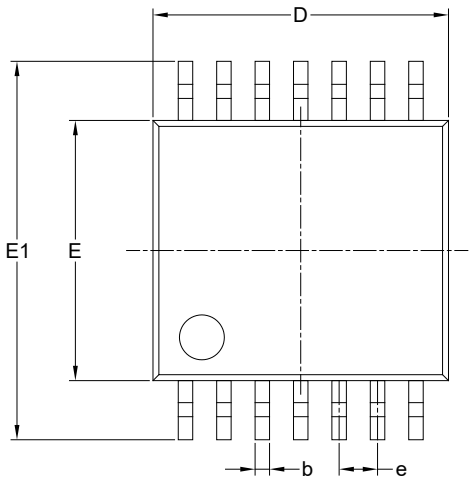
REVISION HISTORY

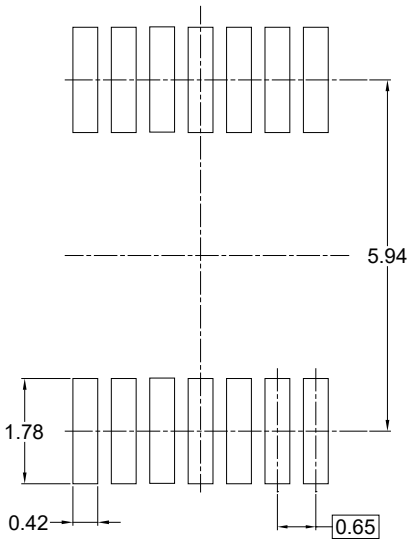
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (APRIL 2025) to REV.A	Page
Changed from product preview to production data	All

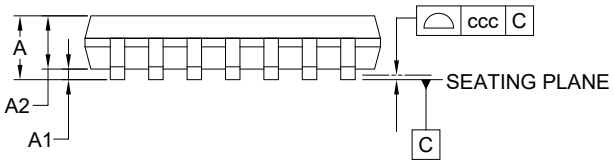
PACKAGE OUTLINE DIMENSIONS

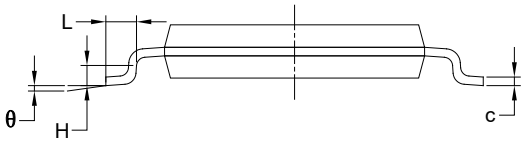
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)



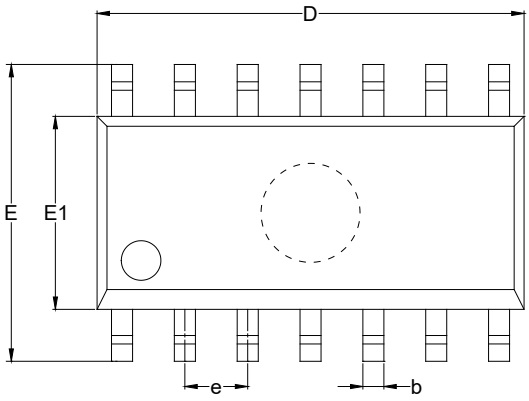


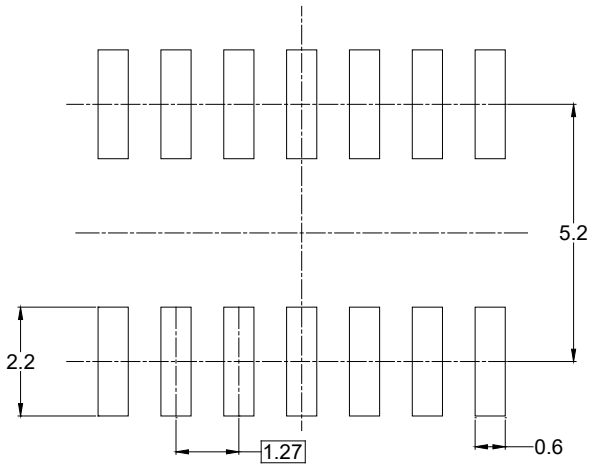
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

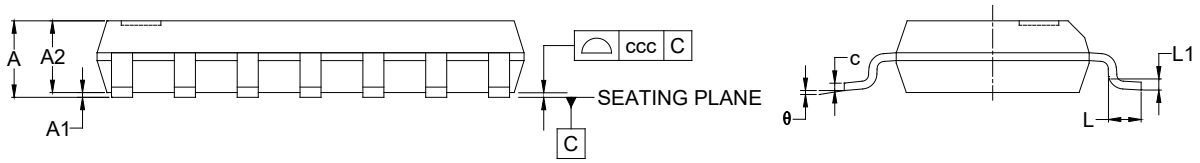
PACKAGE OUTLINE DIMENSIONS

SOIC-14





RECOMMENDED LAND PATTERN (Unit: mm)

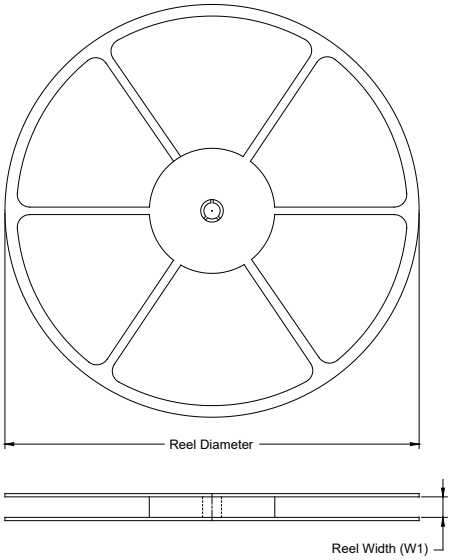


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.310	-	0.510
c	0.100	-	0.250
D	8.450	-	8.850
E	5.800	-	6.200
E1	3.800	-	4.000
e	1.270 BSC		
L	0.400	-	1.270
L1	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

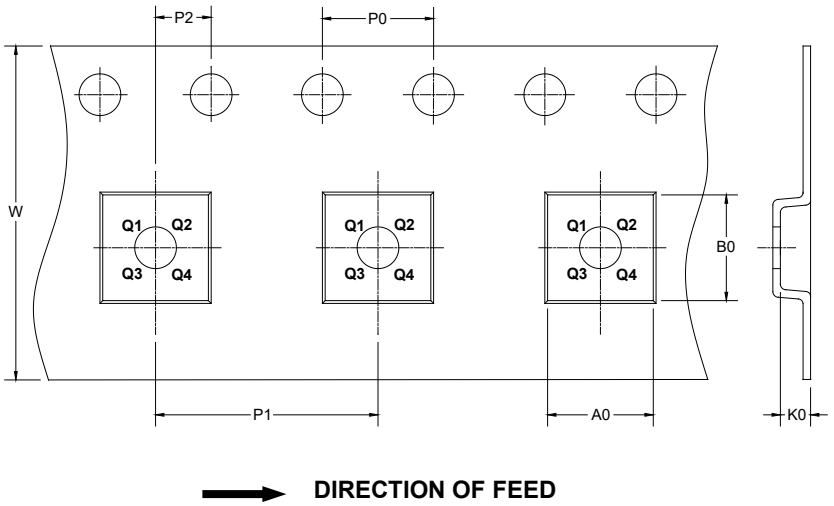
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



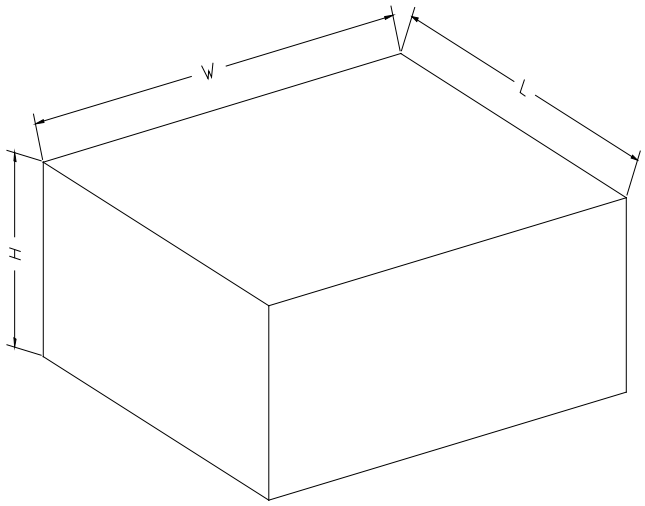
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-14	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
SOIC-14	13"	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002