SGM52412RG
16-Channel, 24-Bit Analog-to-Digital Converter

GENERAL DESCRIPTION

The SGM52412RG is a 24-bit, low-noise, 16 channels, sigma-delta (Σ-Δ) analog-to-digital converter (ADC). The multiplexer supports 8 differential inputs or 16 single-ended inputs configuration. When used with a 5V reference, the input range can be a unipolar range of 5V or true bipolar range of ±2.5V.

The SGM52412RG contains the internal system monitor registers that provide supply voltage monitor, temperature sensor monitor, external reference voltage monitor, and input offset monitor. It has an SPI-compatible interface.

The SGM52412RG has the on-chip configurable current sources that can be used to bias external sensors or verify sensor integrity.

The SGM52412RG operates from a unipolar +5V or bipolar ±2.5V analog supply and a digital supply range from 2.7V to 5.25V.

The SGM52412RG is available in a Green TQFN-7×7-48AL package. It is specified from -40℃ to +125℃.

FEATURES

- **Analog Supply Voltage Range:**
  - **Unipolar: +5V**
  - **Bipolar: ±2.5V**
- **125kSPS Fixed-Channel Data Rate**
- **21.739kSPS/Channel Auto-Scan Data Rate**
- **Support 16 Single-Ended or 8 Differential Inputs**
- **Support Fixed-Channel or Automatic Channel Scan**
- **Low Noise:**
  2μV_{RMS} at 1.9kSPS
- **Integral Nonlinearity: 0.0008%FSR (TYP)**
- **Typical DC Stability:**
  - **Offset Error: 1μV (TYP)**
  - **Gain Error: 0.05% (TYP)**
- **Power Dissipation: 56mW (TYP)**
- **Support Standby Mode, Sleep Mode and Power-Down Mode**
- **Crystal Oscillator 32.768kHz, or External Clock**
- **Support Open-Sensor Detection**
- **Available in a Green TQFN-7×7-48AL Package**

APPLICATIONS

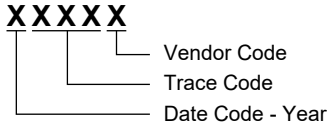
Medical Instruments
Process Control
Industrial Instruments
Factory Automation Equipment
Test and Measurement Systems

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM52412RG	TQFN-7×7-48AL	-40℃ to +125℃	SGM52412RGXTUL48G/TR	SGM52412RG XTUL48 XXXXX	Tape and Reel, 3000
			SGM52412RGXTUL48SG/TR	SGM52412RG XTUL48 XXXXX	Tape and Reel, 500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

AVDD to AVSS ..... -0.3V to 5.5V
AVSS to DGND..... -2.8V to 0.3V
DVDD to DGND ..... -0.3V to 5.5V
Input Current (Momentary)..... 100mA
Input Current (Continuous) 10mA
Analog Input Voltage Range
..... AVSS - 0.3V to AVDD + 0.3V
Digital Input Voltage to DGND ..... -0.3V to DVDD + 0.3V
Package Thermal Resistance
TQFN-7×7-48AL, θ_{JA}..... 20.6℃/W
TQFN-7×7-48AL, θ_{JB}..... 7.9℃/W
TQFN-7×7-48AL, $\theta_{JC\ (TOP)}$ ..... 13.2℃/W
TQFN-7×7-48AL, $\theta_{JC\ (BOT)}$ ..... 2.1℃/W
Junction Temperature..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s)..... +260℃
ESD Susceptibility (1) (2)
HBM..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

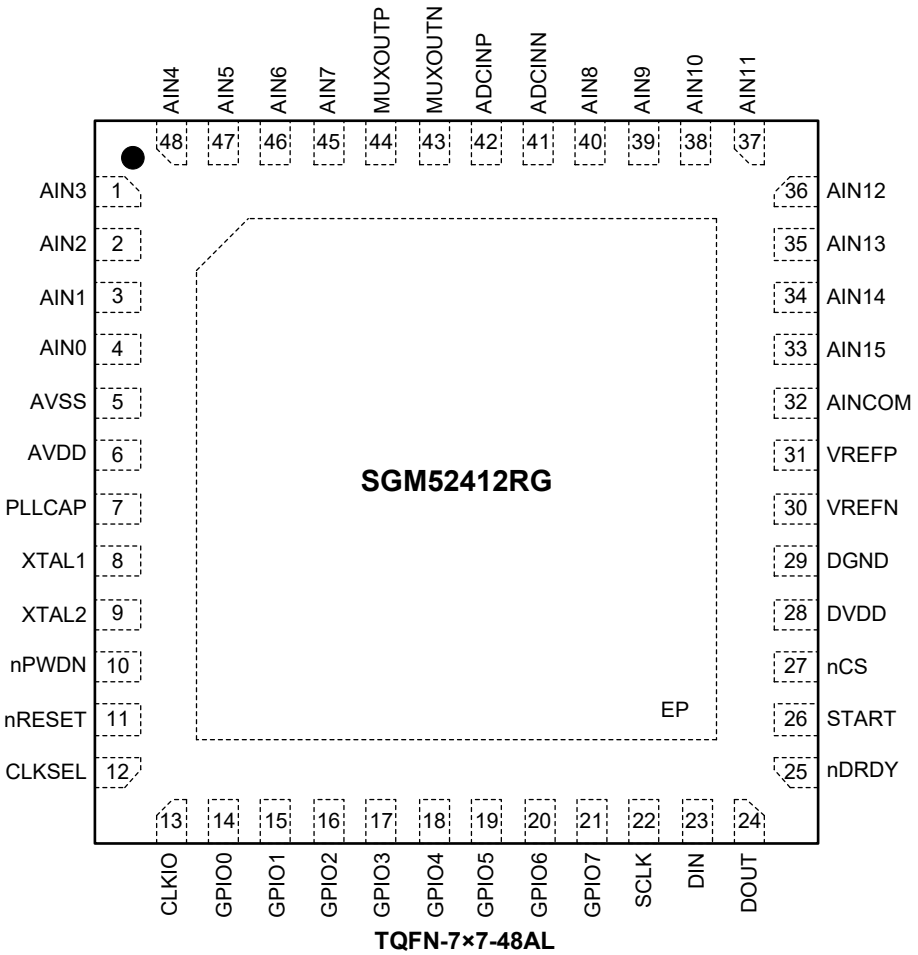
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-7×7-48AL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	AIN3	AI	Analog Input 3.
2	AIN2	AI	Analog Input 2.
3	AIN1	AI	Analog Input 1.
4	AIN0	AI	Analog Input 0.
5	AVSS	Analog	Negative Analog Power Supply Pin. It can be operated from a unipolar 0V or bipolar -2.5V analog supply.
6	AVDD	Analog	Positive Analog Power Supply Pin. It can be operated from a unipolar +5V or bipolar +2.5V analog supply.
7	PLLCAP	Analog	PLL Bypass Capacitor. Connect a 22nF capacitor to AVSS.
8	XTAL1	Analog	32.768kHz Crystal Oscillator Input 1.
9	XTAL2	Analog	32.768kHz Crystal Oscillator Input 2.
10	nPWDN	DI	Power-Down Input Pin. Active low.
11	nRESET	DI	Reset Input Pin. Active low.
12	CLKSEL	DI	Clock Select Input Pin. See Table 1.
13	CLKIO	DIO	System Clock I/O Pin.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
14	GPIO0	DIO	General-Purpose Digital Input/Output 0.
15	GPIO1	DIO	General-Purpose Digital Input/Output 1.
16	GPIO2	DIO	General-Purpose Digital Input/Output 2.
17	GPIO3	DIO	General-Purpose Digital Input/Output 3.
18	GPIO4	DIO	General-Purpose Digital Input/Output 4.
19	GPIO5	DIO	General-Purpose Digital Input/Output 5.
20	GPIO6	DIO	General-Purpose Digital Input/Output 6.
21	GPIO7	DIO	General-Purpose Digital Input/Output 7.
22	SCLK	DI	SPI Interface Clock Input Pin. The data is shifted in on the rising edge of SCLK, and shifted out on the falling edge of SCLK.
23	DIN	DI	SPI Interface Data Input Pin.
24	DOUT	DO	SPI Interface Data Output Pin.
25	nDRDY	DO	Data Ready Output Pin. Active low.
26	START	DI	Start Conversion Input Pin. Active high.
27	nCS	DI	SPI Interface Chip Select Input Pin. Active low.
28	DVDD	Digital	Digital Power Supply.
29	DGND	Digital	Digital Ground.
30	VREFN	AI	Negative Reference Input Pin.
31	VREFP	AI	Positive Reference Input Pin.
32	AINCOM	AI	Analog Input Common.
33	AIN15	AI	Analog Input 15.
34	AIN14	AI	Analog Input 14.
35	AIN13	AI	Analog Input 13.
36	AIN12	AI	Analog Input 12.
37	AIN11	AI	Analog Input 11.
38	AIN10	AI	Analog Input 10.
39	AIN9	AI	Analog Input 9.
40	AIN8	AI	Analog Input 8.
41	ADCINN	AI	Negative ADC Differential Input Pin.
42	ADCINP	AI	Positive ADC Differential Input Pin.
43	MUXOUTN	AO	Negative Multiplexer Differential Output Pin.
44	MUXOUTP	AO	Positive Multiplexer Differential Output Pin.
45	AIN7	AI	Analog Input 7.
46	AIN6	AI	Analog Input 6.
47	AIN5	AI	Analog Input 5.
48	AIN4	AI	Analog Input 4.
Exposed Pad	EP	–	Exposed pad is connected to AVSS.

NOTE: AI = analog input, AO = analog output, DI = digital input, DO = digital output, DIO = digital input and output.

ELECTRICAL CHARACTERISTICS

(AVDD = +2.5V, AVSS = -2.5V, DVDD = +3.3V, V_{REF} = +4.096V, V_{REFN} = -2.5V, f_{CLK} = 16MHz (external clock) or f_{CLK} = 15.729MHz (internal clock), and an AMP buffer between MUX outputs and ADC inputs, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Multiplexer Inputs							
Absolute Input Voltage		AIN0 - AIN15, AINCOM with respect to DGND		AVSS - 0.1		AVDD + 0.1	V
On-Channel Resistance					40		Ω
Crosstalk		f_{IN} = 1kHz			-125		dB
Sensor Bias (Current Source)		SBCS[1:0] = 01			1.5		μA
		SBCS[1:0] = 11			24		
1.5μA:24μA Ratio Error					±1		%
ADC Input							
Full-Scale Input Voltage		V_{IN} = ADCINP - ADCINN			±1.06V_{REF}		V
Absolute Input Voltage		ADCINP, ADCINN		AVSS - 0.1		AVDD + 0.1	V
Differential Input Impedance					7.5		kΩ
System Performance							
Resolution				24			Bits
Data Rate		Fixed-channel mode		1.953		125	kSPS
		Auto-scan mode		1.818		21.739	
Integral Nonlinearity (1)	INL	Differential input			0.0008		% of FSR (2)
Offset Error	E_O	Shorted inputs, after calibration	Chopping off		60		μV
			Chopping on		1		
Offset Drift (3)		Shorted inputs	Chopping off		0.4		μV/℃
			Chopping on		0.4		
Gain Error	E_G	After calibration			0.05		%
Gain Drift (3)						20	ppm/℃
Noise				See Table 2			
Common Mode Rejection Ratio	CMRR	f_{CM} = 50Hz			100		dB
		f_{CM} = 60Hz			100		
Power Supply Rejection Ratio	PSRR	AVDD, AVSS	f_{PS} = 50Hz		80		dB
			f_{PS} = 60Hz		80		
		DVDD	f_{PS} = 50Hz		80		
			f_{PS} = 60Hz		80		
External Voltage Reference Input							
Reference Input Voltage		V_{REF} = V_{REFP} - V_{REFN}		0.5	4.096	AVDD - AVSS	V
Negative Reference Input	V_{REFN}			AVSS - 0.1		V_{REFP} - 0.5	V
Positive Reference Input	V_{REFP}			V_{REFN} + 0.5		AVDD + 0.1	V
Reference Input Impedance					12		kΩ
System Parameters							
External Reference Reading Error					0.2	3.3	%
Analog Supply Reading Error					0.2	4.2	%
Temperature Sensor Reading	Voltage	T_A = +25℃ (4)			156		mV
	Coefficient	See Note 4			365		μV/℃

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = +2.5V, AVSS = -2.5V, DVDD = +3.3V, V_{REF} = +4.096V, V_{REFN} = -2.5V, f_{CLK} = 16MHz (external clock) or f_{CLK} = 15.729MHz (internal clock), and an AMP buffer between MUX outputs and ADC inputs, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Input/Output								
Logic Levels		V_{IH}			0.7 × DVDD		DVDD	V
		V_{IL}			DGND		0.3 × DVDD	
		V_{OH}	I_{OH} = 2mA		0.8 × DVDD		DVDD	
		V_{OL}	I_{OL} = 2mA		DGND		0.2 × DVDD	
Input Leakage			V_{IN} = DVDD, GND				2	μA
Master Clock Input (CLKIO)	Frequency				0.1		16	MHz
	Duty Cycle				40		60	%
Crystal Oscillator	Crystal Frequency					32.768		kHz
	Clock Output Frequency					15.729		MHz
	Start-Up Time (Clock Output Valid)					70		ms
	Clock Output Duty Cycle				40		60	%
Power Supply								
DVDD					2.7		5.25	V
AVSS					-2.6		0	V
AVDD					AVSS + 4.75		AVSS + 5.25	V
DVDD Supply Current			External clock operation	Sleep mode		36	95	μA
				Standby mode		2.5	3	mA
				Converting mode		3.6	5	mA
			Internal oscillator operation, clock output disabled			3.5		mA
			Internal oscillator operation, clock output enabled (5)			4.5		mA
			Power-down (6)			0.5	3	μA
AVDD, AVSS Supply Current			Converting			8.5	12	mA
			Standby			6		mA
			Sleep			0.5		mA
			Power-down			0.85	3	μA
Power Dissipation			Converting			56	80	mW
			Standby			40		mW
			Sleep			2.2		mW
			Power-down			6		μW

NOTES:

1. Best straight line fit method.
2. FSR = Full-scale range = 2.13V_{REF}.
3. Guaranteed by characterization.
4. The SGM52412RG and test PCB are in the same temperature together.
5. CLKIO load = 20pF.
6. No clock applied to CLKIO.

TIMING CHARACTERISTICS

(DVDD = 2.7V to 5.25V, T_A = -40℃ to +125℃, unless otherwise noted.)

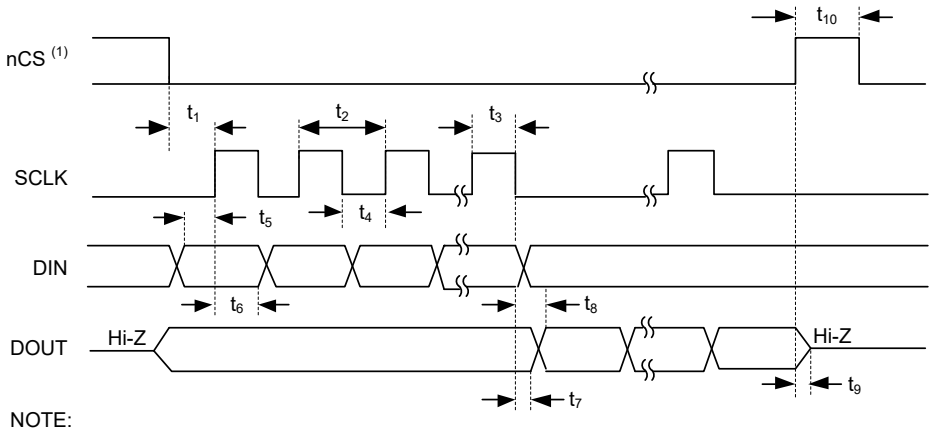
PARAMETER	SYMBOL	CONDITIONS	MIN	TYPE	MAX	UNITS
nCS Low to First SCLK, Setup Time (1)	t_1		2.5			τ_{CLK}
SCLK Period	t_2		2			τ_{CLK}
SCLK High Width	t_3		0.8		4096	τ_{CLK}
SCLK Low Width	t_4		0.8		4096	τ_{CLK}
Valid DIN to SCLK Rising Edge: Setup Time	t_5		10			ns
Valid DIN to SCLK Rising Edge: Hold Time	t_6		5			ns
SCLK Falling Edge to Old DOUT Invalid: Hold Time	t_7		0			ns
SCLK Falling Edge to Valid New DOUT: Propagation Delay (2)	t_8				50	ns
nCS High to DOUT Invalid (Tri-State)	t_9				5	τ_{CLK}
nCS Pulse Width High	t_{10}		2			τ_{CLK}
nDRDY High Pulse Width without Data Read	t_{11}			1		τ_{CLK}
Valid DOUT to nDRDY Falling Edge (nCS = 0)	t_{12}			0.5		τ_{CLK}

NOTES:

1. nCS can be tied low.

2. DOUT load = 20pF || 100kΩ to DGND.

3. τ_{CLK} = master clock period = 1/f_{CLK}.



NOTE:
1. nCS can be tied low.

Figure 1. Serial Interface Timing

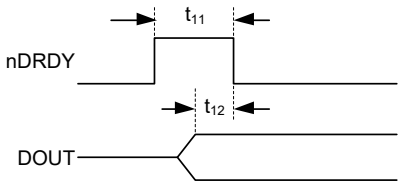
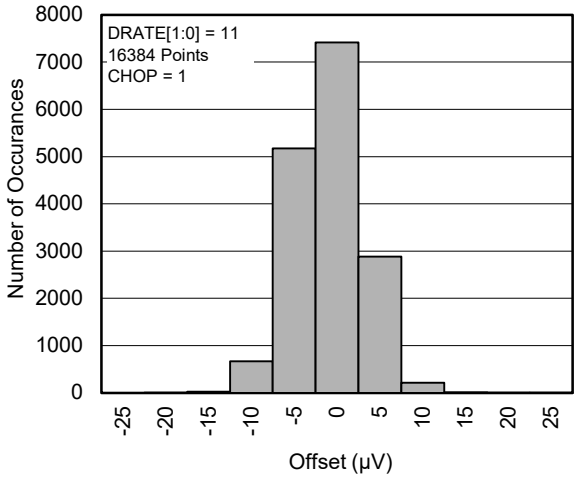


Figure 2. nDRDY Update Timing

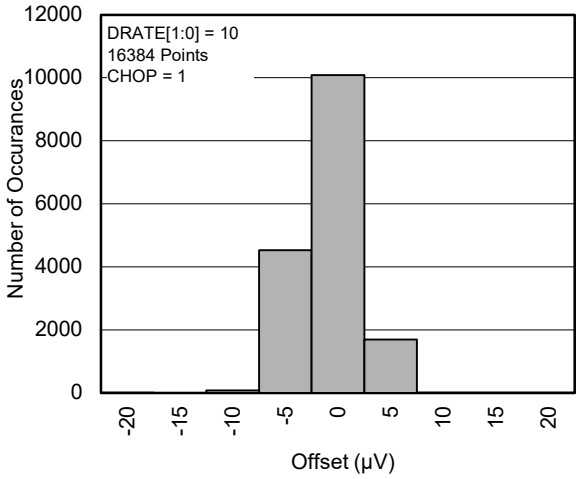
TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = +2.5V, AVSS = -2.5V, DVDD = +3.3V, V_{REF} = +4.096V, V_{REFN} = -2.5V, f_{CLK} = 16MHz (external clock) or f_{CLK} = 15.729MHz (internal clock), and an AMP buffer between MUX outputs and ADC inputs, T_A = -40℃ to +125℃, unless otherwise noted.

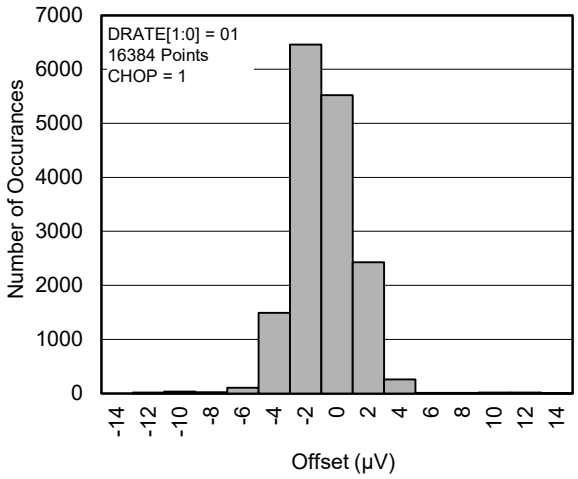
Reading Histogram



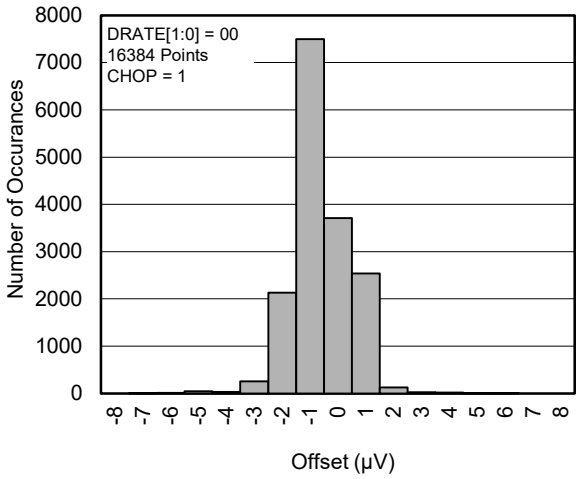
Reading Histogram



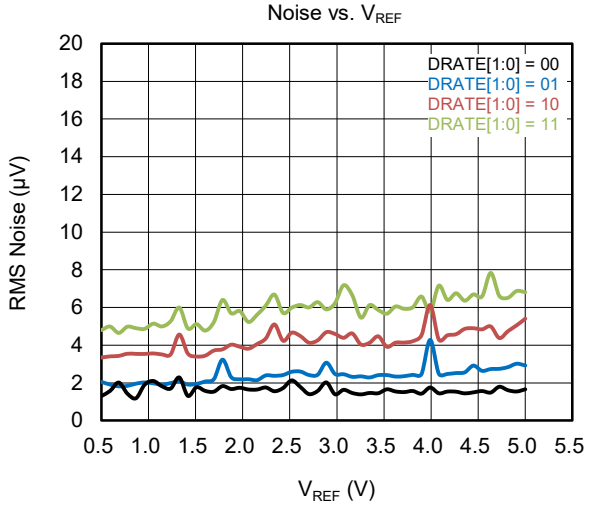
Reading Histogram



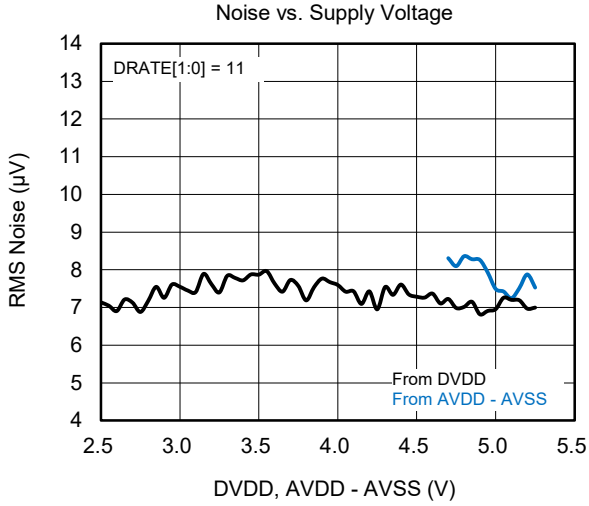
Reading Histogram



Noise vs. V_{REF}



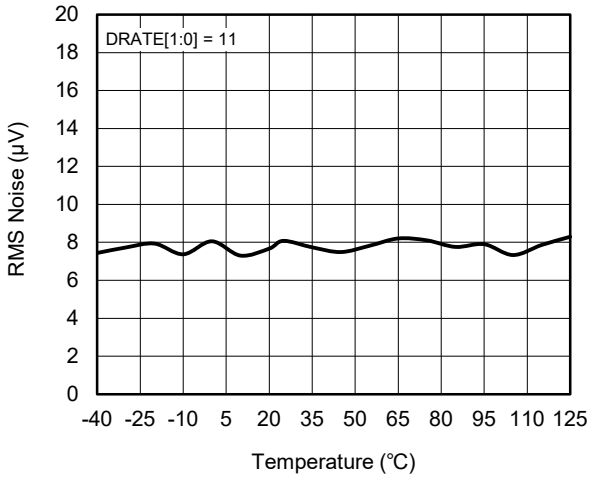
Noise vs. Supply Voltage



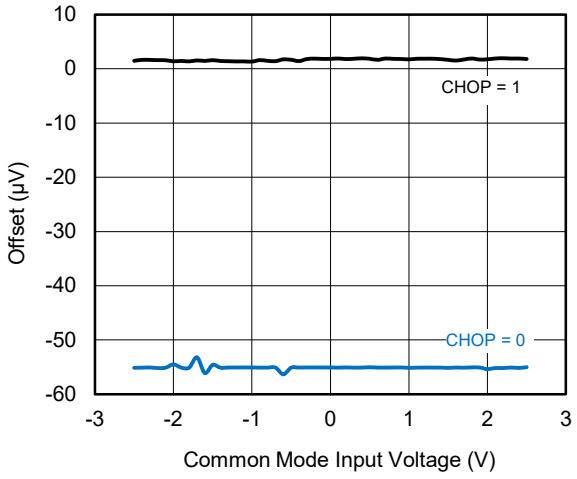
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

AVDD = +2.5V, AVSS = -2.5V, DVDD = +3.3V, V_{REF} = +4.096V, V_{REFN} = -2.5V, f_{CLK} = 16MHz (external clock) or f_{CLK} = 15.729MHz (internal clock), and an AMP buffer between MUX outputs and ADC inputs, T_A = -40℃ to +125℃, unless otherwise noted.

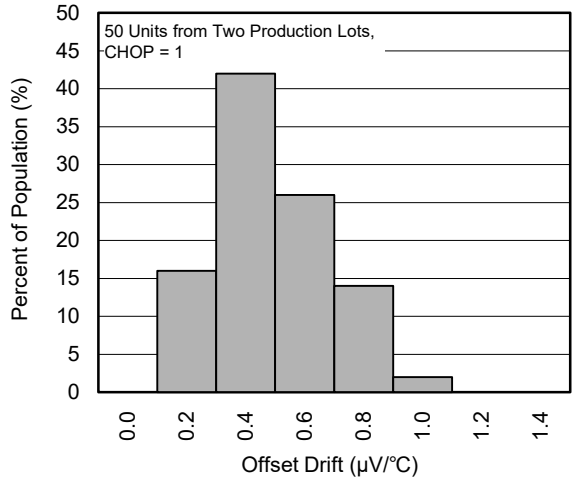
Noise vs. Temperature



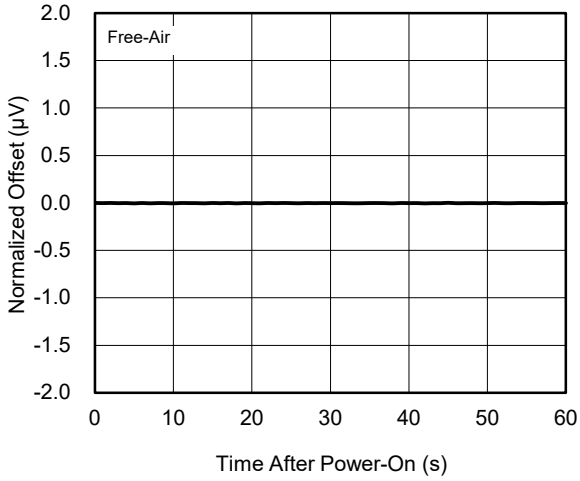
Offset vs. Common Mode Input Voltage



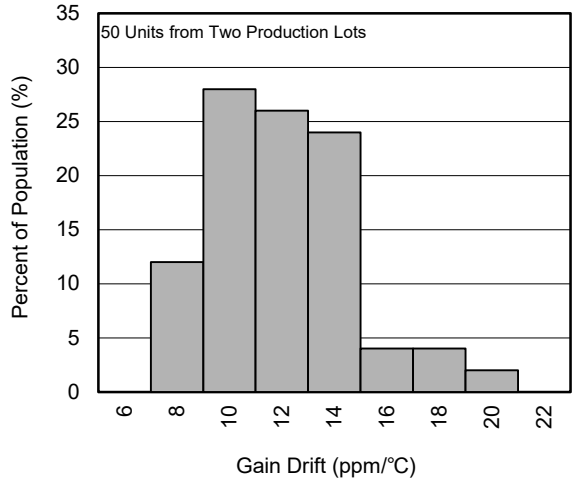
Offset Drift Histogram



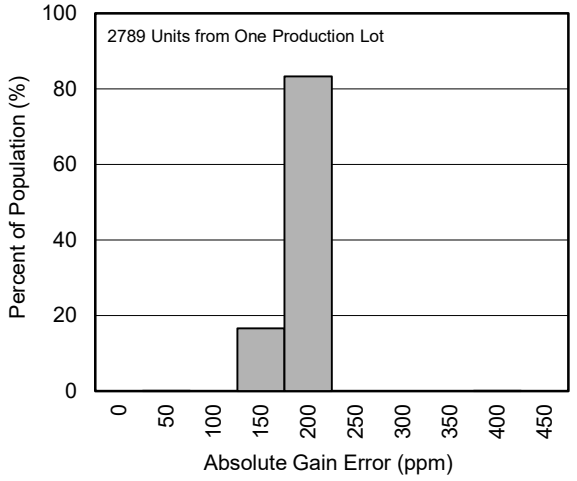
Offset Power-On Warmup



Gain Drift Histogram



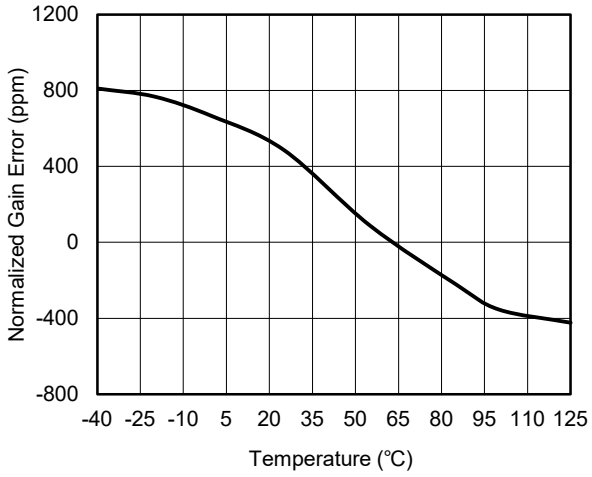
Gain Error Histogram



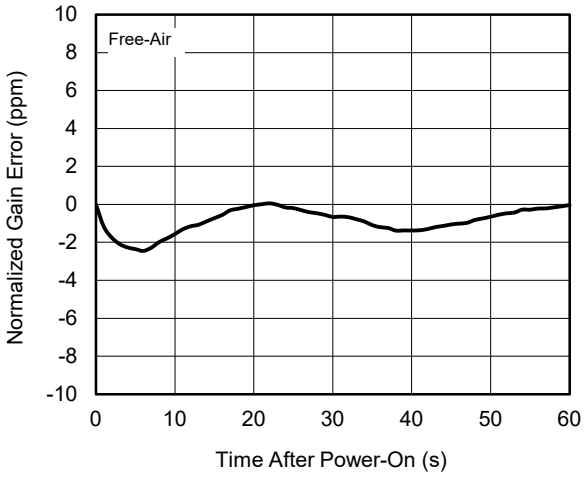
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

AVDD = +2.5V, AVSS = -2.5V, DVDD = +3.3V, V_{REF} = +4.096V, V_{REFN} = -2.5V, f_{CLK} = 16MHz (external clock) or f_{CLK} = 15.729MHz (internal clock), and an AMP buffer between MUX outputs and ADC inputs, T_A = -40℃ to +125℃, unless otherwise noted.

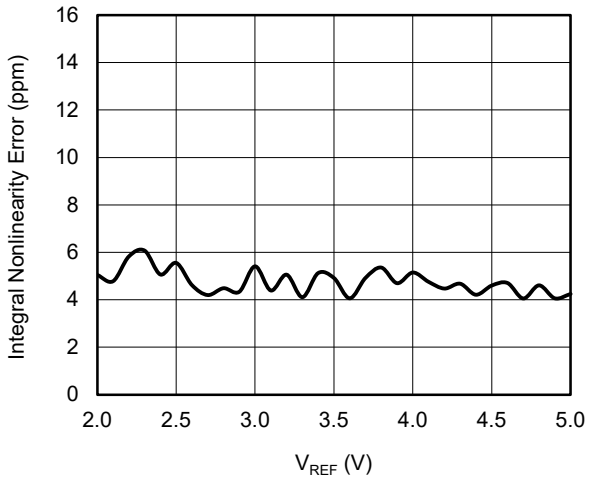
Gain Error vs. Temperature



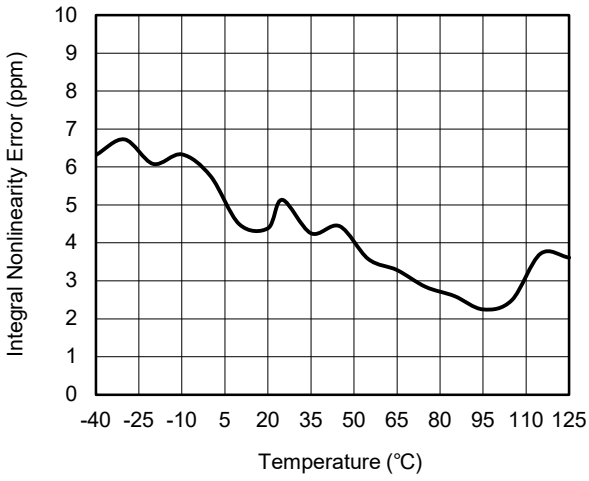
Gain Error Power-On Warmup



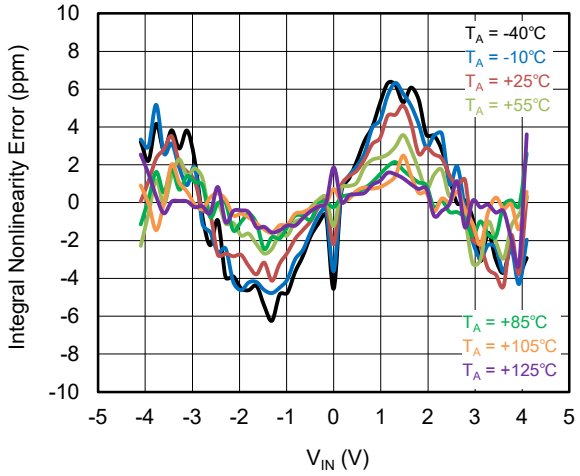
Integral Nonlinearity vs. V_{REF}



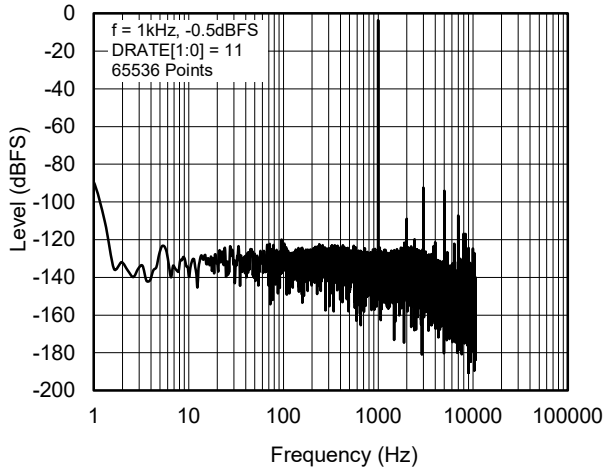
Integral Nonlinearity vs. Temperature



Integral Nonlinearity vs. Input Level



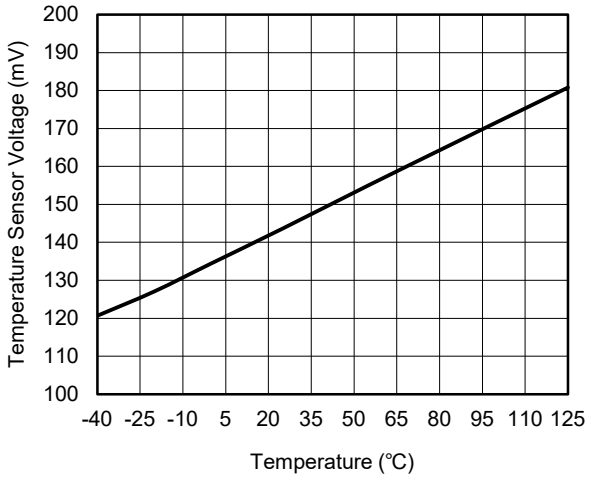
Output Spectrum



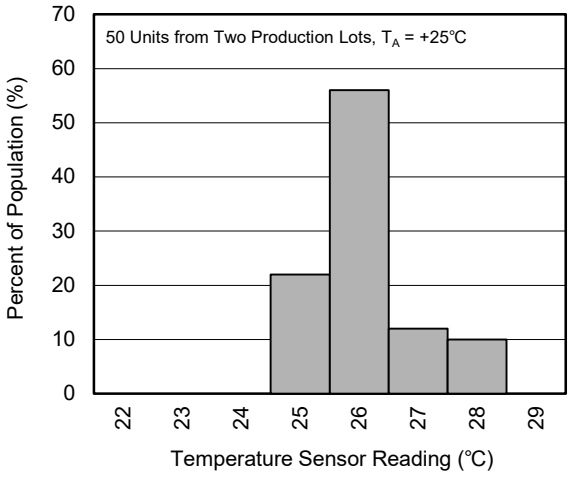
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

AVDD = +2.5V, AVSS = -2.5V, DVDD = +3.3V, V_{REF} = +4.096V, V_{REFN} = -2.5V, f_{CLK} = 16MHz (external clock) or f_{CLK} = 15.729MHz (internal clock), and an AMP buffer between MUX outputs and ADC inputs, T_A = -40℃ to +125℃, unless otherwise noted.

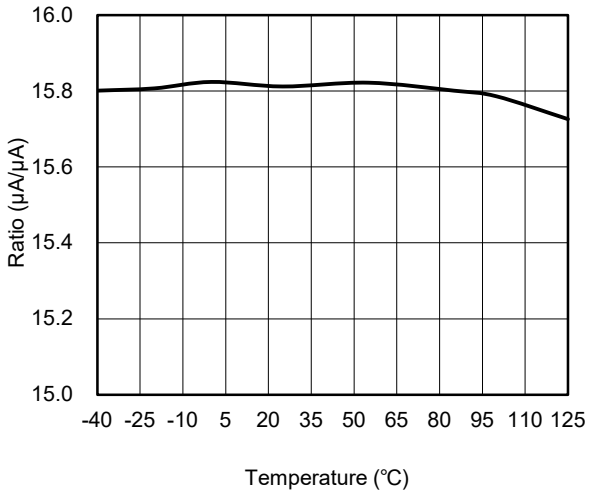
Temperature Sensor Voltage vs. Temperature



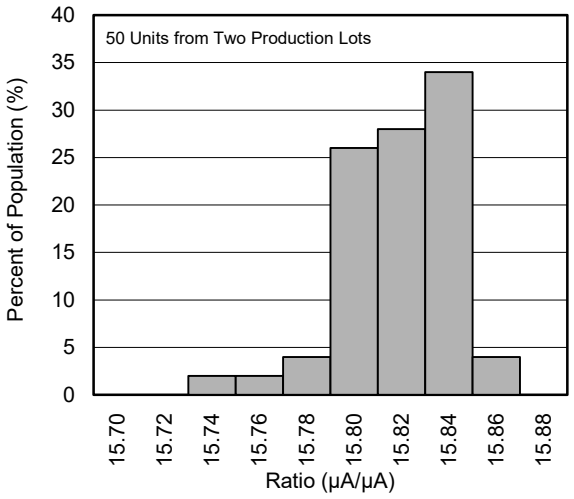
Temperature Sensor Reading Histogram



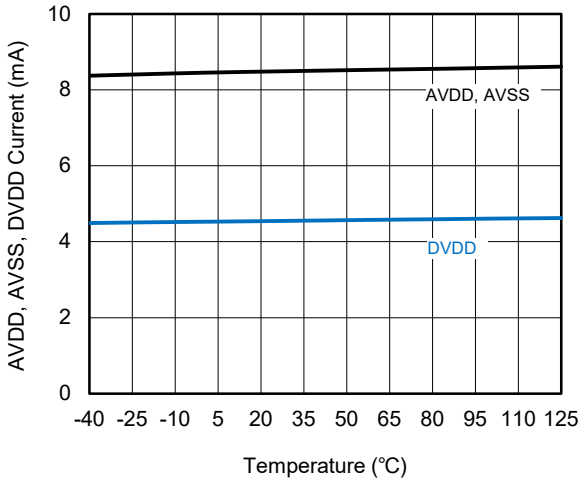
Sensor Bias Current Source Ratio vs. Temperature



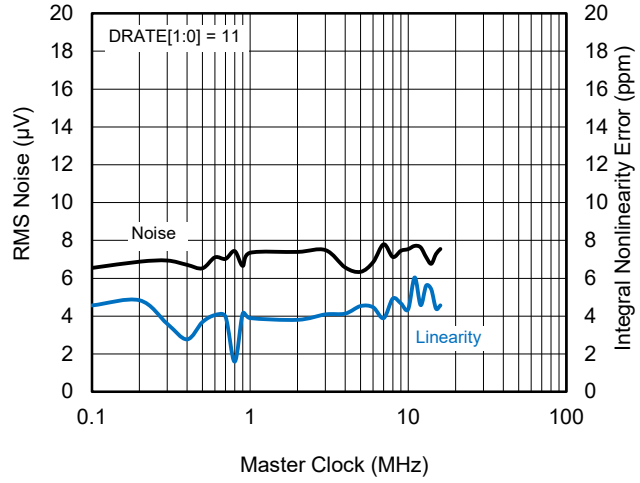
Sensor Bias Current Source Ratio Histogram



Supply Current vs. Temperature



Noise and INL vs. Master Clock



FUNCTIONAL BLOCK DIAGRAM

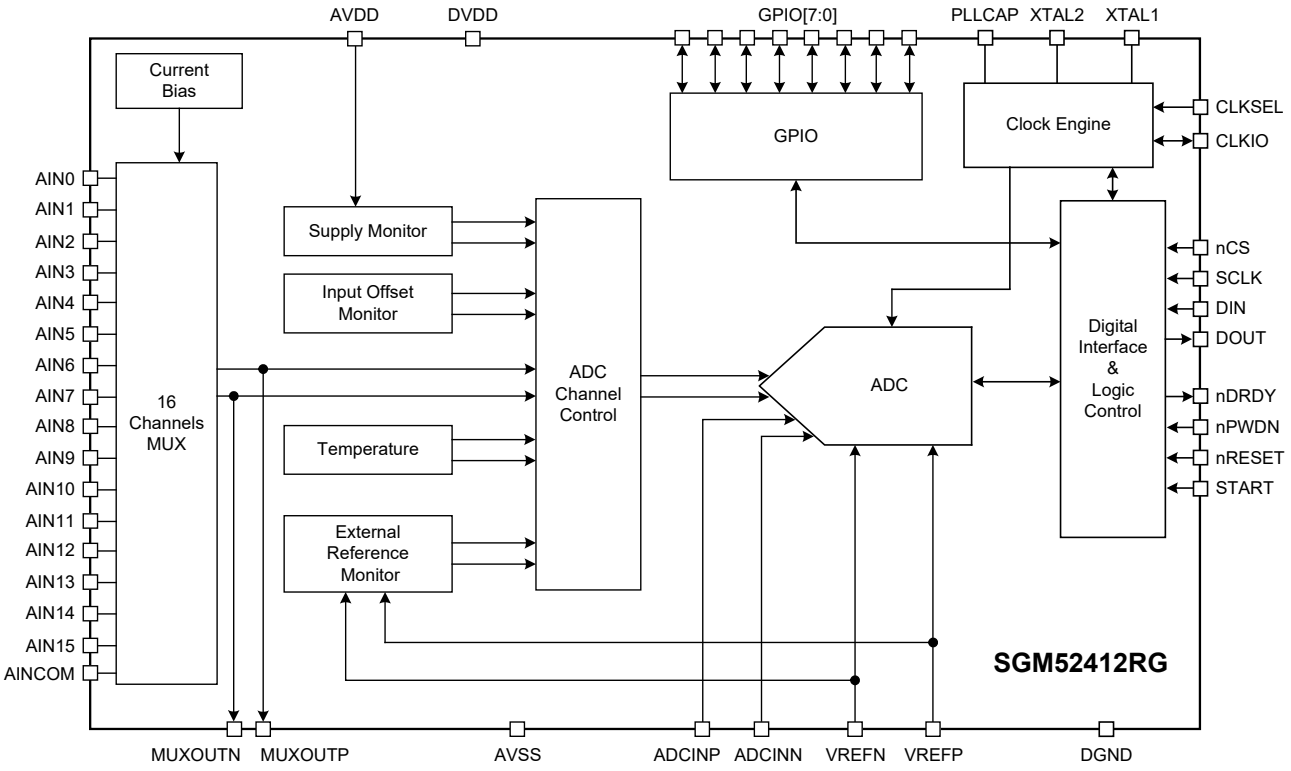


Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM52412RG is an ultra-low noise analog-to-digital converter (ADC). Figure 3 shows a block diagram of the SGM52412RG.

Input Multiplexer

As shown in Figure 3, the multiplexer is connected to one of 16 single-ended external inputs, or one of 8 differential external inputs, or one of the on-chip internal monitor blocks (which includes supply monitor, temperature monitor, input offset monitor, external reference/gain monitor).

Open/Short Sensor Detection

An on-chip current source can be used to bias an external sensor. When the sensor goes open circuit, the internal current source drives the inputs to positive full-scale (ADC conversion results).

General-Purpose Digital I/O (GPIO)

The SGM52412RG has 8 pins GPIO. All GPIO pins are individually set by GPIOCIO and GPIODATA register. During standby and power-down modes, the GPIO remains active. If GPIOs work as output, they keep driving output. If the digital I/O pins are not used, leave them as inputs tied to ground or configure them as outputs. This will reduce the power dissipation.

Clock Engine (f_{CLK})

The SGM52412RG clock source can be an internal oscillator (need an external crystal 32.768kHz), or an external clock source. In Table 1, the CLKSEL pin selects the source of the system clock.

ADC Description

Noise Performance

Table 2 summarizes the typical noise performance under different configurations. The following conditions apply: T_A = +25℃, AVDD = +2.5V, AVSS = -2.5V, DVDD = 3.3V, V_{REF} = 4.096V, and f_{CLK} = 16MHz. The ENOB is defined as:

$$ENOB = \frac{\ln(FSR / RMS\ Noise)}{\ln(2)} \quad (1)$$

Where:
FSR = Full-scale range.

Digital Filter

The ADC digital filter consists of SINC5 filter and a programmable low-pass digital average filter.

If chopping is enabled, the data rate is estimated by Equation 2 or Equation 3:

In auto-scan mode:

$$Data\ Rate = \frac{f_{CLK}}{128\left(4^{11b-DR} + 4.75 + TD\right) \times 2^{CHOP}} \quad (2)$$

In fixed-channel mode:

$$Data\ Rate = \frac{f_{CLK}}{128\left(4^{11b-DR} + CHOP\ (4.75 + TD)\right) \times 2^{CHOP}} \quad (3)$$

Where:
DR = DRATE[1:0] register bits.
CHOP = Chop register bit.
TD = Time delay value is shown in Table 3 from the DLY[2:0] register bits.

Table 1. System Clock Source

CLKSEL Pin	Clock Source	CLKENB Bit	CLKIO Function
0	Crystal Oscillator	0	Disabled (Internally Grounded)
0	Crystal Oscillator	1	Output
1	External Clock Input	X	Input

Table 2. Data Rate Configuration and Noise Performance (1) and -3dB Bandwidth

DRATE[1:0]	Auto-Scan Mode (2)				Fixed-Channel Mode				-3dB Bandwidth (Hz)
	Data Rate (SPS)	Input-Referred Noise (μV_{RMS})	Noise-Free Resolution (Bits)	Effective Number of Bits (ENOB)	Data Rate (SPS)	Input-Referred Noise (μV_{RMS})	Noise-Free Resolution (Bits)	Effective Number of Bits (ENOB)	
11	21739	8.1	17.3	20.0	125000	9.2	17.0	19.9	25390
10	14286	5.5	17.8	20.6	31250	5.9	17.8	20.5	12402
01	6024	3.1	18.8	21.4	7813	3.3	18.6	21.3	3418
00	1818	2.0	19.2	22.0	1953	2.0	19.2	22.0	869

NOTES:

1. V_{REF} = 4.096V, f_{CLK} = 16MHz, CHOP = 0, Delay = 0, Input = 1V, and 2048 sample size.

2. In auto-scan mode, the specified data rate is selected in a single channel, and if multiple channels are selected, the effective data rate is the listed value divided by the selected channel numbers.

DETAILED DESCRIPTION (continued)

Table 3. Effective Data Rates with Different Switch-Time Delay Setting in Auto-Scan Mode (1)

DLY[2:0]	DRATE[1:0] = 11	DRATE[1:0] = 10	DRATE[1:0] = 01	DRATE[1:0] = 00
000	21739	14286	6024	1818
001	18519	12821	5747	1792
010	16129	11628	5495	1767
011	12821	9804	5051	1718
100	9091	7463	4348	1629
101	5747	5051	3401	1475
110	3311	3067	2370	1241
111	2326	2203	1818	1071

NOTES:

1. The time delay and data rates will scale with f_{CLK}. (Table is specified with f_{CLK} = 16MHz)

2. If CHOP = 1, the data rate will be 1/2 of value showed in table.

Frequency Response

The SGM52412RG internal digital filter is composed of a SINC5 filter and an average filter. The filter response is shown by Equation 4.

$$|H(f)| = |H_{sinc^5}(f)| \times |H_{Averager}(f)| = \left| \frac{\sin\left(\frac{128\pi \times f}{f_{CLK}}\right)}{64 \times \sin\left(\frac{2\pi \times f}{f_{CLK}}\right)} \right|^5 \times \left| \frac{\sin\left(\frac{128\pi \times Num\_Ave \times f}{f_{CLK}}\right)}{Num\_Ave \times \sin\left(\frac{128\pi \times f}{f_{CLK}}\right)} \right| \quad (4)$$

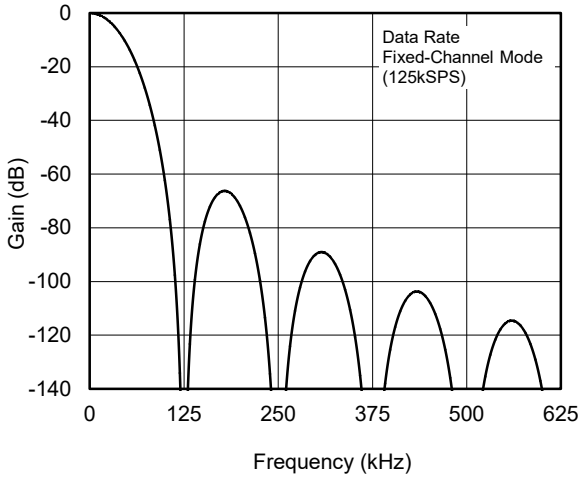


Figure 4. Frequency Response, DRATE[1:0] = 11

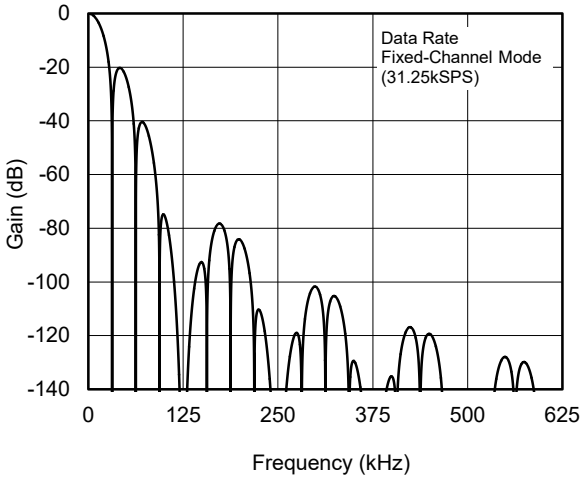


Figure 5. Frequency Response, DRATE[1:0] = 10

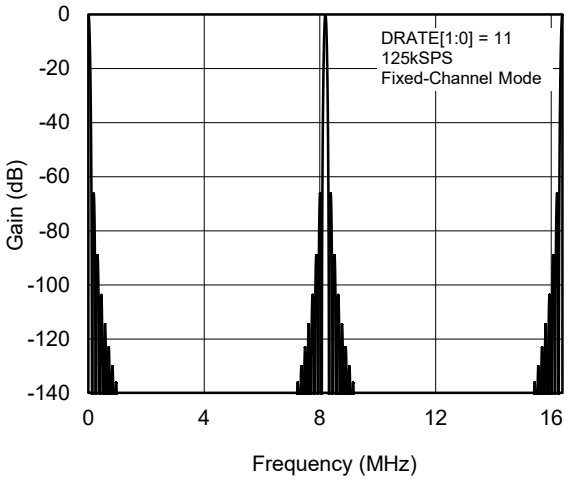


Figure 6. Frequency Response Out to 16MHz

DETAILED DESCRIPTION (continued)

Settling Time

If there is a step input for ADC, the SGM52412RG needs at least 5 complete conversion cycles. In auto-scan mode, the SGM52412RG provides the 5th fully-settled conversion results directly when scanning the input channels (need not discard any data). When the data is ready for each channel, the nDRDY flag goes low. When there is an asynchronous step input, in fixed-channel mode (DRATE[1:0] = 11), for ADC to read out the step input, and the input must remain stable for 5 complete conversion cycles.

When estimating the required time delay, Table 4 shows the ratio of time delay-to-time constant (t/τ) and the corresponding final determination data.

Table 4. Settling Time

t/τ (1)	Final Settling (%)	Final Settling (Bits)
1	63	2
3	95	5
5	99.3	7
7	99.9	10
10	99.995	14
15	99.9999	20
17	99.999994	24

NOTE:

1. The multiple time constants can be approximated by: $(\tau_1^2 + \tau_2^2 + \ldots)^{½}$.

Data Format

The input range of SGM52412RG is scaled to 106.6% by $\pm V_{REF}$. The ideal output codes for different input signals are summarized as shown in Table 5.

Table 5. Ideal Output Code for Different Input Signals

Input Signal V_{IN} (ADCINP - ADCINN)	Ideal Output Code (1)	Description
≥ +1.06 × V_{REF}	7FFFFFh	Maximum Positive Full-Scale before Output Clipping
+V_{REF}	780000h	V_{IN} = +V_{REF}
+1.06 × V_{REF}/(2^{23} - 1)	000001h	+1LSB
0	000000h	Bipolar Zero
-1.06 × V_{REF} × (2^{23} - 1)	FFFFFFh	-1LSB
-V_{REF}	87FFFFh	V_{IN} = -V_{REF}
≤ -1.06 × V_{REF} × (2^{23}/2^{23} - 1)	800000h	Maximum Negative Full-Scale before Output Clipping

NOTE:

1. Except for effects of INL, noise, offset, and gain errors.

Wake-Up Time

Set the nPWDN pin high to wake the device, a wake-up time is required before readings can be taken. The wake-up times are shown in Table 6.

Table 6. Wake-Up Times

Condition	Internal Oscillator (1)	External Clock
nPWDN or CLKSEL (2)	t_{OSC}	2/f_{CLK}
AVDD - AVSS (2)	t_{OSC} + 2^{18}/f_{CLK}	2^{18}/f_{CLK}

NOTES:

1. The wake-up time of the internal oscillator operation is a typical value. The user needs to consider the start-up times of different oscillators (t_{OSC} = oscillator start-up time).

2. When nPWDN or CLKSEL are enable, or When AVDD - AVSS > 3.2V (typical). The analog and digital supplies should be applied before any analog or digital input is driven.

Internal System Readings

Analog Power-Supply Reading (VCC)

The code value is converted to volts by Equation 5:

$$\text{Total Analog Supply Voltage}(V) = \frac{\text{Code}}{786432} \quad (5)$$

Note that it is needed to disable chopping (CHOP = 0) during this reading. The result is the difference voltage between AVDD and AVSS.

Gain Reading (GAIN)

The code value is converted to device gain by Equation 6:

$$\text{Device Gain}(V/V) = \frac{\text{Code}}{7864320} \quad (6)$$

Note that under this reading, the external reference is connected both to the analog input and to the reference input of the ADC.

Reference Reading (REF)

The code value is converted to external reference voltage by Equation 7:

$$\text{External Reference}(V) = \frac{\text{Code}}{786432} \quad (7)$$

Note that under this reading, the external reference is connected to the analog input and an internal reference is connected to the reference of the ADC.

DETAILED DESCRIPTION (continued)

Temperature Reading (TEMP)

The temperature reading is converted to ℃ by Equation 8:

$$\text{Temperature}(℃)=\left(\frac{\text{Temp Reading}(\mu V)-155000\mu V}{\text{Temp Sensor Coefficient}}\right)+25℃ \quad (8)$$

Where:

Temp Sensor Coefficient = 365μV/℃ (SGM52412RG and test PCB temperatures are forced in same temperature).

Note that it is needed to disable chopping (CHOP = 0) prior to taking this reading.

Offset Reading (OFFSET)

Under this reading, the differential output of the multiplexer is shorted together and set to a common mode voltage of (AVDD - AVSS)/2.

Chip Working Modes

The SGM52412RG has 3 basic modes, which includes converting mode, idle mode, and power-down mode.

Power-Down Mode

The analog and digital circuits are disabled in power-down mode.

Idle Modes

When the START pin is taken low, the device completes current conversion and then enters one of the idle modes, standby or sleep. When the START pin is taken high again, it will take some time for chip to re-enter conversion, the time depends on which mode is setting. Please refer to Table 7.

ADC Conversion Modes

The SGM52412RG contains two converting modes: auto-scan mode and fixed-channel mode.

Auto-Scan Mode

The SGM52412RG automatically scans and measures the selected channels, either in a continuous loop or pulse-step fashion.

Refer to Figure 7 and Figure 8. In auto-scan mode, if the STRAT pin is pulled high, the current channel conversion starts, after a while when the current channel data is ready, nDRDY gives a low output. If the START pin continuously keeps high, the ADC indexes to the next channel and converts automatically. If the STARTS pin is low, the chip goes to idle again.

For example, if channels AIN2, AIN3 and AIN7 are selected in auto-scan list. The SGM52412RG converts the channels in that list by priority, skipping all the other channels.

Fixed-Channel Mode

In this mode, any one of the 16 analog input channels (AIN0 - AIN15) can be selected as the positive ADC input or the negative ADC input. Note that in this mode, only the selected differential input is connected to the ADC, the AINCOM input and internal system register are not acquired by the ADC.

Table 7. Ideal Output Code Start Condition to nDRDY Delay, CHOP = 0, DLY[2:0] = 000

DRATE[1:0]	Initial Delay (Standby Mode) (f_{CLK} Cycles)		Initial Delay (Sleep Mode) (f_{CLK} Cycles)	
	Fixed-Channel	Auto-Scan	Fixed-Channel	Auto-Scan
11	708	713	708	713
10	1092	1097	1092	1097
01	2628	2633	2628	2633
00	8846	8846	8846	8846

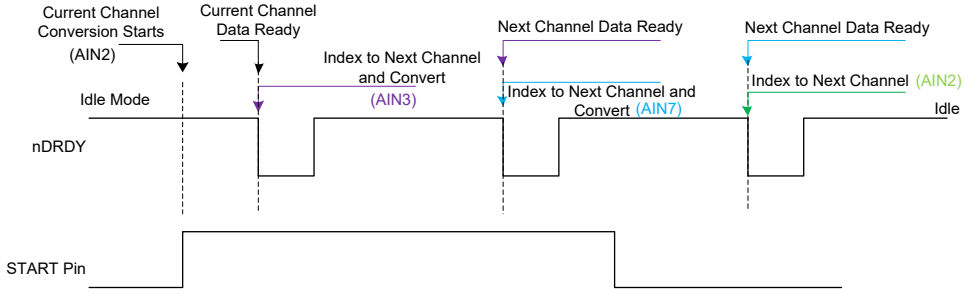


Figure 7. Conversion Control, Auto-Scan Mode

DETAILED DESCRIPTION (continued)

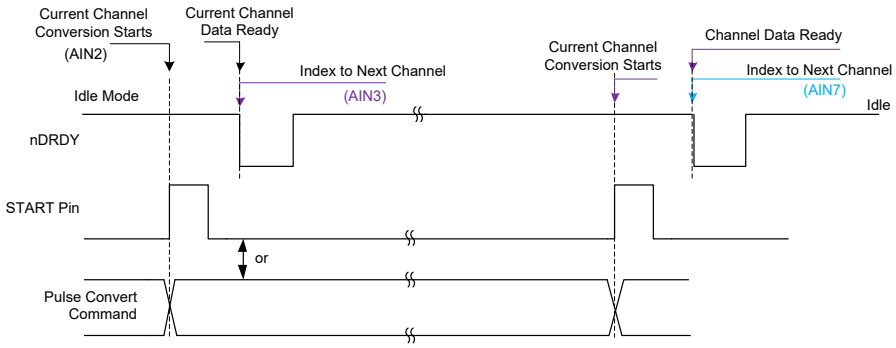


Figure 8. Pulse Conversion, Auto-Scan Mode

Series Interface (SPI Operation)

The SGM52412RG has an SPI-compatible interface. The interface consists of four signals: nCS, SCLK, DIN, and DOUT.

Reading DATA

When there is a channel data ready, nDRDY gives a low output. There are two kinds of method to read data out, read via a direct data read (Channel Data Read Direct) or the data may be read in a register format (Channel Data Register Format Read).

Channel Data Read Direct

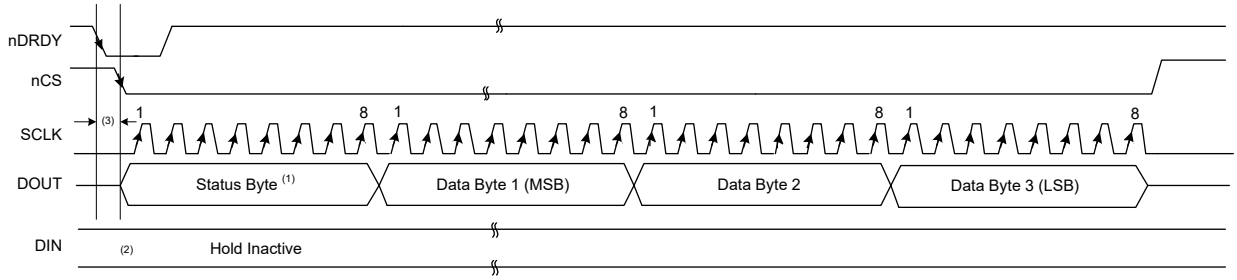
A complete data read operation may have 24 SCLK or 32 SCLK. The number of data bits (24-bit or 32-bit) depends on whether the status byte is enabled. It is shown in Figure 9. In this read format, an 2nd read operation will read out data 0 within the same nDRDY frame.

Channel Data Read Command

To read channel data, the first byte is command byte (the first three bits of the command byte are 001), after the command byte, and then the MSB of the channel data is on DOUT. The data is shifted out on the falling edge of SCLK. A complete read operation must be 40 SCLK. It is different with the direct read mode, the channel data can be read out during an nDRDY transition. See details in Figure 10.

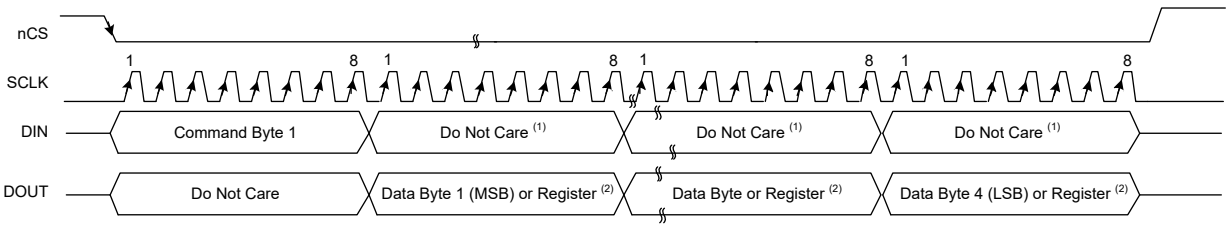
Register Read Command

To read register data, the first byte is command byte (the first three bits of the command byte are 010). The last four bits of the command byte are the beginning register address bits. After the command byte, and then the MSB of the channel data is on DOUT. The data is shifted out on the falling edge of SCLK. A single register or all remain registers from assigned beginning address can be read out. See details in Figure 10.



NOTES:
1. Optional for auto-scan mode, disabled for fixed-channel mode. See Status Byte Enable/Disable Description.
2. After the channel data read operation, nCS must be toggled or an SPI timeout must occur before sending commands.
3. No SCLK activity.

Figure 9. Channel Data Read Direct (No Command)



NOTES:
1. After the first number of registers are read, then more commands can be issued in succession.
2. 4 bytes of channel data register is read. Depends on status byte, one or more bytes for register data is read.

Figure 10. Register and Channel Data (Register Format) Read

DETAILED DESCRIPTION (continued)

Register Write Command

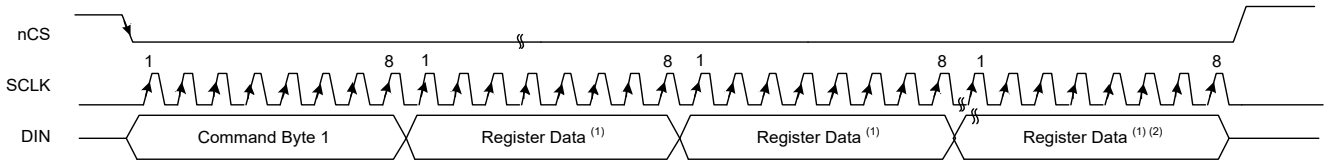
To write register data, the first byte is command byte (the first three bits of the command byte are 011). And also the command byte contains of register address bits. The data is shifted in on the rising edge of SCLK. A single register or all remain registers from assigned beginning address can be written. See details in Figure 11.

Reset Command

If there is a reset command, all registers are reset to their default values. A conversion in process will continue but conversion result data is invalid. Note that the SPI interface may need a reset to function it correctly. To ensure device resets properly, do the following, toggle nCS high then low and send the reset command. Or firstly reset SPI by hold SCLK inactive for $256/f_{CLK}$ or $4096/f_{CLK}$ and then send the reset command. The control commands are shown in Figure 12.

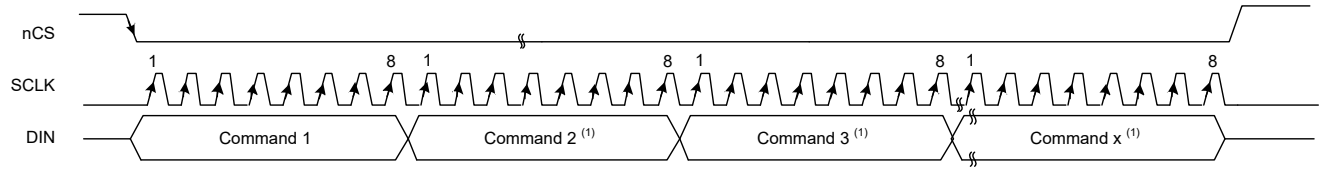
Channel Data Format

The data read operation may get 4 bytes out or 3 bytes out. It depends on the setting of STAT bit in CONFIG0 register. The channel data format is described in Table 8.



NOTES:
1. One or more bytes depending on MUL bit.
2. After the prescribed number of registers are read, then one or more additional can be issued in succession.

Figure 11. Register Write Operation



NOTE:
1. One or more commands can be issued is succession.

Figure 12. Control Command Operation

Table 8. Channel Data Format

Byte		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	STATUS	NEW	OVF	SUPPLY	CHID4	CHID3	CHID2	CHID1	CHID0
2	MSB	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16
3	MSB-1	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8
4	LSB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

NOTES:

1. The bit of STATUS, please refer to Table 9.

2. The ADC output data are 24 bits (DB[23:0]). DB23 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). The data is coded in binary two's complement format.

DETAILED DESCRIPTION (continued)

Table 9. Status Byte Format

BITS	BIT NAME	DESCRIPTION
DB[7]	NEW	0 = Channel data has not been updated since the last read operation 1 = Channel data has been updated since the last read operation The NEW bit is set when the channel data is update. It will not be reset until there is a read out. Once there is a read out, the bit is cleared. The conversion data will be not updated until there is a new conversion is completed.
DB[6]	OVF	1 = This indicates the differential voltage applied to the ADC inputs have exceeded the range of the converter $\|V_{IN}\| > 1.06 \times V_{REF}$ Note: If $V_{IN} \geq 1.06 \times V_{REF}$, the conversion result is clamped to positive full-scale. If $V_{IN} \leq -1.06 \times V_{REF}$, the conversion result is clamped to negative full-scale.
DB[5]	SUPPLY	0 = When the value rises 50mV higher (typically) than the lower trip point 1 = When the value falls below 4.3V (typically) The analog power-supply voltage (AVDD - AVSS) is below a preset limit.
DB[4:0]	CHID[4:0]	Channel ID shows the conversion data from which channel. Refer to Table 10 for the channel ID definition. Note that in fixed channel mode, these bits mean nothing.

Table 10. Channel ID and Measurement Order (Auto-Scan Mode) Description

Bits CHID[4:0]	Priority	Channel	Description
00h	1 (Highest)	AIN0 - AIN1 (DIFF0)	Differential 0
01h	2	AIN2 - AIN3 (DIFF1)	Differential 1
02h	3	AIN4 - AIN5 (DIFF2)	Differential 2
03h	4	AIN6 - AIN7 (DIFF3)	Differential 3
04h	5	AIN8 - AIN9 (DIFF4)	Differential 4
05h	6	AIN10 - AIN11 (DIFF5)	Differential 5
06h	7	AIN12 - AIN13 (DIFF6)	Differential 6
07h	8	AIN14 - AIN15 (DIFF7)	Differential 7
08h	9	AIN0	Single-Ended 0
09h	10	AIN1	Single-Ended 1
0Ah	11	AIN2	Single-Ended 2
0Bh	12	AIN3	Single-Ended 3
0Ch	13	AIN4	Single-Ended 4
0Dh	14	AIN5	Single-Ended 5
0Eh	15	AIN6	Single-Ended 6
0Fh	16	AIN7	Single-Ended 7
10h	17	AIN8	Single-Ended 8
11h	18	AIN9	Single-Ended 9
12h	19	AIN10	Single-Ended 10
13h	20	AIN11	Single-Ended 11
14h	21	AIN12	Single-Ended 12
15h	22	AIN13	Single-Ended 13
16h	23	AIN14	Single-Ended 14
17h	24	AIN15	Single-Ended 15
18h	25	OFFSET	OFFSET
1Ah	26	VCC	AVDD - AVSS Supplies
1Bh	27	TEMP	Temperature
1Ch	28	GAIN	Gain
1Dh	29 (Lowest)	REF	External Reference

DETAILED DESCRIPTION (continued)

Command and Register Definitions

Table 11. Command Byte

BITS	BIT NAME	DESCRIPTION
DB[7:5]	CMD[2:0]	Command Bits See Table 12.
DB[4]	MUL	Multiple Register Access If MUL is 0, only one addressed register can be read out or be written within a single read or write operation sequence. If MUL is 1, multiple registers can be read out or be written with a single read or write operation sequence. The registers from addressed register to address 09h registers can be all read out or be written within one operation sequence, or some of them (depends of numbers of SCLK). 0 = Disable multiple register access 1 = Enable multiple register access There are 3 ways to terminate multiple registers operation: 1. Set nCS high to reset SPI. 2. Hold SCLK for 4096 f_{CLK} cycles. 3. Register address reaches to 09h.
DB[3:0]	ADDR[3:0]	Register Address Bits These bits are the register addresses for a register read or write operation, see Table 13.

Table 12. CMD[2:0] Command Bits Description

CMD[2:0]	DESCRIPTION	COMMENTS
000	Channel Data Read Direct (No Command)	Toggle nCS or allow SPI timeout before sending command
001	Channel Data Read Command (Register Format)	Set MUL = 1, the status byte is always included in data
010	Register Read Command	A[3:0] = 0000
011	Register Write Command	
100	Pulse Convert Command	MUL and A[3:0] don't care
101	Reserved	
110	Reset Command	MUL and A[3:0] don't care
111	Channel Data Read Direct (No Command)	Toggle nCS or allow SPI timeout before sending command

REGISTER MAPS

Table 13. Register Maps

Address Bits A[3:0]	Register Name	Default Value	TYPE (Read/ Write)	DB[7]	DB[6]	DB[5]	DB[4]	DB[3]	DB[2]	DB[1]	DB[0]
0x00	CONFIG0	0x0A	R/W	0	SPIRST	MUXMOD	BYPAS	CLKENB	CHOP	STAT	0
0x01	CONFIG1	0x03	R/W	IDLMOD	DLY2	DLY1	DLY0	SBCS1	SBCS0	DRATE1	DRATE0
0x02	MUXFCH	0x00	R/W	AINP3	AINP2	AINP1	AINP0	AINN3	AINN2	AINN1	AINN0
0x03	MUXDIF	0x00	R/W	DIFF7	DIFF6	DIFF5	DIFF4	DIFF3	DIFF2	DIFF1	DIFF0
0x04	MUXSES0	0xFF	R/W	AIN7	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0
0x05	MUXSES1	0xFF	R/W	AIN15	AIN14	AIN13	AIN12	AIN11	AIN10	AIN9	AIN8
0x06	SYSREADS	0x00	R/W	0	0	REF	GAIN	TEMP	VCC	0	OFFSET
0x07	GPIOCIO	0xFF	R/W	CIO7	CIO6	CIO5	CIO4	CIO3	CIO2	CIO1	CIO0
0x08	GPIODATA	0x00	R/W	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
0x09	DEVICEID	0x8B	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

REG0x00: Configuration Register 0 (CONFIG0) [Reset = 0x0A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
DB[7]	0	0	R	Must be zero. (default)
DB[6]	SPIRST	0	R/W	SPI Interface Reset Timer 0 = Reset when SCLK inactive for 4096 f_{CLK} cycles (256μs, f_{CLK} = 16MHz) (default) 1 = Reset when SCLK inactive for 256 f_{CLK} cycles (16μs, f_{CLK} = 16MHz) To be used hold SCLK inactive to reset SPI interface, the bit sets how many inactive f_{CLK} cycles are needed.
DB[5]	MUXMOD	0	R/W	0 = Auto-scan mode (default) 1 = Fixed-channel mode See Auto-Scan Mode section and Fixed-Channel Mode section.
DB[4]	BYPAS	0	R/W	0 = ADC inputs use internal multiplexer connection (default) 1 = ADC inputs use external ADC inputs (ADCINP and ADCINN) Temperature, V_{CC}, gain, and reference internal monitor readings have internal connection. The BYPAS bit has no effect on them.
DB[3]	CLKENB	1	R/W	The clock output is from the device crystal oscillator and PLL circuit. 0 = Clock output on CLKIO disabled 1 = Clock output on CLKIO enabled (default) Note that is CLKSEL is pulled up to '1', the CLKIO pin works as an input. The CLKENB bit setting has no effect on it.
DB[2]	CHOP	0	R/W	This bit configures the chopping feature on the external multiplexer. 0 = Chopping disabled (default) 1 = Chopping enabled Note that when there is an internal system readings (temperature, V_{CC}, gain, and reference), the CHOP bit must be disabled.
DB[1]	STAT	1	R/W	Status Byte Enable 0 = Status byte disabled 1 = Status byte enabled (default) Table 14 shows the modes which the status byte can be disabled.
DB[0]	0	0	R	Must be zero.

Table 14. Status Byte Enable/Disable Description

Mode	Channel Data Read Command	Channel Data Read Direct
Auto-Scan	Always Enabled	Enabled/Disabled by STAT Bit
Fixed-Channel	Always Enabled (Byte is Undefined)	Always Disabled

REGISTER MAPS (continued)

REG0x01: Configuration Register 1 (CONFIG1) [Reset = 0x03]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
DB[7]	IDLMOD	0	R/W	0 = Select standby mode (default) 1 = Select sleep mode This bit selects the idle mode when the device is not converting, standby or sleep.
DB[6:4]	DLY[2:0]	000	R/W	These bits set the amount of delay time that before the ADC starts a conversion. See details in Digital Filter section.
DB[3:2]	SBCS[1:0]	00	R/W	These bits select the internal bias current. 00 = Sensor bias current source off (default) 01 = 1.5μA Source 10 = Reserved 11 = 24μA Source
DB[1:0]	DRATE[1:0]	11	R/W	See Table 15. These bits set the data rate of the converter.

Table 15. DRATE[1:0] Bits Description

DRATE[1:0]	Data Rate Auto-Scan Mode (SPS)	Data Rate Fixed-Channel Mode (SPS)
11	21739	125000
10	14286	31250
01	6024	7813
00	1818	1953

NOTE: f_{CLK} = 16MHz, CHOP = 0, Delay = 0.

REG0x02: Multiplexer Fixed-Channel Register (MUXFCH) [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
DB[7:4]	AINP[3:0]	0000	R/W	In fixed-channel mode, the AINP[3:0] bits select the analog input channel for the positive ADC input.
DB[3:0]	AINN[3:0]	0000	R/W	In fixed-channel mode, the AINN[3:0] bits select the analog input channel for the negative ADC input.

REG0x03: Multiplexer Differential Input Select Register (MUXDIF) [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
DB[7]	DIFF7	0	R/W	The register selects the input channels and the internal readings in auto-scan mode. Writing to the register will reset the internal channel pointer to the highest priority channel (see Table 10). 0 = Channel is not selected within a reading sequence 1 = Channel is selected within a reading sequence
DB[6]	DIFF6	0	R/W	
DB[5]	DIFF5	0	R/W	
DB[4]	DIFF4	0	R/W	
DB[3]	DIFF3	0	R/W	
DB[2]	DIFF2	0	R/W	
DB[1]	DIFF1	0	R/W	
DB[0]	DIFF0	0	R/W	

REGISTER MAPS (continued)

REG0x04: Multiplexer Single-Ended Input Select Register 0 (MUXSES0) [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
DB[7]	AIN7	1	R/W	The register selects the input channels and the internal readings in auto-scan mode. Writing to the register will reset the internal channel pointer to the highest priority channel (see Table 10). 0 = Channel is not selected within a reading sequence 1 = Channel is selected within a reading sequence
DB[6]	AIN6	1	R/W	
DB[5]	AIN5	1	R/W	
DB[4]	AIN4	1	R/W	
DB[3]	AIN3	1	R/W	
DB[2]	AIN2	1	R/W	
DB[1]	AIN1	1	R/W	
DB[0]	AIN0	1	R/W	

REG0x05: Multiplexer Single-Ended Input Select Register 1 (MUXSES1) [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
DB[7]	AIN15	1	R/W	The register selects the input channels and the internal readings in auto-scan mode. Writing to the register will reset the internal channel pointer to the highest priority channel (see Table 10). 0 = Channel is not selected within a reading sequence 1 = Channel is selected within a reading sequence
DB[6]	AIN14	1	R/W	
DB[5]	AIN13	1	R/W	
DB[4]	AIN12	1	R/W	
DB[3]	AIN11	1	R/W	
DB[2]	AIN10	1	R/W	
DB[1]	AIN9	1	R/W	
DB[0]	AIN8	1	R/W	

REG0x06: System Reading Select Register (SYSREADS) [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
DB[7]	0	0	R	The register selects the input channels and the internal readings in auto-scan mode. Writing to the register will reset the internal channel pointer to the highest priority channel (see Table 10). 0 = Channel is not selected within a reading sequence 1 = Channel is selected within a reading sequence
DB[6]	0	0	R	
DB[5]	REF	0	R/W	
DB[4]	GAIN	0	R/W	
DB[3]	TEMP	0	R/W	
DB[2]	VCC	0	R/W	
DB[1]	0	0	R	
DB[0]	OFFSET	0	R/W	

NOTE: The bits indicated as '0' must be set to 0.

REGISTER MAPS (continued)

REG0x07: GPIO Configuration Register (GPIOCIO) [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	
DB[7:0]	CIO[7:0]	1	R/W	CIO7: Configuration Bit for Pin GPIO7	0 = GPIO is an output 1 = GPIO is an input (default) Set corresponding GPIO pins as input or output.
		1	R/W	CIO6: Configuration Bit for Pin GPIO6	
		1	R/W	CIO5: Configuration Bit for Pin GPIO5	
		1	R/W	CIO4: Configuration Bit for Pin GPIO4	
		1	R/W	CIO3: Configuration Bit for Pin GPIO3	
		1	R/W	CIO2: Configuration Bit for Pin GPIO2	
		1	R/W	CIO1: Configuration Bit for Pin GPIO1	
		1	R/W	CIO0: Configuration Bit for Pin GPIO0	

REG0x08: GPIO Data Register (GPIODATA) [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	
DB[7:0]	DIO[7:0]	0	R/W	DIO7: Data Bit for Pin GPIO7	0 = GPIO is logic low (default) 1 = GPIO is logic high It is used for GPIO pins data read and write. When the GPIO pin is an input configuration, a write operation has no effect on it. A read operation is effective on both input pins and output pins.
		0	R/W	DIO6: Data Bit for Pin GPIO6	
		0	R/W	DIO5: Data Bit for Pin GPIO5	
		0	R/W	DIO4: Data Bit for Pin GPIO4	
		0	R/W	DIO3: Data Bit for Pin GPIO3	
		0	R/W	DIO2: Data Bit for Pin GPIO2	
		0	R/W	DIO1: Data Bit for Pin GPIO1	
		0	R/W	DIO0: Data Bit for Pin GPIO0	

REG0x09: Device ID Register (DEVICEID) [Reset = 0x8B]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
DB[7]	ID7	100	R	Factory-Programmed Version Bits Read-only.
DB[6]	ID6			
DB[5]	ID5			
DB[4]	ID4	0 1011	R	Factory-Programmed ID Bits Read-only.
DB[3]	ID3			
DB[2]	ID2			
DB[1]	ID1			
DB[0]	ID0			

APPLICATION INFORMATION

Figure 13 illustrates the SGM52412RG interfacing with high-level ±10V inputs. In this configuration, the bipolar power supplies are employed, and the input resistors are used to reduce the level of the 10V input signal to within the ADC range. The external amplifiers (SGM8965A) convert the single-ended input to a fully differential output, and then drive the ADC inputs. The 10nF capacitor at the ADC inputs is essential for bypassing the ADC sampling currents, while 5.1Ω resistors isolate the operational amplifier outputs from the filter capacitor. The voltage reference (SGM4029A) is buffered to ensure a low-noise reference input to the ADC. The ADC chop feature can be leveraged to minimize offset and offset drift in the amplifiers.

For input signals within the ADC range, the input resistor divider can be omitted and replaced with a series protection resistor. For 20mA input signals, the input resistor divider can be replaced by a 50Ω resistor, and each input is connected to AINCOM.

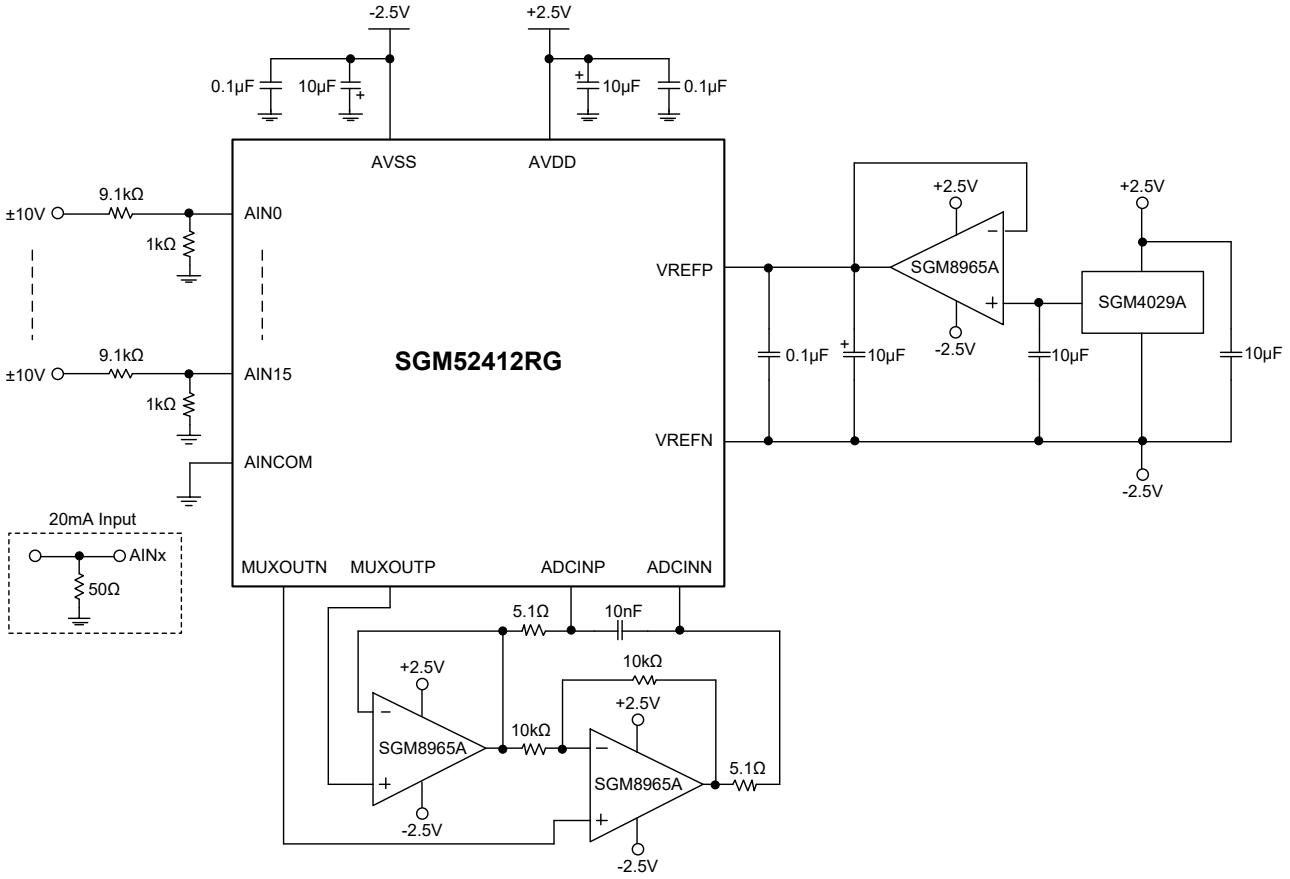


Figure 13. Multichannel, ±10V Single-Ended Input, Bipolar Supply Operation

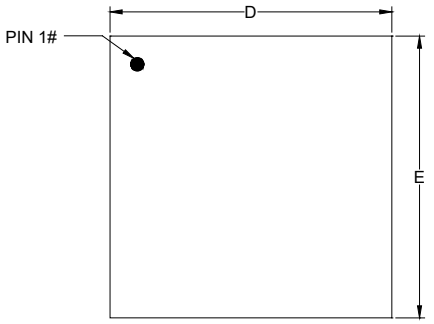
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

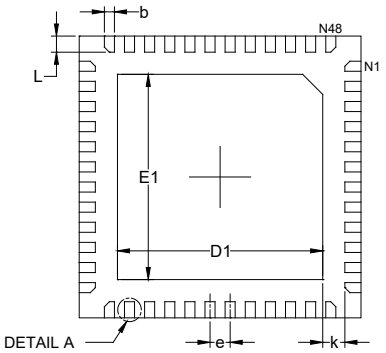
Changes from Original (MAY 2025) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

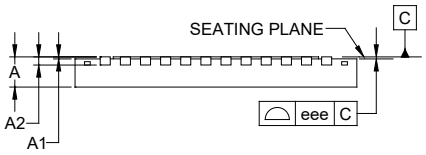
TQFN-7×7-48AL



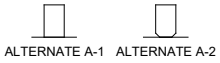
TOP VIEW



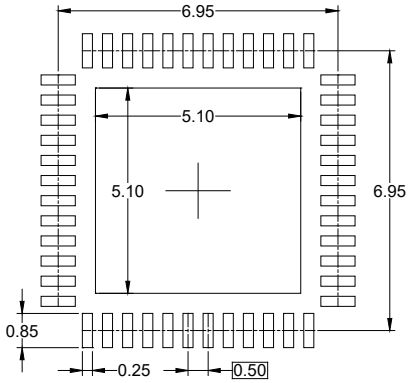
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



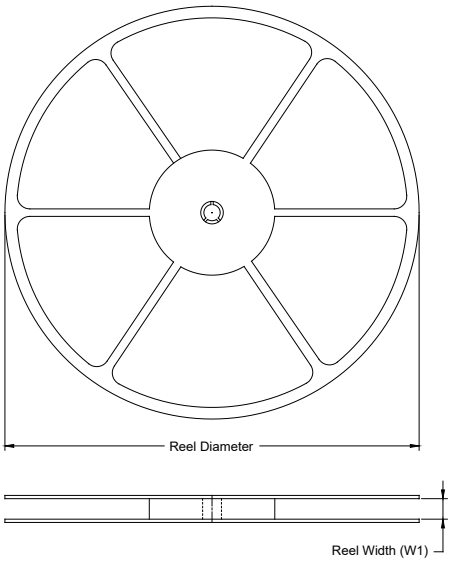
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
D	6.900	-	7.100
E	6.900	-	7.100
D1	5.000	-	5.200
E1	5.000	-	5.200
e		0.500 BSC	
k		0.550 REF	
L	0.300	-	0.500
eee		0.080	

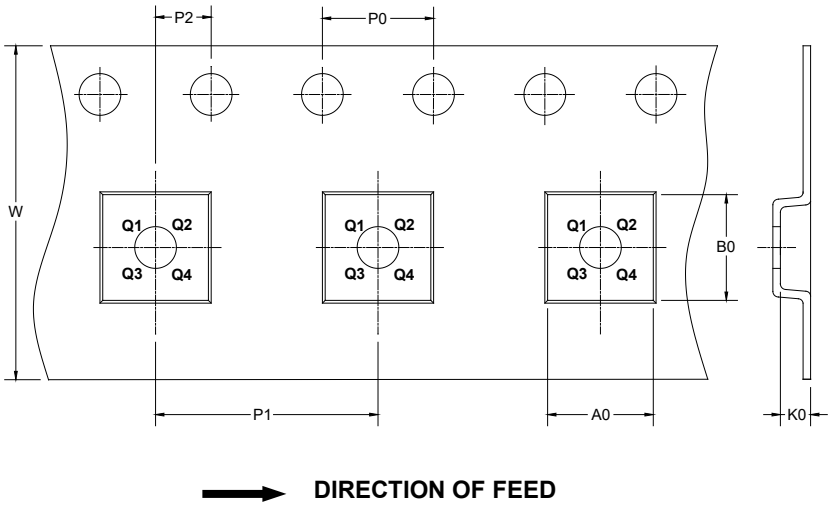
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



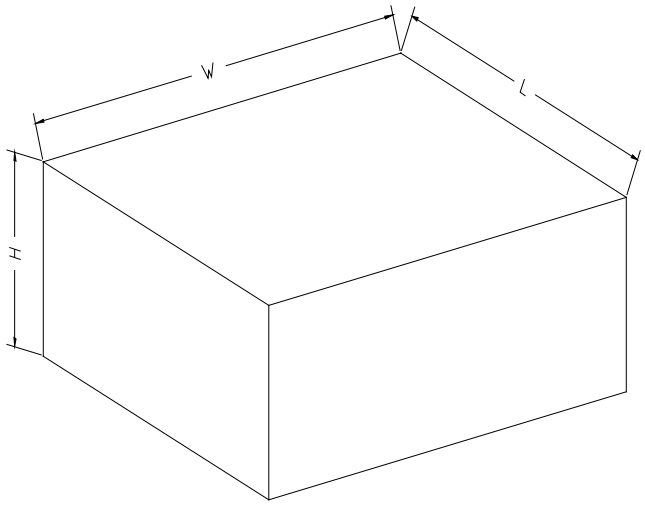
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-7×7-48AL	13″	16.4	7.30	7.30	1.20	4.0	12.0	2.0	16.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002